Register Number:……..

KUMARAGURU
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GENERAL INSTRUCTIONS TO THE CANDIDATES

1. Candidates are instructed to answer the questions as per Bloom's Taxonomy knowledge level (K_1 to K_6)
2. Candidates are strictly instructed not to write anything in the question paper other than their roll number.
3. Candidates should search their pockets, desks and benches and handover to the Hall Superintendent/ Invigilator if any paper, book or note which they may find therein as soon as they enter the examination hall.
4. Candidates are not permitted to bring electronic watches with memory, laptop computers, personal systems, walkie-talkie sets, paging devices, mobile phones, cameras, recording systems or any other gadget / device /object that would be of unfair assistance to him / her.
5. Corrective measures as per KCT examination policies will be imposed for malpractice in the hall like copying from any papers, books or notes and attempting to elicit the answer from neighbours.

B.E DEGREE EXAMINATIONS: JUNE 2015

(Regulation 2014)

Second Semester

COMPUTER SCIENCE AND ENGINEERING

U14CST201 : Digital Systems and Design

Time: Three Hours **Maximum Marks: 100**

Answer all the Questions:-

PART A (10 x 1 = 10 Marks)

1. Match the items in list-I with list-II [K_1]

List I	List II
A. Sequential circuit	i. Half adder
B. Combinational circuit	ii. Flip-flop
C. CMOS logic family	iii. High speed operation
D. ECL IC family	iv. High noise immunity

	A	B	C	D
a)	i	ii	iii	iv
b)	ii	i	iv	iii
c)	iv	iii	ii	i
d)	iii	i	ii	iv

2. Convert $(101010.011)_2$ to base 16 [K_2]

a) 2A.6 b) B2.5

c) 2A.2 d) 2C.1

3. Simplify F= X'Y'+X'Y'Z' [K_3]

a) X'+YZ b) XY

c) X+Y' d) X'Y'

4. Number of control lines required for 8 to 1 MUX is [K_1]

a) 1 b) 3

c) 2 d) 4

5. In a state diagram: [K_1]

1. The number of circles is not equal to the number of states.
2. Every state is given a label written inside the corresponding circle.
3. The number of arcs leaving any circle is n, where n is the number of inputs of the sequential circuit.
4. The label of each arc has the notation x/y, where x is the input vector that causes the state transition, and y is the value of the output during that present state.
5. An arc may leave a state and end up in the same or any other state.

Which of these statements are correct?

a) 2,4,5 b) 1,3

c) 1,2,5 d) 2,3

6. A register that has both shifts and parallel load is [K_1]

a) Universal Shift register b) register

c) Synchronous counter d) Ripple counter

7. Assertion (A): we can correlate the required transitions in a state transition table with the excitation tables of different flip-flops. [K_2]

Reason (R): The functionality of the required combinational logic is encapsulated in the excitation table.

a) both A and R are individually true and R is the correct explanation of A

b) both A and R are individually true but R is not the correct explanation of A

c) A is true but R is false

d) A is false but R is true.

8. A decoder with enable input can function as [K_1]

a) MUX b) DeMUX

c) Encoder d) FF

9. The recommended steps for the design of sequential circuits can be given as [K_1]

1. State diagram 2. State table 3. State minimization 4. Logic diagram

a) 2-3-4-1 b) 1-2-3-4

c) 3-4-2-1 d) 4-1-3-2

10. The most basic type of FFs operate with signal levels called [K_1]

a) T -FF b) RS- FF

c) Latches d) JK- FF

PART B (10 x 2 = 20 Marks)

(Answer not more than 40 words)

11. Convert the given expression in canonical SOP form Y = AC + AB + BC [K_2]

12. Find the complement of the functions F1 = x'yz' + x'y'z and F2 = x(y'z' + yz). [K_2]

13. Implement the following four Boolean expressions with three half adders: [K_3]

$D = A \oplus B \oplus C$
$E = A'BC + AB'C$
$F = ABC' + (A' + B')C$
$G = ABC$

14. What are decoders? List out the applications of decoder. [K_1]

15. What is the difference between truth table and excitation table? [K_1]

16. Give the excitation table of JK flip flop. [K_2]

17. Does Hazard occur in asynchronous sequential circuit? If so what is the problem caused? [K_3]

18. Compare synchronous and asynchronous counters [K_1]

19. List the various characteristics of digital ICs used to compare their performances. [K_1]

20. What is programmable logic array? How does it differ from ROM? [K_2]

Answer any FIVE Questions:-

PART C (5 x 14 = 70 Marks)

(Answer not more than 300 words)

Q.No. 21 is Compulsory

21. i) Construct a 16 x 1 multiplexer with two 8 x 1 and one 2 x 1 multiplexers. Use block diagrams. (7) [K_2]

ii) Implement the following Boolean function with a multiplexer. (7)

$F(A, B, C, D) = \sum(0, 2, 5, 7, 13, 14)$

22. i) Simplify the following functions, and implement them with NAND gate circuits: (8) [K_2]

$F(w,x,y,z) = \sum (1, 2, 3, 4,5)$

ii) Simplify the Boolean function F = $\sum$ (0,1,2,7,8,9,10,11,14,15) using Tabular method. (6)

23. Design an excess-3-to-binary converter using the unused combinations of the code as don't-care conditions. [K_3]

24. A sequential circuit has two *JK* flip-flops *A* and *B* and one input *x*. The circuit is described by the following flip-flop input equations: [K_2]

$JA = x \quad KA = B$

$JB = x \quad KB = A'$

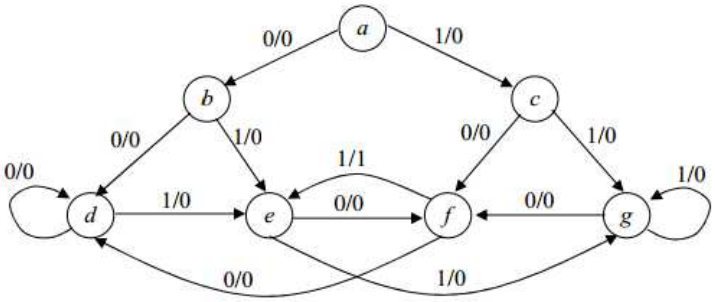
(i) Derive the state equations $A(t + 1)$ and $B(t + 1)$ by substituting the input equations for the *J* and *K* variables. (7)

(ii) Draw the state diagram of the circuit. (7)

25. The state diagram of a sequential circuit is given as below. [K_2]

(i) Tabulate the related state table. (6)

(ii) Reduce the state table to a minimum number of states using an implication chart and draw the reduced state diagram. (8)



26. Draw a PLA circuit to implement the functions [K_3]

$F1 = A'B + AC' + A'BC'$ and $F2 = (AC + AB + BC)'$

Develop the programming table for the PLA.

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