KUMARAGURU
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Register Number:……..…

M.E DEGREE EXAMINATIONS: NOV/DEC 2014

(Regulation 2013)

Third Semester

COMMUNICATION SYSTEMS

P13COTE12 : High Speed Switching Architecture

Time: Three Hours **Maximum Marks: 100**

Answer all the Questions:-

PART A (10 x 2 = 20 Marks)

1. Write the AAL type 1 frame format and significance of each field in the frame.
2. What are the three different layers in SDH architecture?
3. At what layer of the OSI model does a switch operate, and how does this compare with a Bridge?
4. Write the advantages and disadvantages of VLAN.
5. Draw the schematic diagram of Horizontally extended banyan network with N=16 and m=2
6. Write the steps in loop algorithm?
7. What is the need for queuing in ATM switches?
8. Compare combined input, output and shared queuing.
9. What do you mean by multicasting?
10. Define topology driven IP switching.

Answer any FIVE Questions:-

PART B (5 x 16 = 80 Marks)

Q.No:11 is Compulsory

11. (i) State the buddy property and constrained reachability property of a banyan network and explain with 16 x16 SW-banyan topology. (6)

    (ii) State and prove Paull's theorem (10)

12.	(i)	Explain about protocol architecture of ATM adaption layers.	(6)
	(ii)	Draw the SDH multiplexing structure and explain.	(10)
13.	(i)	Compare cut through forwarding and store and forwarding techniques.	(6)
	(ii)	Discuss in detail about switch path control techniques.	(10)
14.	(i)	What is deflection routing? What are the advantages and disadvantages of deflection routing?	(6)
	(ii)	Explain the recursive network construction procedure to build a non blocking full connection multistage network.	(10)
15.		Discuss in detail about input queuing network architecture.	
16.	(i)	Explain about photonic switching architecture.	(8)
	(ii)	With schematic diagrams explain about IP Over ATM protocol.	(8)

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