KUMARAGURU
college of technology
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Register Number:……..…

M.E DEGREE EXAMINATIONS: NOV/DEC 2014

(Regulation 2013)

Third Semester

APPLIED ELECTRONICS

P13AETE04: DSP Integrated Circuits

Time: Three Hours **Maximum Marks: 100**

Answer all the Questions:-

PART A (10 x 2 = 20 Marks)

1. Find the addition and multiplication of 6 and 5 using residue number system?
2. Determine the energy consumed per complex multiplication for a shift accumulator using clock frequency of 175 MHz at 5V, $P_{shift\ acc}$=53mv and $P_{clock+control}$=30.4 mv.
3. Draw the signal flow graph for the equations
   s(n)=3a(n)+5b(n-2); x(n)=2s(n)+4s(n-3)
4. Why FIR filters are preferred over IIR filter in implementation of adaptive filters?
5. Write down the specification of IIR filters.
6. In which type of filters parasitic oscillations are present? Why?
7. Why CMOS technology is better than MOS technology?
8. What are the merits of ASIC's?
9. Bring about the features of Harvard architectures.
10. Give the relationship between bit rate and W_M when bit serial PE is busy?

Answer any FIVE Questions:-

PART B (5 x 16 = 80 Marks)

Q.No:11 is Compulsory

11. A stable digital filter has the following transfer function
    $H(Z) = (1.2Z+1.2)/(Z^2-1.6Z+0.63)$.
    a) Determine impulse response, step response and region of convergence. (10)
    b) Plot the magnitude response and pole zero configuration in the Z-plane. (6)

12.	a)	Analyze the various implementations of bit-serial multiplier.	(10)
	b)	Implement a linear phase FIR structure using distributed arithmetic.	(6)
13.	a)	Write the algorithm to implement the Sande-Tukey FFT.	(10)
	b)	With an example show the features of conventional number system	(6)
14.	a)	Show that an FIR interpolator can be decomposed into L parallel filters that operate and produce a combined output signal with L time's higher sampling rate.	(6)
	b)	Analyze the finite word length effects on signal processing.	(10)
15.	a)	Give a detail description of the different phases of design of a FFT processor.	(8)
	b)	Enumerate the steps involved in VLSI Process technology.	(8)
16.	a)	What are the limitations of shared memory architecture? Discuss the different approaches in reducing these limitations?	(10)
	b)	With an example show the numerically equivalent implementation of WDF's.	(6)

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