KUMARAGURU college of technology
character is life

Register Number:……

M.E DEGREE EXAMINATIONS: DEC 2015

(Regulation 2014)

Third Semester

APPLIED ELECTRONICS

P14AETE63: DSP Integrated Circuits

Time: Three Hours **Maximum Marks: 100**

Answer all the Questions:-

PART A (10 x 1 = 10 Marks)

1. Booth's encoding is an example of CO1 [K_1]

   a) Conventional number system b) Residue number system

   c) Redundant number system d) Non-redundant number system

2. The equation y = a.x + b corresponds to CO1 [K_2]

   Shift accumulation b) Convolution

   Shift addition d) Correlation

3. The complexity of N-point FFT is CO1 [K_2]

   a) N^2 b) N+2

   c) N/2 (log N) d) N/2 (log N/2)

4. Matching type item with multiple choice code CO1 [K_2]

List I	List II
A. Transfer function	i. Hardware architecture
B. Block diagram	ii. Sampling
C. Signal flow graph	iii. Stability
D. Digital signal processing	iv. Data flow

	A	B	C	D
a)	iii	ii	iv	i
b)	iii	i	iv	ii
c)	iii	iv	ii	i
d)	ii	iii	i	iv

5. Assertion (A): Filter should be highly stable CO2 [K_2]

   Reason (R): IIR filters are highly stable

a) Both A and R are true
b) A is false but R is true.
c) A is true but R is not the correct explanation of A
d) A is true and R is the correct explanation of A

6. An interpolator has an interpolation factor L. If 'f' is the sampling frequency, the effect of interpolation on sampling is — CO3 — [K_2]

a) f/L
b) fL
c) f^L
d) F + L

7. A DSP processor may have the following features: — CO4 — [K_2]

1. Harvard architecture 2. Multiple buses 3. MAC unit 4. DMA. The most important ones are:

a) 1,2
b) 1,2,4
c) 2,3
d) 1,2,3

8. Assertion (A): Feature size is the gate length of basic switch. — CO5 — [K_1]
Reason (R): Smaller feature size leads to higher complexity

a) Both A and R are true
b) A is true and R is the correct explanation of A
c) A is false but R is true.
d) Both A and R are false.

9. The main difference between Von Neumann and Harvard architectures is — CO1 — [K_1]

a) Use of multiple processors
b) Having more than one control unit
c) Use of shift accumulators
d) Availability of multiple buses

10. Arrange the following items in the order of importance: — CO1 — [K_2]

1. Memory 2. Control 3. Processing element 4. Interconnect

a) 1, 2, 3, 4
b) 1, 3, 4, 2
c) 3, 1, 4, 2
d) 3, 1, 2, 4

PART B (10 x 2 = 20 Marks)

11. List various fixed-point number representations. — CO1 — [K_1]
12. A residue number system (RNS) uses 5, 7, 9 as modulus. Compute the largest that could be represented. Indicate the drawback of RNS? — CO1 — [K_2]
13. State the drawbacks of under- sampling and over-sampling. — CO1 — [K_2]
14. Justify the choice of DCT for image coding. — CO2 — [K_2]
15. Compare interpolation and interpolation. — CO3 — [K_2]
16. Summarize the drawbacks of finite size of registers. — CO4 — [K_2]
17. Draw a flowchart indicating main phases in DSP system design. — CO5 — [K_2]

18.	Identify the important steps in design transformation.	CO1	[K_2]
19.	Explain the basic principle of self-times systems.	CO5	[K_2]
20.	State and explain memory-bandwidth bottleneck equation.	CO5	[K_2]

PART C (10 x 5 = 50 Marks)

21.	Explain and compare the working and operation of any two parallel adders.	CO1	[K_2]
22.	Outline the salient features of any two redundant number representations.	CO1	[K_2]
23.	Illustrate 4-point DIT-FFT with a signal flow graph.	CO1	[K_2]
24.	Outline how FIR filters are specified. Also, Compare FIR filters with IIR filters.	CO2	[K_2]
25.	Illustrate how computations are reduced in linear-phase FIR structure when compared to direct form structure.	CO2	[K_2]
26.	A 16-bit adder is to be designed. Identify hierarchical representation of the circuit. Justify your answer.	CO3	[K_2]
27.	Explain any one adaptive DSP algorithm used.	CO2	[K_2]
28.	Describe the resource-time trade-off with respect to DSP system design.	CO1	[K_2]
29.	Illustrate how a fast bit-serial memory could be constructed?	CO1	[K_2]
30.	Describes techniques used to reduce memory access time.	CO3	[K_2]

PART D (2 x 10 = 20 Marks)

31.	It is desired to combine telephonic speech and CD quality stereo audio into a single processing system. Suggest a suitable multi-rate, assuming standard data rates, system to combine and transmit the same.	CO3	[K_3]
32.	A DSP system uses 3 processing elements (PEs) with balanced architecture. It is required to build a large DSP system. Suggest cascade and parallel forms for the same. Explain the basic operation.	CO1	[K_3]

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