KUMARAGURU college of technology
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Register Number: ……..

B.E DEGREE EXAMINATIONS: NOV 2015

(Regulation 2009)

Seventh Semester

ELECTRONICS AND COMMUNICATION ENGINEERING

ECE119: VLSI Design

Time: Three Hours **Maximum Marks: 100**

Answer all the Questions

PART A (10 x 1 = 10 Marks)

1. Arranging atoms in a single crystal fashion upon a single crystal substrate is called

   a) Etching b) Photolithography

   c) Epitaxy d) Masking

2. Which material is used as an insulator in SOI process?

   a) Ceramic b) Graphite

   c) Carbon d) Sapphire

3. The threshold voltage of a P channel MOSFET is always _____

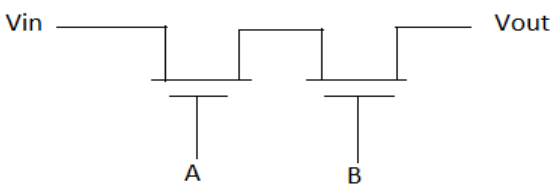
   a) Zero b) Positive

   c) Negative d) Both a & c

4. Gate area (A_g) of a transistor is scaled by _____

   a) $1/\alpha^2$ b) $1/\alpha$

   c) $1/\beta$ d) $1/\beta^2$

5. 

   In the above diagram if A=B=1 and $V_{in} = V_{DD}$ then V_{out} = _____

   a) V_{in} b) 1

   c) 0 d) A+B

6. Dynamic CMOS logic has the following phase of operation:

a) Pre charge b) Evaluate

c) Both a and b d) Inversion

7. Which of the following PLD has programmable OR array and programmable AND array.

a) FPGA b) ASIC

c) PLA d) PAL

8. In FPGA which block provides connection of CLB's with external package pins

a) Input b) Output

c) IOB d) MUX

9. Interconnection between the elements in a logic circuit can be declared with the keyword

a) Cable b) Wire

c) Connection d) Register

10. List the logical operators used in verilog HDL

a) <, >, <=, >= b) +, -, /

c) ~, l, ~□, & d) ==, ===, =

PART B (10 x 2 = 20 Marks)

11. List the various steps involved in the fabrication of integrated circuits.
12. List the advantages of CMOS technology.
13. Define Threshold voltage.
14. What is the significance of stick diagram? Draw the stick diagram of NMOS transistor.
15. Illustrate the structure of transmission gate.
16. Implement two way multiplexer using NMOS switch.
17. Categorize the programmable logic devices.
18. What are the internal blocks of an FPGA?
19. Compare initial and always statements.
20. Write a verilog code for a D flip flop using behavioral modeling .

PART C (5 x 14 = 70 Marks)

21. a) Explain the steps involved in the fabrication of NMOS transistor with neat diagrams.

(OR)

b) (i) Describe the fabrication of CMOS using P well process with neat sketch. (10)

(ii) Discuss the advantages of SOI process. (4)

22. a) Derive the DC current equation of MOSFET and explain the operation and characteristics of enhancement NMOS transistor.

(OR)

b) (i) What are the Lambda based design rules? (7)

(ii) Draw the circuit diagram and layout of two input CMOS NAND gate. (7)

23. a) (i) Explain dynamic CMOS logic for a three input NAND gate. (7)

(ii) With two input NOR gate describe the clocked CMOS logic. (7)

(OR)

b) (i) Illustrate the structured design of parity generator and explain. (7)

(ii) Realize an 8 bit dynamic shift register using CMOS register cells. (7)

24. a) Design and realize NMOS NOR NOR PLA structure with product lines $P_0=I_0' I_1'$, $P_1=I_0' I_1$, $P_2=I_0 I_1 I_2'$, $P_3=I_0 I_2$ and output lines $Y_0= P_1$, $Y_1= P_0+ P_2+ P_3$, $Y_2= P_1+ P_2$.

(OR)

b) Explain the IOB and CLB architectures of Xilinx XC4000 FPGA with neat block diagram.

25. a) (i) Describe the various processes involved in VLSI design flow. (10)

(ii) Write short note on VLSI back end tools. (4)

(OR)

b) (i) Discuss about the case statement used in Verilog HDL with example. (4)

(ii) Design a 4 bit ripple counter and write a Verilog code for the same. (10)

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