KUMARAGURU college of technology
character is life

Register Number: ……..

B.E DEGREE EXAMINATIONS: NOV 2015

(Regulation 2009)

Seventh Semester

ELETRONICS AND INSTRUMENTATION ENGINEERING

EIE117: VLSI Design

Time: Three Hours **Maximum Marks: 100**

Answer all the Questions:-

PART A (10 x 1 = 10 Marks)

1. The ---------- is the most popular standard logic family today
   a) TTL b) CMOS
   c) ECL d) LSI
2. MOS layers are ------
   a) n- diffusion b) p- diffusion
   c) Polysilicon & Metal d) All of the above
3. In CMOS inverter, Propagation delay of a gate can be minimized by
   a) Increase load capacitance b) Decrease supply voltage(Vdd)
   c) Increase W/L ratio of transistors d) None of the above
4. As per Lamda design rule ,Contact Minimum Size in CMOS nwell is
   a) 1 λ b) 2 λ
   c) 3 λ d) 4 λ
5. Multiplexer has
   a) Several data-input lines and one output b) One date input and many data outputs
   c) Many data-input lines and many output d) One data input line and one output
6. Switch logic based on
   a) Pass transistors only b) Transmission gates only
   c) Pass transistors or transmission gates d) Barrel shifter
7. In PLA
   a) AND array is fixed and OR array is Programmable b) OR array is fixed and AND array is Programmble
   c) Both AND and OR arrays are fixed d) Both AND and OR arrays are Programmable

8. Most FPGA logic modules utilize an ----- approach to create the desired logic functions

a) AND array b) Look Up Table

c) OR array d) AND and OR array

9. In VHDL always the ---------- file is included

a) Library b) Header

c) Assembly d) Target

10. In VHDL to declare the inputs and outputs of circuit --------- statements is used

a) Architecture b) Component

c) Process d) Entity

PART B (10 x 2 = 20 Marks)

11. Compare CMOS and Bipolar technology.
12. Define CMOS latch up ? How it can be prevented?
13. Define lamda based rule.
14. Define a Super buffer.
15. What is a tally circuit?
16. What is meant by ratioed logic?
17. Draw the basic NMOS PLA structure.
18. List out two advantages and two disadvantages of FPGA based design.
19. Mention the different types of modeling styles in VHDL?
20. Define test bench?

PART C (5 x 14 = 70 Marks)

21. a) i) Derive the threshold voltage equation of nMOS Enhancement transistor. (7)

ii) Examine the operation of nMOS depletion mode transistor with three operating regions. (7)

(OR)

b) Elaborate the steps involved in the fabrication of CMOS technology.

22. a) Draw the stick diagram for (i) 2 input NOR gate (ii) CMOS NAND gate.

(OR)

b) Explain the operation of inverting and non-inverting type NMOS super buffer.

23. a) i) Write short notes on Dynamic CMOS design. (7)

ii) Design a 4 bit barrel shifter using multiplexer. (7)

(OR)

	b)	i)	Implement a multiplexer using Transmission gate.	(7)
		ii)	Evaluate an array multiplier with an example.	(7)
24.	a)	i)	Infer the architecture of CPLD device with neat diagram.	(7)
		ii)	With a neat sketch explain the general architecture of PAL device.	(7)

(OR)

	b)		Infer the general architecture of FPGA and clearly bring out the different blocks used.	
25.	a)		Write a behavioural and structural VHDL program for a J-K flip flop.	

(OR)

	b)	i)	Illustrate the concurrent and sequential assignments in VHDL.	(7)
		ii)	Write the VHDL code to realize 4 bit synchronous counter.	(7)

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