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M.E DEGREE EXAMINATIONS: DEC 2015

(Regulation 2014)

Third Semester

EMBEDDED SYSTEM TECHNOLOGIES

P14ESTE18: VLSI Design

Time: Three Hours **Maximum Marks: 100**

Answer all the Questions:-

PART A (10 x 1 = 10 Marks)

1. The threshold voltage at non saturated region is CO1 [K_1]

   a) $Vt= V_{ds}$ b) $Vt> V_{gs}$

   c) $Vt< V_{gs}$ d) $Vt=V_{gs}$

2. The expansion of CMOS is CO1 [K_2]

   a) Complementary metal of silicon b) Complementary metal oxide silicon

   c) Complementary metal oxide semiconductor d) Common mode oxidation on silicon

3. A CMOS design having the following process 1) draw CMOS circuit diagram2)obtain Boolean expression 3) fabrication 4) draw the layout design CO2 [K_1]

   a) 1-2-3-4 b) 4-3-2-1

   c) 4-3-1-2 d) 2-4-3-1

4. Which of the following statement correct? CO1 [K_2]

   A. N-type switch is suitable for ON state.

   B. Best suitable material for n-type is phosphorus

   C. LOCAS is used for ion implantation.

   D. Replacement of nMOS and pMOS is CMOS

   a) A alone b) B alone

   c) A & B only d) B & D only

5. A Layout design having the following process 1) interconnections 2) input and out leads 3) to draw V_{dd} & V_{ss} 4) formation of well CO2 [K_2]

   a) 1-2-3-4 b) 4-3-2-1

   c) 4-3-1-2 d) 3-4-1-2

6. Match the following CO2 [K_2]

	OPTIONS		Answers

A	n-type material	1	No latch up problem
B	CMOS	2	Polysilica
C	SOI	3	Phosphorus
D	Gate material	4	Good for both ON state and OFF state

a) A1,B2,C3,D4 b) A3, B4, C1,D2

c) A4,B3,C2,D1 d) A4, B3, C1,D2

7. Match the following CO3 [K_1]

	OPTIONS		Answers
A	Fault	1	multiplexer
B	testing	2	Initial step for fabrication of Ic's
C	Layout design	3	Stuck at '1'
D	Pass transistor	4	Automatic test pattern generator

a) A1,B2,C3,D4 b) A3, B4, C2,D1

c) A4,B3,C2,D1 d) A3, B4, C1,D2

8. Which of the following statement correct? CO2 [K_2]

A. nMos is nearer to V_{ss} in CMOS circuit

B. PMos is nearer to Vdd in CMOS circuit

C. Metal-3 is used for internal contact

D. Contact are used to connect two or more similar metals.

a) A & B only b) B & D only

c) C & B only d) A, B &D only

9. Assertion (A) : testing is essential in digital circuits CO3 [K_2]
Reason (R): nMOS is good for OFF state

a) A and R are true but not related b) A is true and R is false

c) A and R are true and related d) R is true and A is false

10. Assertion (A) : Most of the IC's are fabricated with CMOS logic. CO1 [K_1]
Reason (R): the stick diagrams are sketch without dimensions.

a) A and R are true but not related b) A is true and R is false

c) A and R are true and related d) R is true and A is false

PART B (10 x 2 = 20 Marks)

11. Define threshold voltage. CO1 [K_2]

12. Differentiate between n-type switch with p-type switch. CO1 [K_2]

13. Differentiate between n-well process with p-well process CO2 [K_2]

14. Tabulate the design rule for contacts between devices. CO2 [K_1]

15.	What is pass transistor?	CO2	[K_2]
16.	What is two phase clocking?	CO2	[K_2]
17.	List the need for layout design rule.	CO3	[K_1]
18.	Differentiate between Latches and flip flop.	CO2	[K_2]
19.	List the need for testing.	CO3	[K_2]
20.	List the different types of testing.	CO3	[K_2]

PART C (6 x 5 = 30 Marks)

21.	What is bird's beak encroachment? Also explain how to eliminate the above problem	CO1	[K_2]
22.	Draw and explain the characteristics of depletion type MOS transistor	CO1	[K_2]
23.	Draw the 2 input CMOS layout.	CO2	[K_3]
24.	Design and draw CMOS 4x1MUX.	CO3	[K_2]
25.	Design CMOS circuit diagram for the given Boolean function. a) $y = \overline{(A+B)\ (C+D)}$ b) $F= \overline{ABC}$	CO3	[K_2]
26.	Explain the basic operation of boundary scan test	CO3	[K_3]

PART D (4 x 10 = 40 Marks)

27.	Explain the procedure for fabrication steps of CMOS transistor through Silicon On Insulator technique with neat sketches.	CO1	[K_2]
28.	Explain the second order effects of MOS transistor	CO2	[K_3]
29.	Explain the working principle of JK flip flop	CO2	[K_2]

30. Explain the step by stem procedure for automatic test pattern generator with block diagrams. CO3 [K_3]

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