Register Number:……..

KUMARAGURU
college of technology
character is life

GENERAL INSTRUCTIONS TO THE CANDIDATES

1. Candidates are instructed to answer the questions as per Bloom's Taxonomy knowledge level (K_1 to K_6)
2. Candidates are strictly instructed not to write anything in the question paper other than their roll number.
3. Candidates should search their pockets, desks and benches and handover to the Hall Superintendent/ Invigilator if any paper, book or note which they may find therein as soon as they enter the examination hall.
4. Candidates are not permitted to bring electronic watches with memory, laptop computers, personal systems, walkie-talkie sets, paging devices, mobile phones, cameras, recording systems or any other gadget / device /object that would be of unfair assistance to him / her.
5. Corrective measures as per KCT examination policies will be imposed for malpractice in the hall like copying from any papers, books or notes and attempting to elicit the answer from neighbours.

B.E DEGREE EXAMINATIONS: DEC 2015

(Regulation 2014)

Third Semester

COMPUTER SCIENCE & ENGINEERING

U14CST302 : Computer Architecture

Time: Three Hours **Maximum Marks: 100**

Answer all the Questions:-

PART A (10 x 1 = 10 Marks)

1. Match the following: CO1 [K_1]

List I	List II
A. Machines that store operands in stack	i. addressing modes
B. Different ways in which operand location is specified in an instruction	ii. Register mode
C. Program counter	iii. zero address instructions
D. Operand is in processor register	iv. Relative mode

	A	B	C	D
a)	iv	ii	i	iii
b)	iii	i	iv	ii
c)	iv	ii	i	iii
d)	iii	i	ii	iv

2. In immediate addressing mode, the operand is placed ---------- CO1 [K_1]

a) in the CPU register
b) after Opcode in the instruction
c) in memory
d) in stack

3. How many address lines are needed to address each memory location in a 2048 x 4 memory chip? CO2 [K_2]

a) 10
b) 8
c) 11
d) 12

4. What is the function of control unit in the CPU? CO3 [K_2]

a) To transfer data to primary storage
b) to perform logic operations
c) to store program instruction
d) to decode program instruction

5. Which of the following is true about primary storage CO2 [K_1]

i. It is a part of the CPU
ii. It allows tastest access to data
iii. It is relatively more expensive compared to secondary storage
iv. It is large in size compared to secondary storage

a) i,ii,iii
b) iii only
c) ii,iii,iv
d) ii only

6. The extra time needed to bring the data into memory in case of a cache miss is called --------- CO4 [K_1]

a) Delay
b) Propagation time
c) Miss rate
d) Miss penalty

7. Assertion (A): The amount of time required to read a block of data from a disk into memory depends on the rotational latency. CO5 [K_1]

Reason(R): Rotational latency refers to the time it takes for the platter to make a full rotation

a) Both A and R are individually true and R is the correct explanation of A
b) Both A and R are individually true and R is not the correct explanation of A
c) A is true but R is false
d) A is false and R is false

8. The average time required to reach a storage location in memory and obtain its contents is called ---------- CO5 [K_1]

a) seek time b) turnaround time

c) transfer time d) access time

9. The sequence of steps involved in Integer division are CO4 [K_1]

1. Shifting 2. Subtraction 3. Restoring

a) 3 - 2- 1 b) 1- 3- 2

c) 1 - 2 - 3 d) 2 -1- 3

10. Which of the following registers is used to keep track of address of the memory location where the next instruction is located? CO3 [K_1]

a) Memory Data Register b) Memory Address Register

c) Instruction Register d) Program Register

PART B (10 x 2 = 20 Marks)

(Answer not more than 40 words)

11.	How many memory locations can be addressed with 42 bits? Express the answer using the appropriate terminology.	CO1	K_2
12.	Draw the timing diagram of memory read operation.	CO1	K_1
13.	What do you mean by virtual memory?	CO2	K_1
14.	Show the memory hierarchy and write a note about it.	CO2	K_1
15.	Perform multiplication of (-5 x 4) using Booth algorithm.	CO3	K_2
16.	Show the steps of the integer division of (1100 / 11) in binary.	CO3	K_1
17.	Define: microprogram counter and control store.	CO4	K_1
18.	What is meant by Superscalar operation?	CO4	K_1
19.	Summarize the sequence of events involved in handling an interrupt request from a device.	CO5	K_2
20.	Name any 4 input and 4 output devices.	CO5	K_1

Answer any FIVE Questions:-

PART C (5 x 14 = 70 Marks)

(Answer not more than 300 words)

Q.No. 21 is Compulsory

21.	(i) Explain the principle of pipelining and show how it enhances the speed of instruction execution.	(7)	CO4	K_2
	(ii) Describe the types of pipeline hazards with suitable examples.	(7)		K_2

22.	(i) How do you classify the addressing modes? Explain with examples.	(7)	CO1	K_2
	(ii) Compare the characteristic features of stacks and queues.	(7)		K_2
23.	What is a cache? Explain the types of cache memory with neat sketches.		CO2	K_2
24.	Discuss the operation of a Floating point adder/ subtractor unit with a block diagram.		CO3	K_2
25.	Explain the working of a hardwired control unit with relevant sketches.		CO4	K_2
26.	What do you mean by DMA? Describe the concept of data transfer using DMA.		CO5	K_2

****