



GENERAL INSTRUCTIONS TO THE CANDIDATES

1. Candidates are instructed to answer the questions as per Bloom's Taxonomy knowledge level (K_1 to K_6)
2. Candidates are strictly instructed not to write anything in the question paper other than their roll number.
3. Candidates should search their pockets, desks and benches and handover to the Hall Superintendent/ Invigilator if any paper, book or note which they may find therein as soon as they enter the examination hall.
4. Candidates are not permitted to bring electronic watches with memory, laptop computers, personal systems, walkie-talkie sets, paging devices, mobile phones, cameras, recording systems or any other gadget / device /object that would be of unfair assistance to him / her.
5. Corrective measures as per KCT examination policies will be imposed for malpractice in the hall like copying from any papers, books or notes and attempting to elicit the answer from neighbours.

B.E DEGREE EXAMINATIONS:DEC 2015

(Regulation 2014)

Third Semester

ELECTRONICS AND INSTRUMENTATION ENGINEERING

U14EIT305: Digital Fundamentals and Circuits

Time: Three Hours

Maximum Marks: 100

Answer all the Questions:-

PART A (10 x 1 = 10 Marks)

1. Matching the following

CO1 [K₂]

List I	List II
A. NAND	1. $\overline{\overline{A + B}}$
B. NOR	2. $\overline{A + B}$
C. XNOR	3. $\overline{A.B} + A.B$
D. AND	4. $\overline{A.B}$

	A	B	C	D
a)	2	4	3	1
b)	4	1	3	2
c)	3	1	4	2
d)	4	2	1	3

2. The desirable characteristics of a digital family are:

CO1 [K₃]

- 1) Large Fan-out.
- 2) Large Threshold voltage.

- 3) Large noise immunity.
- 4) Small threshold voltage.

- a) 1,2 are correct.
- b) 2,3 are correct
- c) 1,3,4 are correct
- d) 1,3 are correct

3. The decimal number -15 is represented in 8-bit signed as CO1 [K₁]

- a) 1010001
- b) 11100111
- c) 11110001
- d) 10001111

4. The Boolean expression $\overline{A+B+C}$ is equal to CO2 [K₃]

- a) $\overline{A+B+C}$
- b) $\overline{A.B.C}$
- c) $\overline{A+B+C}$
- d) $A.(B+C)$

5. CO2 [K₅]

PQ →	00	01	11	10
RS ↓				
00	0	0	0	0
01	1	0	0	1
11	1	0	0	1
10	0	1	0	0

A K-Map is given above. The correct Boolean sum of product is

- i) $PQRS + \overline{Q}.S$
- ii) $PQR + \overline{Q}.S$
- iii) $\overline{P.Q}.S + \overline{Q}.S + P.\overline{Q}.S$
- iv) $\overline{PQRS} + \overline{Q}.S$

- a) (i) and (iii) both
- b) (ii) and (iv) both
- c) (iii) only
- d) (iv) only

6. CMOS logic gate has CO5 [K₁]

- a) Highest speed among all logic families.
- b) Very low quiescent power consumption.
- c) Very low output impedance
- d) Very high output impedance

7. Without any additional circuitry, an 8:1 MUX can be used to obtain CO4 [K₃]

- a) Some but not all Boolean functions of 3 variables.
- b) All function of 3 variables but none of 4 variables.
- c) All function of 3 variables and some but not all 4 variables.
- d) All function of 4 variables.

8. Correct order of steps to design a synchronous counter are CO2 [K₁]

- 1) Write values of inputs
- 2) Draw the logic diagram
- 3) Specify present state & next state
- 4) Check excitation table of flip flop

- a) 1,2,3,4
- b) 4,3,2,1
- c) 3,4,1,2
- d) 3,4,2,1

9. Assertion (A): A universal shift register can be operated in all modes CO3 [K₄]

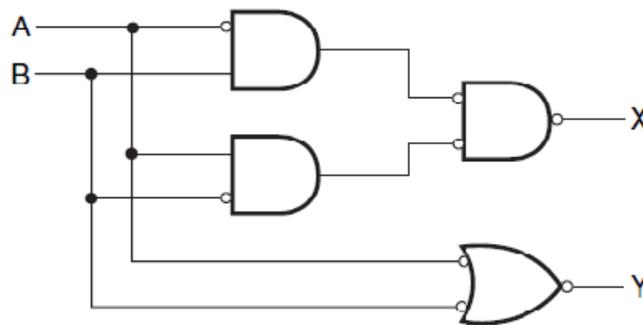
Reason (R): Universal shift register can be constructed with only 4 Flip flops

- a) A is true & R is false
- b) A & R are true
- c) A & R are false
- d) A is false & R is true

10. A master- slave JK flip-flop has the characteristics that CO4 [K₁]
- | | |
|---|--|
| a) Change in the input immediately reflected in the output. | b) Change in the output occurs when the state of master is affected. |
| c) Change in the output occurs when the state of slave is affected. | d) Both the master and slave states are affected at the same time. |

PART B (10 x 2 = 20 Marks)
(Answer not more than 40 words)

11. Determine the hexadecimal equivalent of $(82.25)_{10}$. CO2 [K₅]
12. How can you implement a NOT circuit using a two-input EX-OR gate? CO1 [K₂]
13. State distributive law of Boolean algebra. CO2 [K₁]
14. Starting with the Boolean expression for a two-input OR gate, apply Boolean laws and theorems to modify it in such a way as to facilitate the implementation of a two-input OR gate by using two-input NAND gates only. CO2 [K₄]
15. The logic diagram shown in Figure below performs the function of a very common arithmetic building block. Identify the logic function. CO2 [K₄]



16. Write the truth table of an 8 x 3 encoder. CO3 [K₄]
17. Define Propagation delay in a flip flop. CO3 [K₁]
18. Determine the number of flip-flops required to construct (a) a MOD-10 ring counter and (b) a MOD-10 Johnson counter. CO3 [K₂]
19. Define bidirectional shift register. CO4 [K₁]
20. Compare ROM, PAL & PLA CO5 [K₁]

Answer any FIVE Questions:-
PART C (5 x 14 = 70 Marks)
(Answer not more than 300 words)

Q.No. 21 is Compulsory

21. (i) Outline the different steps involved in the subtraction of larger-bit binary numbers for the following cases: (7) CO2 [K₃]
- Both minuend and subtrahend are positive. The subtrahend is the larger of the two.
 - The minuend is positive. The subtrahend is negative and smaller in magnitude.
- (ii) Draw the TTL NAND gate & explain its working (7) CO2 [K₃]

22. Show the logic arrangements for implementing: CO1,2 [K₃]
 (a) a four-input NAND gate using two-input AND gates and NOT gates;
 (b) a three-input NAND gate using two-input NAND gates;
 (c) a NOT circuit using a two-input NAND gate;
 (d) a NOT circuit using a two-input NOR gate;
23. Minimize the Boolean function $f(A,B,C) = \sum (0, 1, 3, 5) + \sum \phi (2, 7)$ using the mapping method in both minimized sum-of-products and product-of-sums forms. CO2 [K₃]
24. (i) Briefly describe the concept of look-ahead carry generation with respect to its use in adder circuits. (9) CO3 [K₄]
 (ii) Implement a full adder circuit using a 3-to-8 line decoder. (5) CO3 [K₃]
25. (i) Show the logic implementation of an R-S flip-flop having active HIGH R and S inputs. Draw its truth table and mark the invalid entry. (4) CO4 [K₂]
 (ii) Design a synchronous counter that counts as 000, 010, 101, 110, 000, 010... (10) CO4 [K₅]
 Ensure that the unused states of 001, 011, 100 and 111 go to 000 on the next clock pulse. Use J-K flip-flops. What will the Counter hardware look like if the unused states are to be considered as 'don't care's.
26. (i) Explain the working sequence of four bit SISO Shift register with relevant timing diagrams. (7) CO4 [K₂]
 (ii) What are complex programmable logic Array (PLA)? Briefly outline salient features of these devices and application areas where these devices fit the best. (7) CO4 [K₂]
