Register Number:……..

KUMARAGURU
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GENERAL INSTRUCTIONS TO THE CANDIDATES

1. Candidates are instructed to answer the questions as per Bloom's Taxonomy knowledge level (K_1 to K_6)
2. Candidates are strictly instructed not to write anything in the question paper other than their roll number.
3. Candidates should search their pockets, desks and benches and handover to the Hall Superintendent/ Invigilator if any paper, book or note which they may find therein as soon as they enter the examination hall.
4. Candidates are not permitted to bring electronic watches with memory, laptop computers, personal systems, walkie-talkie sets, paging devices, mobile phones, cameras, recording systems or any other gadget / device /object that would be of unfair assistance to him / her.
5. Corrective measures as per KCT examination policies will be imposed for malpractice in the hall like copying from any papers, books or notes and attempting to elicit the answer from neighbours.

B.TECH DEGREE EXAMINATIONS: DEC 2015

(Regulation 2014)

Third Semester

INFORMATION TECHNOLOGY

U14ITT304: Computer Architecture

Time: Three Hours **Maximum Marks: 100**

Answer all the Questions:-

PART A (10 x 1 = 10 Marks)

1. Match the following: CO3 [K_2]

List I	List II
A. Hexa decimal	i. If the sign of A is 1, restore A
B. Restoring division	ii. Carry generation and propagation
C. Carry Save Addition	iii. Four bit representation
D. Carry Look ahead adder	iv. Array multiplier

	A	B	C	D
a)	iii	i	iv	ii
b)	ii	iii	iv	i
c)	iii	ii	i	iv
d)	i	iv	iii	ii

2. Match the following: CO2 [K_2]

List I	List II
A. Memory mapped I/O	i. Repeated checking of status flag for I/O synchronization.

B. DMA	ii. Speed mismatch
C. polling	iii. shared address space for memory and I/O
D. buffering	iv. direct transfer of data between memory I/O

	A	B	C	D
a)	iv	ii	iii	i
b)	i	iv	ii	iii
c)	i	ii	iii	iv
d)	iii	iv	ii	i

3. In case of 8-bit numbers, the minimum number that can be stored in computer is ---------- and maximum number is ---------- CO1 [K_2]
   a) 10000000, 01111111
   b) 00000000, 11111111
   c) 00000001, 11111110
   d) 10000000, 11111111

4. In a vectored interrupt CO2 [K_2]
   a) the branch address is assigned to a fixed location in memory
   b) the interrupt source supplies the branch information to the processor through an interrupt vector
   c) the branch address is obtained from a register in the processor
   d) none of the above

5. Select the instructions which are true: CO1 [K_2]
   1. Fixed point representation suffers from a drawback that the representation can only represent a finite range (and quite small) range of numbers.
   2. A floating point number is in normalized form if the decimal point is to the left of the first significant digit.
   3. Representing an exponent in 2's complement form turns out to be more beneficial than to represent the exponent in excess notation.
   4. A double precision format provides more precision and range.

   a) 1,2,4
   b) 2,3,4
   c) 1,3,4
   d) 2,3

6. Select the instructions which are true: CO1 [K_2]
   1. RAM is a volatile memory and hence used as user memory.
   2. Queue works on first in last out operation.
   3. Register is the simplest storage unit of a processor.
   4. The data transfer rate of peripherals is often much faster than that of the memory or processor.

   a) 2,3
   b) 1,2,3
   c) 1,4
   d) 1,3

7. Assertion: Speed of cache is highest when sequential file is accessed. CO2 [K_2]
   Reason: The cache need not be replaced frequently when there is a sequential data read going on.
   a) A is true but R is false
   b) both A and R are individually true and R is the correct explanation of A

c) both A and R are individually true but R is not the correct explanation of A
d) A is false but R is true.

8. CO4 [K_3]

	time							
	t0	t1	t2	t3	t4	t5	t6	t7 . . . .
(I1) ADD	F1	D1	EX1	M1	W1			
(I2) J 200		F2	D2	EX2	M2	W2		
(I3) ADD			F3	nop	nop	nop	nop	
(I4) ADD				F4	D4	EX4	M4	W4

Assertion : The branch penalty in this pipeline can be reduced by branch folding.
Reason: All pipeline stages require the same time to complete, and there is no interruption throughout program execution

a) both A and R are individually true and R is the correct explanation of A
b) A is false but R is true.
c) both A and R are individually true but R is not the correct explanation of A
d) A is true but R is false

9. The actions needed to execute Move (R1),R2 are as follows: CO4 [K_3]

1. MAR ← [R1]
2. Start a read operation on the memory bus
3. Load MDR from the memory bus
4. R2 ← [MDR]
5. Wait for the MFC response from the memory

Write the sequence.

a) 1,2,5,3,4
b) 1,2,3,4,5
c) 1,3,2,4,5
d) 1,2,4,3,5

10. Sequencing: Select the correct sequencing for a carry save addition. CO3 [K_2]

1. Group the summands in threes and perform carry-save addition on each of these groups in parallel.
2. Group all of the S and C vectors into threes, and perform carry-save addition on them, generating a further set of S and C vectors in one more full-adder delay.
3. Continue with this process until there are only two vectors remaining.
4. This generates a set of S and C vectors in one full-adder delay

a) 2,4,3,1
b) 3,4,1,2
c) 2,3,4,1
d) 1,4,2,3

PART B (10 x 2 = 20 Marks)
(Answer not more than 40 words)

11. With an example, explain what a zero address instruction is. CO1 [K_2]
12. Explain the difference between stacks and queues. CO1 [K_2]
13. Is it necessary for all the pages of a process to be in main memory while the process is executing? Justify your answer. CO2 [K_2]
14. Suggest reasons why the page size in a virtual memory system should be neither very small nor very big. CO2 [K_2]
15. Perform a restoring division for 1000 / 11. CO3 [K_2]
16. List the different truncation methods and explain any one of them. CO3 [K_2]

17.	How does the processor recognize a device requesting an interrupt?		CO2	[K_2]
18.	Enumerate the different reasons why an I/O module is necessary between a device and a computer.		CO2	[K_2]
19.	How can we reduce the branch penalty?		CO4	[K_2]
20.	Write the microprogram sequence for a conditional branch instruction with the condition to check the zero flag.		CO4	[K_3]

Answer any FIVE Questions:-
PART C (5 x 14 = 70 Marks)
(Answer not more than 300 words)

Q.No. 21 is Compulsory

21.	i) Draw the multiple bus architecture and explain control word generation for the instruction: Add the immediate number NUM to register R1.	(8)	CO4	[K_3]
	ii) Ascertain whether the two instructions Mul R2, R3, R4 and Add R5, R4, R6 give rise to stalling when used with a 4 stage pipeline.	(6)	CO4	[K_3]
22.	With block diagrams explain how a 1024 bit memory can be organised as a 128 x 8 array and a 32 x 32 array.		CO2	[K_2]
23.	(i) With block diagram, explain the connections between processor and memory.	(10)	CO1	[K_2]
	(ii) Calculate the program execution time for executing a total of 200 machine language instructions in a program. Assume that on an average there are 6 basic steps needed to execute 1 machine instruction and each basic step is completed in 1 clock cycle. The clock rate is 600 cycles/second.	(4)	CO1	[K_2]
24.	Multiply 5 * -8 using Bit-pair recoding of multipliers. Explain how recoding is done and compare it with Booth's algorithm with the same example.		CO3	[K_4]
25.	With suitable block diagrams, explain about the different types of bus arbitrations.		CO2	[K_2]
26.	(i) With suitable diagrams relate how virtual memory address translation is achieved.	(8)	CO2	[K_2]
	(ii) For a DRAM Cache with 8 cycle access time for the first word and 4 cycles for the subsequent words, analyse how memory interleaving with four and eight modules will improve the performance of the Cache.	(6)	CO2	[K_4]

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