KUMARAGURU
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M.E DEGREE EXAMINATIONS: JAN 2015

(Regulation 2014)

First Semester

APPLIED ELECTRONICS

P14AET101: Advanced Digital System Design

Time: Three Hours   **Maximum Marks: 100**

Answer all the Questions:-

PART A (10 x 1 = 10 Marks)

1.   The present output is a function of present input and state in ----------- network.   [K_1]

   a) Moore   b) Mealy

   c) ASM   d) synchronous

2.   Match List I with List II and select the correct answer in the order of A-B-C-D   [K_2]

List I	List II
A. State Assignment	1. Same output
B. State Equivalence	2. Next state
C. State Reduction	3. Adjacency map
D. State Transition	4. Implication table

   a) 1-2-3-4   b) 1-4-2-3

   c) 3-1-4-2   d) 3-4-1-2

3.   Examine the two statements carefully and select the correct answer.   [K_4]
   Assertion(A) : When there is change in the inputs to an asynchronous sequential
         circuit, there might be multiple next states.
   Reason(R) : Propagation delays are different.

   a) R is the correct explanation of A   b) R is not the correct explanation of A

   c) A is true but R is false   d) A is false but R is true.

4.   The output boxes present in ASM charts correspond to :   [K_2]
      1. Mealy model circuits
      2. Moore model circuits
      3. Controlled architecture
      4. Fundamental mode circuits
   The answer is given by:
   a) 3, 4   b) 2, 3

c) 1, 4   d) 1, 3

5. Feedback connections are available in :   [K_2]

a) PROM   b) PAL

c) CLB   d) PLA

6. PAL22V10 consists of :   [K_2]
    1. Programmable AND array
    2. Fixed OR array
    3. Macrocell
    4. Inputs only

a) 1,2,3   b) 2,3,4

c) 1,3,4   d) 1,2

7. Examine the two statements carefully and select the correct answer.   [K_4]
    Assertion(A) : Component instantiation is used in structural modeling of circuits.
    Reason(R) : Component instantiation is used in test benches.

a) R is the correct explanation of A   b) R is not the correct explanation of A

c) A is true but R is false   d) A is false but R is true.

8. Sequential processing is achieved in VHDL using ------- statement.   [K_2]

a) BEGIN   b) ARCHITECTURE

c) IF-ELSE   d) PROCESS

9. The PN sequence generator is used in :   [K_3]
    1. SISR
    2. MISR
    3. LFSR
    4. ALFSR
    The answer is given by:

a) 1,2   b) 2,3

c) 3,4   d) 1,2,3,4

10. The steps involved in the verification of the state table in the scan path design method is :   [K_2]
    1. Select normal mode
    2. Select test mode
    3. Shift a known pattern into the memory
    4. Verify the next state
    5. Apply input and verify the state transitions
    6. Verify the output
    The sequence to be followed is :

a) 2-3-5-6-1-4   b) 1-2-3-4-5-6

c) 2-3-4-5-6-1   d) 1-2-3-6-5-4

PART B (10 x 2 = 20 Marks)

11. Draw the state diagram for a Moore model full adder.   [K2]

12. Why are state adjacencies important?   [K4]

13. What is critical race in asynchronous sequential circuit?   [K2]

14. Draw the ASM chart for a 3-bit binary up counter.   [K2]

15. State any two important applications of PROM.   [K2]

16. How many inputs and outputs are there in PAL 16R4 device?   [K2]

17. How will you implement delays in VHDL?   [K3]

18. Distinguish between behavioral and structural modeling.   [K2]

19. What is the implication of the result obtained in a network as follows?   [K4]

    $F^{1/0}$ XOR $F^{2/0} = 0$.

20. What is an interconnect fault?   [K2]

PART C (6 x 5 = 30 Marks)

21. The state table of a CSSN is given below: [K4]

Present State	Next State		Output z	
	x = 0	x = 1	x = 0	x = 1
A	B	A	0	0
B	A	C	1	0
C	D	A	0	0
D	D	E	1	0
E	C	D	1	1

Determine the minimal sum excitation and output expressions assigning binary codes to the various states and compare the results by using state assignment rules. Assume use of D flipflops.

22. Explain dynamic hazard with an example of your own.   [K2]

23. Draw the structure of a registered PLD and explain.   [K2]

24. Write VHDL code to implement the combinational logic circuit given by the Boolean expression : F = xy' + z   [K3]

25. A combinational logic circuit is specified by the following expression: $F = ((x_1x_2)'.x_3))'$. Determine the function realized by the network for each of the following faults : (i) 1/0 (ii) 1/1 (iii) 3/0 (iv) 4/1   [K₃]

26. Using exclusive OR method, determine all the tests for the faults given in the above problem.   [K₃]

PART D (4 x 10 = 40 Marks)

27. Obtain a minimal state table for a clocked synchronous sequential network having a single input line x to which binary inputs are applied and a single output line z. The network is to produce an output of 1 coincident with each input 1 that is immediately preceded by at least three 1's. At all other times the network is to produce an output of 0. An example of input / output sequence is :   [K₃]

$$x = 0110011111110000111101$$
$$z = 000000000111000000100$$

28. Obtain a primitive flow table and a minimal row flow table for a fundamental mode asynchronous sequential network meeting the following requirements :   [K₃]

   (i)   There are two inputs x_1 and x_2 and a single output z.
   (ii) The inputs x_1 and x_2 never change simultaneously.
   (iii) The output is to be 1 every other time the input state is $x_1x_2 = 10$; otherwise the output is to be 0.

29. Use PROM to develop a binary to gray code converter.   [K₃]

30. Develop VHDL code to implement a two stage shift register using D flipflops and write test bench for the same.   [K₄]

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