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Register Number:……..…

M.E., DEGREE EXAMINATIONS: JAN 2015

(Regulation 2014)

First Semester

APPLIED ELECTRONICS

P14AET102: VLSI Design Techniques

Time: Three Hours **Maximum Marks: 100**

Answer all the Questions:-

PART A (10 x 1 = 10 Marks)

1. Current conduction between the source and drain of the MOSFET is modulated by [K_2]

   a) The drain voltage b) The gate voltage

   c) The source voltage d) The substrate voltage

2. Calculate the negative threshold voltage for an NMOS transistor at 300K for a process with a Si substrate with N_A =1.8X10^{16}, SiO_2 with thickness 200A^o, ϕ_b=0.36volts, ϕ_{ms}= - 0.9V, Q_{fc}=0, C_{ox}=1.726X10^{-7} Farads/cm^2. [K_3]

   a) 0.32 Volts b) 0.16 Volts

   c) 0.45 Volts d) 0.25 Volts

3. The junction between the poly silicon layer and diffusion layer is called [K_2]

   a) Budding contact b) Burried contact

   c) Ohmic Contact d) Metal Contact

4. Which of the following blocks are available in Clocked CMOS logic [K_2]

   1. Pull up P block
   2. Complementary N block
   3. Clock input
   4. Inverter

   a) 1,2 b) 1,2,3

   c) 1,4 d) 1,2,4

5. Match the following list of materials and maximum sheet resistance values [K_3]

A. Inter metal	1. 30 Ohms/Sq
B. Polysilicon	2. 100 Ohms/Sq
C. Diffusion	3. 5 Kilo Ohms/Sq
D. N well	4. 0.1 Ohm/Sq

   a) 4,1,2,3 b) 4,3,2,1

   c) 3,2,4,1 d) 2,1,3,4

6. The following item consists of two statements, one labeled as the "Assertion (A)" and the other as "Reason (R). You are to examine those two statements carefully and select the answers to these items using the codes given below: [K_2]

Codes:

a. both A and R are individually true and R is the correct explanation of A
b. both A and R are individually true but R is not the correct explanation of A
c. A is true but R is false
d. A is false but R is true.

Assertion : When V_{dd} increases dynamic power dissipation also increases
Reason: Dynamic power is inversely proportional to V_{dd}

a) a b) b

c) c d) d

7. Match list I with list II and select the correct answer using the codes given below. [K_2]

List I	List II
A. Latency	1. Carry select adder
B. Signed arithmetic	2. Carry skip adder
C. Multiple narrow adder	3. Baugh Wooley multiplier
D. High speed	4. Carry look ahead adder

Codes:

	A	B	C	D
(a)	2	1	3	4
(b)	3	4	2	1
(c)	4	3	1	2
(d)	3	1	2	4

8. Calculate the dissipated power if C=2000pF, f=100MHz and V_{DD}=5Volts [K_3]

a) 5 watts b) 10 Watts

c) 15 Watts d) 20 Watts

9. Which of the following are the categories of design for testability? [K_2]

1. Ad hoc testing
2. Scan based approaches
3. Self test and built in testing
4. Boundary scan

a) 1,2,4 b) 1,2,3

c) 1,4,3 d) 2,3,4

10. _____ allows to test circuit board interconnections, external components and the state of chip digital I/Os to be sampled [K_2]

a) Level sensitive scan register b) Boundary scan register

c) TAP register d) Test data register

PART B (10 x 2 = 20 Marks)

11.	Discuss the advantages of SOI process.	[K_2]
12.	Express threshold voltage and body effect.	[K_2]
13.	Outline the stick diagram of CMOS inverter.	[K_2]
14.	Differentiate pass transistor and transmission gate.	[K_2]
15.	Identify the capacitive components of MOS capacitance.	[K_2]
16.	Discriminate static and dynamic power dissipation.	[K_2]
17.	Design a 2 to 1 multiplexer using switch logic.	[K_3]
18.	Discuss about floor planning.	[K_2]
19.	Identify the importance of testing.	[K_2]
20.	List the objectives of Built In Self Test (BIST).	[K_1]

PART C (6 x 5 = 30 Marks)

21.	Explain the small signal AC characteristics of MOS transistor.	[K_2]
22.	Discuss about the steps of fabrication of CMOS using N well process.	[K_2]
23.	Describe the CMOS static and dynamic logic with suitable example.	[K_2]
24.	Illustrate the expressions for the routing capacitance and explain.	[K_2]
25.	Design a 4 bit shift register using CMOS dynamic register cell.	[K_2]
26.	Explain the boundary scan testing method in detail.	[K_2]

PART D (4 x 10 = 40 Marks)

27.	Determine the inverter ratio of an NMOS inverter driven through one or more pass transistor.	[K_4]
28.	Discuss the switching characteristics of CMOS inverter and find the expression for rise time, fall time and propagation delay.	[K_2]

29. Describe carry look ahead adder circuits in detail with neat diagram and obtain the CLA terms using nFET logic. [K_2]

30. Explain the testing of combinational and sequential logic circuit with suitable example. [K_2]

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