KUMARAGURU college of technology
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M.E DEGREE EXAMINATIONS: JAN 2015

(Regulation 2014)

First Semester

EMBEDDED SYSTEM TECHNOLOGIES

P14EST101: Advanced Digital System Design

Time: Three Hours **Maximum Marks: 100**

Answer all the Questions:-

PART A (10 x 1 = 10 Marks)

1. _____ is an example for Combinational logic circuit [K_2]

   a) Half adder b) Flip Flop

   c) Memory d) Buffer

2. Consider the following statements: [K_2]

   1. In sequential circuit, the output depends on both present and past inputs.
   2. Sequential circuits are higher in speed of operation.
   3. In sequential circuit, the output depends on present input only.
   4. Sequential circuit uses clock pulses.

   Which of these statements are correct?

   a) 1,3 b) 1,4

   c) 1,2 d) 2,3

3. Assertion (**A**) : In Hybrid digital circuit the problem of logic race can occur. [K_3]

   Reason (**R**) : In two level logic there is no problem of logic race.

   a) Both **A** and **R** are correct and **R** is the correct explanation of **A** b) Both **A** and **R** are correct and **R** is the not correct explanation of **A**

   c) **A** is true, **R** is false d) **A** is false, **R** is true

4. We can eliminate essential hazards by providing _____ [K_1]

   a) Logic gates b) Flip Flops

   c) Delay d) Inverters

5. In SA-0 fault faulty line is permanently set to _____ [K_1]

a) 1 b) 0

c) Either 0 or 1 d) Floating state

6. A combination of test vector is a _____ [K_2

a) Test inputs b) Test set

c) Primary inputs d) Set of inputs

7. Match the following: [K_1]

List I	List II
A. ROM	1. UltraViolet Rays
B. RAM	2. One time programmable ROM
C. PROM	3. Volatile
D. EPROM	4. Non Volatile

a) A3,B2,C1, D4 b) A2,B4,C3,D1

c) A4, B3,C2, D1 d) A2,B1,C3,D4

8. Field-programmable gate arrays (FGPAs) use _____ memory technology. [K_1]

a) DRAM b) SRAM

c) ROM d) RAM

9. Any VHDL description must contain at least ___ number of entity. [K_2]

a) Two b) Three

c) One d) Either one or two

10. Identify the symbol used for signal assignment? [K_4]

a) == b) =

c) := d) <=

PART B (10 x 2 = 20 Marks)

11. Distinguish between melay and moore models. [K_4]

12. Write the characteristic equation of RS Flip flop and T Flipflop. [K_1]

13. Explain the significance of primitive flow table. [K_2]

14. Define critical race. [K_1]

15. Name the different types of faults. [K_1]

16. State the types of PLD and its applications. [K_2]

17. Draw the block diagram of FPGA? Mention its advantages. [K_4]

18. List out the Xilinx FPGA series? [K_1]

19. Explain the compilation and simulation of VHDL code? [K_2]

20. Write down the general syntax for switch case statement in VHDL. [K_2]

PART C (6 x 5 = 30 Marks)

21. Develop an ASM chart for Binary UP- DOWN Counter. [K_4]

22. Explain the different types of hazards and how to eliminate it? [K_2]

23. Explain how an EPROM can be used to realize a sequential circuit. [K_2]

24. Briefly discuss about Built in self test? [K_2]

25. Explain kohavi algorithm with an example? [K_2]

26. Write a short note on different VHDL operators and data types? [K_2]

PART D (4 x 10 = 40 Marks)

27. Design a CSSN having single input line X and single output line Z. The ouput of 1 is to be produced if and only if three input symbols following two consecutive zeros consists of atleast one 1 at all other times output is to be zero. [K_6]

    X = 0100010010010010000000011

    Z = 0000001000000100000000001

28. Discuss the design steps of Asynchronous sequential circuit with suitable example? [K_2]

29. Construct a PLA structure for the given min terms [K_4]

F1(A,B,C,D) = £ (0,1,4,5,11,13) and F2(A,B,C,D) = £ (0,1,2,5,11,13,15)

30. Explain of the architecture of Xilinx 2000 series. [K_2]

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