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Register Number: …...…….

B.E DEGREE EXAMINATIONS: DEC 2014

(Regulation 2013)

Second Semester

COMPUTER SCIENCE AND ENGINEERING

U13CST201**:** Digital Systems and Design

Time: Three Hours **Maximum Marks: 100**

Answer all the Questions:-

PART A (10 x 1 = 10 Marks)

1. Simplify F = X'Y'+ YZ + X'Y'Z'
   a) XYZ b) X'+YZ
   c) X+YZ' d) X+Y'Z
2. Complete the following: (x+y)' = _____
3. Which of the following is a non-weighted code?
   a) XS-3 b) 8421
   c) 2421 d) 5432
4. The number of control lines required for 8 to 1 MUX is _____
5. A register that performs both shifts and parallel load is called
   a) Universal shift register b) Ripple counter
   c) Register d) Synchronous counter
6. The characteristic equation of JK - FF is _____
7. Example of a sequential circuit is
   a) Binary multiplier b) Half adder
   c) Flip-flop d) Half subtractor
8. State equation is also called as _____
9. High speed operation of the ECL IC family is due to
   a) Saturation of transistors b) High density
   c) Non-saturation of transistors d) Low power consumption
10. If a counter has 10 flip-flops, then the maximum count that can be obtained is _____

PART B (10 x 2 = 20 Marks)

(Not more than 40 words)

11. Reduce AB + (AC)' + AB'C(AB + C)
12. Find the complement of the function F = x'yz' + x'y'z
13. Implement the following four Boolean expressions with three half adders:
    $D = A \oplus B \oplus C$
    $E = A'BC + AB'C$
    $F = ABC' + (A' + B')C$
    $G = ABC$
14. What are decoders? List out the applications of decoder.
15. Give the excitation table of SR flip flop.
16. What are the models used to represent clocked sequential circuits?
17. Compare synchronous and asynchronous counters.
18. Does Hazard occur in asynchronous sequential circuit? If so what is the problem caused?
19. How many 32K * 8 RAM chips are needed to provide a memory capacity of 256KB?
20. What is programmable logic array? How does it differ from ROM?

PART C (5 x 14 = 70 Marks)

(Not more than 400 words)

Q.No. 21 is Compulsory

21. Explain the working of a four-bit universal shift register with a circuit diagram.

22. a) (i) With the use of maps, find the simplest sum-of-products form of the function F = f g, where f = abc' + c'd + a'cd' + b'cd' and g = (a + b + c' + d') (b' + c' + d) (a' + c + d') (7)

    (ii) Implement the following Boolean expression with XOR and AND gates: (7)

    $F = AB'CD' + A'BCD' + AB'C'D + A'BC'D$

    (OR)

    b) (i) Draw the multiple-level NAND circuit for the expression: w(x + y + z) + xyz (7)

    (ii) Simplify the following function and implement with NOR gate circuit: (7)
    $F(w,x,y,z) = \sum (1, 2, 13, 14)$

23. a) Design an excess-3-to-binary converter using the unused combinations of the code as don't-care conditions.

    (OR)

    b) (i) Construct a 16x1 multiplexer with two 8x1 and one 2x1 multiplexers. Use block diagrams. (7)

    (ii) Implement the following Boolean function with a multiplexer (7)
    $F(A,B,C,D) = \sum(0, 2, 5, 7, 13, 14)$

24. a) A sequential circuit has two JK flip-flops A and B and one input *x*. The circuit is described by the following flip-flop input equations:

$JA = x \quad KA = B$

$JB = x \quad KB = A'$

Derive the state equations $A(t+1)$ and $B(t+1)$ by substituting the input equations for the J and *K* variables. Also draw the state diagram of the circuit.

(OR)

b) Show that a Johnson counter with *n* flip-flops produces a sequence of 2*n* states. List the ten states produced with five flip-flops and the Boolean terms of each of the 10 AND gate outputs.

25. a) Draw a PLA circuit to implement the functions and develop the programming table for PLA

$F1 = A'B + AC' + A'BC'$ and $F2 = (AC + AB + BC)'$

(OR)

b) Explain the operation of CMOS NAND and CMOS NOR gates with relevant circuit diagrams.

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