KUMARAGURU
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Register Number:………….

B.E DEGREE EXAMINATIONS: NOV/DEC 2014

(Regulation 2013)

Third Semester

ELECTRONICS AND INSTRUMENTATION ENGINEERING

U13EIT301: Electronic Circuit Design

Time: Three Hours   **Maximum Marks: 100**

Answer all the Questions:-
PART A (10 x 1 = 10 Marks)

1.   Determine the reading on the meter when VCC = 20 V, RC = 5 kΩ, and IC = 2 mA.

   a)   10V   b)   -10V

   c)   0.7V   d)   20V

2.   For the BJT to operate in the active (linear) region, the base-emitter junction must be _____-biased and the base-collector junction must be _____-biased.

3.   Class B amplifiers are greatly preferred over Class A designs for high-power applications such as audio power amplifiers, because there is
   a)   Less power loss   b)   Low noise level
   c)   High bandwidth   d)   High amplification

4.   If a tuned amplifier has a bandwidth of 30 kHz and f0 = 120 kHz, then the Q of the circuit is _____.

5.   For the dc analysis, the network can be isolated from the indicated ac levels by replacing the capacitor with _____.
   a)   an open circuit equivalent   b)   a short circuit equivalent
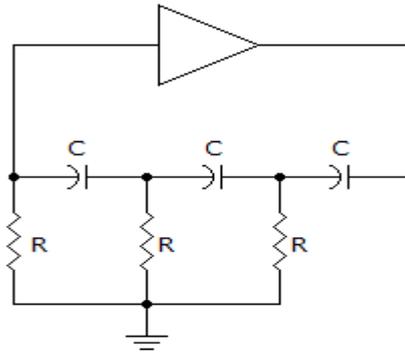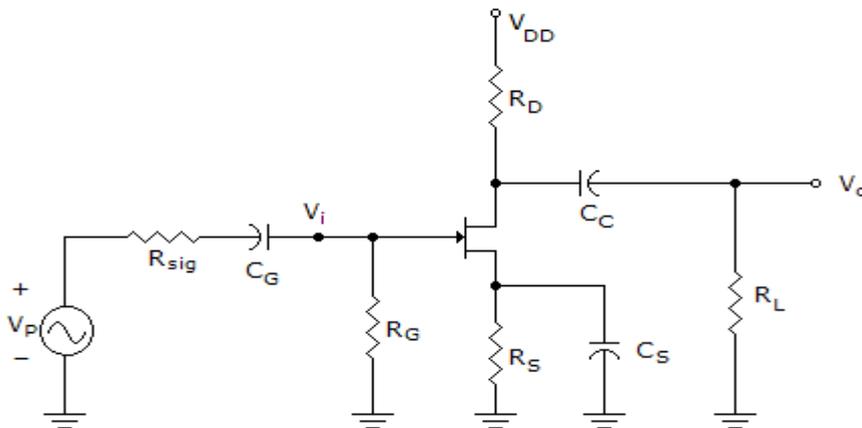   c)   a source voltage   d)   None of the above

6. This circuit is a _____ oscillator.

7. A clipping circuit that clips the input at two identical levels during the positive and negative time periods is called a
    a) limiter   b) positive clipper
    c) slicer   d) negative clipper
8. A Schmitt trigger is a comparator with _____ triggering points.
9. Which type of transformer is required to create a 180 degree input to a rectifier?
    a) center-tapped secondary   b) step-down secondary
    c) stepped-up secondary   d) split winding primary
10. The dc current through each diode in a bridge rectifier equals_____ of the load current.

PART B (10 x 2 = 20 Marks)
(Not more than 40 words)

11. What are the advantages of negative feedback over positive feedback?
12. Determine the lower cutoff frequency of this network.

C_G = 100 pF	R_{sig} = 10 kΩ	I_{DSS} = 8 mA
C_C = 0.5 μF	R_G = 1 mΩ	V_P = -4 V
C_S = 2 μF	R_D = 4.7 kΩ	r_d = ∞ Ω
	R_S = 1 kΩ	V_{DD} = 20 V
	R_L = 2.2kΩ	

13. What are the Barkhausen criterions?
14. Draw a common collector amplifier and its equivalent circuit.
15. What is a synchronously tuned amplifier?
16. Define line regulation and load regulation of a voltage regulator.

17. Calculate the value of C1 = C2 for the Wien bridge oscillator to operate at a frequency of 20 kHz. Assume R1 = R2 = 50 kΩ and R3 = 3R4 = 600 Ω?
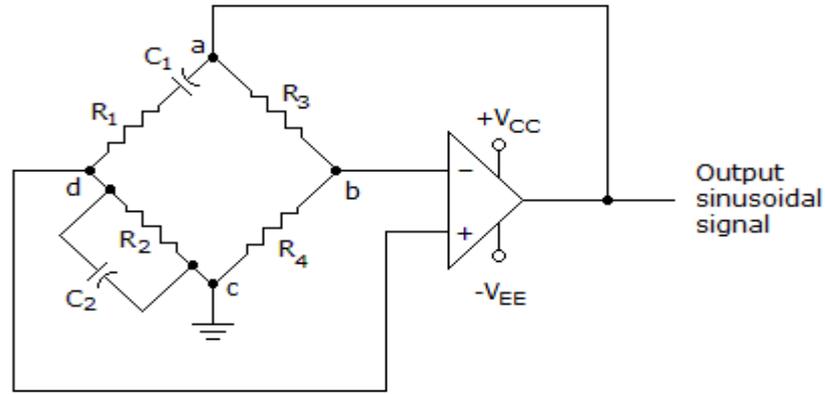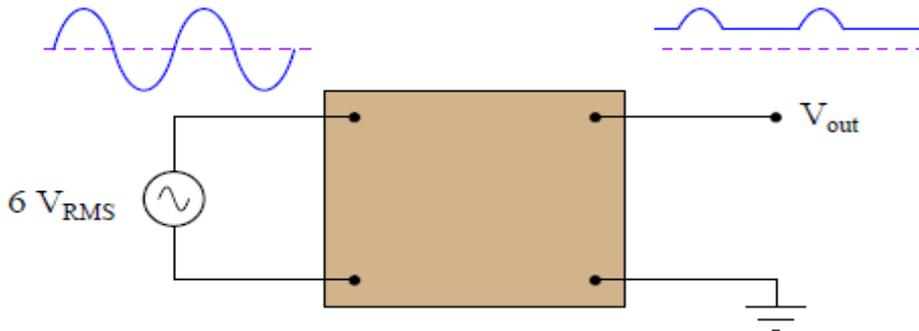

18. Why are commutating capacitors used in bistable multivibrator?
19. Write notes on diode shunt clipper.
20. How can the linearity of current sweep generators be improved?

PART C (5 x 14 = 70 Marks)
(Not more than 400 words)

Q.No. 21 is Compulsory

21. (i) Design an electronic circuit to perform the following. (9)

(ii) Give reason: Thermal runaway is of importance in BJT amplifier but not so in (5) FET amplifier.

22. a) Discuss and derive for the low frequency response of BJT in all the modes.

(OR)

b) Draw and explain the two biasing circuit of JFET and also find Q point using mathematical and graphical methods.

23. a) Design a classAB push-pull large signal amplifiers as the interface stage between a signal generator and low impedance load. This large signal amplifiers should be capable of delivering a maximum of 1 watt 10 a100hm load. Use Fig 1 in the large signal amplifiers. Design constraints use TIP31 and TIP32 BJT transistors. Assume that the sinasoidar 1/D source has a source impedance of 500hm. Use a 10 0hm power resistor as the load to the large signal amplifiers. Use 20volt supply voltages.Use 1/P coupling capacitors to block DC.
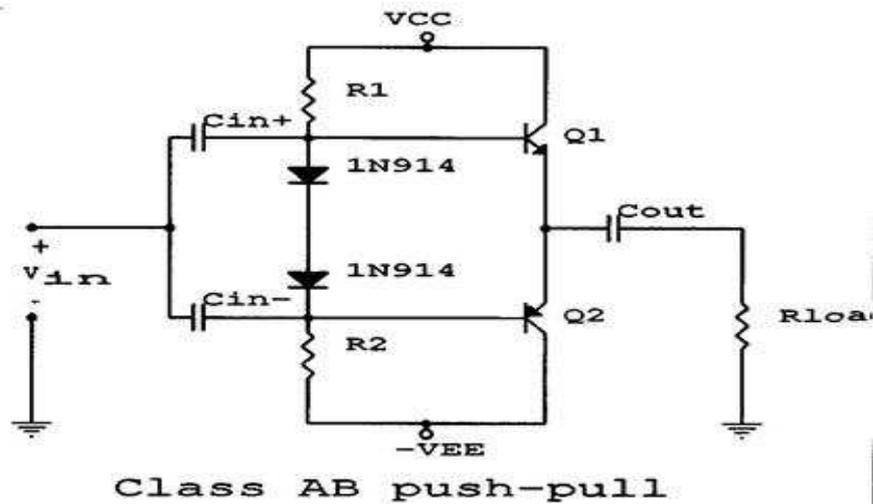
Fig.1

(OR)

b)   Discuss in details the biasing of Darlington amplifier in detail and also elaborate on DC and AC analyses.

24. a)   Design the following negative feedback amplifier circuits with the available data.

(i) voltage-series (ii) voltage-shunt (iii) current-series feedback and (iv) current-shunt

Data given: A=100, Ri=10 KΩ, RO=20 KΩ and β=0.1.

(OR)

b) (i)   Draw the circuit diagram of a pierce crystal oscillator and explain its operation.   4

     (ii)   Draw the circuit diagram of Hartley Oscillator and explain its operation. Obtain   10 the expression for its frequency of oscillations.

25. a)   Discuss in detail the following for a switched mode power supply

     (i) Working principle with circuit

     (ii) Applications

(OR)

b)   Design a full wave rectifier as dc power supply with a 1kΩ load that operates from a 120Vrms, 60Hz supply through a 10 to 1 step down transformer. The capacitor is connected to parallel to the load to provide the peak to peak ripple voltage of 2% of the peak output. The diodes have 0.7V turn on voltage.

A) Draw a complete rectifier circuit to design.

B) Specifly the peak voltage that must appear across the transformer secondary.

C) Find peak value of the rectified voltage across the load.

D) Find average output voltage.

E) Find required value of the filter capacitor

F) Find required diode PIV rating.

G) Calculate the peak diode current.

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