KUMARAGURU college of technology
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Register Number: …….

B.E DEGREE EXAMINATIONS: APRIL/MAY 2016

(Regulation 2013)

Sixth Semester

ELECTRONICS AND COMMUNICATION ENGINEERING

U13ECT603**:** ARM Architecture and Programming

Time: Three Hours **Maximum Marks: 100**

Answer all the Questions:-

PART A (10 x 1 = 10 Marks)

1. The feature that ARM inherited from Berkeley RISC I is
   a) Register window b) Delayed branches
   c) Load store architecture d) Single cycle execution
2. ARM processor uses fixed length_____ bit instructions.
3. The instruction used to finish executing the user program and return to the monitor program is
   a) FIQ b) SWINE
   c) SWI d) BL
4. The formula for the time required to execute a given program is _____.
5. Thumb code uses _____ less external memory power than ARM code
   a) 30% b) 40%
   c) 50% d) 60%
6. The status of the registers are r0=0x00000000, r1=0x00000000, r2=0xf0000002, r3=0x00000002. The output of the registers r0 and r1 if the instruction UMULL r0, r1, r2, r3 is executed is _____.
7. CAM refers to
   a) Cache Addressed Memory b) Carry Addressed memory
   c) Content Addressed Memory d) Compare addressed memory
8. Two approaches to memory management are _____ and _____
9. _____ allow objects of different types to occupy the same space at different times.
   a) Structures b) Unions
   c) pointers d) arrays
10. The normalized representation of 1995 is _____.

PART B (10 x 2 = 20 Marks)

(Answer not more than 40 words)

11. Specify the Clocking Scheme of ARM processor.
12. Write an instruction used for decrementing loop counters? Illustrate with a simple example.
13. State the use of Barrel shifter with Arithmetic instructions.
14. List out the role of Co-processor registers supported by ARM architecture.
15. Write the binary coding of THUMB Software interrupt instruction.
16. Brief about the switching done between ARM instruction and THUMB instruction in programming.
17. Distinguish between functions and arrays with an example.
18. Distinguish between hit rate and miss rate.
19. Enumerate the features of memory protection unit in ARM940T processor.
20. Mention the features of Strong ARM SA-110 processor.

PART C (5 x 14 = 70 Marks)

(Answer not more than 400 words)

Q.No. 21 is Compulsory

21. Describe about the 3-stage and 5-stage pipeline organization of ARM7 processor with relevant block diagrams.

22. (a) (i) Explain about the binary encoding and assembler format of Branch, Branch with Link, Branch with Link and Exchange instructions of ARM processor architecture with examples. (10)

(ii) Write the binary coding and assembler format for Count Leading Zeros in ARM processor architecture with an example. (4)

(OR)

(b) Explain about the co-processor data processing, data transfer and register transfer instructions with examples

23. (a) (i) Describe about the THUMB programmer's model with block diagram. (7)

(ii) Explain the THUMB instruction Decompressor organization with neat block diagram. (7)

(OR)

(b) (i) Explain about the THUMB Single register and Multiple register data transfer instructions with binary coding and assembler format. (10)

(ii) Enumerate the properties and applications of THUMB instructions. (4)

24. (a) Describe the ARM3cache organization and investigate the unified cache performance with respect to size and bandwidth requirement.

(OR)

(b) Describe the internal organization of FPA10 ARM processor and specify the binary coding format of various instructions used in it.

25. (a) Describe the features and organization of ARM920T processor with block diagram.

(OR)

(b) (i) Describe about the features of ARM7TDMI processor core and its synthesis process. (10)

(ii) Summarize few applications of ARM7TDMI processor. (4)

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