KUMARAGURU
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B.E DEGREE EXAMINATIONS : APRIL/ MAY 2016

(Regulation 2013)

Sixth Semester

ELECTRICAL AND ELECTRONICS ENGINEERING

U13EETE14: VLSI Design

Time: Three Hours   **Maximum Marks: 100**

Answer all the Questions:-

PART A (10 x 1 = 10 Marks)

1. Which of the following statements are true.

    1. MOSFET is a voltage controlled device.

    2. CMOS having high power dissipation.

    3. MOSFET has low input impedance.

    4. CMOS occupies less area in the integrated circuit.

    a) 1,4   b) 2,3

    c) 3,4   d) 1,2

2. _____ law describes the exponential growth in VLSI process.

3. The separation between two metal layers in the lambda based design rule must be _____.

    a) 1λ b) 3λ

    c) 2λ d) 4λ

4. The pull up to pull down ratio of pseudo NMOS logic is _____ .

5. In the clocked CMOS logic circuit the output logic is evaluated only during the _____ period of clock.

    a) Positive   b) OFF

    c) Negative   d) ON

6. Silicon dioxide layers on integrated circuits usually store charges in capacitors, including the gate to channel capacitance, such charge is called _____.

7. Clock rate of Xilinx XC4000 ranges between _____.

    a) 80 MHz – 250 MHz   b) 80 MHz – 100 MHz

    c) 80 MHz – 150 MHz   d) 80 MHz – 200 MHz

8. In _____ programmable logic device, only OR plane is programmable while AND plane is fixed.

9. The relational operator used in verilog HDL is

    a)   <=,>=,<,>   b)   +,-, /

    c)   =,==,===   d)   &, !, ||

10. What is the value of 'd' in the following verilog code?

```
initial
begin
        b=1'b1;c=1'b1;
        #10 b=1,b0;
initial
begin
        d = #25 (b|c);
end
```

PART B (10 x 2 = 20 Marks)

(Answer not more than 40 words)

11. Differentiate CMOS and BJT technology.

12. Discuss about the advantages of Twin Well process.

13. Express the scaling factors of gate area and gate capacitance.

14. Outline the stick diagram of CMOS inverter.

15. Illustrate the structure of transmission gate.

16. Categorize the programmable logic devices.

17. What are the internal blocks of FPGA.

18. Outline the VLSI design flow process.

19. Compare initial and always blocks in Verilog HDL.

20. Write a verilog HDL code for full adder.

PART C (5 x 14 = 70 Marks)
(Answer not more than 400 words)

Q.No. 21 is Compulsory

21.   (i)   Explain the steps involved in the fabrication of NMOS transistor with neat   (10) diagrams.

    (ii)   Differentiate enhancement and depletion mode PMOS transistors.   (4)

22. (a) (i)   Obtain the drain to source current equation of MOS transistor in saturation   (4) region.

    (ii)   Outline the scaling of MOS circuits and discuss the limitations of scaling.   (10)

(OR)

(b) (i) Draw the stick diagram and layout diagram of two input NMOS NAND gate.   (7)

  (ii) Determine the pullup to pulldown ratio of an NMOS inverter driven through   (7)
       another NMOS inverter.

23. (a) (i) Explain the dynamic CMOS logic for a three input NAND gate.   (7)

  (ii) Design and implement 4:1 multiplexer using NMOS transistors and draw its   (7)
       stick diagram.

(OR)

(b) Design 4 bit dynamic shift register using CMOS dynamic register cell and draw
     the stick diagram of the same circuit.

24. (a) Discuss the configurable logic block used in Xilinx 4000 FPGA architecture.

(OR)

(b) Explain the architectural features of Altera Cyclone III.

25. (a) (i) Illustrate the operators used in verilog HDL and give examples.   (7)

  (ii) Compose a verilog code for JK Flipflop.   (7)

(OR)

(b) (i) Compose a verilog Code for a 4 bit ripple counter.   (7)

  (ii) Discuss about the back end tools for designing VLSI circuits.   (7)

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