KUMARAGURU college of technology
character is life

Register Number:……

M.E DEGREE EXAMINATIONS: JUNE 2017

(Regulation 2015)

Second Semester

APPLIED ELECTRONICS

P15AET203 : ASIC Design

COURSE OUTCOMES

CO1: Describe different types of ASICs

CO2: Illustrate internal architecture of commercially available FPGAs.

CO3: Develop algorithms to implement digital design on FPGAs

CO4: Distinguish various steps in FPGA design implementation

CO5: Evaluate case studies of FPGA architectures and logic synthesis

Time: Three Hours **Maximum Marks: 100**

Answer all the Questions:-

PART A (10 x 1 = 10 Marks)

1. Assertion (A):In profit model, total sales is increased if product is introduced in time. CO1 [K2]
   Reason (R): In profit model, total sales is declined if product is introduced in delayed time.
   a) both A and R are individually true and R is the correct explanation of A
   b) both A and R are individually true but R is not the correct explanation of A
   c) A is true but R is false
   d) A is false but R is true.

2. CBIC contains CO1 [K2]
   a) Standard AND gates
   b) Standard AND, OR gates MUX, Flip Flops
   c) Standard OR gates
   d) Standard XOR gates

3. ONO stands for CO2 [K1]
   a) Oxide-Nitride-Oxide
   b) Oxide-Nitrogen=Oxygen
   c) Oxygen-Nitrogen=Oxygen
   d) Oxide-Nitride-Oxygen

4. Matching type item with multiple choice code CO2 [K3]

List I	List II
A. Antifuse	i. Metal-Metal Antifuse
B. Amorphous Si	ii. EPROM Erase
C. Floating gate	iii. FPGA
D. UV ray	iv. EEPROM technology

	A	B	C	D
a)	ii	i	iii	iv
b)	iii	iv	ii	i
c)	ii	iv	iii	i
d)	iii	i	iv	ii

5. Assertion (A): AC output IO cell can drive very high speed devices. CO3 [K4]
Reason (R): AC output IO cell works on frequency less than 1Mhz.

a) Both A and R are Individually true and R is the correct explanation of A
b) Both A and R are Individually true but R is not the correct explanation of A
c) A is true but R is false
d) A is false but R is true

6. $V_{IH(min)}$ and $V_{IL((max)}$ for TTL logic are CO3 [K1]

a) 2.0 V and 0.8 V
b) 2.2V and 0.8V
c) 0.8V and 2.0V
d) 0.8V and 2.2V

7. Multiple selection item with multiple choice code CO4 [K2]
In Xilinx LCA:

1. Vertical and horizontal lines run only above CLBs.
2. Genera-purpose interconnect joins switch boxes.
3. Long lines run across entire chip.
4. Direct connections pass through the switch matrices.

Identify the correct statements.

a) 1 & 3
b) 1 & 4
c) 1& 2
d) 2 & 3

8. Sheet resistance and line capacitance of aluminium metallization used in programmable interconnect are: CO4 [K2]

a) 500 milliohm/square and 2pF/cm
b) 50milliohm/square and 0.2pF/cm
c) 5milliohm/square and 0.2pF/cm
d) 500milliohm/square and 0.2pF/cm

9. Four value logic system are CO5 [K2]

a) 0, 1, X & Z
b) 0, 1, weak-0 & Z
c) 0, 1, weak-0 & weak-1
d) 0, 1, X & weak-1

10. Sequence the following EDA process correctly CO5 [K4]

1. Synthesize
2. Simulation
3. Schematic /coding entry
4. compilation

a) 2-3-4-1
b) 1-3-2-4
c) 3-4-2-1
d) 4-1-3-2

PART B (10 x 2 = 20 Marks)

11.	Differentiate full custom and semi custom design.	CO1	[K_4]
12.	List out the various types of parasitic capacitances in MOS transistor.	CO1	[K_2]
13.	Write the part naming convention of Xilinx FPGA XC4010-10 PG156C,	CO2	[K_3]
14.	Draw the architecture view of Logic Array Block used in Altera Max device.	CO2	[K_3]
15.	Justify the need for CLOCK and POWER IO cell in FPGA.	CO3	[K_3]
16.	Why clamp diodes are required in DC output IO cell of FPGA?	CO3	[K_3]
17.	Tell the applications of programmable interconnect.	CO4	[K_1]
18.	Illustrate simple RC delay model of antifuse connections.	CO4	[K_3]
19.	What are the types of simulations?	CO5	[K_1]
20.	What is logic sysnthesis?	CO5	[K_2]

PART C (6 x 5 = 30 Marks)

21.	Describe the working of Flip Flop in sequential logic cell with circuit diagram and waveform.	CO1	[K_2]
22.	Illustrate Shannon's expansion theorem with suitable example.	CO2	[K_3]
23.	Illustrate the supply bounce issue in AC output IO cell with necessary circuit and waveform.	CO3	[K_4]
24.	Analyse the performance of AC output IO cell for parasitic capacitance when system is with few chips that are connected by tri-state bus.	CO3	[K_4]
25.	Describe the interconnect architecture of Altera Max 9000 with required diagram.	CO4	[K_2]
26.	Describe with simulation cycle steps how logic simulation works?	CO5	[K_2]

Answer any FOUR Questions

PART D (4 x 10 = 40 Marks)

27.	Design 6-bit array multiplier using appropriate adder circuit and explain the working with block diagram.	CO1	[K_3]
28.	Explain the internal architecture of CLB used in XC4000 FPGA with necessary diagram.	CO2	[K_2]
29.	Elaborate on timing model of CLOCK signal with necessary diagram for registered input and output configuration.	CO3	[K_2]
30.	Draw and explain the interconnect architecture and components of interconnect delay in Xilinx LCA array.	CO4	[K_2]
31.	Illustrate with suitable example for synthesis of any one combinational and sequential logic using VHDL. Use any type of modeling.	CO5	[K_4]

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