Register Number:……..

KUMARAGURU
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B.E DEGREE EXAMINATIONS: MAY 2017

(Regulation 2015)

Fourth Semester

ELECTRONICS AND INSTRUMENTATION ENGINEERING

U15EIT404 :Digital Fundamentals and Circuits

COURSE OUTCOMES

CO1: Comprehend the knowledge of numeration systems and logic families

CO2: Demonstrate an understanding of minimizing logic circuits using Boolean operations

CO3: Understand principles, operations and design combinational logic circuits

CO4: Describe the operating concepts of sequential logic circuits

CO5: Analyze and design Finite state machines and memories

Time: Three Hours **Maximum Marks: 100**

Answer all the Questions:-

PART A (10 x 1 = 10 Marks)

1. Matching type item CO1 [K_2]

List I	List II
A. The gates required to build a half adder	i. 100
B. Hexadecimal equivalent of 256_{10}	ii. $(1010\ 0011)_2$
C. Convert $A3_H$	iii. EX-OR gate and AND gate
D. Add $(1\ 0\ 1\ 0)_2$ and $(0\ 0\ 1\ 1)_2$	iv. 1101

	A	B	C	D
a)	ii	i	iii	iv
b)	iii	iv	ii	i
c)	ii	iv	iii	i
d)	iii	i	ii	iv

2. MIN term M0 is represented as CO1 [K_1]

a) A'+ B'+C' b) A.B.C

c) A+B+C d) A'.B'.C'

3. Boolean function of full adder is given by CO2 [K_1]

1.) S=A'B'C+A'BC'+AB'C'+ABC

2) C=AB+BC+CA

3) S=AB'C+A'BC'+AB'C'+ABC'

4) C=AB+BC+CA

a) 1,3 b) 1,4

c) 1,2 d) 2,3

4. A binary code in which a number changes from successive number by only one bit CO2 [K_2]

a) Excess 3 Code b) Gray Code

c) BCD Code d) Binary Code

5. With regard to a D latch, CO3 [K_2]

Assertion (A): the Q output follows D input when clock enable is low

Reason (R): the Q output follows D input when clock enable is high

a) Both A and R are Individually true and R is the correct explanation of A b) Both A and R are Individually true but R is not the correct explanation of A

c) A is true but R is false d) A is false but R is true

6. A Combinational circuit that converts 'n' number of input lines to a maximum of 2^n output lines is CO3 [K_1]

a) Encoder b) Multiplexer

c) Decoder d) Comparator

7. How is JK flip-flop is made to toggle when CO4 [K_1]

1) J=1 and K=1

2) J=1 and K=0

3) J=0 and K=0

4) J= 0 and K=1

a) 2-3-4-1 b) 1-3-2-4

c) 3-4-2-1 d) 4-1-3-2

8. EPROM contents can be erased by exposing it to CO5 [K1]

a) Ultraviolet rays b) Infrared rays

c) Burst of microwaves d) Intense heat radiations

9. Assertion (A): In asynchronous two states can be changed simultaneously CO5 [K_2]

Reason (R): In synchronous two states can be changed simultaneously

a) Both A and R are Individually true and R is the correct explanation of A b) Both A and R are Individually true but R is not the correct explanation of A

c) A is true but R is false d) A is false but R is true

10. 4 bit magnitude comparator has A = 1011, B= 1001 determine which output is true — CO4 [K_1]

a) A > B b) A=B

c) A<B d) Understand

PART B (10 x 2 = 20 Marks)

(Answer not more than 40 words)

11. What is binary equivalent of decimal number $(46)_{10}$ — CO1 [K_2]
12. Add the following numbers i) 11_2+11_2 ii)110_2+100_2 — CO1 [K_2]
13. Simplify the following Boolean expression into one literal. — CO2 [K_3]

    A'BC+BC+AC
14. State De-Morgan's theorem. — CO2 [K_2]
15. Construct a full adder circuit using two half adder circuits. — CO3 [K_3]
16. Implement the following function using 8:1 multiplexer — CO3 [K_3]

    F(A,B,C,D)= $\sum$m(1,3,4,8,9,15)
17. Compare asynchronous sequential circuit with synchronous sequential circuit — CO4 [K_2]
18. What is static 1 Hazard and static 0 Hazard — CO4 [K_2]
19. Draw the logic diagram of static RAM cell — CO5 [K_2]
20. Draw the block diagram of PAL and PLA and compare the working of two. — CO5 [K_3]

Answer any FIVE Questions:-

PART C (5 x 14 = 70 Marks)

(Answer not more than 300 words)

Q.No. 21 is Compulsory

21. i) Draw and Explain the block diagram of a 4-bit BCD adder to add the contents of two register (10) CO3 [K_3]

    ii) Implement the following function using only the NAND gates (4)

    F = A(CD +B)+BC'

22. i) Subtract $(11100)_2$ with $(101011)_2$ (7) CO1 [K_3]

    ii) Implement the following function using NOR gate. (7)

    Y= (A+C) (A+D')(A+B+C)

23. Minimize the given terms using F (a,b,c,d) = $\sum_m$(0,1,2,5,6,7,8,9,10,14) CO2 [K_4]

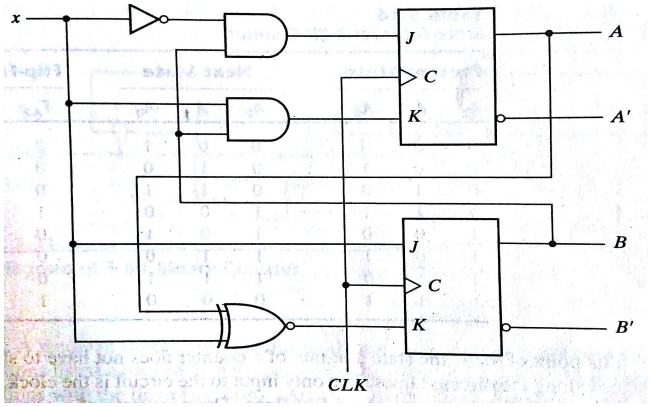
24. i) Express the Boolean function F = XY + X'Z as POS and realize with NOR gate. (7) CO2 [K_4]

ii) Convert the following function to Canonical POS. (7)

F(X,Y,Z) = (X'+Y)(X'+Z)

25. Draw and Explain the block diagram of a 4-blit parallel adder / subtracter to add the contents of two register CO3 [K_3]

26. Analysis the following sequential circuit and obtain the state diagram for the same as shown in Figure 1 CO4 [K_4]



27. i) A combinational circuit is defined by the functions. (8) CO5 [K_4]
F1==∑m(3,5,7),F2==∑m(4,5,7).Implement the circuit with a PLA having 3 inputs,3 product term and 2 output term.

ii) Using eight 64X8 ROM chips with an enable input and a decoder, construct a 512X8 ROM (6)

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