KUMARAGURU
college of technology
character is life

B.TECH DEGREE EXAMINATIONS: MAY 2017

(Regulation 2015)

Fourth Semester

INFORMATION TECHNOLOGY

U15ITT403: Computer Architecture

COURSE OUTCOMES

CO1: Understand micro level operations of computer using the concepts of hardware and software coordination.

CO2: Compare different types of memories and their performances.

CO3: Apply the knowledge of binary arithmetic operations to understand the design of hardware components

CO4: Enumerate various control methodologies using programming and their effect on the hardware components

CO5: Understand the performance enhancement techniques for data handling and I/O handling

Time: Three Hours   **Maximum Marks: 100**

Answer all the Questions:-

PART A (10 x 1 = 10 Marks)

1. Matching List I with appropriate choice in List II   CO1 [K2]

List I	List II
A. Multiprogramming	1.Having several ALUs
B. Multitasking	2.overlapping of CPU and I/O operation
C. Multiprocessing	3.Locality of reference
D. Cache memory	4.Fixing a time-slice for process execution

	A	B	C	D
a)	3	4	1	2
b)	2	4	1	3
c)	4	2	1	3
d)	2	4	3	1

2. _____ holds the address of the location to be accessed   CO1   [K2]

   a) MDR   b) MAR

   c) PC   d) IR

3. Which of the following statement(s) is (are) false? CO1 [K$_2$]

1. At the beginning of the execution of a program, PC contains the address of the first instruction
2. System software is responsible for the coordination of all activities in a computing system
3. In immediate addressing mode, the address of the operand is specified directly in the instruction
4. The number of bits actually stored or retrieved in one memory access is defined as the word length of a computer

a) 1,3

b) 1,4

c) 1,2

d) 2,3

4. Which of the following statement(s) is (are) false? CO3 [K$_2$]

1. A 64-bit adder can be built from 4, 16-bit adders

2. Number of gate delay for S63 is 12 and C64 is 7

3. Number of gate delay for S63 is 18 and C64 is 17

4. Number of gate delay for S63 is 63 and C64 is 64

a) 1 only

b) 1 and 3

c) 1 and 2

d) 1and 4

5. Assertion (A): Registers, ALU and interconnecting bus are collectively called as data path CO4 [K$_2$]

Reason (R)   : Instruction decoder and control logic is responsible for implementing action

specified by an instruction in IR service routine

a) Both A and R are Individually true and R is the correct explanation of A

b) Both A and R are Individually true but R is not the correct explanation of A

c) A is true but R is false

d) A is false but R is true

6. Pipelining is commonly known as a_____ operation CO5 [K$_2$]

a) Sequential

b) Assembly line

c) Parallel

d) Free hazard

7. Arrange the following memory components in decreasing order of access speed CO2 [K$_2$]

1. Hard disk

2. Cache memory

3. Main memory

4. Registers

a) 2-3-4-1

b) 1-3-2-4

c) 3-4-2-1

d) 4-2-3-1

8. Arrange the sequence to multiply two floating point numbers   CO3   [K_2]

     1. Normalize the value obtained

     2. Multiply Mantissa

     3. Determine the sign of result

     4. Add exponent and subtract 127

a) 1,2,3,4   b) 4,3,2,1

c) 1,3,2,4   d) 4,2,3,1

9. Assertion (A): A cascaded connection of n full adder blocks are used to add two n-bit numbers   CO3   [K_2]

Reason (R)   : Since carries propagate through cascade it is called n-bit ripple-carry adder

a) Both A and R are Individually true and R is the correct explanation of A   b) Both A and R are Individually true but R is not the correct explanation of A

c) A is true but R is false   d) A is false but R is true

10. Operand forwarding avoids _____ hazard   CO5   [K_2]

a) Data   b) Overflow

c) Instruction   d) Structure

PART B (10 x 2 = 20 Marks)

(Answer not more than 40 words)

11.	Compare carry flag and overflow flag	CO1	[K_2]
12.	Compare PROM, EPROM, EEPROM	CO2	[K_2]
13.	Compute hit ratio when number of cache memory access is 5000 and success is 4200.	CO2	[K_3]
14.	Analyze write-through and write-back policies pointing out their relative merits and demerits	CO2	[K_2]
15.	List the control sequence for unconditional branch instruction.	CO3	[K_2]
16.	Justify the reason for giving constant 4 as input to MUX in three-bus organization of data path even though there is a PC incrementor.	CO4	[K_3]
17.	Outline the method used by processor and I/O device to share memory access.	CO5	[K_3]
18.	What is control Store?	CO4	[K_2]
19.	What is the ideal speedup expected in a pipelined architecture with 'n' stages? Justify your answer.	CO5	[K_3]
20.	Compare software and hardware interrupts.	CO5	[K_2]

Answer any FIVE Questions:-

PART C (5 x 14 = 70 Marks)

(Answer not more than 300 words)

Q.No. 21 is Compulsory

21. Analyze the need for various addressing modes, with illustration and example for each type.	CO1	[K_3]

22. Summarize various mapping techniques used for mapping memory blocks with cache blocks	CO2	[K_2]

23. Divide 1000 / 11 using restoring and non restoring division	CO3	[K_3]

24. i) Multiply 13 and -6 using Booths multiplication   (7)   CO3   [K_3]

ii) Multiply 16 * -11 using bit pair recoding method   (7)   CO3   [K_3]

25. Describe micro programmed control method of generating control system.   CO4   [K_3]

26. Analyze ways to avoid instruction hazard in pipelining.   CO5   [K_2]

27. Outline the mechanisms used by a processor to handle interrupts   (7)   CO5   [K_2]

Summarize the bus arbitration mechanism used by DMA to access memory.   (7)   CO5   [K_2]

****