KUMARAGURU
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Register Number:……..…

M.E DEGREE EXAMINATIONS: MAY 2018

(Regulation 2015)

Second Semester

APPLIED ELECTRONICS

P15AET203**:** ASIC Design

COURSE OUTCOMES

CO1: Describe different types of ASICs

CO2: Illustrate internal architecture of commercially available FPGAs.

CO3: Develop algorithms to implement digital design on FPGAs

CO4: Distinguish various steps in FPGA design implementation

CO5: Evaluate case studies of FPGA architectures and logic synthesis

Time: Three Hours **Maximum Marks: 100**

Answer all the Questions:-

PART A (10 x 1 = 10 Marks)

1. Sequence the following: CO1 [K_2]

In design flow,

1. System partitioning
2. Routing
3. Pre-layout simulation
4. Floor Planning

a) 1-2-3-4 b) 3-2-4-1

c) 1-3-4-2 d) 3-1-4-2

2. Consider the following statements. CO1 [K_2]

Options for cell libraries for designers to design a logic function are

1. Buy an ASIC-vendor library from a library vendor.
2. Use a design kit from the ASIC vendor.
3. You can build your own cell library.

Which of these statements are correct?

a) 1,2 b) 1,2,3

c) 1,3 d) 2,3

3. Electronic equipment has to survive in a variety of environments. Match the temperature ranges for different applications. CO2 [K_2]

List I	List II
A. Commercial	i. -55 to +125^oC
B. Industrial	ii. -45 to +85^oC
C. Military	iii. 0 to 70^oC

a) (A) – (ii), (B) – (iii), (C) – (i)
b) (A) – (iii), (B) – (ii), (C) – (i)
c) (A) – (i), (B) – (iii), (C) – (ii)
d) (A) – (i), (B) – (ii), (C) – (iii)

4. To convert the wired-logic array into a programmable-AND array, we need to CO2 [K_2]

a) convert the sense of the inputs
b) apply logic 1 at input
c) invert the sense of the inputs
d) apply logic 0 at input

5. Match the Interconnect inside the logic cells: CO3 [K_2]

List I	List II
A. Actel ACT1	i. EEPROM
B. Xilinx XC 3000	ii. Poly-diffusion Antifuse
C. Altera MAX 7000	iii. 32- bit SRAM
D. Altera MAX 5000	iv. EPROM

a) (A) – (ii), (B) – (iii), (C) – (i), (D) –(iv)
b) (A) – (ii), (B) – (iii), (C) – (iv), (D) –(i)
c) (A) – (i), (B) – (ii), (C) – (iii), (D) –(iv)
d) (A) – (iv), (B) – (ii), (C) – (i), (D) –(iii)

6. A totem-pole output buffer has CO3 [K_2]

a) Four transistors of same type
b) Four transistors of complementary type
c) Two transistors of same type
d) Two transistors of complementary type

7. Assertion (A): Actel divides the fixed interconnect wires within each channel into various lengths or wire segments. CO4 [K_2]
Reason (R): Actel allows programming of interconnect.

a) both A and R are individually true and R is the correct explanation of A
b) both A and R are individually true but R is not the correct explanation of A
c) A is true but R is false
d) A is false but R is true

8. Which of the following statements are correct? CO4 [K_2]

1. The ACT 1 architecture uses two antifuses for routing nearby modules
2. The ACT 1 architecture uses three antifuses to join horizontal segments
3. The ACT 1 architecture uses four antifuses to use a horizontal
4. The ACT 1 architecture uses five antifuses to use vertical long track.

a) 1,2,4 b) 2,3,4

c) 1,2,3 d) 1,3,4

9. Sequence the following: CO5 [K_2]

In Xilinx design system,

1. Translate to Xilinx format
2. Create netlist
3. Map to Xilinx logic cell

a) 1-2-3 b) 2-3-1

c) 1-3-2 d) 2-1-3

10. Assertion (A): Xilinx provides a software program (Xilinx design editor, XDE) that permits manual control over the placement and routing of a Xilinx FPGA. CO5 [K_2]

Reason (R): The Program is useful to check an automatically generated layout, or to explore critical routing paths.

a) both A and R are individually true and R is the correct explanation of A

b) both A and R are individually true but R is not the correct explanation of A

c) A is true but R is false

d) A is false but R is true

PART B (10 x 2 = 20 Marks)

11. Define effort delay. CO1 [K_2]
12. How to develop symbolic layout in library-cell design? CO1 [K_3]
13. Mention the advantage of metal antifuse. CO2 [K_2]
14. Compare Xilinx LCA with Actel architecture. CO2 [K_3]
15. What are noise margin conditions for two logic systems to be compatible? CO3 [K_2]
16. How to debounce the bouncing of the pulses of a switch? CO3 [K_3]
17. What is the function of PIP in the interconnect architecture of Xilinx? CO4 [K_2]
18. What is the greatest challenge faced by Actel FPGA architects? CO4 [K_2]
19. What is the standard format for interchanging information between different EDA tools? CO5 [K_2]
20. What are the different types of simulation? CO5 [K_2]

PART C (6 x 5 = 30 Marks)

21.	Compare semi-custom and full custom ICs.	CO1	[K_3]
22.	Analyze the SRAM, EPROM and EEPROM programming technologies.	CO2	[K_3]
23.	Draw and explain the Xilinx XC3000 configurable logic block.	CO2	[K_2]
24.	Explain the different ways to terminate a transmission line.	CO3	[K_2]
25.	Explain the Altera FLEX interconnect scheme with appropriate diagram.	CO4	[K_2]
26.	Discuss about the hierarchical design with a schematic example.	CO5	[K_2]

Answer any FOUR Questions

PART D (4 x 10 = 40 Marks)

27.	Elaborate on the steps involved in VLSI Design flow.	CO1	[K_2]
28.	Analyze the Actel ACT1, 2, 3 logic modules and the timing model.	CO2	[K_3]
29.	How does the supply bounce impacts on AC output?	CO3	[K_3]
30.	Describe the Xilinx EPLD architectures with diagrams.	CO4	[K_2]
31.	Discuss about the Electronic design interchange format.	CO5	[K_2]

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