



**M.E DEGREE EXAMINATIONS: JUNE 2018**

(Regulation 2015)

Second Semester

**EMBEDDED SYSTEM**

P15EST203: Embedded Processors

**COURSE OUTCOMES**

**CO1:** Describe the functional requirements of the hardware and software components of ARM processor Families.

**CO2:** Recall the instruction set and able to write program for DSP applications.

**CO3:** Outline the Black fin processor in all aspects.

**Time: Three Hours**

**Maximum Marks: 100**

**Answer all the Questions:-**

**PART A (10 x 1 = 10 Marks)**

1. Assertion (A): The handler then identifies the external interrupt source and executes the appropriate interrupt service routine. CO2 [K<sub>1</sub>]

Reason (R): The ISR services the external interrupt source and resets the interrupt.

- |  |  |
|--|--|
| a) Both A and R are true                 | b) A is true but R is false                                    |
| c) R is true but A is not related with R | d) Both A and R are true and R is not correct explanation of A |

2. ARM processors where basically designed for \_\_\_\_\_ CO1 [K<sub>1</sub>]

- |                       |                        |
|-----------------------|------------------------|
| a) Main frame systems | b) Distributed systems |
| c) Mobile systems     | d) Super computers     |

3. \_\_\_\_\_ is the deeply embedded, low level software that provides an interface between the hardware and the application. CO2 [K<sub>2</sub>]

- |                |                             |
|----------------|-----------------------------|
| a) Boot loader | b) Firmware                 |
| c) API         | d) Command line interpreter |

4. Match List I with List II

CO1 [K<sub>1</sub>]

List I	List II
A. IIR	i. Multiply and load store
B. FIR	ii. Pipelining
C. ARM	iii. Infinite response
D. DSP	iv. Digital filter

- |    | A   | B  | C   | D  |
|----|-----|----|-----|----|
| a) | ii  | i  | iii | iv |
| b) | iii | iv | ii  | i  |
| c) | ii  | iv | iii | i  |
| d) | iii | i  | ii  | Iv |

5. Assertion (A): Hardware breakpoints are not suitable for debugging exception handlers. CO2 [K<sub>1</sub>]

Reason (R): Hardware breakpoints can be used to debug code running from read - only memory

- |   |   |
|---|---|
| a) Both A and R are Individually true and R is the correct explanation of A | b) Both A and R are Individually true but R is not the correct explanation of A |
| c) A is true but R is false   | d) A is false but R is true   |

6. Blackfin DSPs incorporate the industry's highest performance \_\_\_\_\_ DSP architecture. CO3 [K<sub>1</sub>]

- |            |           |
|------------|-----------|
| a) 32 bit  | b) 16 bit |
| c) 128 bit | d) 64 bit |

7. Memory can be accessed in ARM systems by \_\_\_\_\_ instructions. CO1 [K<sub>1</sub>]

1. Memory
2. Store
3. Move
4. Decode

- |        |        |
|--------|--------|
| a) 1,3 | b) 1,4 |
| c) 1,2 | d) 2,3 |

8. A sine wave whose frequency can be varied from \_\_\_\_\_ to \_\_\_\_\_. CO2 [K<sub>1</sub>]

- |                |                |
|----------------|----------------|
| a) 1 to 25 kHz | b) 3 to 25 kHz |
| c) 2 to 20 kHz | d) 1 to 20 kHz |



**Answer any FOUR Questions**

**PART D (4 x 10 = 40 Marks)**

- |     |  |     |                   |
|-----|--|-----|-------------------|
| 27. | List out the different stage of pipeline used in ARM controller and explain each stage.        | CO3 | [K <sub>2</sub> ] |
| 28. | Identify the different filters are used in digital signal processing and explain each filters. | CO1 | [K <sub>1</sub> ] |
| 29. | Explain Thumb instruction set with an example.   | CO2 | [K <sub>1</sub> ] |
| 30. | Describe the architecture of BLACKFIN processor with a suitable diagram.                       | CO1 | [K <sub>1</sub> ] |
| 31. | Explain the design of IIR filter-based graphic equalizer using Balackfin Simulator.            | CO3 | [K <sub>2</sub> ] |

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