Register Number:……..

KUMARAGURU college of technology
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B.E DEGREE EXAMINATIONS: MAY 2018

(Regulation 2015)

Fourth Semester

ELECTRONICS AND COMMUNICATION ENGINEERING

U15ECTE10 : Computer Architecture

COURSE OUTCOMES

CO1: Explain the functional units of computers (K2).

CO2: Design modules for performing computer arithmetic (K3).

CO3: Illustrate the concepts of control unit design (K2).

CO4: Compare the different types of memories (K2).

CO5: Design interfaces for I/O devices (K3).

CO6: Describe the structure and networking of multiprocessors (K2).

Time: Three Hours **Maximum Marks: 100**

Answer all the Questions:-

PART A (10 x 1 = 10 Marks)

1. Matching type item with multiple choice code CO4 [K_2]

List I	List II
A.TLB	i.Increase in performance
B.Memory interleavng	ii.Dynamic RAM
C.refreshing	iii.Very low power consumption
D.CMOS SRAM	iv.Virtual Memory

	A	B	C	D
a)	ii	i	iii	iv
b)	iv	i	ii	iii
c)	ii	iv	iii	i
d)	iii	i	ii	iv

2. Overflow can occur only when adding two numbers that _____ CO2 [K_2]

a) have the different sign b) have the same sign

c) Are in floating point representation d) Are natural numbers

3. Select the instructions which are true: CO1 [K_2]

1. Size of data bus is mainly specified by the data storage capacity of each location of memory module
2. Size of address bus depends on the processor speed.
3. The control unit to generate the appropriate signal at appropriate time for the proper functioning of the computer
4. The program is machine specific, and it is related to the instruction set of the machine.

a) 1,2,4 b) 2,3,4

c) 1,3,4 d) 2,3

4. Sequencing: Select the correct sequencing for a carry save addition. CO2 [K_2]

1. Group the summands in threes and perform carry-save addition on each of these groups in parallel.
2. Group all of the S and C vectors into threes, and perform carry-save addition on them, generating a further set of S and C vectors in one more full-adder delay.
3. Continue with this process until there are only two vectors remaining.
4. This generates a set of S and C vectors in one full-adder delay

a) 2,4,3,1 b) 3,4,1,2

c) 2,3,4,1 d) 1,4,2,3

5. Assertion: When the answer from a loop operation is transferred to memory to be retained, an incrementing of address is required CO1 [K_2]

Reason R:The store operation destroys the content of the memory

a) Both A and R are Individually true and R is the correct explanation of A
b) Both A and R are Individually true but R is not the correct explanation of A
c) A is true but R is false
d) A is false but R is true

6. Assertion: Parallel computers use multiple processors, each with their own memory banks. CO6 [K_2]

Reason : The multiple processors split up data intensive tasks.

a) A is true but R is false
b) both A and R are individually true and R is the correct explanation of A
c) both A and R are individually true but R is not the correct explanation of A
d) A is false but R is true.

7. Consider the following sequence of micro operations for branch operation: CO3 [K_2]

MBR ← PC + 1
Memory ← MBR
PC ← MBR
MBR ← Memory
PC ← X
Which one of the following is the correct sequence?

a) 1,5,4,2,3 b) 2,1,5,4,3

c) 3,2,1,4,5 d) 1,2,5,4,3

8. Select the reasons for introducing an I/O module with a processor: CO5 [K_2]

1. Different peripherals use various methods of operation.
2. The data transfer rate of peripherals is often much slower than that of the memory or processor
3. The I/O devices do not come with memory.
4. Peripherals often use different data formats and word lengths than the computer to which they are attached

a) 1,2,4 b) 1,2

c) 1,2,3 d) 1,3

9. Pipelining improves system performance in terms of throughput CO3 [K_2]

a) By introducing a faster memory b) by arranging the hardware so that more than one operation can be performed at the same time

c) By operating with a higher clock speed d) By changing the time needed to perform an operation

10. CO5 [K_2]

List I	List II
A. Memory mapped I/O	i. Repeated checking of status flag for I/O synchronization.
B. DMA	ii. Speed mismatch
C.Polling	iii. shared address space for memory and I/O
D.Buffering	iv. direct transfer of data between memory I/O

	A	B	C	D
a)	iii	iv	i	ii
b)	i	ii	iii	iv
b)	i	iv	ii	iii
d)	iv	ii	iii	i

PART B (10 x 2 = 20 Marks)
(Answer not more than 40 words)

11. Define zero address instruction with an example. CO1 [K_2]

12. Differentiate between stacks and queues. CO1 [K_2]

13. List the different truncation methods and explain any one of them. CO2 [K_2]

14. Write the microprogram sequence for a conditional branch instruction with the condition to check the zero flag. CO3 [K_2]

15. Suggest reasons why the page size in a virtual memory system should be neither very small nor very big. CO4 [K_2]

16.	Is it necessary for all the pages of a process to be in main memory while the process is executing? Justify your answer.	CO4	[K_3]
17.	How can we reduce the branch penalty?	CO3	[K_2]
18.	What are the advantages of time shared bus organisation multiprocessor system?	CO6	[K_2]
19.	Perform a restoring division for 1000 / 11.	CO2	[K_3]
20.	Enumerate the different reasons why an I/O module is necessary between a device and a computer.	CO5	[K_2]

Answer any FIVE Questions:-
PART C (5 x 14 = 70 Marks)
(Answer not more than 300 words)

Q.No. 21 is Compulsory

21.	With block diagrams explain how a 1024 bit memory can be organised as a 128 x 8 array and a 32 x 32 array.		CO4	[K_2]
22.	Describe the direct mapping technique of Cache with suitable diagrams.		CO4	[K_2]
23.	(i) With block diagram, explain the connections between processor and memory.	(10)	CO1	[K_2]
	(ii) Calculate the program execution time for executing a total of 200 machine language instructions in a program. Assume that on an average there are 6 basic steps needed to execute 1 machine instruction and each basic step is completed in 1 clock cycle. The clock rate is 600 cycles/second.	(4)	CO1	[K_2]
24.	Multiply 5 * -8 using Bit-pair recoding of multipliers. Explain how recoding is done and compare it with Booth's algorithm with the same example.		CO2	[K_3]
25.	i) Draw the multiple bus architecture and explain control word generation for the instruction: Add the immediate number NUM to register R1.	(8)	CO3	[K_3]
	ii) Ascertain whether the two instructions Mul R2, R3, R4 and Add R5, R4, R6 give rise to stalling when used with a 4 stage pipeline.	(6)	CO3	[K_3]
26.	With suitable block diagrams, explain DMA transfer.		CO5	[K_2]
27.	Draw the organisation of a multiprocessor system and explain any one of the bus organisation elaborately.		CO6	[K_2]

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