Register Number:……..

KUMARAGURU
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B.E DEGREE EXAMINATIONS: MAY 2018

(Regulation 2015)

Fourth Semester

ELECTRICAL AND ELECTRONICS ENGINEERING

U15EET405**:** Digital Electronics

COURSE OUTCOMES

CO1: Translate the number systems and apply the basic postulates of Boolean algebra (K2)
CO2: Design and analyze combinational logic circuits (K2)
CO3: Design and analyze simple sequential logic circuits (K2)
CO4: Apply state reduction techniques for sequential circuit design (K2)
CO5: Explain the digital logic families and implement combinational circuits using programmable logic devices (K2)
CO6: Design digital logic circuits for various applications (K3)

Time: Three Hours **Maximum Marks: 100**

Answer all the Questions:-

PART A (10 x 1 = 10 Marks)

1. Match the Boolean Laws with its expression CO1 [K_1]

Boolean Law	Expression
A. Distributive Law	i. A + AB = A
B. Associative Law	ii. A+BC = (A+B)(A+C)
C. Absorption Law	iii. A+B = B+A
D. Commutative Law	iv. A(BC)=(AB)C

	A	B	C	D
a)	ii	i	iii	iv
b)	ii	iv	i	iii
c)	ii	iv	iii	i
d)	iii	i	ii	iv

2. How is a J-K flip flop made to toggle ? CO3 [K_1]

a) J=0, K=0 b) J=0, K=1

c) J=1, K=0 d) J=1, K=1

3. The subtraction of a binary number Y from another binary number X, done by adding 2's complement of Y to X, results in a binary number without overflow. This implies that the result is — CO1 [K_2]

1. Positive
2. Negative
3. In Normal Form
4. 2's Complement form

a) 1,3 b) 2,4

c) 1,4 d) 2,3

4. CMOS behaves as a/an — CO5 [K_1]

a) Adder b) Subtractor

c) Inverter d) Comparator

5. Assertion (A): NAND and NOR gates are called as Universal Gates. — CO1 [K_2]

Reason (R): They can be used to implement any Boolean function without the need to use any other gates.

a) Both A and R are Individually true and R is the correct explanation of A
b) Both A and R are Individually true but R is not the correct explanation of A
c) A is true but R is false
d) A is false but R is true

6. How many different states does a 3-bit asynchronous counter have ? — CO3 [K_2]

a) 2 b) 4

c) 8 d) 16

7. Arrange the following in a correct sequence for converting SR Flip Flop into T Flip Flop. — CO3 [K_1]

1. Draw the circuit diagram for T Flip Flop.
2. Find the logic expression for excitation inputs of SR Flip Flop.
3. Design the decoder logic.
4. Append the excitation input values of SR Flip Flop to the Present State-Next State Table of T Flip Flop

a) 2-3-4-1 b) 1-3-2-4

c) 3-4-2-1 d) 4-2-3-1

8. Which is not a characteristic of a shift register ? — CO4 [K_1]

a) Serial IN/Parallel IN b) Serial IN/Parallel OUT

c) Parallel IN/ Serial OUT d) Parallel IN/Parallel OUT

9. Assertion (A): Carry Look Ahead Adder reduces the propagation delay. — CO2 [K_2]

Reason (R): In Carry Look Ahead Adder, the carry signals are calculated in advance, based on the input signals.

a) Both A and R are Individually true and R is the correct explanation of A

b) Both A and R are Individually true but R is not the correct explanation of A

c) A is true but R is false

d) A is false but R is true

10. ROM is a — CO5 [K_2]

a) Sequential Circuit

b) Combinational Circuit

c) Magnetic Circuit

d) Static Circuit

PART B (10 x 2 = 20 Marks)
(Answer not more than 40 words)

11. Convert the given expression in canonical SOP Form, Y = AC + AB + BC — CO1 [K_2]
12. State DeMorgan's Theorem. — CO1 [K_1]
13. Draw the logic diagram of a 4 bit parallel adder circuit. — CO2 [K_2]
14. Define Multiplexer. — CO2 [K_1]
15. Draw the NAND based logic diagram for D Flip Flop. — CO3 [K_1]
16. Differentiate combinational and sequential circuits. — CO3 [K_1]
17. Compare Moore and Mealy Circuits. — CO3 [K_1]
18. What are hazards in sequential circuits? — CO4 [K_1]
19. What is FPGA? — CO5 [K_1]
20. Define: Fan-in and Fan-out characteristics of Digital Logic Families. — CO5 [K_1]

Answer any FIVE Questions:-
PART C (5 x 14 = 70 Marks)
(Answer not more than 300 words)

Q.No. 21 is Compulsory

21. Obtain the minimum SOP using Quine McClusky's Method and verify using K-Map. — CO1 [K_2]

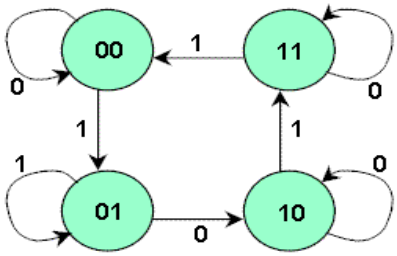
F=∑m(0,2,4,8,9,10,11,12,13)

22. (i) Design and implement Half Adder and Full Adder circuits using Logic Gates. (8) — CO2 [K_2]

(ii) In a certain application, four inputs A,B,C, D (both true and complement forms available) are fed to logic circuit, producing an output F, which operates a relay. The relay turns on when F(ABCD) = 1 for the following states of the inputs (ABCD) : '0000', '0010', '0101', '0110', '1101' and '1110'. States '1000' and '1001' do not occur, and for the remaining states, the relay is off. Minimize F with the help of a Karnaugh Map and realize it using a minimum number of NAND Gates. (6) — CO6 [K_3]

23. Design a synchronous decade counter using T Flip Flop. CO3 [K_2]

24. Design a synchronous sequential circuit for the given state diagram using JK Flip Flop. CO4 [K_2]



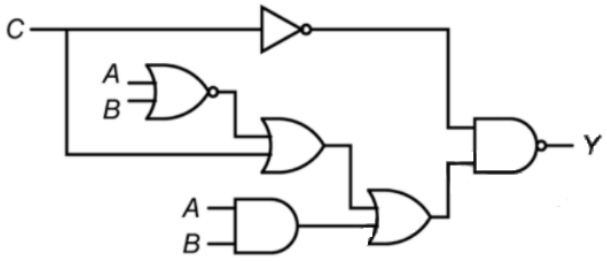
25. (i) Implement the following two Boolean functions with a PLA: (7) CO5 [K_2]

$F1(A,B,C) = \sum(0,1,2,4)$ and $F2(A,B,C) = \sum(0,5,6,7)$

(ii) Explain with suitable sketches, the working principle and characteristics of TTL Logic Family. (7) CO5 [K_2]

26. (i) If X = 1 in the logic equation $[X + Z\{Y' + (Z' + XY')\}] [X' + Z' (X + Y)] = 1$, then what is the value of Z ? (4) CO1 [K_2]

(ii) In the circuit shown in the figure, if C = 0, find the simplified expression for Y. (4) CO1 [K_2]



(iii) Perform the following conversions : (6) CO1 [K_2]

(a) $(10110001101011.111100000110)_2$ to Octal

(b) $(0.6875)_{10}$ to Binary

(c) $(11001100)_2$ to Excess 3 Code

27. (i) Implement the following boolean function using a multiplexer: (8) CO2 [K_2]

$F(A,B,C,D) = \sum m(1,3,4,11,12,13,14,15)$

(ii) Design a 1-bit magnitude comparator. (6) CO2 [K_2]

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