



**B.E. DEGREE EXAMINATIONS : MAY 2018**

(Regulation 2015)

Fourth Semester

**ELECTRONICS AND INSTRUMENTATION ENGINEERING**

U15EIT404 : Digital Fundamentals and Circuits

**COURSE OUTCOMES**

- CO1:** Understand, demonstrate and troubleshoot the different types of logic gates  
**CO2:** Demonstrate an understanding of minimizing logic circuits using Boolean operations  
**CO3:** Understand principles and operations, demonstrate and troubleshoot combinational logic circuits.  
**CO4:** Understand principles and operations, demonstrate and troubleshoot sequential logic circuits.  
**CO5:** Understand principles and operations, demonstrate and troubleshoot registers and counters.

**Time: Three Hours**

**Maximum Marks: 100**

**Answer all the Questions:-  
PART A (10 x 1 = 10 Marks)**

1. Assertion (A): Binary representation uses two symbols, '0' and '1'. CO2 [K<sub>1</sub>]  
Reason(R): Hexa-decimal and Octal are shorthand notation for Binary.
- a) Both A and R are True b) A is true and R is correct explanation of A  
c) A is True but R is false d) A is true but R is not correct explanation of A
2. One of the following is an alpha-numeric code - CO2 [K<sub>1</sub>]  
a) BCD b) Gray  
c) 8421 d) ASCII
3. SOP corresponds to CO2 [K<sub>1</sub>]  
a) Max terms b) Min-terms  
c) Literals d) Venn Diagrams
4. A group of four '1's in K-map is called CO2 [K<sub>1</sub>]  
a) Octet b) Two pairs  
c) Quad d) Fours
5. Parallel adder is also called CO3 [K<sub>1</sub>]  
a) Ripple carry adder b) Carry look-ahead adder  
c) BCD adder d) Word adder



**Answer any FIVE Questions:-**  
**PART C (5 x 14 = 70 Marks)**  
**(Answer not more than 300 words)**

**Q.No. 21 is Compulsory**

21. a) Given  $\sum m[0,2,5,7,8,10] + d[13, 15]$ , implement using SOP method. (10) CO2 [K<sub>2</sub>]  
b) Obtain expression for C<sub>4</sub> of Parallel adder from first principles. (4) CO2 [K<sub>2</sub>]
22. Illustrate basic TTL NAND and CMOS inverter switch level circuit and discuss their working. CO1 [K<sub>2</sub>]
23. State and prove DeMorgan's laws. CO2 [K<sub>2</sub>]
24. Design and construct a 4 – bit magnitude comparator. CO3 [K<sub>2</sub>]
25. Construct a four stage universal shift register and describe its operation. CO4 [K<sub>2</sub>]  
Draw timing diagrams as necessary.
26. Design a sequence detector using Moore model describe as follows: The system receives binary data stream at its input, X. When an input combination/sequence of '011' is received, the output, Y goes HIGH otherwise, it remains LOW. Data arrives from left, first bit, '1' or '0', second bit, '1' or '0' and so on. Draw state transition diagram, construct state synthesis table and obtain reduced circuit using K-map. CO5 [K<sub>2</sub>]
27. Illustrate the architecture of PLA. Also, discuss how 3-variable Boolean expression could be implemented on PLA using your own example. CO4 [K<sub>2</sub>]

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