Register Number:……..

KUMARAGURU college of technology
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B.TECH DEGREE EXAMINATIONS: MAY 2018

(Regulation 2015)

Fourth Semester

INFORMATION TECHNOLOGY

U15ITT403 : Computer Architecture

COURSE OUTCOMES

CO1: Understand micro level operations of computer using the concepts of hardware and software coordination

CO2: Compare different types of memories and their performances.

CO3: Apply the knowledge of binary arithmetic operations to understand the design of hardware components

CO4: Enumerate various control methodologies using programming and their effect on the hardware components

CO5: Understand the performance enhancement techniques for data handling and I/O handling

Time: Three Hours **Maximum Marks: 100**

Answer all the Questions:-

PART A (10 x 1 = 10 Marks)

1. Match the items in List I with that of items in List II CO3 [K_2]

List I	List II
A. Guard bits	i. remove all the extra bits
B. Chopping	ii. A 1 is added to the LSB position of the bits to be retained if there is a 1 in the MSB position of the bits being removed
C. Von Neumann rounding	iii. Extra bits
D. Rounding	iv. If any of the bits to be removed are 1, the LSB of the retained bit is set to 1

	A	B	C	D
a)	ii	i	iii	iv
b)	iii	iv	ii	i
c)	ii	iv	iii	i
d)	iii	i	iv	ii

2. WMFC stands for CO4 [K_2]

a) Wait for Main function completed
b) Wait for Main function completion
c) Wait for Memory function computed
d) Wait for Memory function completed

3. Which of the statements are true? CO2 [K_2]

1.Spatial locality of reference means instructions in close proximity to a recently executed instruction are likely to be executed soon

2. In write-through protocol, the cache location and main memory are not updated simultaneously

3.The address generated by the processor is referred to as physical address

4. A 16 bit computer that generates 16 bit addresses is capable of addressing up to 2 *16 memory locations

a) 1,3
b) 1only
c) 1,2,4
d) 2,3

4. The basic performance equation is CO1 [K_2]

a) T = (N*S)/R
b) T = (R*S)/N
c) T = (N*R)/S
d) T = (N**S)/R

5. Assertion (A): System software is required for the proper functioning of all the components of a computing system CO1 [K_2]

Reason (R): System software is required for managing processor unit, memory unit, I/O unit and file system

a) Both A and R are Individually true and R is the correct explanation of A
b) Both A and R are Individually true but R is not the correct explanation of A
c) A is true but R is false
d) A is false but R is true

6. The micro routines for all instructions in the instruction set of a computer are stored in a special memory called ---------- CO4 [K_2]

a) Cached memory
b) Control memory
c) Control store
d) Control word

7. Arrange the following memory in terms of decreasing order of access speed CO2 [K_2]

1. Main memory
2. cache memory
3. Hard disk
4. Registers

a) 3-1-2-4 b) 4-3-2-1

c) 3-2-1-4 d) 4-2-1-3

8. If a pipeline is stalled because of a delay in the availability of an instruction, it is called CO5 [K_2]

a) Data hazard b) Function hazard

c) Structural hazard d) Control hazard

9. Assertion (A): Bit-pair recoding of multipliers is a fast multiplication method CO3 [K_2]

Reason (R): It is because it halves the maximum number of summands

a) Both A and R are Individually true and R is the correct explanation of A b) Both A and R are Individually true but R is not the correct explanation of A

c) A is true but R is false d) A is false but R is true

10. If the branch prediction decision changes depending on execution history, it is called CO5 [K_2]

a) Dynamic branch prediction b) Static branch prediction

c) Constant branch prediction d) Predictive branch prediction

PART B (10 x 2 = 20 Marks)

(Answer not more than 40 words)

11. State any two differences between RISC and CISC. CO1 [K_2]
12. Compare Big-endian and Little-endian assignment. CO1 [K_2]
13. Give four applications of flash memory. CO2 [K_2]
14. What is meant by read miss? CO2 [K_2]
15. When a floating point binary number is said to be normalized? CO3 [K_2]
16. Write the Divide rule for floating point binary numbers. CO3 [K_2]
17. Write the control sequence for the instruction Move (R1), R2. CO4 [K_3]
18. What is the function of RUN control signal? CO4 [K_2]
19. When structural hazard occurs? CO5 [K_2]
20. What is the disadvantage of polling scheme? CO5 [K_2]

Answer any FIVE Questions:-

PART C (5 x 14 = 70 Marks)

(Answer not more than 300 words)

Q.No. 21 is Compulsory

21. (i) Divide 11111/111 using non-restoring division method. (7) CO3 [K_3]

(ii) Multiply -5 * -8 using Booth algorithm. (7) CO3 [K_3]

22.	(i) Write the control sequence for fetching and executing the instruction Add R1,R2	(4)	CO4	[K_3]
	(ii) Explain about the hardwired control method of generating control signals.	(10)	CO4	[K_2]
23.	Explain about Data hazard in detail.		CO5	[K_2]
24.	(i) Multiply -9 * 4 using Bit-pair recoding method.	(7)	CO3	[K_3]
	(ii) Describe about DMA.	(7)	CO5	[K_2]
25.	(i) Consider a cache with 10-word blocks. On a read miss, the block that contains the desired word must be copied from the memory into the cache. Assume that the hardware has the following properties. It takes one clock cycle to send an address to the main memory. The first word is accessed in 8 cycles and the subsequent words of the block are accessed in 5 clock cycles per word. One clock cycle is needed to send one word to the cache. Calculate the total time needed to load the desired block into the cache if	(7)	CO2	[K_3]
	(a) A single memory module is used. (b) Memory is constructed as five interleaved modules		CO2	[K_2]
	(ii) Describe any two mapping techniques used for mapping memory blocks with cache blocks	(7)		
26.	What is the need for addressing modes? Explain the different types of addressing modes with example for each type.		CO1	[K_2]
27.	(i) Describe about three bus organization of the data path with an example instruction.	(7)	CO4	[K_2]
	(ii) Draw a ROM cell and describe about the types of ROM.	(7)	CO2	[K_2]

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