Register Number:……..

KUMARAGURU college of technology
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**B.E DEGREE EXAMINATIONS: MAY 2018**

(Regulation 2015)

Sixth Semester

**ELECTRONICS AND COMMUNICATION ENGINEERING**

U15ECT603 : VLSI Design

**COURSE OUTCOMES**

**CO1:** Explain working and electrical properties of MOSFET

**CO2:** Discuss MOS Fabrication Technologies

**CO3:** Outline static behavior of MOS Inverters

**CO4:** Implement digital circuits using different logic

**CO5:** Discuss various design implementation methodologies

**CO6:** Implement combinational and sequential logic circuits using verilog HDL

**Time: Three Hours** **Maximum Marks: 100**

**Answer all the Questions:-**

**PART A (10 x 1 = 10 Marks)**

1. Matching type item with multiple choice code CO1 [$K_1$]

| List I | List II |
|---|---|
| A. *p* type semiconductor | i. electrons are majority carriers |
| B. Intrinsic semiconductor | ii. is a metal |
| C. *n* type semiconductor | iii. holes are majority carriers |
| D. Tungsten | iv. silicon |

| | A | B | C | D |
|---|---|---|---|---|
| a) | ii | i | iii | iv |
| b) | iii | iv | i | ii |
| c) | ii | iv | iii | i |
| d) | iii | i | ii | iv |

2. In twin-tub process the electrical property of the layer depends on ---------- CO1 [$K_1$]

a) Polysilicon b) Impurity

c) Dopant and concentration of silicon d) Oxidation

3. What is the indication of a short to ground in the output of a driving gate? CO3 [$K_1$]

I. Only the output of the defective gate is affected.

II. There is a signal loss to all load gates.

III. The node may be stuck in either the HIGH or the LOW state.

IV. The affected node will be stuck in the HIGH state.

a) I and II are correct b) III and IV are correct

c) II alone is correct d) II and III are correct

4. Transmission gates degrades ---------- logic CO3 [$K_1$]

a) Neither 0 nor 1 b) Both 0 and 1

c) Only 0 d) Only 1

5. Assertion (A): In CMOS chips latch up problem occurs. CO4 [$K_2$]

Reason (R): As they have low impedance path between power supply and ground rails.

a) Both (A) and (R) are true and (R) is not the reason for (A) b) (A) is true and (R) is not the reason for (A)

c) Both (A) and (R) is true, (R) is the reason for (A) d) Both (A) and (R) are false

6. Domino logic is the evolution of ……..logic CO4 [$K_1$]

a) Pass transistor logic b) Ratio logic

c) Dynamic logic d) Pseudo NMOS logic

7. Full custom design flow CO5 [$K_1$]

1. Place and route
2. Synthesis
3. Design schematics
4. Design simulation

a) 2-3-4-1 b) 1-3-2-4

c) 3-4-2-1 d) 4-1-3-2

8. In Xilinx XC 4000, ……cells throughout determine the functionality of the device CO5 [$K_1$]

a) IOBs b) CLBs

c) SRAMs d) DRAMs

9. Assertion (A): Test bench generates clk, reset and required test vectors. CO6 [$K_2$]

Reason (R): RTL blocks are functionally verified using test bench.

a) Both A and R are Individually true and R is the correct explanation of A
b) Both A and R are Individually true but R is not the correct explanation of A
c) A is true but R is false
d) A is false but R is true

10. Fast-look-ahead carry circuits found in most 4-bit full adder circuits: CO6 [$K_1$]
a) Determine sign and magnitude
b) Reduce propagation delay
c) Add a 1 to complemented inputs
d) Increase ripple delay

**PART B (10 x 2 = 20 Marks)**
**(Answer not more than 40 words)**

11. What are the reasons for preferring CMOS over MOS? CO1 [$K_1$]
12. Enumerate the effects of scaling of threshold voltage. CO1 [$K_1$]
13. What are the various steps used in IC fabrication. CO2 [$K_1$]
14. Discuss the Lambda based design rules. CO2 [$K_1$]
15. Give the limitations of MOSFET and draw the stick diagram of CMOS Inverter. CO3 [$K_2$]
16. Write a note on Pseudo NMOS. CO4 [$K_2$]
17. Realize a 2x1 MUX using Pass transistor logic. CO4 [$K_3$]
18. Mention the configurable elements in FPGA. CO5 [$K_1$]
19. Differentiate blocking and non-blocking statements in verilog. CO6 [$K_1$]
20. Construct the logic diagram for 1x4 Demultiplexer. CO6 [$K_1$]

**Answer any FIVE Questions:-**
**PART C (5 x 14 = 70 Marks)**
**(Answer not more than 300 words)**

**Q.No. 21 is Compulsory**

21. Design a 16-bit Carry select adder using verilog HDL. CO6 [$K_6$]

22. Describe the operation of PMOS transistor and obtain the expressions for drain current ($I_d$) in the three regions of operation. CO1 [$K_3$]

23. Discuss the fabrication of NMOS Transistor with neat diagrams. CO2 [$K_2$]

24. Describe the operation of CMOS inverter with the characteristics in the five regions of operation. CO3 [$K_2$]

| | | | |
|---|---|---|---|
| 25. | Explain the operation of 4x4 array multiplier with necessary diagrams. | CO4 | [$K_2$] |
| 26. | With neat diagrams, explain in detail the FPGA architecture of Xilinx XC 4000. | CO5 | [$K_2$] |
| 27. | Write technical notes on gate delay in verilog with an example. What is test bench? Write the test bench for a half adder. | CO6 | [$K_3$] |

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