MICROPROCESSOR BASED CONTROL FOR AN ELECTRIC VEHICLE

PROJECT REPORT

Submitted by

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Estd-1984

2003- 2004

Guided by

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In partial fulfillment of the requirements for the Award of the degree of Bachelor of Engineering in Electrical and Electronics Engineering Branch of Bharathiar University, Coimbatore

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

KUMARAGURU COLLEGE OF TECHNOLOGY

COIMBATORE - 641 006

Estd-1984

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CERTIFICATE

This is to certify that the project report entitled

MICROPROCESSOR BASED CONTROL FOR AN ELECTRIC VEHICLE

is the bonafide work done by

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SYNOPSIS

Electric vehicles are entirely different from that of the conventional automobiles. In the conventional automobile, the output mechanical power from the Internal Combustion (I.C) engine is used for driving the vehicle. Here I.C. engine acts as a drive whose fuel input may be either diesel or petrol whereas in the case of an electric vehicle, the drive is an electric motor whose fuel input is obviously the electric supply voltage.

As of now, all the electric vehicles used in BHEL, Tiruchirapalli for their internal transport purposes is running only under two speed or four speed modes. Also as the vehicles are designed with the Rheostatic method of speed control, there is a considerable amount of power loss in the motor. Project aims to developing an electric vehicle with variable speed as that of a conventional automobile and with negligible amount of power loss compared to that of a Rheostatic method of speed control.

The variable speed vehicles has obviously many advantages over these two speed vehicles like quick transportation from one place to another thereby saving lot of time by which the productivity of an industry can be increased to certain extent. The objective is achieved with the help of the recently developed power electronic devices.

As we employ both microprocessor for governing the entire operation starting from keying ON till shutting down the electric vehicle and a closed loop control system, the speed control system will be very effective and highly accurate with quick response. Therefore the vehicle can be used as a multipurpose vehicle for internal transport and material handling purposes.

ABOUT BHEL

Bharat Heavy Electricals Limited (BHEL) who has sponsored the project is one of the biggest public sector undertakings in India. Its production has entered in diverse fields with the help of its large manpower and highly sophisticated modern instruments. Its production includes manufacturing of alternators, transformers, railway coaches, and vehicles for defence sectors, high-pressure boilers.

BHEL's various manufacturing units are located all over India. One of the units located in Tiruchirapalli concentrates mainly in the production of high-pressure boilers. It's various departments and sections with their sincere and joint co-operation and with their **Total Quality Management (TQM) policy** is responsible for producing the output within the stipulated time period so as to satisfy the needs of the customer.

The Maintenance and Services department (M&S) is responsible for maintenance and service work in electrical section which includes attending and rectifying the faults in all electrical equipments like generators, motors, hoists and also in electronic equipments like CNC machines etc.

The transportation department is responsible for servicing all the vehicles used for internal transport, which includes electric vehicles also. The electric vehicles here are all running with two speed or four speed modes.

INTRODUCTION

1 INTRODUCTION

Electric Vehicles have appeared throughout automotive history but have never experienced the wave of attention that they do today. Pollution, higher gas prices, an impending oil shortage and major technology improvements have caused a flurry of activity to bring this promising technology to market.

1.1 AN ELECTRIC VEHICLE

Unlike a gasoline car powered by an engine, an EV is powered by an electric motor and batteries stored inside the car. There are approximately 4000 vehicles on the road today in the US. Many of those are conversions made from existing cars such as Geo Metros, Ford Escorts, Volksagon Rabbits, Hondas and trucks like the Chevy S-10 and Ford Ranger.

The others are purpose built vehicles built in small quantities by several companies throughout the world. In our project we have tried out a design of an electric vehicle whose entire operation is taken by the microprocessor.

1.2 ADVANTAGES

There are several unique advantages for driving an EV

- No exhaust or emissions test.
- No more messy oil and antifreeze changes
- Totally silent operation
- Costs 60%-75% less to operate
- High efficiency
- Easy construability
- Can be started on load

1.3 RANGE AND PERFORMANCE

Depending on driving habits and terrain, a typically EV averages 40 to 70 miles pr charge. Range records are being broken every year and many EVs being built are in 60-125 mile range. The batteries are very expensive they should be competitively priced within the

Because EVs are so quiet and peppy they are fun to drive. Most EVs today can outperform their gasoline cousins. The GM EV1 will accelerate from 0 to 60 in under nine seconds.

By nature of their design, electric motors are very powerful. Electric motors have instantaneous torque when they are turned on whereas the gasoline engines have t build up power before they reach their peak r.p.m range. Most heavy vehicles such as subway trains locomotives, and heavy mining equipment use electric motors because of the tremendous amount of torque they offer.

1.4 HISTORY

EVs appeared shortly after 1830 when Joseph Henry invented the first DC powered motor. Thomas Davenport is credited with building the first practical EV in 1834. In 1847 Moses Farmer build a two passenger electric car and in 1851 Charles Page invented a twenty mph electric car. Gaston Plante paved the way for early electrics when he builds a rechargeable battery in 1859.

Although the early gasoline powered cars were noisy and often broke down their range was better than that of electric cars. The demise of electric cars came in 1912 when Charles Kettering invented the electric starter. The model T revolutionized mass production and gasoline was plentiful. The golden age of the gasoline-powered car had begun.

The Golden age lasted for almost 50 years into the 1960s.However it produced a golden haze in the sky, which raised concerns about air pollution. The oil crisis of the 1970s caused another way of interest in EVs. Ford continued development of the year Sodium Sulphur battery and Chrysler teamed with GE to work on the EV-1 program.

EV activity slowed during 1980s as oil supplies were plentiful and the gas prices remained close to early 1970s levels. Cars were more fuel efficient and equipped with anti pollution devices. However EV components continued to improve with the development of solid-state control devices and more advanced motors.

1.5 CURRENT TREND

Most EVs on the road today are conversions built by hobbyists. Technological improvements have given them a choice of components to build a conversion that is comparable to today's gasoline cars.

Electric buses are also proving to be a cleaner means of transport in cities where smog is a constant health hazard. These require minimum maintenance and reduce the amount of particulate matter that enters the atmosphere. As we enter the next century the EV will become a predominant people mover in our society. The final outcome of this transition towards EVs as a viable means of transportation is an environment that will be healthier for future generations to enjoy.

An electrical vehicle consists of the following four main blocks, which replaces the similar blocks in conventional IC engine powered vehicle.

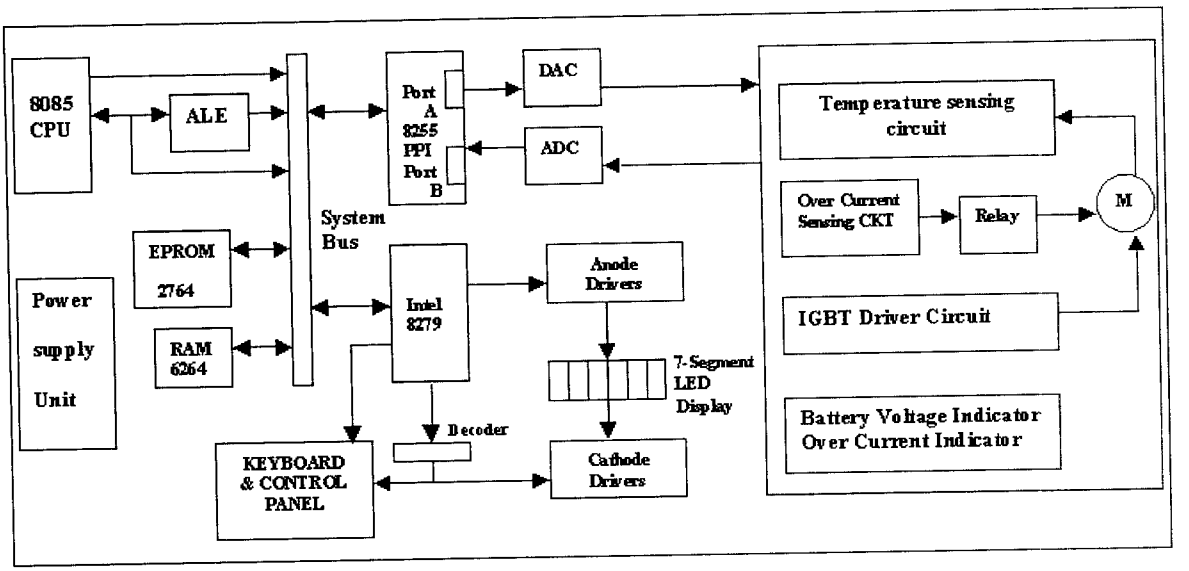
Electric drive	- Replaces the conventional IC engine
Battery	- Replaces the gasoline fuel
Chopper	- Replaces the part that controls the flow of fuel
Microprocessor	- The master controller

2. MICROPROCESSOR BASED CONTROL

Unlike automobiles based on I.C. engines, which uses mechanical systems to control its operation, an electric vehicle may use microprocessor to control all the operations of the vehicle.

That is why the microprocessor (8085) is called the MASTER CONTROLLER of our project. It governs the entire operation right from the starting of the vehicle till the shut down operation. This provides safer and stable operation.

2.1 BLOCK DIAGRAM OF μP BASED CONTROL FOR AN EV



The 8255-PPI (programmable peripheral interface) provides ADC & DAC interfacing. The 8255 PPI has 3 ports [port-A, port-B & port-C (upper & lower)], of which port-A and port-C (upper) are initialized as input ports and those of port-B and port-C (lower) are initialized as output ports.

The 8279 Provides keyboard & LED display interfacing. ADC (0808) is used for Converting analogue to digital data and that of DAC (0801) is used for Converting digital to analogue data.

2.2 CHECKING THE BATTERY VOLTAGE

In a conventional automobile driver could see the fuel level of the tank through an indicator on the dashboard. The dual of the fuel in an EV is the charge of the battery. Hence it is necessary to check the battery voltage before starting the EV. In the case of a microprocessor controlled EV, a voltage sample proportional to the battery voltage is taken and given to the ADC which converts this voltage into its equivalent 8 bit digital value. Then this value is compared with a reference voltage already stored in the memory location of the microprocessor. The two voltage levels with which the battery voltage is compared are,

LEVEL 1:

A safe voltage, above which the vehicle should always operate with.

LEVEL 2:

A lower unsafe voltage, below which the vehicle should never be operated. (This level is similar to the reserve capacity of an I.C. engine vehicle).

Since the motor is a 96V motor, 92V is taken as the first safer voltage level and 88V is taken as the second unsafe voltage level. so the present battery voltage is first checked with 92V before starting the vehicle. If it is found lesser, then a low voltage indication will be given. But still the vehicle will be in its way to operate. This indication signifies that the driver has to charge the battery immediately.

Even if the driver fails to see the indication, the vehicle operates until the battery voltage falls below the second voltage level ie.,88V. But when the battery voltage falls below 88V the vehicle will be shut down immediately along with the low voltage indication. This is similar to the condition prevailing in an I.C. engine vehicle when the fuel tank becomes empty. Now the microprocessor will not allow the vehicle to start until the battery voltage becomes more than 92V. This check up is very essential before starting or while in operation of EV. Else it leads to damage of the battery due to over discharging. The damage may be either buckling or sulphation of the plates.

2.3 STARTING PROCESS

After this process, the microprocessor executes next step of operation, which is the checking the position of the key. The key position is sensed by the '0'/ '1' input received by the microprocessor through port-A.

When the input is '1', it means that the driver is opting to start the vehicle. Until the input becomes '1', the microprocessor will not go for executing next set of instruction. The next instruction is to open all the switches of the 4-quadrant chopper and the contactor is positioned for forward operation. During successive execution of the program instructions, the position of the contactor is manipulated according to the driver's option for forward/reverse operation of the vehicle.

2.4 FORWARD/REVERSE OPERATION

The next step is to check the driver's option for forward/reverse operation. If it is forward, then the microprocessor outputs a bit pattern such that the choppers 1 & 4 are turned ON and the contactor is positioned for forward operation.

Now the current and the flux are in such a way that the motor is in the forward motoring mode. On the other hand if the driver opts for reverse operation, then the microprocessor outputs a bit pattern such that the choppers 2 & 3 are turned ON and the contactor is positioned for reverse operation.

Now the current and the flux are in such a way that the motor is in the reverse motoring mode. This in conjunction with the condition for the reverse operation of the motor. i.e., when the current in the armature and the field changes simultaneously, the direction of rotation remains unchanged. On the other hand, when the current either in the armature or the field changes, the direction of rotation changes.

2.5 SPEED CONTROL

Now the microprocessor gets the option for speed from the driver. This is taken from a variable pot operated externally by the driver. It can trace a minimum voltage of 0V and a maximum voltage of 5V along with any intermediate voltage. This voltage is proportional to the duty cycle of the chopper. Hence, this voltage is given to the microprocessor through the ADC. Now the ON time of the chopper, Ton is calculated. The time delay proportional to Ton is taken in a counter and during this Ton period, the switch corresponding to forward/ reverse operation is switched ON. After this, starts the OFF period.

As we have adopted PWM (Pulse Width Modulation) technique to control the duty cycle of the chopper, the total time period T has to be fixed. The Ton and Toff will vary depending upon the acceleration given by the driver. We have,

Ton/T α acceleration α voltage across the pot

This voltage is digitized and is given as input to the microprocessor for further processing.

2.6 CURRENT SENSING

The motor may be damaged, if the current flowing through it exceeds the rated value. Therefore the microprocessor has to check the motor current periodically. So we have used a series resistor whose voltage drop is proportional to the current flowing through the winding. This voltage drop is then fed to the microprocessor through the ADC.

If the drop across the series resistor exceeds 3V, then the microprocessor will give an alarm for over current indication.

2.7 TEMPERATURE SENSING

If the temperature of the winding exceeds a certain limit, then the motor will get damaged. Therefore the condition for over temperature is also checked. The temperature of the machine may increase due to the following reasons.

Overloading

Internal faults

For the machine to operate safely, the winding temperature should not exceed 80°c. If the temperature exceeds this limit, then the microprocessor will provide an over temperature indication. A transducer bridge followed by an instrumentation amplifier circuit senses the temperature.

2.8 REGENERATION

As the series motor drive can operate in all the 4-quadrants, there may be a possibility for regeneration ie., the condition under which the power flows from the load to the machine. Therefore, the battery can be charged with this power for a small period of time, which will further increase the running period of the vehicle. Whenever the speed of the vehicle exceeds the critical running speed, the back EMF of the motor is greater than its supply voltage. Therefore the K.E. available in the wheel is converted into electrical energy and subsequently the battery is charged. And so the microprocessor is programmed to indicate the possibility of regeneration.

During regeneration, the current reverses its direction. A resistor connected in series with the motor, senses this condition. The voltage drop developed across the series resistor, proportional to the current flowing during regeneration is taken into account for finding the occurrence of regeneration. But the polarity reversal can occur under two conditions as given below.

During driver's option for reverse operation

During regeneration

Therefore the microprocessor has to differentiate between these two possibilities. Since the ADC cannot handle –ve values, we have provided a positive offset of 5V to the –ve voltages and a +ve offset of 2.5V for voltages above 0V. After producing the offset by a summing amplifier circuit followed by an inverter circuit, the voltage is digitized and then given to the microprocessor. If the last bit is zero, it means that the current is reversed. Again to differentiate the above two conditions, the last bit is XORed with the driver's option of

The following truth table indicates the various conditions for the above operation.

Last bit	F/R bit (Driver's option)	After XOR	Condition
0	1	1	Regeneration
0	0	0	Normal
0	1	1	Normal
0	0	0	Regeneration

2.9 INTERRUPT

It is well known that any vehicle should not be accelerated to very high speed immediately after applying the mechanical brakes. Also it is not necessary to supply any voltage, under the above case. The microprocessor is so programmed that once the mechanical brakes are applied, the program execution commences from the beginning, irrespective of the present operation. To provide such a facility, we have used a sensor to sense the application of the brake. The output of the mechanical brake sensor, F/R switch and the key sensor are given to the TRAP (highest priority interrupt) pin of the microprocessor chip. Out of these outputs, the output of the brake sensor and the F/R sensor are active high and that of the key-closing sensor is active low. So the key position signal is given to the TRAP pin through a NOT gate. As soon as the TRAP pin is enabled, the microprocessor terminates the present operation and turns OFF all the choppers. It then proceeds with the execution of the program right from the beginning.

HARDWARE IMPLEMENTATION

3 HARDWARE DESIGN

3.1 SPEED CONTROL CIRCUIT

The speed of a DC motor is given by,

$$N = A\,(V - (Ia\,Ra))/Z\Phi P$$

$$= K\,(V - (Ia\,Ra))/\Phi \quad \text{r.p.s}$$

Where Ra = armature circuit resistance

V=supply voltage

Φ=flux per pole

From the above equation it is obvious that speed can be controlled by varying

1. Flux (flux control)
2. Armature circuit resistance (Rheostatic control)
3. The applied voltage (voltage control)

In our project we have employed the voltage control method with the use of power devices.

DC chopper method is the efficient method for smooth speed control.

3.1.1 PRINCIPLE

A chopper is a static device that provides a variable DC output voltage from a fixed DC input voltage. A chopper is usually represented, as a switch with an arrow the device used as a chopper may be any of the power semiconductor devices.

The choppers are classified into different types depending on the operation in four quadrants. A four quadrant DC chopper finds itself ahead of 1 and 2 quadrant choppers because of its ability to operate in four quadrants. This simplifies the hardware because a single chopper circuit can look after the forward, reverse and braking operations.

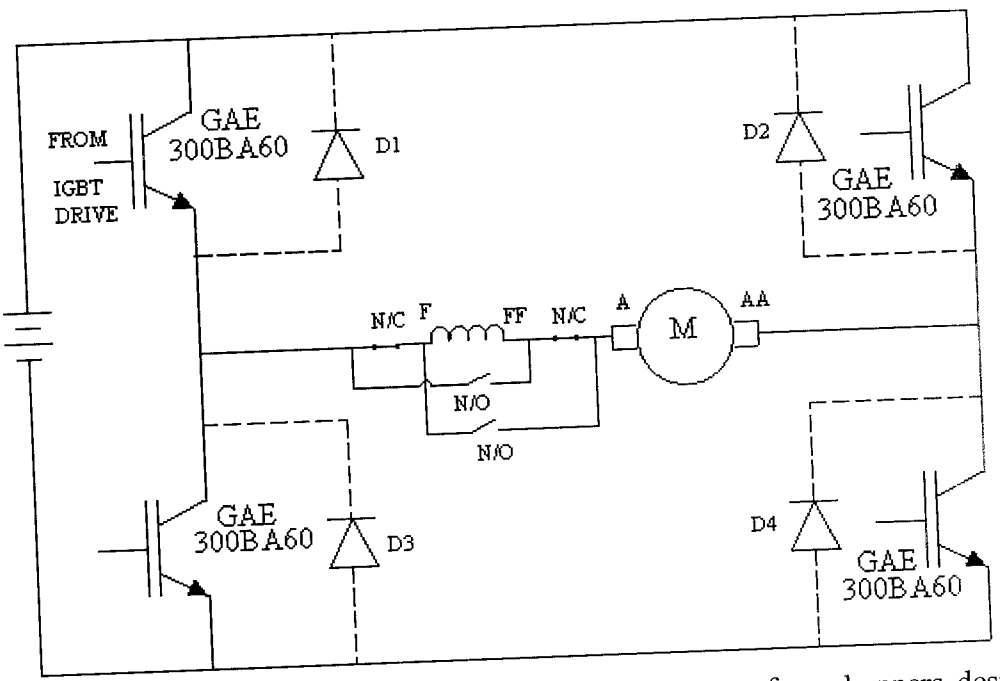
The action of a DC chopper is to apply the unidirectional voltage pulses to the load. By regulating the duty cycle of the conduction pulses the overload voltage can be controlled. The output voltage is proportional to the duty cycle of the chopper. Accordingly the speed can be controlled.

3.1.2 REGENERATION IN FOUR-QUADRANT CHOPPER

In the fourth quadrant, the regenerative breaking is obtained. In regenerative breaking most of the braking energy is returned to the supply. The condition for regeneration is that the rotational emf must be more than the applied voltage so that the current is reversed and mode of operation changes from motoring to generating. Also the driver can select this mode of operation when the vehicle moves in a slope and there is no need for the motoring operation. According to the drivers option the drivers option the microprocessor generates the signals for reversing the field.

It is observed that about 35% of the energy put into an automotive vehicle during typical urban tractions is recoverable by regenerative braking.

CIRCUIT DIAGRAM:



In the above figure IGBT acts as the chopper. There are four choppers designated as CH1, CH2, CH3 and CH4.according to the driver's option whether to drive in forward or reverse direction the choppers get turned ON. During the forward mode of operation the choppers CH1 &CH4 get turned ON. The load voltage is positive if the ON time is longer than the OFF time. The load current may be either positive. The positive load current flows through CH1, CH4, D3, and D2 and on adjustment of duty ratio, the load current may be negative and flows through D1 and D4.

During the reverse operating mode the choppers CH2 and CH3 get turned ON. The load current may be negative and flows through CH2, CH3, D1 and D4.

3.1.3 IGBT BASICS

Recent technology advances in power electronics have arisen primarily from improvements in semiconductor power devices, with insulated gate bipolar transistors (IGBT) leading the market today for medium power applications. IGBTs special features includes a MOS input gate, high switching speed, low conduction voltage, high current carrying capability and a high degree of robustness. The IGBT combines the positive attributes of BJTs and MOSFETs. BJTs have lower on state conduction loses but have longer switching times especially at turn off while MOSFETs can be turned ON and OFF much faster but their on state conduction loses are larger. Hence IGBTs have lower on state voltage drop with fast switching speeds.

IGBT is chosen because of the following advantages

- Low on state voltage drop
- On state voltage varies very little with increasing temperature
- Faster switching time.
- Minimum need for snubber circuit.

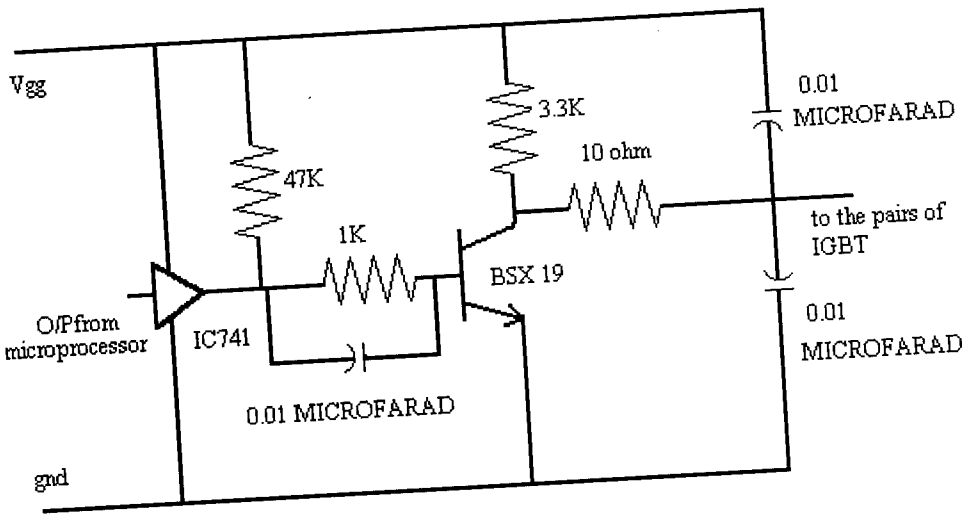
3.1.4 DESIGN OF IGBT DRIVER

The pulses that trigger the IGBT should have mere zero rise and fall time i.e., the time taken by the pulses to reach its maximum amplitude and to reach zero crossing from the maximum amplitude should be mere zero.

But the triggering pulses from the microprocessor have certain definite rise time as well as fall time due to supply fluctuations.

This has to be rectified before the triggering signal reaches the IGBT. For this purpose a Schmitt trigger followed by an amplifier is used in between the microprocessor and the IGBT.The Schmitt trigger is used for producing the pulse train with the mere zero rise and fall time. The amplifier then amplifies it.

The combined circuit of Schmitt trigger and amplifier is called IGBT device driver circuit.



The upper threshold voltage and the lower threshold voltage of the Schmitt trigger is given by,

$$Vut = Vlt = (R2 * Vsat) / (R1+R2)$$

In the above circuit the value if R1 is taken as 4.7KΩ.the output of the driver circuit is dropped at the resistance R2 whose value is taken as 1KΩ.in order to improve the transient stability of the circuit, a capacitor of value 0.001μF is connected across R2.The amplifier should be such that it should have higher bandwidth and faster switching speed. The bandwidth of the transistor used is of the order of 500KHz.The current handling capacity is about 300mA, which is sufficient to drive the base of IGBT.

The capacitors C1 and C2 are used to avoid electromagnetic interference. In order to provide necessary base and collector bias for the transistor the value of R3 and R4 is taken as 10KΩ and 3.3KΩ respectively

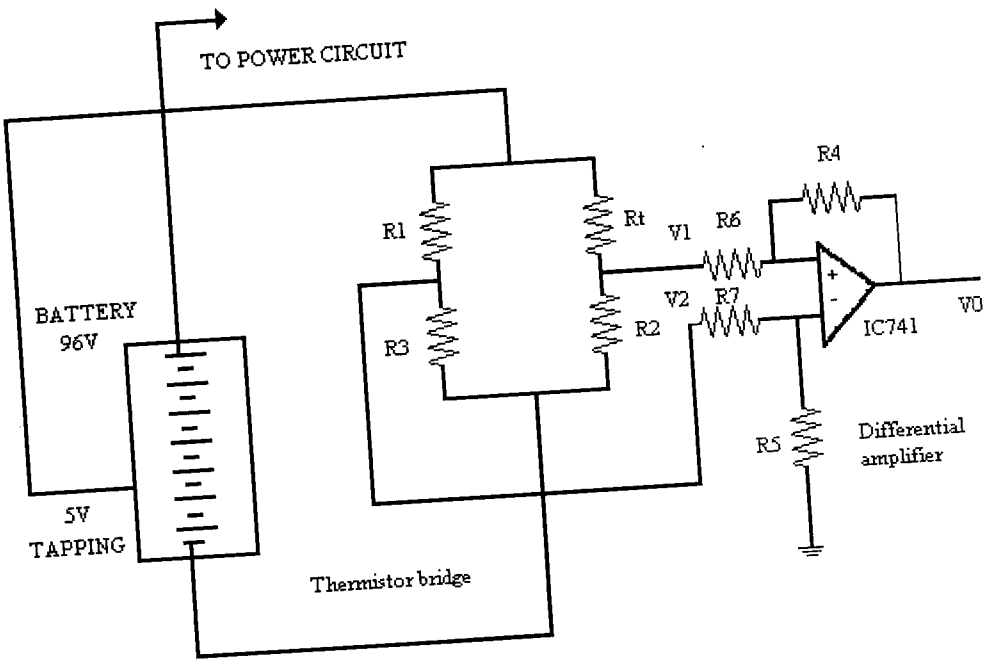
3.2 DESIGN OF TEMPERATURE SENSING CIRCUIT

The maximum permissible temperature of the machine considered here is 90°C .An over temperature indication is given when the temperature exceeds the permissible value. the machine should shut down.

For this, we have designed a thermistor transducer bridge, which can produce an output of nearly 4.5V at maximum permissible temperature. The design of bridge is such that the output must not exceed 5V.this is because the reference voltage given to ADC is only 5V.Also the ADC cannot respond to a voltage above 5V and hence the severity of the faults occurring cannot be known.

Before designing a thermistor bridge, the variation of the resistance of thermistor along with the temperature has to be considered. From the above figure it is known that when the temperature of the thermistor is 0°C, the resistance is 10KΩ. But when the temperature increases above 0°C, the resistance starts decreasing. When the temperature is at 90°C, the resistance falls nearly to 0.5KΩ. Using this property, a suitable temperature sensing circuit is designed using an instrumentation amplifier.

CIRCUIT DIAGRAM:



3.2.1 CIRCUIT ANALYSIS

The output of the differential amplifier is given by,

$$Vo=(R4/R6)(V1-V2)$$

The above output voltage is for the condition,

Choose the value of RT to be 10KΩ

Under abnormal conditions (i.e., when the temperature goes beyond 90°C), we need an output voltage of 4.5V.This happens when RT=0.5KΩ.

Under balanced conditions,

$$R1/RT = R3/R2$$

So choose,

$$R1 = RT = 10K\Omega$$

$$R2 = R3 = 2K\Omega$$

Therefore during normal operating conditions,

$$VR2 = VR3 = 0.833V$$

At such conditions the output of the differential amplifier will be 0V.

Under abnormal conditions, voltage across R2 is given by,

$$VR2 = (5*R2) / (R2+RT)$$

On substituting all the above given values in VR2, we get,

$$VR2 = 4V = V1$$

$$V2 = 0.833V$$

Therefore the output voltage,

$$Vo=V1-V2 = 3.16\ V$$

But under abnormal conditions the output voltage should lie between 4 and 5V.

So we have to provide a gain of,

$$R4/R6 = 1.42$$

Fixing the value of R4 to 5KΩ,

$$R6 = 5 / 1.42 = 3.5K\Omega$$

Therefore,

$$R4 = 5K\Omega$$

$$R6 = 3.5K\Omega$$

Now,

$$Vo = (V1-V2)\ (R4 / R6)$$

$$= 3.16*1.42$$

$$= 4.6\ V$$

When the temperature is 80°C, the output voltage Vo becomes 4V.At such times; an alarm indication is given to the driver.

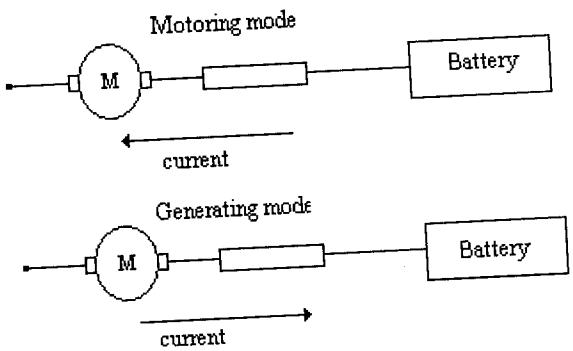
Thus by using this circuit, safe operation is achieved.

3.3 OVERCURRENT SENSING CIRCUIT

When the current flowing through the motor exceeds the rated value, the motor may get damaged heavily. A series resistor connected to it measures this overcurrent. The drop across the resistor is proportional to the current flowing through the winding.

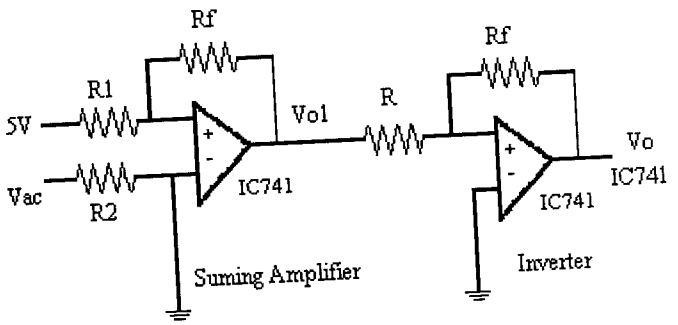
The ADC 0808 is a unipolar one that cannot accept a negative signal as its input. But in the motor circuit the current may flow in either directions i.e., from supply to motor (motoring) or from motor to supply (generating at the time of regeneration). As the input voltage given to ADC should exceed 5V,a safe drop of 3V is considered across the series resistor. For the maximum current of 160 A, the resistance value will be = (3 / 160) = 0.01875Ω. Since a series resistor is taken for measuring current, the polarity of the drop across the resistor changes with the change in the direction of the current as shown below.

CIRCUIT DIAGRAM:



As the ADC 0808 cannot accept a negative signal, it is converted into its equivalent positive value by a summing amplifier followed by an inverter circuit as shown in the following circuit:

CIRCUIT DIAGRAM



This circuit will give the correct equivalent positive reading for negative values obtained. The drop across the series resistor is given as Vac to the summing circuit. The output of the summing circuit (V01) is given as input to the inverter circuit whose output is a positive one.

Output of the summing amplifier is given by,

$$V01 = -5(Rf/Ro) - Vac(Rf/R2)$$

Choosing R1 = R2 = R, we get,

$$V01 = -(Rf/Ro)(5+Vac)$$

Output equation of the inverter is given by,

$$Vo = (Rf/Ro)(5+Vac)$$

Choosing Rf = 5KΩ and R = 10KΩ we have,

$$Vo = 2.5+(Vac/2)$$

When the motor current is 160A,the drop Vac will be 3V and the output of the summing amplifier is 4V.So when the summing amplifier output is 4V,the vehicle should shut down. Similarly when the current is 150A,the drop is 2.8V and the output of the summing circuit is 3.9V.Now the processor gives an over current indication to the driver.

The range of a.c. input signal is ± 5V.For the variation in input voltage from +5V to –5V,the output Vo varies from 0V to 5V.

Few values are shown below:

INPUT Vac (Volts)	OUTPUT Vo (Volts)
-5	0
0	2.5
+5	5

The output Vo of the inverter circuit is applied to an S/H circuit whose output is given to the input terminal of the ADC 0808.

The results of the conversion is shown below:

Analog input voltage (volts)	Digital output (volts)
-5	00
-4	1C
-3	30
-2	4A
-1	64
0	80
1	93
2	B9
3	C7
4	ED
5	FF

3.4 DESIGN OF VOLTAGE REGULATOR

Only the battery has to supply all the control and power circuits in the EV system. The battery voltage of 96V cannot be given as such for biasing various components in the circuit.

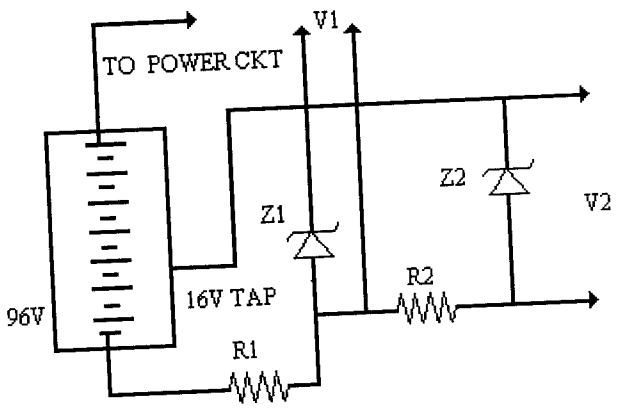
In our case we need two different voltage levels,

1) 5V for microprocessor,ADC and differential amplifier,

2) 12V for IGBT driver circuit.

But it is the fact that all the measuring circuits and control operations will be proper only with proper biasing. But the battery voltage may vary with its present charge conditions. So the voltage given to these circuits should be regulated. For that purpose, a voltage regulator circuit is employed.

CIRCUIT DIAGRAM



3.4.1 CIRCUIT OPERATION

- A 16V tapping is taken from the battery stack that comprises of 48 individual 2V cells and from this two regulators are connected.
- Zener Z1 is for 12V circuits and zener Z2 is for 5V circuits. Power rating of both the zener diodes will be 3W.
- Now Vtap = 16V and Vz1=12V.So the drop in between the tapping of the battery and zener z1 will be 4V.Full load current of Z1 = 3/12 = 250mA.
- Assuming that only 25% of the alone is flowing in the circuit,

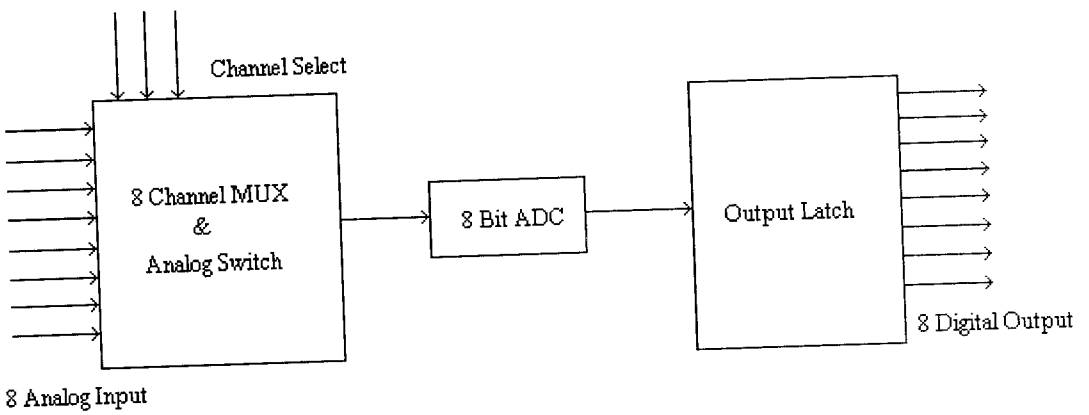
$$R = 4 / (25\% \text{ of } 250 \text{ mA}) = 64\Omega = R1.$$

- R2 is in between Z1 and Z2 and hence there is a drop of 7V.Full load current of Z2 = (3/5) = 0.6A and 25% of 0.6A is 0.15A.
- R2=7/0.15 = 46.666Ω.
- Standard values of R1 and R2 will be 62Ω and 47Ω respectively.

3.5 SELECTION OF ADC

The selection of ADC depends upon the number of variables (parameters) taken into consideration. If there is only one parameter to be converted into digital form, then single analog to digital converter is sufficient. If there are number of parameters to be considered, then it is not economical to employ individual ADCs to each parameter. For this purpose, multichannel ADCs are used to handle all the parameters. A multichannel ADC consist of a multiplexer to select the parameters one by one according to the control signals given to it. The microprocessor gives out the corresponding control signal bit

CIRCUIT DIAGRAM



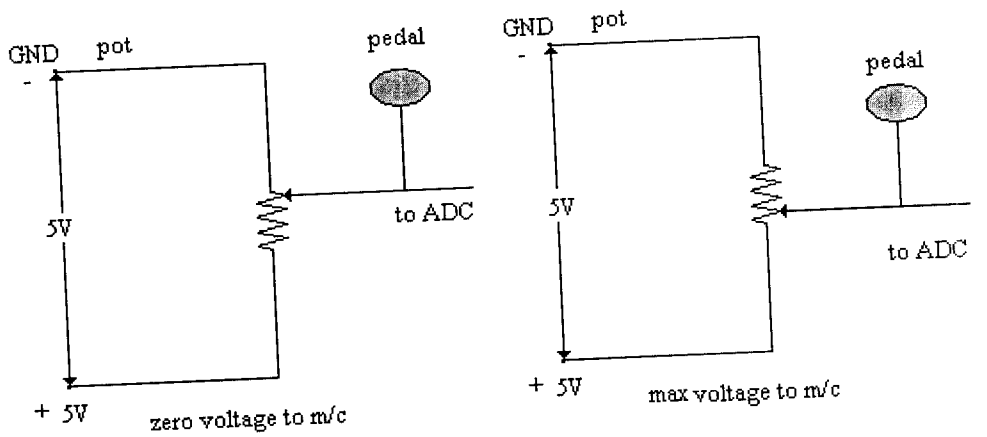
3.6 SELECTION OF PEDAL POTENTIOMETER

In any automobile, when the accelerator pedal is at rest, the speed of the engine is zero. When the pedal is pressed, the speed increases correspondingly and when it is in its [illegible] the speed should be maximum. In case of an IC engine based

automobile, with the pressing of the pedal, the fuel supplied to the engine increases. Similarly in our case, with the pedal at its rest the voltage supplied to the machine increases and hence the duty cycle of the chopper should be zero. They should increase correspondingly with the pressing of the pedal.

The voltage should be maximum to the machine when the pedal is at its maximum position. This is shown in the figure

CIRCUIT DIAGRAM



For such a pedal potentiometer, we have selected a POT with a resistance of 10K value.

The maximum current flowing through the pot may be,

$$I = V/R$$
$$= 5/10000$$
$$= 0.0005 \text{ A}$$

Power can be,

$$P = I*I*R$$
$$= 0.0005*0.0005*10000$$
$$= 2.5 \text{ mW}$$

So on the safer side, we can take a value of 3W for the POT.

CONVERSION

4. CONVERSION

A normal battery operated EV can be converted to a µp controlled EV, if the above discussed hardware circuits are added to the existing EV. But still partial requirements are only fulfilled. Our objective will be satisfied only if the necessary software has also been included. Such a µp-controlled vehicle will possess the following advantages.

4.1 ADVANTAGES:

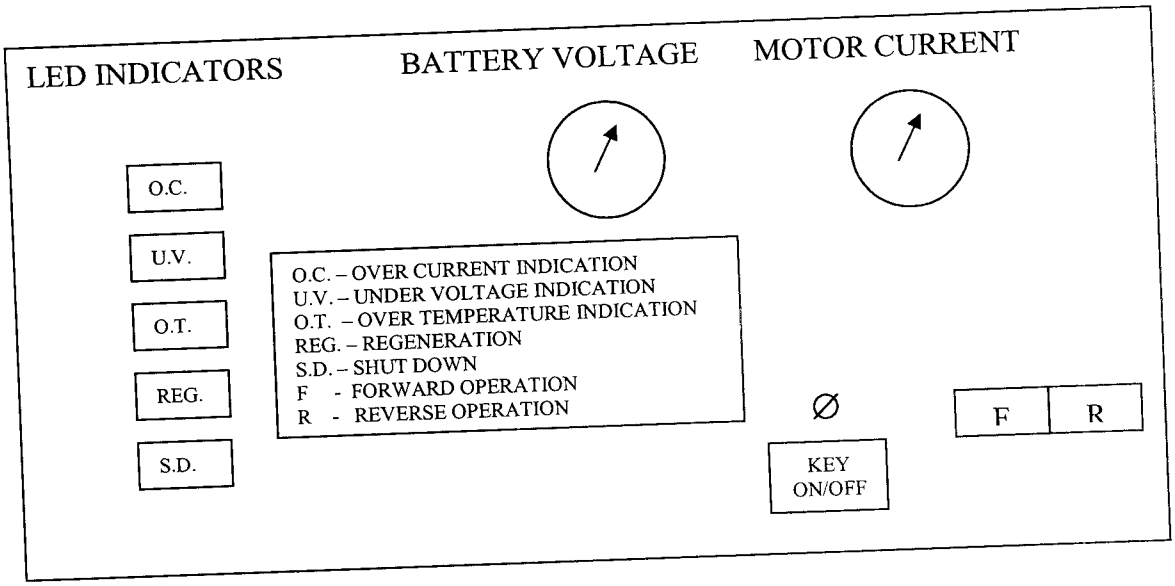
- Precise and accurate speed control
- Ensures safer operation
- Almost nil maintenance
- Cost effective
- Application oriented speed control

The vehicle so designed will have the following specifications along with a specially designed dashboard shown below.

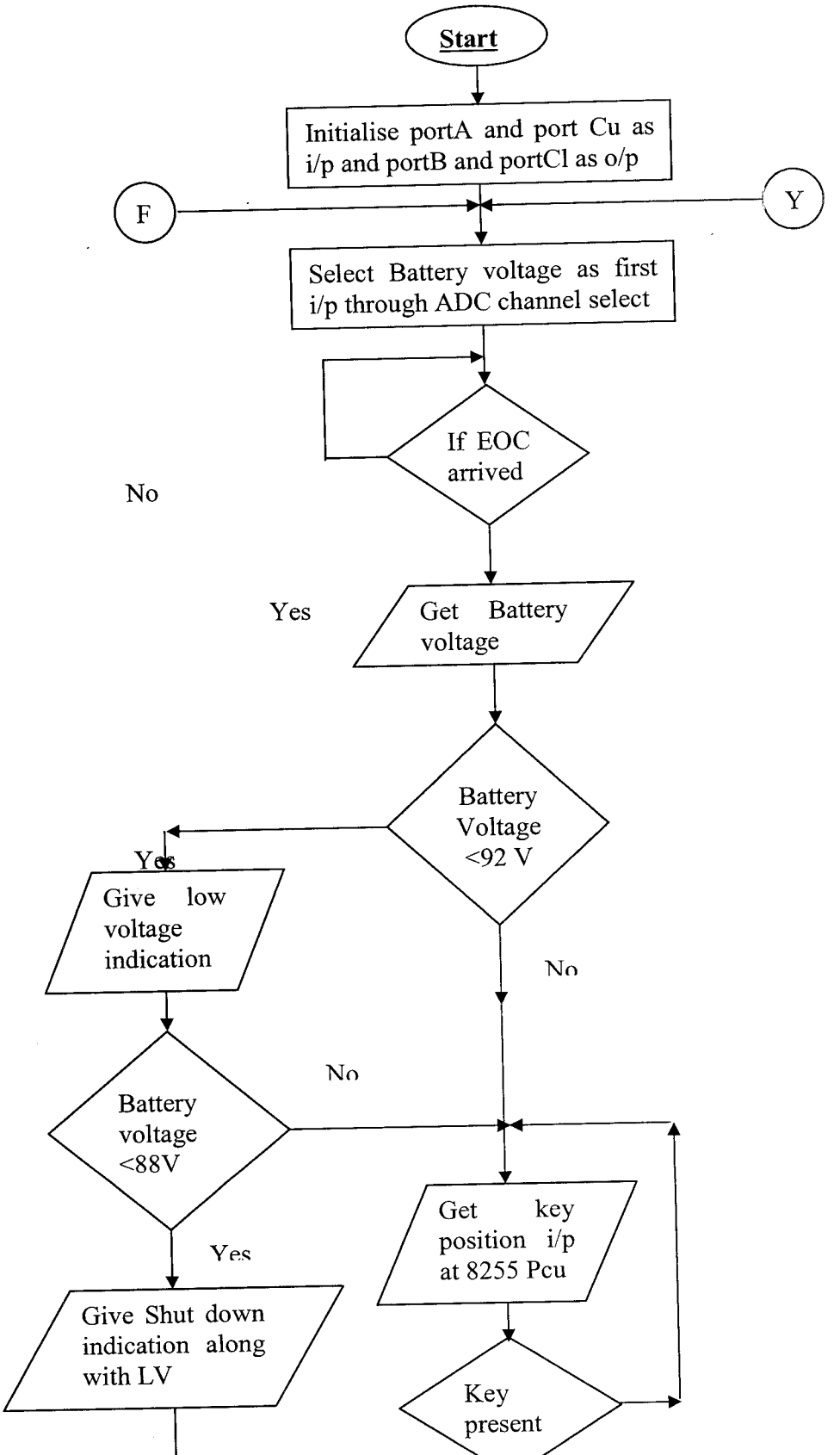
4.2 VEHICLE SPECIFICATIONS:

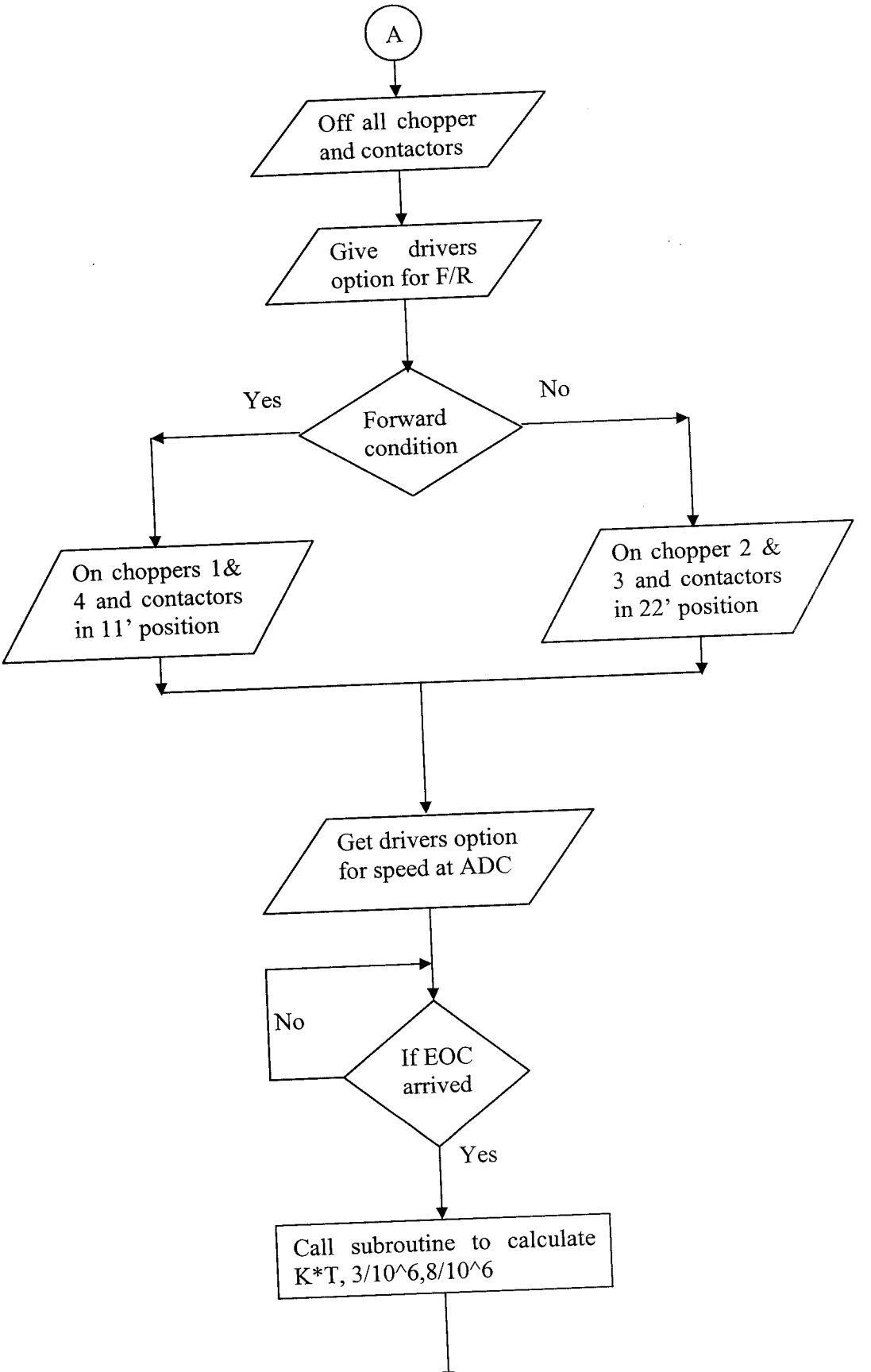
Unloaded weight	2,600 kg
Pay load	13 persons
Range/charge	Upto 100km @ 40 km/hr
Cruising speed	40 km/hr
Max. Speed	50 km/hr
Acceleration	0.14 km/hr in 4 sec
Consumption	0.7 kw-hr/km
Battery charging time (Lead Acid Battery)	8 hrs

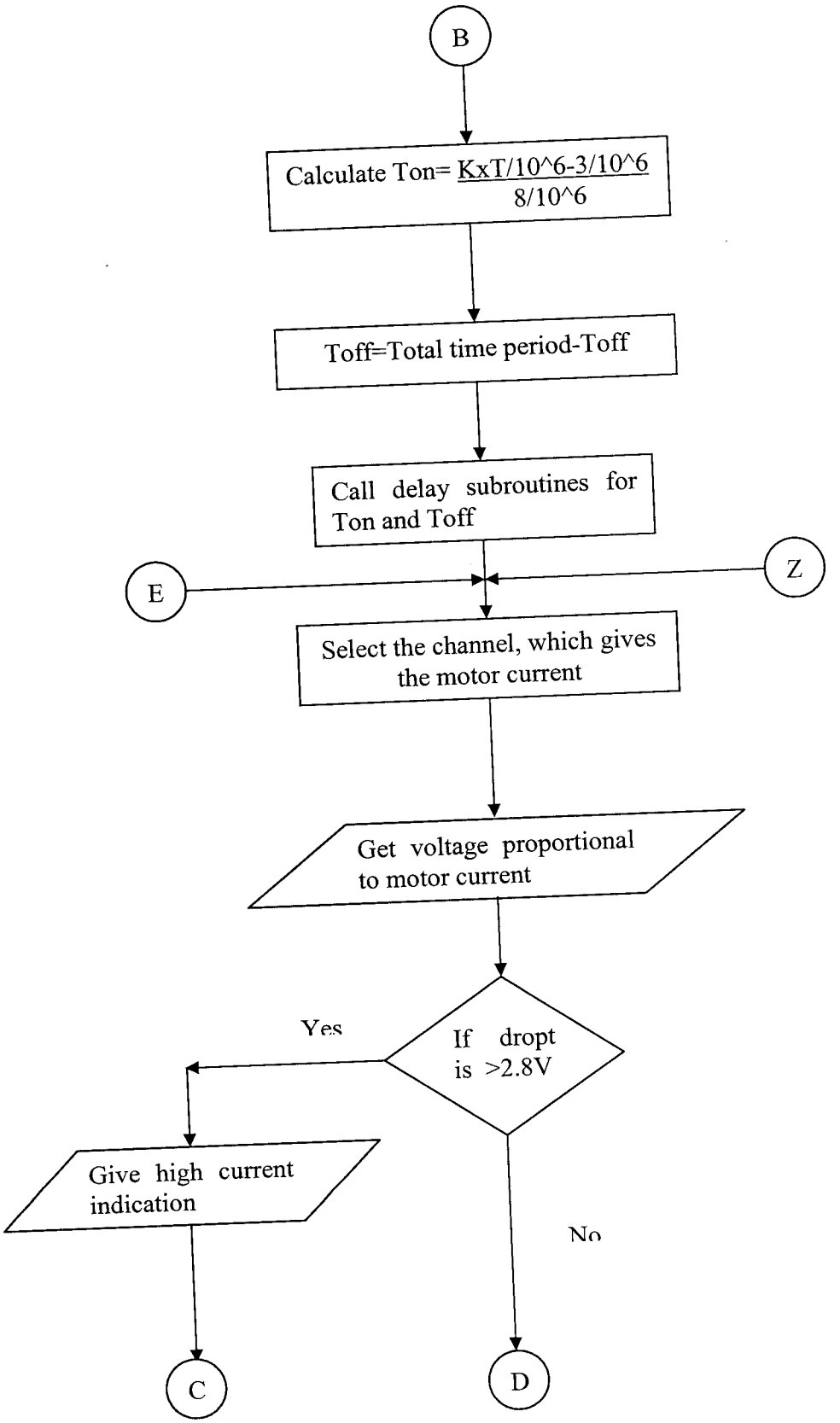
4.3 DASH BOARD DESIGN:

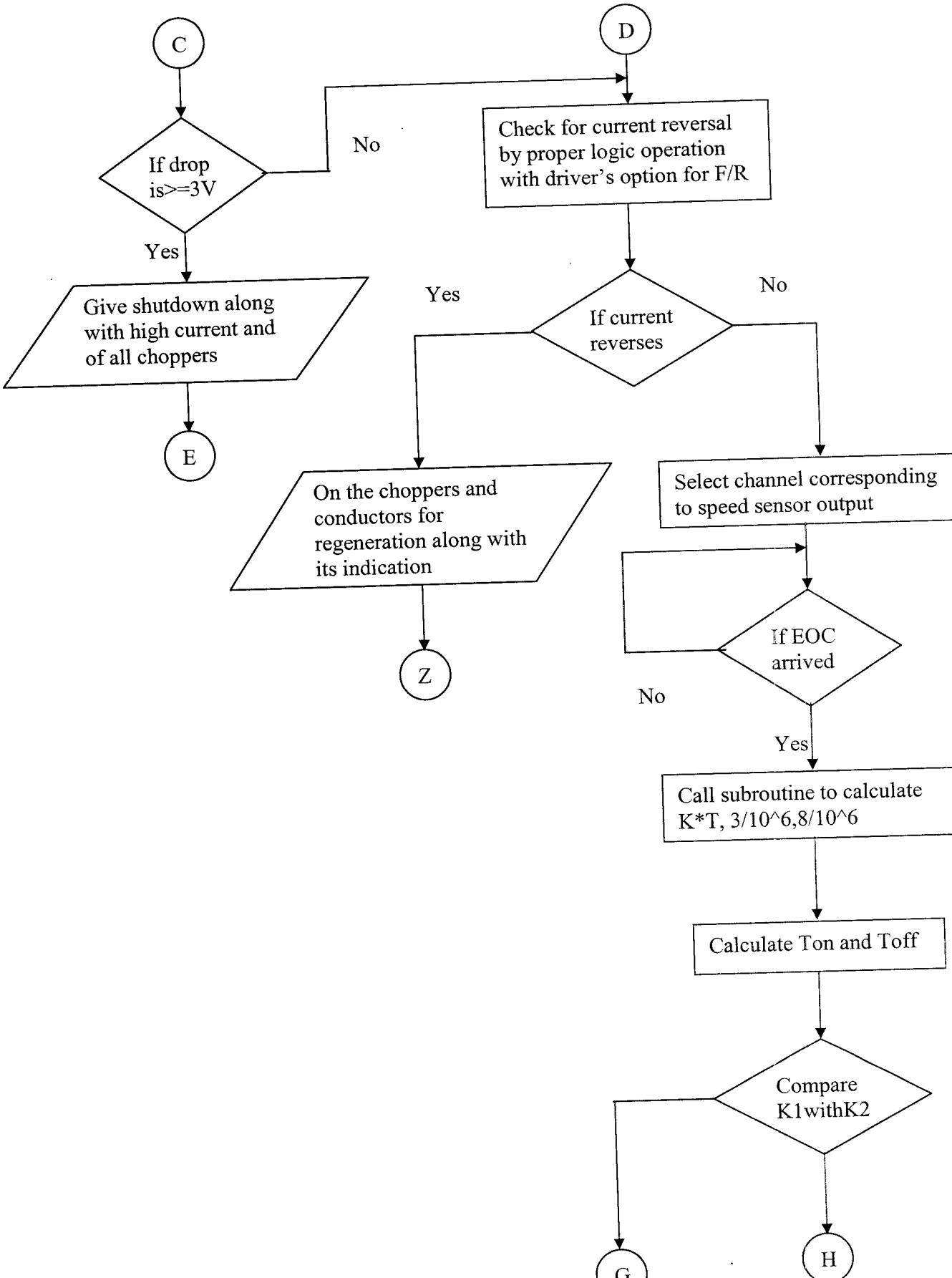


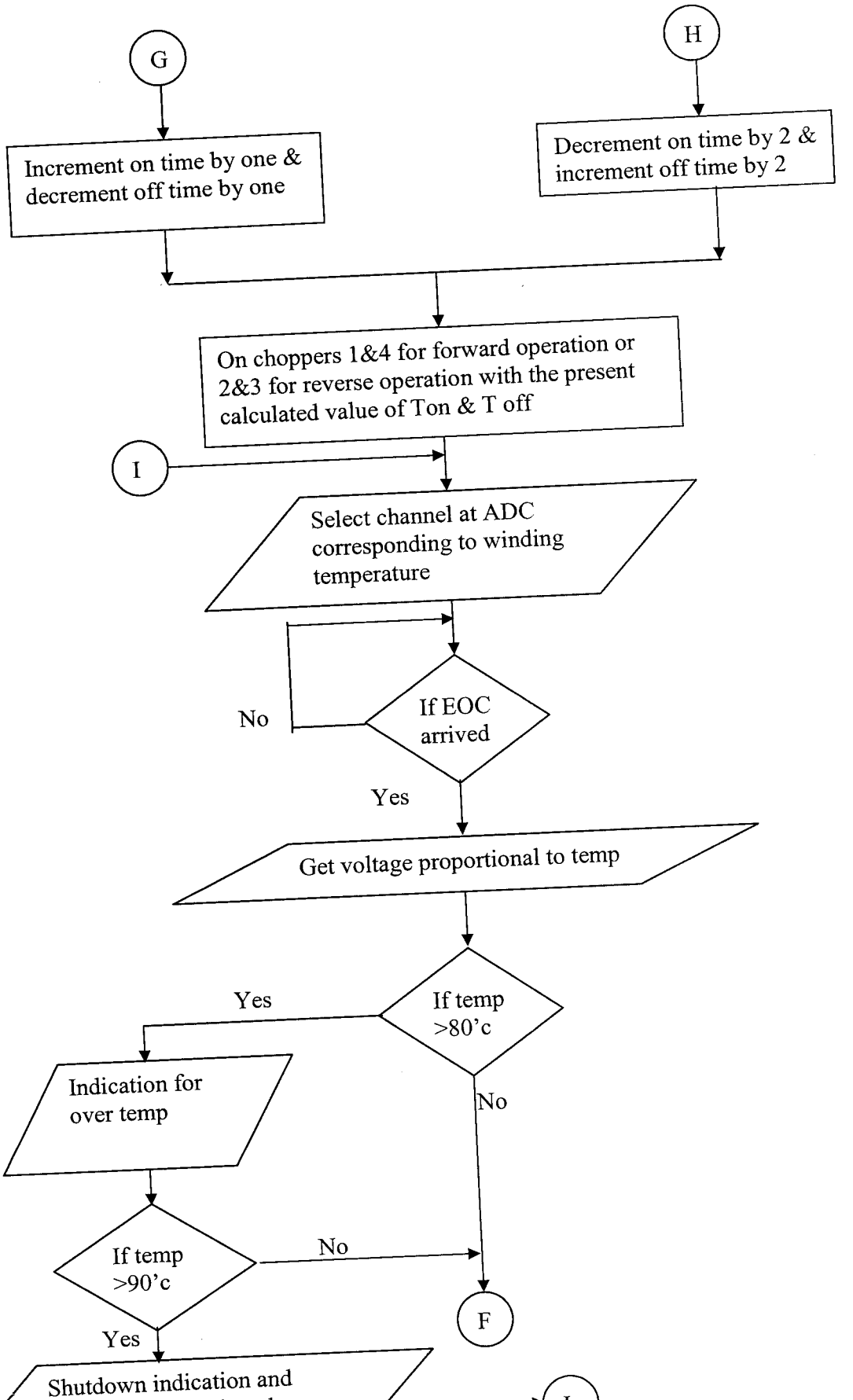
SOFTWARE CODING


Start
Initialise portA and port Cu as i/p and portB and portCl as o/p
F
Y
Select Battery voltage as first i/p through ADC channel select
If EOC arrived
No
Yes
Get Battery voltage
Battery Voltage <92 V
Yes
Give low voltage indication
No
Battery voltage <88V
No
Yes
Get key position i/p at 8255 Pcu
Give Shut down indication along with LV
Key present


A
Off all chopper and contactors
Give drivers option for F/R
Forward condition
Yes
No
On choppers 1& 4 and contactors in 11' position
On chopper 2 & 3 and contactors in 22' position
Get drivers option for speed at ADC
No
If EOC arrived
Yes
Call subroutine to calculate K*T, 3/10^6,8/10^6


B
Calculate Ton= KxT/10^6-3/10^6 / 8/10^6
Toff=Total time period-Toff
Call delay subroutines for Ton and Toff
E
Z
Select the channel, which gives the motor current
Get voltage proportional to motor current
If dropt is >2.8V
Yes
No
Give high current indication
C
D


C
If drop is>=3V
No
Yes
Give shutdown along with high current and of all choppers
E
D
Check for current reversal by proper logic operation with driver's option for F/R
Yes
If current reverses
No
On the choppers and conductors for regeneration along with its indication
Z
Select channel corresponding to speed sensor output
If EOC arrived
No
Yes
Call subroutine to calculate K*T, 3/10^6,8/10^6
Calculate Ton and Toff
Compare K1withK2
G
H


G
H
Increment on time by one & decrement off time by one
Decrement on time by 2 & increment off time by 2
On choppers 1&4 for forward operation or 2&3 for reverse operation with the present calculated value of Ton & T off
I
Select channel at ADC corresponding to winding temperature
No
If EOC arrived
Yes
Get voltage proportional to temp
Yes
If temp >80'c
Indication for over temp
No
If temp >90'c
No
F
Yes
Shutdown indication and

80B8	C2		JNZ 80B5	
80B9		B5		
80BA		80		
80BB	DB		IN 80	Get current through Pa
80BC		80		
80BD	57		MOV D,A	Store A in D
80BE	FE		CPI C6	Check for over current
80BF		C6		
80C0	D2		JNC 80F7	If yes jump to 80f5
80C1		F7		
80C2		80		
80C3	07		RLC	If no check for regeneration
80C4	D3		JNC 80DB	If carry , reverse the
80C5		DB		contactor switch
80C6		80		
80C7	06		MVI B,FF	If carry is not present
80C8		FF		regeneration is during
80C9	7A		MOV A,D	reverse operation
80CA	A8		XRA B	
80CB	CA		JZ 80E9	
80CC		E9		
80CD		80		
80CE	DE		MVI A,00	
80CF		00		
80D0	D3		OUT 81	
80D1		81		
80D2	C3		JMP 8109	
80D3		81		
80D4		09		
80D5	03		MVI B,00	
80D6		00		

80D7	7A		MOV A,D	
80D8	CA		XRA B	
80D9	A2		JZ 80F0	
80DA		F0		
80DB		80		
80DC	3E		MVI A,00	
80DD		00		
80DE	D3		OUT 81	
80DF		81		
80E0	C3		JMP 8109	
80E1		09		
80E2		81		
80E3	3E		MVI A,12	Indication for regeneration
80E4		12		open all the switch with
80E5	D3		OUT 81	reversal of contactor
80E6		81		
80E7	C3		JMP 80B1	
80E8		B1		
80E9		80		
80EA	3E		MVI A,10	Indication for regeneration
80EB		10		
80EC	D2		OUT 81	
80ED		81		
80EE	C3		JMP 80B1	
80EF		B1		
80F0		80		
80F1	3E		MVI A,20	Indication for over current
80F2		20		
80F3	D3		OUT 81	
80F4		81		
80F5	DB		IN 80	

80F6		80		
80F7	FE		CPI CC	Check for current that
80F8		CC		equal to 3V
80F9	D2		JNC 8105	
80FA		05		
80FB		81		
80FC	C3		JMP 80C9	
80FD		C9		
80FE		80		
80FF	3E		MVI A,90	
8100		90		Indicate the vehicle should
8101	D3		OUT 81	not be run now
8102		81		
8103	3E		MVI A,0B	Get the speed sensor
8104		0B		output as the next input to
8105	D3		OUT 82	the ADC
8106		82		
8107	DB		IN 82	
8108		82		
8109	FE		CPI E0	Check for the arrival of the
810A		E0		EOC signal
810B	CA		JZ 8119	
810C		19		
810D		81		
810E	FE		CPI D0	
810F		D0		
8110	C2		JNZ 810D	
8111		0D		
8112		81		
8113	CD		CALL B020	Program to calculate time
8114		20		

8115		D0		
8116	67		MOV H,A	
8117	3E		MVI A,03	
8118		03		
8119	CD		CALL B050	
811A		B0		
811B		50		
811C	6F		MOV L,A	
811D	7C		MOV A,H	
811E	90		SBB L	
811F	67		MOV H,A	
8120	3E		MVI A,08	
8121		08		
8122	CD		CALL B050	
8123		50		
8124		B0		
8125	47		MOV B,A	
8126	CD		CALL B070	
8127		70		
8128		B0		
8129	26		MVI H,00	
812A		00		
812B	59		MOV E,C	
812C	7D		MOV A,L	
812D	BB		CMP E	
812E	D2		JZC 8139	Compare the duty cycle
812F		39		stored in L
8130		81		With that of present duty
8131	2C		INRL	cycle stored in E
8132	0D		DCR C	
8133	CA		JZ 813E	

8134		3E		
8135		81		
8136	2D		DCR L	
8137	0C		INR C	
8138	06		MVI D,00	
8139		00		
813A	DB		IN 82	
813B		82		
813C	FE		CPI 60	Check for forward / reverse operation
813D		60		
813E	CA		JZ 815D	
813F		81		
8140		5D		
8141	FE		CPI 50	
8142		50		
8143	C2		JNZ 8140	
8144		40		
8145		81		
8146	3E		MVI A,06	If reverse, then execute
8147		06		delay program with new on
8148	D3		OUT 81	time count obtained on
8149		81		close loop
814A	CD		CALL B003	Execute new off time count
814B		03		
814C		B0		
814D	3E		MVI A,00	
814E		00		
814F	B3		OUT 81	
8150		81		
8151	CD		CALL B103	
8152		03		

8153		B1		
8154	C3		JMP 8163	
8155		63		
8156		81		
8157	3E		MVI A,01	If forward, then execute the
8158		01		delay for on time count&
8159	D3		OUT 81	new off time count
815A		81		
815B	CD		CALL B003	
815C		03		
815D		B0		
815E	3E		MVI A,00	
815F		00		
8160	D3		OUT 81	
8161		81		
8162	CD		CALL B003	
8163		B0		
8164		03		
8165	3E		MVI A,0C	Get temperature
8166		0C		
8167	D3		OUT 82	
8168		82		
8169	DB		IN 82	
816A		82		
816B	FE		CPI E0	Check for EOC signal
816C		E0		arrival with key position on
816D	CA		JZ 8195	& with f/r operation
816E		95		
816F		81		
8170	FE		CPI D0	
8171		D0		

8172	C2		JNZ 816F	
8173		6F		
8174		81		
8175	DB		IN 80	Get temperature through the port A
8176		80		
8177	FE		CPI CC	Check for temperature
8178		CC		
8179	DA		JC 8192	
817A		92		
817B		81		
817C	3E		MVI A,80	If > 80 C indicate for over temperature
817D		80		
817E	D3		OUT 81	
817F		81		
8180	DB		IN 81	
8181		81		
8182	FE		CPI E6	Check for over temperature > 90C
8183		E6		
8184	DA		JC 8192	If yes indicate shutdown and also over temp indication
8185		92		
8186		81		
8187	3E		MVI A,C0	
8188		C0		
8189	D3		OUT 81	
818A		81		
818B	C3		JMP 8004	
818C		04		
818D		80		

SALIENT FEATURE

6. SALIENT FEATURES

- Ensures safer operation as battery voltage is 1st checked before starting the vehicle.
- Precise speed control is achieved using IGBT driving circuit depending on the application.
- Power loss is low as compared with rheostatic control.
- As temperature-tripping circuit is designed, this enables safer operation of the motor and the other auxiliary circuits.
- As braking is of regenerative type, smoother operation of the vehicle is achieved.
- Current sensing and tripping circuits are used to ensure that the load current doesn't exceed the safer current limits.
- No need of external power supply for our design circuit as we have employed the battery that is already existing in the EV.
- Provisions for further enhancement of EV can be implemented by making slight changes in the coding alone.

CONCLUTION

CONCLUSION

The entire hardware and software that controls the complete operation of an electric vehicle has been successfully developed. The multi-speeded electric vehicle that we have designed is perfectly suitable for the internal transportation at BHEL, Trichy. The vehicle can operate both in forward and reverse direction along with regenerative braking.

Nowadays, hybrid electric vehicles are available in the market commercially. The idea behind the hybrid technology is the ability of the vehicle to run in both conventional fuels as well as in traction battery. The vehicle can operate normally in any of the modes. Whenever the voltage level in the battery reaches below the safe operating value, then the vehicle will immediately switch over to I.C. engine and vice versa.

The same logic and software that we have employed in our project can be implemented in hybrid technology, if slight modifications are done on the coding part alone. Also the entire circuit can be controlled using Microcontroller instead of the Microprocessor so that, the cost of the control circuitry can be reduced greatly.

APPENDIX

APPENDIX

IGBT

Type	GAE300BA60
Current Handling Capacity	300 A
Delay Time, Ton	0.4 ms
Delay Time, Toff	0.8 ms
Rise Time	0.2 ms
Fall Time	0.8 ms
Reverse Recovery Time	0.1 ms

ADC 0808

Input Range	± 5 V or 10 V
Supply Voltage	5 Vdc & - 12 Vdc
Resolution	8 bits
Linearity	± 1 LSB
Conversion Speed	40 Clk Periods
Clock Range	50 – 800 kHz

BSX 19

Current Handling Capacity	300 mA
Voltage Handling Capacity	30 V
h_{fe}	300
Band Width	500 kHz

CONTACTOR

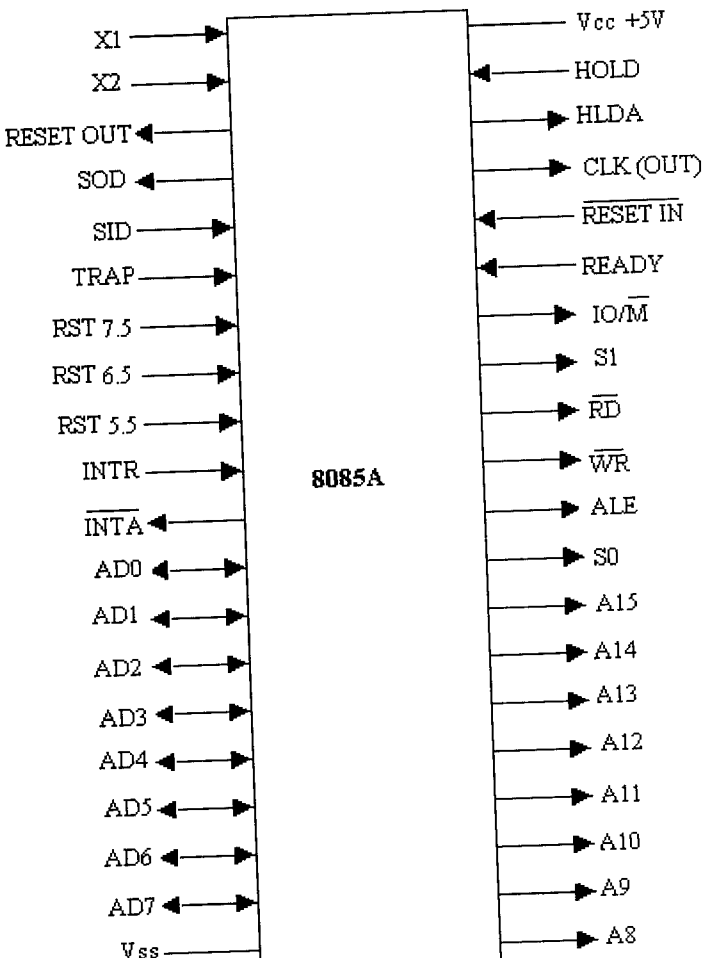
Voltage Rating	12 V
Current Rating	200 mA

A.1 INTEL MICROPROCESSOR 8085

The INTEL 8085 is an 8-bit microprocessor. It operates on an 8-bit data and uses 16-bit address. Since it uses 16-bit address, it can directly address 64K memory locations. The 8085 are designed using NMOS transistor in 40 pins DIP. It required a signal power supply of +5 volts. The 8085 generate a clock signal internally and divide by two for internal operations.

The 8085 are available in two versions 8085A and 8085 A-2 with maximum internal clock frequency of 3.03 MHz and 5 MHz respectively. Thus the pin configuration of 8085 is shown in figure.

A.1.1 PIN DIAGRAM (fig A.1)



The lower-order address byte and data lines AD0 to AD7are multiplexed. At the beginning of a machines cycle the address is given out on AD0 to AD7 and it is latched into external latch by using ALE. Then the lines AD0 to AD7 are used to carry data. The pins A8 to A 15 are unidirectional and contain the high bit of the address.

The $\overline{RD}$ signal is asserted low by the 8085 during the memory or I/O READ operation. Similarly $\overline{WR}$ pin signal is asserted low during a memory or I/O WRITE operation.

The IO/M, S0 and S1 are output by the by 8085 during its internal operation which can be interrupted. The READY input can be used by slower external device for obtaining extra time in order to communicate with the 8085. The ready is made low to provide wait state clock period in machine cycle.

The HOLD and HLDA signals are used for Direct Memory Access (DMA) type of data transfer. The DMA controller place a HIGH ON HOLD pin in order to take control of the system bus. The HOLD function is acknowledged by the 8085 by placing a HIGH Output on the HLDA pin.

The 8085 have five interrupts pin. The order of priority of the interrupt is TRAP, RST 7.5,RST6.5, RST5.5 and INTR. The interrupt TRAP, RST 7.5, RST6.5, RST5.5 are hardware vectored interrupt and enabled by the appropriate signals at the appropriate pins of 8085. When a vectored interrupt is enabled and if it is accepted then the program execution branches to vectored address specified by INTEL. The interrupt RST7.5, RST6.5 and RST5.5 are maskable interrupt by software.

The INTR is enabled by appropriate signal at its pin. In order to service INTR one of the eight opcodes (RST 0 to RST 7) has to provide on the 8085, AD0-AD7 bus by external logic. The 8085 then execute this instruction and vectors to the appropriated address to service the interrupt. The vector address for an interrupt RST n is given by (08 x n)H (TRAP is RST 4.5). The vector address are listed in Table-1 below

The 8085 have the clock generation circuit on the chip but an external quartz crystal or LC circuit or RC circuit should be connected at the pins X1 and X2 is divided by 2 internally for internal clock. The frequency of the output clock signal is same as that of internal clock.

The RESET IN signal, when pulsed LOW, cause the 8085 to execute the first instruction at the 0000H location. In addition, the 8085 resets instruction register, interrupt mask bits and other registers. The $\overline{\text{RESET IN}}$ must be held LOW for at least three-clock period.

A.1.2 Intel 8085 Architecture

The architecture of 8085 is shown in figure A.3, the 8085 include the ALU, timing and control unit, instruction register and decoder, register array, interrupt control and serial I/O control.

The ALU performs the arithmetic and logical operations. The operations performed by ALU of 8085 are addition, subtraction, increment, decrement, logical AND, OR, EXCLUSIVE-OR, compare, complement and left/ right shift. The accumulator and temporary register are used to hold the data during an arithmetic / logical operation. After an operation the result is stored in the accumulator and the flags are set or reset according to the result of the operation.

There are five flags in 8085; they are sign flag (S), zero flag (Z), auxiliary carry flag (AC), parity flag (P) and carry flag (C). The bit positions reserved for those flags in the flag register as shown in fig A.2

Fig

S	Z		Ac		P		Cy

A.2

After an ALU operation if the most significant bit of the result is 1,the sign flag is set. The zero and it is reset if the result is non-zero. In an arithmetic operation, when a carry is generated by the lower nibble the auxiliary carry flag is set. After an arithmetic or

logical operation if the result has an even number of 1's the parity flag is set otherwise it is reset.

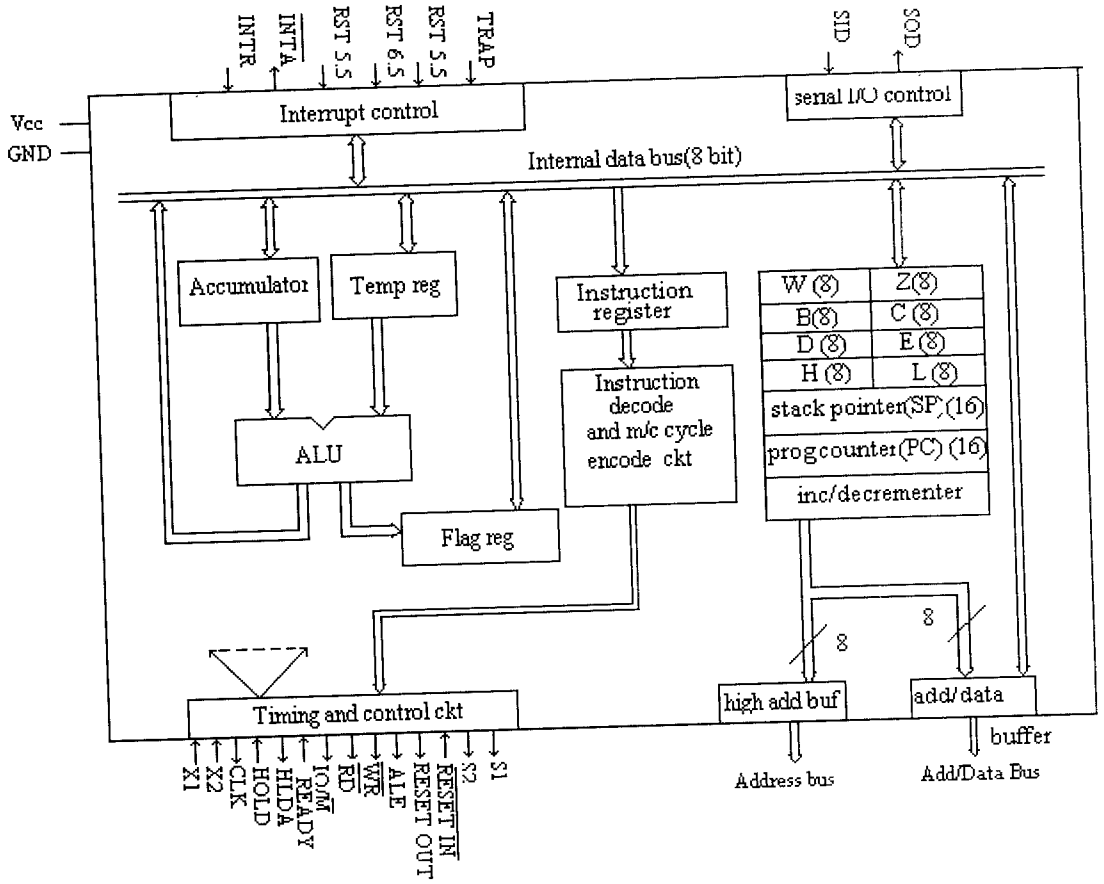


Fig A.3

If an arithmetic operation result in a carry, the carry flag is set otherwise it is reset. Among the five flags, the AC flag is used internally for BCD arithmetic and the programmer to check the conditions of the result of an operation can use other four flags. The timing and control unit synchronizes all the microprocessor operations with the clock, and generates the control signal necessary for communication between the microprocessor and peripheral.

When an instruction is fetched from memory it is placed in instruction register. Then it is decoded and encode into various machine cycles. Apart from accumulator (A-reg) there are six general-purpose programmable registers B, C, D, E, H and L. They can

be used as 8-bit registers or paired to store 16-bit data. The allowed pairs are B-C, D-E and H-L. The temporary register W and Z cannot use by the programmer.

The stack pointer SP holds the address of the stack top. The stack is a sequence of RAM memory location defined by the programmer. The stack is used to save the content of registers during the execution of a program.

The program counter (PC) keeps track of program execution. To execute a program the starting address of the program is located in program counter. The PC sends out an address to fetch a byte of instruction from memory and increment its content automatically. Hence when a byte of instruction is fetched, the PC holds the address of the next byte of the instruction or the next instruction.

A.1.3 Machine cycles of 8085

The 8085 microprocessor has seven basic machine cycles. They are

1. Opcode fetch cycle (4T or 6T).
2. Memory read cycle (3T).
3. Memory write cycle (3T).
4. I/O read cycle (3T).
5. I/O write cycle (3T).
6. Interrupt acknowledge cycle 6T or12T).
7. Bus idle cycle (2T or 3 T).

Each instruction of the 8085 processor consists of one to five machine cycles, when the 8085 processor executes an instruction; it will execute some of the machine cycles in a specific order. The processor takes a defined time to execute the machine cycles. The time taken by the processor to execute a machine cycle is expressed in T- state. One T-state is equal to the time period of the internal clock signal of the processor.

A.1.4 Instruction format of 8085

The 8085 have 74 basic instructions and 246 total instructions. The instruction set of 8085 is defined by manufacture Intel Corporation. Each instruction of 8085 has 1 byte opcode. The size of 8085 instructions can be 1 byte, 2 bytes or 3 bytes. The 1-byte instruction has an opcode followed by an eight-bit address or data. The 3-byte instruction has an opcode followed by 16-bit address or data.

Addressing Modes

Every instruction of a program has to operate on a data. The method of specifying the data to be operate by the instruction is called addressing. The 8085 has 5 different types of addressing.

1. Immediate Addressing.
2. Direct Addressing.
3. Register Addressing.
4. Register Indirect Addressing.
5. Implied Addressing.

Immediate Addressing

In immediate addressing mode, the data is specified in the instruction itself. The data will be a part of the program instruction.

Direct Addressing

In direct addressing mode, the address of the data is specified in the instruction. The data will be in memory. In this addressing mode, the program instruction and data can be stored in different memory blocks.

Register Addressing

In register addressing mode, the instruction specifies the name of the register in which the data is available.

Register Indirect Addressing

In register indirect addressing mode, the instruction specifies the name of the register in which the address of the data is available. Here the data will be in memory and the address will be in the register pair.

Implied Addressing

In implied addressing mode, the instruction itself specifies the data to be operated.

Instruction Set of 8085

The 8085 instruction set can be classified into the following five functions,

1. Data Transfer Instruction.
2. Arithmetic Instruction.
3. Logical Instruction.
4. Branching Instruction.
5. Machine Control Instruction.

A.2 INTEL 8255 (Programmable Peripheral Interface)

The 8255 have three ports A, B and C. the port A and B are 8 bit parallel ports. Port A can be programmed to work in any one of the three operating modes are input or output port. The three operating modes are

Mode-0 = Simple I/O port

Mode-1= Handshake I/O port

Mode-2= Bi-directional I/O port

The port B can be programmed to work either in mode-0 or mode-1 as input or output port. The port C pins have different assignments depending on the mode of port A and B. if port A and B are programmed in mode-0, then the port C can perform any one of the following function.

1. As 8 bit parallel port in mode-0 for input or output.
2. As two numbers of 4 bit parallel port in mode-0 for input or output.
3. The individual pins of port C can be set or reset for various control applications.

If port A and B are programmed in mode-1 or mode-2, then some of the pins of port C are used for handshake signals and the remaining pins can be used as input/output lines or individually set/reset for control application.

A.2.1 I/O Modes of 8255

Mode-0: In this mode al the three ports can be programmed either as input or output port. In mode-0, the outputs are latched and the inputs are not latched. The do not have handshake or interrupt capability. The port in mode-0 can be used to interface DIPswitches, Hexa-keypad, LED's and 7 segments LED's to the processor.

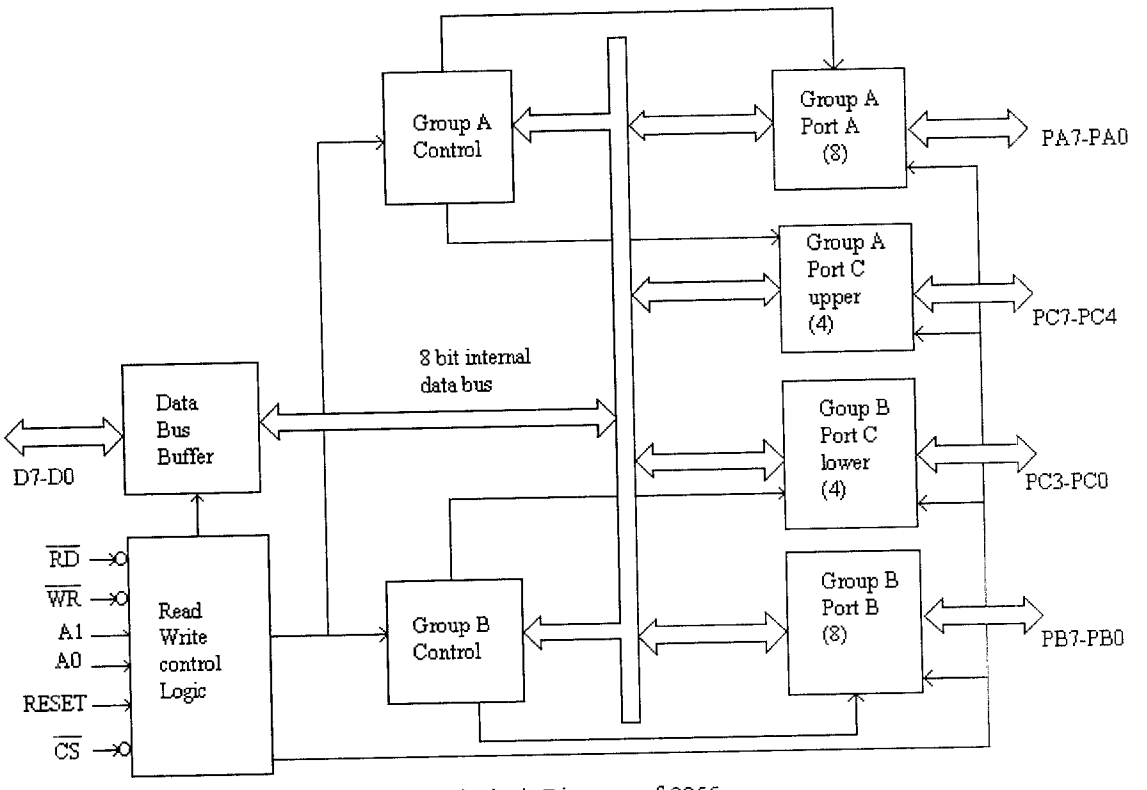
Mode-1: In this mode, only port A and B can be programmed either as input or output port. In mode-1, handshake signals are exchanged between the processor and peripheral prior to data transfer. The port C pins are used for

handshake signals. Input and output data are latched. Interrupt driven data transfer scheme is possible.

Mode-2: In this mode port will be a bi-directional port. Only port A can be programmed to work in mode-2. Five pins of port C are used for handshake signals. This mode is used primarily in applications such as data transfer between two computers or floppy disk controller interface.

A.2.3 Internal Block Diagram of 8255

The ports are grouped as Group A and group B. the group a has port A, port C_{upper} and its control circuit. The group B comprises of port B, port C_{lower} and its control circuit. The read/Write control logic requires six control signals. These signals are given below.



Internal Block Diagram of 8255

RD (Read): This control signal enables the read operation. When this signal is LOW, the microprocessor reads data from a selected I/O port of 8255A.

WR (Write): this control signal enables the write operation. When this signal goes LOW, the microprocessor writes into a selected I/O port or the control register.

RESET: This is an active HIGH signal. It clears the control register and set all ports in the input mode.

CS, A0 & A1: These are device select signals. The CS is connected to the decoder in the system. A0 and A1 are generally connected to A0 and A1 of the processor.

Internal Address		Device Selected
A1	A0	
0	0	Port A
0	1	Port B
1	0	Port C
1	1	Control Register

D7	D6	D5	D4	D3	D2	D1	D0

The 8255 can be either memory mapped in the system or it can be I/O mapped in the system. When $\overline{CS}$ is LOW the 8255 is selected. The A0 and A1 selected. The A0 and A1 select any one of the four internal devices as shown in table

The 8255 have two control words, one for specifying I/O functions and another for bit set/reset mode of port C. Both the control words are written in the same control register. The control register differentiates them by the value of bit D7. The bit set/ reset function. If D7=1 then the bits D6-D0 determine I/O functions in various modes. If bit D7=0 then the bits D6-D0 determine the pin of port C to be set or reset.

A.3 INTEL 8279 KEYBORD INTERFACE

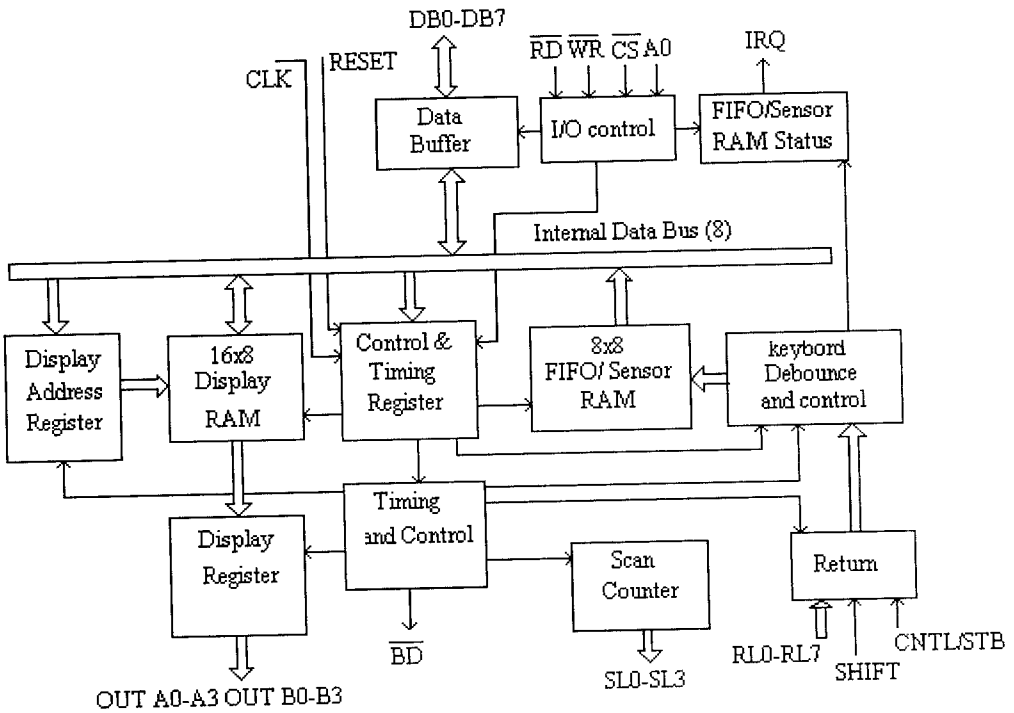
The INTEL 8279 is a dedicated controller specially developed for keyboard/ display interfacing in 8085/ 8086/ 8088 microprocessor based system. It relives the processor from the time consuming task like keyboard scanning and display refreshing.

The 8279 provide an interface for max of 64-contact key matrix. Keyboard entries are debouched and store in internal FIFO RAM. It generates an interrupt signal for each key entry, to inform the processor to read the key from FIFO. It provides a multiple interface for 7 segment LED's and other popular display devices.

The 8279 are a 40-pin IC. It has 2 internal address decided by logic level of A0. If A0 is low then the processor can read or write to 8279. If A0 is high then the processor can write to control register or read status register. The 8279 can be either I/O mapped or memory mapped in the system.

A.3.1 Block diagram of 8279

The functional block diagram of 8279 is shown in fig... The four major sections of 8279 are keyboard; scan, display and CPU interface.



Keyboard Section

The keyboard section consists of eight return lines RL0-RL7 that can be used to form the columns of keyboard matrix. It has tow additional inputs shift and control/strobe. The keys are automatically denounced. The two operating modes of keyboard section are pressed simultaneously; only the first key is recognized. In the N-key rollover mode simultaneously keys are recognized and their codes are stored in FIFO.

Scan section

The scan section has a scan counter and four scan lines, SL0 to SL3. In decoded scan mode, the output of scan lines will be similar to a 2 to 4 decoder. In encoded scan mode, the output of scan lines will be binary count, and so an external decoder should be used to convert the binary count to decoded output. The scan lines are common for keyboard and display.

Display section

The display section has eight output lines divided into two groups A0-A3 and B0-B3. The output lines can be used either as group of 8 lines or as 2 group of 4, in conjunction with the scan lines for a multiplexing display. The outputs lines are connected to the anodes through driver transistor in case of common cathode 7 segment LED's. The cathodes are connected to scan lines through driver transistors.

CPU interface section

The CPU interface section takes care of data transfer between 8279 and the processor. This section has 8 bi-directional data lines DB0-DB7 for data transfer between 8279 and CPU. It requires 2 internal address A0==0 or 1, for selecting either data buffer or control register of 8279. The control signal WR, RD, CS, &A0 are used for read/write to 8279. It has an interrupt request line IRQ, for interrupt driven data transfer with processor.

The 8279 require an internal clock frequency of 100kHZ. This can be obtained by dividing the input clock by an internal prescaler. The prescaler can take a value from 2 to 31, which is programmable. The RESET signal set the 8279 in 16-character display with two-key lockout keyboard mode. Also the reset will set the clock prescaler to 31.

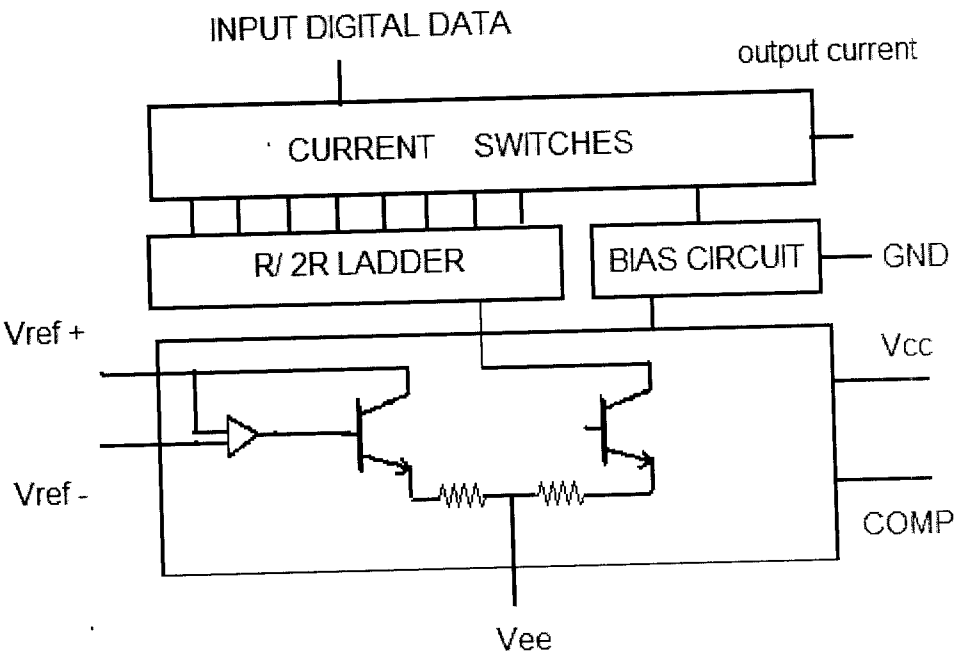
A.4 DAC- 0808

The DAC 0808 of National Semiconductor corporation is an example of 8 bit DAC without internal latch and I to V converting amplifier digital to analog converters compatible to microprocessor are available with or without internal latch.

The processor sense an address decoded by decoder in the microprocessor system to produce chip selection signal. Then the processors sense a digital data to the latch. The buffer and the inverter will produce sufficient delay for chip selection signal so that, the latch is clocked only after the data is arrived in the input lines of the latch.

When the latch is clocked the digital data is send to DAC. The DAC will produce a corresponding current signal, which is converted, to voltage signal by the op amp-741. The typical settling time of DAC 0808 is 150 nano seconds. Therefore the processor need not wait for loading next data.

BLOCK DIAGRAM OF DAC 0808



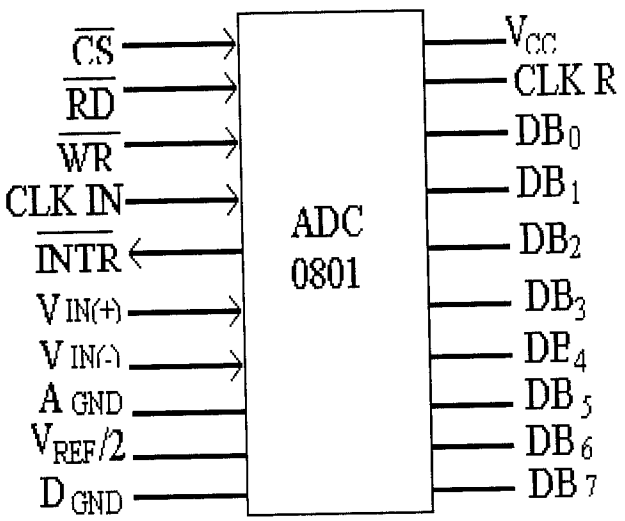
In many applications the microprocessor has to produce analog signal for controlling certain analog devices. Basically microprocessor system can produce only digital signals. In order to convert digital signals to analog signals these DAC are used. DAC 0808 is widely used in all application.

Every DAC will have n input lines and an analog output line. The DAC requires a Vref and a I (current ref). A smallest possible analog value that can be represented by n bit binary code, which is called as resolution. Resolution of DAC with n bit binary input is ½^n of reference analog voltage. Every analog output will be multiplied by the resolution.

In some converters input reference analog signals will be multiplied or divided by a constant to get full-scale value. Now the resolution will be ½^n of full-scale value.

A.5 ADC –0801

The ADC can be interfaced to 8085 microprocessor system through tri state buffer or port device such as 8255/8155.The ADC 0801 is single channel, 8bit successive approximation type A/D converter from national semiconductor corporation. It is a 20 pin IC available in DIP.



The ADC 0801 has two analog inputs Vin (+) and Vin (-). Both the analog inputs are used for differential mode of operation. When the analog signal is single ended positive, then Vin (+) is used as input and Vin (-) is grounded. When the analog signal is single ended negative, then terminals are interchanged. The ADC requires an external clock frequency range of 100 to 800 KHZ.

Typically the clock frequency is chosen as 640 KHZ to produce a conversion time of 100μsec. The ADC is connected to system through tri state buffer. The ADC can either be memory mapped or I/O mapped in the system. The chip selection signal is obtained from the address decoder. The conversion is initiated when both chip selection and write terminals are asserted low.

Write control signal is used to reset the successive approximation register of ADC and to give start of conversion. WRITE signal of DAC can be connected to write signal terminal of 8085 processor. On the falling edge of WRITE signal the SAR is resetted and at the rising edge conversion starts.

Asserting INTR LOW indicates the end of conversion and this signal can be inverted to interrupt the 8085 processor. The processor reads the digital data using RD and when the data is read, the

A.5 THE INSULATED GATE BIPOLAR TRANSISTOR (IGBT)

A.5.1 Structure

Fig.1 shows the structure of a typical n-channel IGBT. All discussion here will be concerned with the n-channel type but p-channel IGBT's can be considered in just the same way.

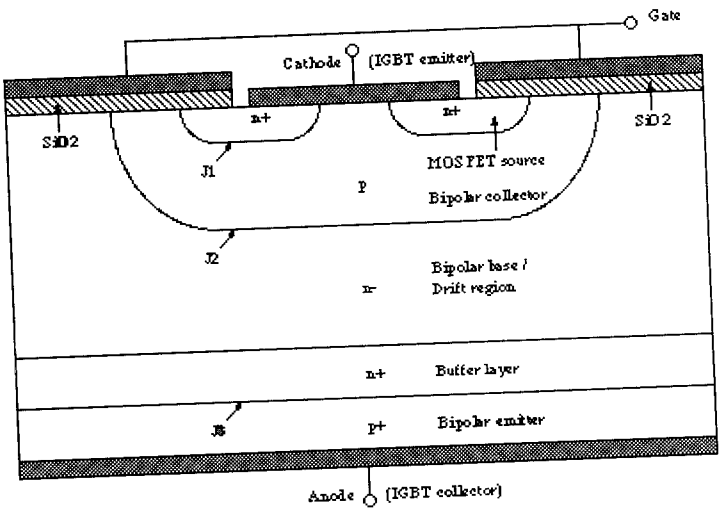


Fig.1: A typical IGBT structure

The structure is very similar to that of a vertically diffused MOSFET featuring a double diffusion of a p-type region and an n-type region. An inversion layer can be formed

under the gate by applying the correct voltage to the gate contact as with a MOSFET. The main difference is the use of a p^+ substrate layer for the drain. The effect is to change this into a bipolar device as this p-type region injects holes into the n-type drift region.

A.5.2 OPERATION

Blocking Operation

The on/off state of the device is controlled, as in a MOSFET, by the gate voltage V_G. If the voltage applied to the gate contact, with respect to the emitter, is less than the threshold voltage V_{th} then no MOSFET inversion layer is created and the device is turned off. When this is the case, any applied forward voltage will fall across the reversed biased junction J2. The only current to flow will be a small leakage current.

The forward breakdown voltage is therefore determined by the breakdown voltage of this junction. This is an important factor, particularly for power devices where large voltages and currents are being dealt with. The breakdown voltage of the one-sided junction is dependent on the doping of the lower-doped side of the junction, i.e. the n^- side. This is because the lower doping results in a wider depletion region and thus a lower maximum electric field in the depletion region. It is for this reason that the n^- drift region is doped much lighter than the p-type body region. The device that is being modeled is designed to have a breakdown voltage of 600V.

The n^+ buffer layer is often present to prevent the depletion region of junction J2 from extending right to the p bipolar collector. The inclusion of this layer however drastically reduces the reverse blocking capability of the device as this is dependent on the breakdown voltage of junction J3, which is reverse, biased under reverse voltage conditions. The benefit of this buffer layer is that it allows the thickness of the drift region to be reduced, thus reducingon-statelosses.

On-state Operation

The turning on of the device is achieved by increasing the gate voltage V_G so that it is greater than the threshold voltage V_{th}. This results in an inversion layer forming under the gate that provides a channel linking the source to the drift region of the device. Electrons are then injected from the source into the drift region while at the same time junction J3, which is forward biased, injects holes into the n^- doped drift region (Fig.2).

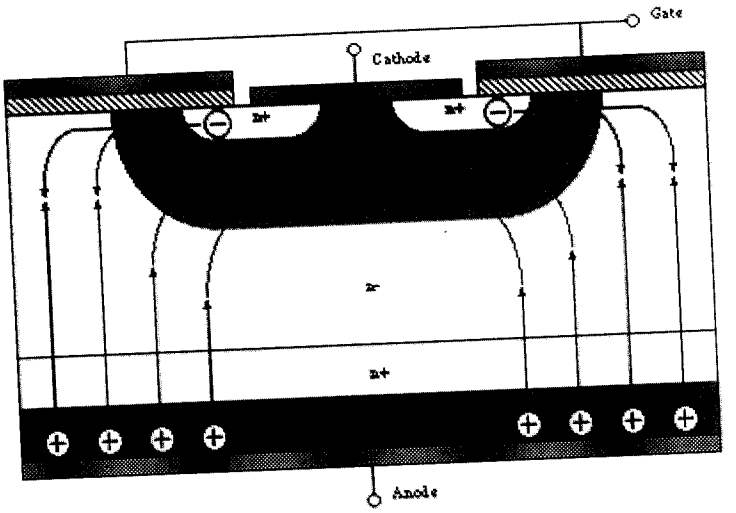


Fig 2: Hole and electron flow in the IGBT during on-state

This injection causes conductivity modulation of the drift region where both the electron and hole densities are several orders of magnitude higher than the original n^- doping. It is this conductivity modulation, which gives the IGBT its low on-state voltage because of the reduced resistance of the drift region. Some of the injected holes will recombine in the drift region, while others will cross the region via drift and diffusion and will reach the junction with the p-type region where they will be collected. The operation of the IGBT can therefore be considered like a wide-base pnp transistor whose base drive current is supplied by the MOSFET current through the channel. A simple equivalent circuit is therefore as shown in Fig.3 (a)

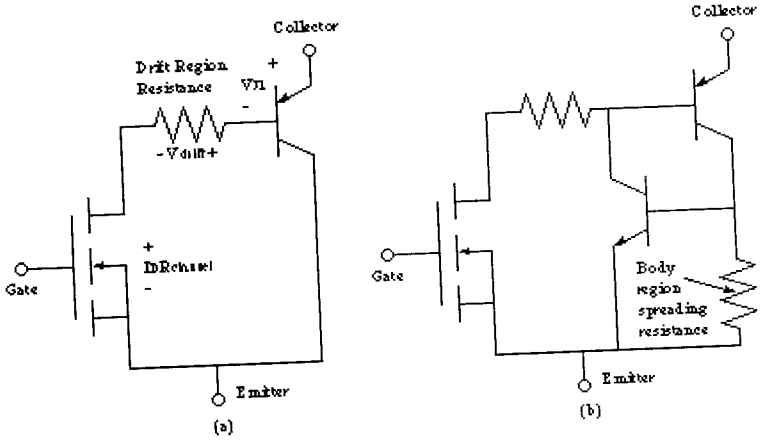


Fig 3: (a) Simple equivalent circuit for the IGBT; (b) more complete equivalent circuit showing the transistors which make up the parasitic thyristor

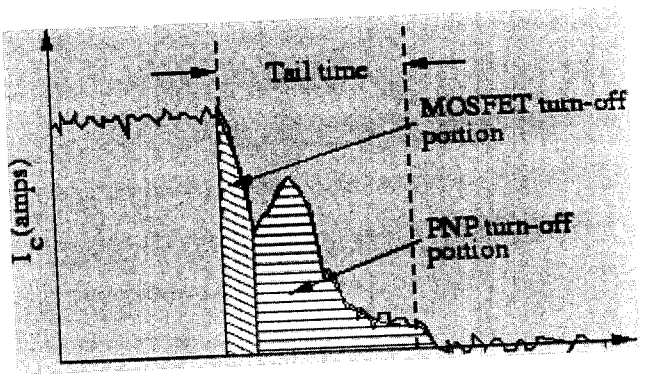
Fig.3(b) shows a more complete equivalent circuit which includes the parasitic npn transistor formed by the n^+-type MOSFET source, the p-type body region and the n^--type drift region. Also shown is the lateral resistance of the p-type region. If the current flowing through this resistance is high enough it will produce a voltage drop that will forward bias the junction with the n^+ region turning on the parasitic transistor which forms part of a parasitic thyristor. Once this happens there is a high injection of electrons from the n^+ region into the p region and all gate control is lost. This is known as latch up and usually leads to device destruction.

A.5.3 SWITCHING BEHAVIOR

Blocking operation

As shown in the figure is turn-on and the turn-off states of the MOSFET are controlled by the gate voltage. If the gate voltage is less than the threshold voltage with respect to the emitter, no MOSFET inversion layer is created and the device is turned off. Here any applied forward voltage will drop across the reversed biased junction J_2. The forward breakdown voltage is therefore given by the breakdown voltage of this junction at the turn-off time. This is an important factor, particularly for power devices where high voltages and currents are being dealt with. The breakdown voltage of junction J_2 depends on the doping of the lower doped side of the junction, i.e., the n^-epi region. This is because the lower doping results in a wide depletion region and thus a lower maximum electric field in the depletion region. This is a reason the n^- drift region is doped much lighter than the p^+ body region.

The current turn-off state of the IGBTs.



Until recently, the limitation of the IGBTs to serve many applications has been a result from slow turn-off speed when compared to the power MOSFETs. While turn-on is fairly rapid, the turn-off time of the IGBT is slow because minority carriers are stored in the n^-epi region. Figure illustrates the turn-off switching waveform, the tail time and contributing factors of the fast IGBT designed for a Pulse Width Modulation (PWM) motor control service When the gate is initially brought below the threshold voltage, the n^-epi contains a very large concentration of electrons.

There will be significant injection into the p^+ substrate and a corresponding whole injection into the n^-epi region. As the electron concentration in the n^-epi decreases, the electron injection decreases, leaving the rest of electrons to recombine. Therefore, the turn-off state of the IGBT has two phases: *An injection phase* where the collector current falls very quickly, and *a recombination phase* which the collector current decreases more slowly.

On-state operation

Turning the device on is achieved by increasing the gate voltage that is greater than the threshold voltage. This state forms an inversion layer under the gate, which provides a channel linking between the source and the drift region of the device. Electrons are then injected from the source into the drift region, while junction J_3 is in the forward bias state and injects holes into the n^-epi drift region.

The injection causes the conductivity modulation of the drift region where both the electron and hole densities are several orders of magnitude higher than the original n-doping. It is the conductivity modulation that gives the IGBT its low on-state voltage because of the reduced resistance of the drift region. Some of the injected holes will recombine in the drift region, while others will cross this region via drift and diffusion mechanism and reach the junction of the p-type region where they will be collected.

For high performance systems, electronic package design has been moved towards larger chips, higher number of I/O ports, increased circuit density and improved reliability. Greater circuit density means increased power density (W/m^2). Power density has increased exponentially over the past fifteen years and it appears that it will continue to do so in the uture. As the power density is high, thermal management should be considered carefully.

A.6 IC741- OPERATIONAL AMPLIFIER

IC-741 is a IC type 8 pin operation amplifier. It has two inputs and two supply pins and one output terminal.

Pin no	Operation
1	DC Offset
2	Inverting terminal
3	Non-inverting terminal
4	-Vcc
5	DC Offset
6	Output terminal
7	+Vcc
8	NC

A.6.1 IDEAL OPERATION:

Op-amp is said to be identical if it has following characteristic

- Open loop voltage gain Aol = ∞
- Input Impedance Ri = ∞
- Output Impedance Ro = 0
- Bandwidth BW = ∞

Zero Offset Vo=0 when V1=V2=0

It can be seen that

- An ideal op-amp draws no current at both the input terminal. I1=I2=0 because of infinite input impedance, any signal source can drive it and there is no loading on the preceding driver stage
- Since gain is infinity, the voltage between the inverting and non-inverting terminals is essentially zero for finite output voltage Vo.
- The output voltage Vo is independent of the current drawn from the output as Ro =0. The output thus can drive an infinite number of other devices.

A.6.2 OPERATION OF OP-AMP:

OPEN LOOP OPERATION

The simple way to use the op-amp is in open loop mode. Since gain is infinity, the o/p voltage Vo is either +ve or –ve. The o/p assume one of the two possible o/p states i.e., +Vsat or –Vsat and the amplifier act as a switch only.

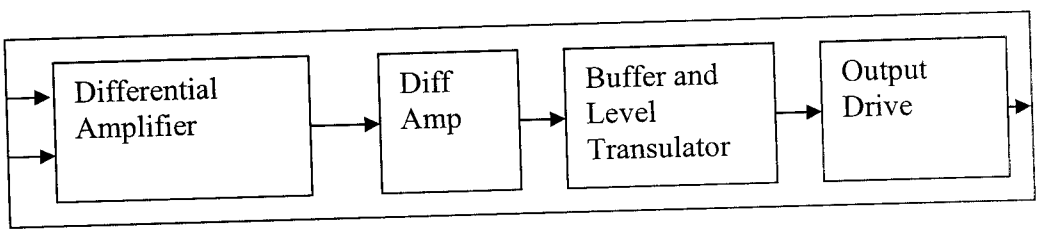
A.6.3 FEEDBACK IN IDEL OP-AMP:

The unity of an op-amp can be greatly increased by providing negative feedback. There are two basic feedback connection used. In order to understand the operation of these circuits, we make two realistic simplifying assumptions

- The current drawn by either of the i/p terminal in negligible.
- The differential i/p voltage Vd between non-inverting and inverting terminal is essentially zero.

A.6.4 OPERATIONAL AMPLIFIER INTERNAL CIRCUIT:

Commercial integrated circuit op-amp usually consists of four-cascaded block. The first two stages are cascaded difference amplifier used to provide high gain. The third stage is the o/p driver. The buffer is usually an emitter follower whose i/p impedance is very high so that it prevents loading of the high gain stage. The o/p stage is designed to provide low o/p impedance as demanded by ideal op-amp.



The o/p voltage should swing symmetrically reference to ground. The buffer stages along with the o/p stage also act as level shifter so that o/p voltage is zero to zero inputs.

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