HEART PULSE MONITORING SYSTEM THROUGH TELEPHONE LINE

PROJECT REPORT P-11 44

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DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

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CERTIFICATE

This is to certify that the project report entitled

HEART PULSE MONITORING SYSTEM THROUGH TELEPHONE LINE

Is the bonafide work done by

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_____   _____
Internal Examiner   Extenal Examiner

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ACKNOWLEDGEMENT

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SYNOPSIS

This project involves the design of a system to monitor the patients heart beat and body temp in the absence of the doctor and to transmit these vital signals to a remote monitoring station. This process requires a telephone network for transmission of data.

The system is designed to transmit the signals at periodic intervals and in case of abnormality in the heartbeat. The heartbeat is sensed through an infrared sensor and is passed to a micro controller. The system is designed to operate a Hook's relay, which helps in establishing a connection between the patient's telephone and the monitoring station for the transmission of data. A DTMF encoder is used to convert the BCD signals to their corresponding frequencies.

On the receiver side a ring sensor is used to detect the incoming data, which activates the DTMF decoder to decode these frequencies into the corresponding BCD codes. These signals are passed to a micro controller, which is interfaced with a PC at the monitoring station. The signals are recorded and displayed.

Further, an alarm is provided in the monitoring system so that the doctor can be called at any time, as and when required by the patient.

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CONTENTS

INTRODUCTION

INTRODUCTION

Heart – the pumping station of the human body is responsible for the circulation of blood. It receives impure blood from all parts of the body, purifies it and circulates it back. The pumping action is achieved by periodic contraction and relaxation of the cardiac muscles. This periodic motion forces the blood to flow in the form of packets.

The rate at which the heart pumps blood is called as heart pulse. Under normal conditions the rate is 72 per minute. If the heart pulse does not fall within the specified range that is 65 to 80 beats per minute it indicates an abnormality in the functioning of the heart. So in any heart monitoring system the heart pulse is the most important parameter.

The system designed here monitors the heart pulse and the temperature, which gives a broader perspective of the patient's health. This system is placed next to the patient, which monitors these parameters continuously and transmits these data to a remote monitoring station. Thereby eliminating the presence of the doctor near the patient all the time.

FEATURES OF THE PROJECT

> No need for the doctor's presence near the patient.
> Several patients can be monitored at the same time
> Since we make use of telephone lines this system is error free.
> Since telephone networks are well established this can be implemented anywhere
> No cost is involved in case we make use of intercom.
> Any type of data can be transmitted.

TRANSMITTER SIDE:

SENSORS:

The heart pulse is detected using the photoelectric sensor, which is basically an infrared sensor. It consists of a transmitter and receiver. The transmitter emits infrared rays and the receiver is nothing but a LDR. When the finger is placed inside the sensor the heart pulse is detected as the intensity of the blood flow varies during the pumping action. Temperature is sensed using a transducer. It converts the heat energy to electrical energy. An ADC converts this analog signal to digital form after amplification.

MICROCONTROLLER:

It is main control unit of the system which is a 40 pin IC .It receives the signals from the ADC and the heart beat sensor. It converts these signals to their ASCII equivalent to operate the LCD. The BCD data from the sensors are fed to the DTMF encoder along with the destination telephone number. It also controls the hook's relay, which is used to establish the connection.

DTMF ENCODER:

This is an integrated circuit eighteen-pin package, which needs only a few components to make it work. It gets the sensor signals and the destination telephone number in BCD form from the micro controller as input. The block is given with the telephone lines the circuit encodes the bit BCD data into its corresponding DTMF signal.

RINGER AND HOOK SWITCH RELAY:

The ringer module detects the presence of a ring in the local telephone to which the application is connected. The ringer generates an interrupt a high going signal i.e. from logical 0 to a logical 1. This interrupt is given to a micro

controller as a bit change interrupts. The micro controller on receiving the interrupt suspends the present operation and gives an instruction to establish a telephone connection with the called party by activating the hook's switch relay. This relay replaces the normal mechanical relay inside the telephone.

BLOCK DIAGRAM
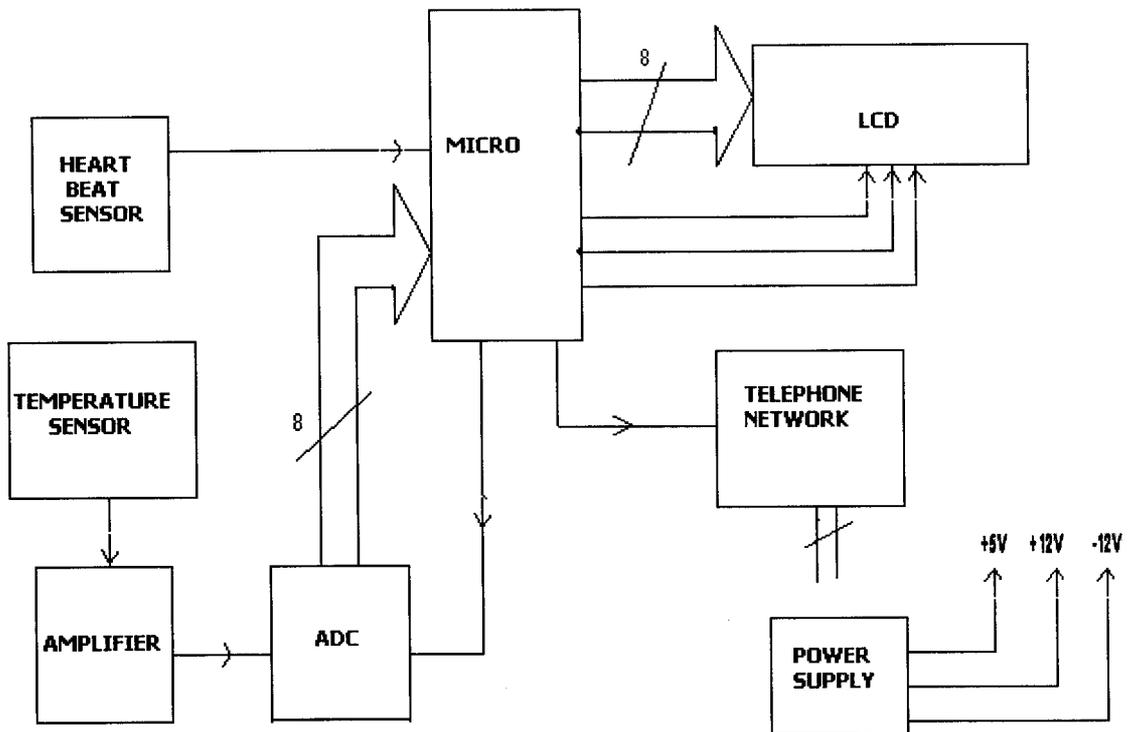
RECEIVER SIDE:

DTMF DECODER:

This block is used to decode the key pressed by the operator from the remote location. The block is given with the telephone line, the circuit picks up the ac DTMF signal alone and it decodes it into a 4 bit binary data. This data is given to the micro controller along with a strobe line to indicate the presence of new data.

MICRO CONTROLLER:

Here, the BCD data from the DTMF decoder is converted into its ASCII equivalent and it is displayed on the LCD. Further, whenever the heart pulse exceeds the range i.e. from 65 to 80, an alarm is activated. Also, when the temperature goes beyond 100 F, again the alarm is activated indicating abnormalities in the patient condition.

MAX 232 & PC INTERFACE:

The micro controller is designed on the TTL logic. Similarly, the PC is designed on the RS 232 logic. In order to interface these two logics, we go in for MAX 232. The data from the MAX232 are transmitted serially to the computer through the COMM port, to be displayed on the computer monitor.

BLOCK DIAGRAM

```
                                                    8
  ┌──────────┐        ┌────────┐      ───/──▷    ┌──────────┐
──┤TELEPHONE │────────┤        │                 │          │
──┤NETWORK   │───/──▷ │ MICRO  │                 │   LCD    │
  └──────────┘        │        │                 │          │
                      │        │                 └──────────┘
                      │        │
                      │        │
                      └───┬────┴──▷      ┌──────────┐      ┌──────────┐
                          │              │ MAX 232  │──/──▷│    PC    │
                          │              └──────────┘      └──────────┘
                          ▽
                      ┌──────────┐
                      │  ALARM   │
                      └──────────┘
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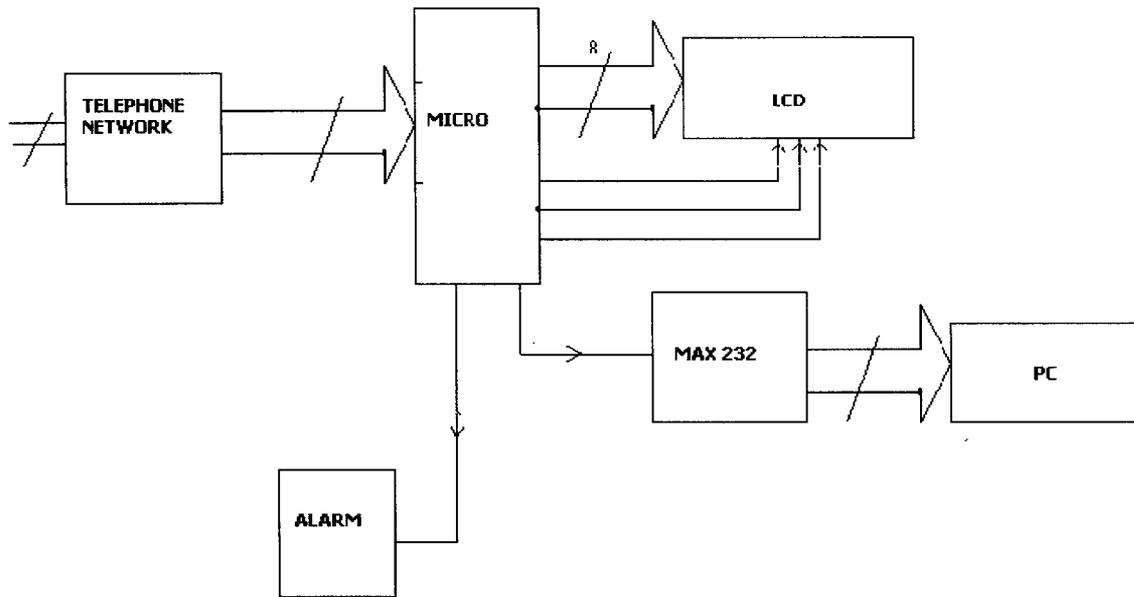
POWER SUPPLY

The power supply provides regulated output voltage of+5V, +12V and -12V. The power supply consists of

- Transformer
- Bridge rectifier
- Filter
- Voltage regulator

TRANSFORMER:

The transformer is used to step down 230V A.C from the mains to 12V A.C. the transformer is a center tapped type

BRIDGE RECTIFIER:

In the bridge circuit the sinusoidal input is converted into unidirectional waveforms. It is a full wave rectifier the peak inverse voltage of each diode is less.

FILTER:

Filters are used to remove A.C component from the dc output capacitive filter is used, as capacitance value increases ripples decrease.

VOLTAGE REGULATOR:

A voltage regulator is a circuit that supplies a constant voltage regardless of changes in the load currents. IC voltage regulators are versatile and inexpensive. A 7805 IC &7812 IC are used to obtain positive 5 volts and 12 volts respectively and a 7912 IC is used to obtain negative 12 volts.
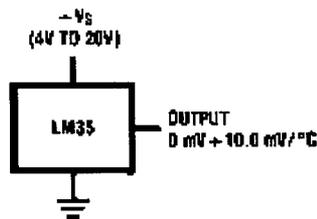
SENSORS

BASICS OF TEMPERATURE SENSING:

Temperature sensing is done by integrated circuit temperature sensor LM35.The LM35 series are precision integrated-circuit temperature sensors, whose output voltage is linearly proportional to the Celsius (Centigrade) temperature. It outputs 10 mV/degree Celsius. The LM35 does not require any external calibration or trimming to provide typical accuracies of ±1/4 °C at room temperature and ±3/4°c over a full temperature range of −55 to +150°C. Low cost is assured by trimming and calibration at the wafer level. The LM35's low output impedance, linear output, and precise inherent calibration make interfacing to readout or control circuitry especially easy. It can be used with single power supplies, or with pulse and minus supplies. As it draws only 60 μA from its supply, it has very low self-heating, less than 0.1°c in still air. The LM35 is rated to operate over a −55° to +150°C temperature range, while the LM35C is rated for a −40° to 110°C range (-10° with improved accuracy).

BASIC CENTIGRADE TEMPERATURE SENSOR:

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CIRCUIT DESCRIPTION:

The sensor IC is directly connected to the micro controller as shown. For a temperature range of 0-150° the supply voltage of 5V is given to the sensor. Thus it gives an output voltage of 10 mV/degree. This analog voltage is converted to digital value of 10-bit resolution inside the micro controller. The reference voltage is given as the system voltage itself that is the reference voltage is given as +5V. When the input is 5V the temperature is then 150°.

TEMPERATURE SENSOR AND AMPLIFIER
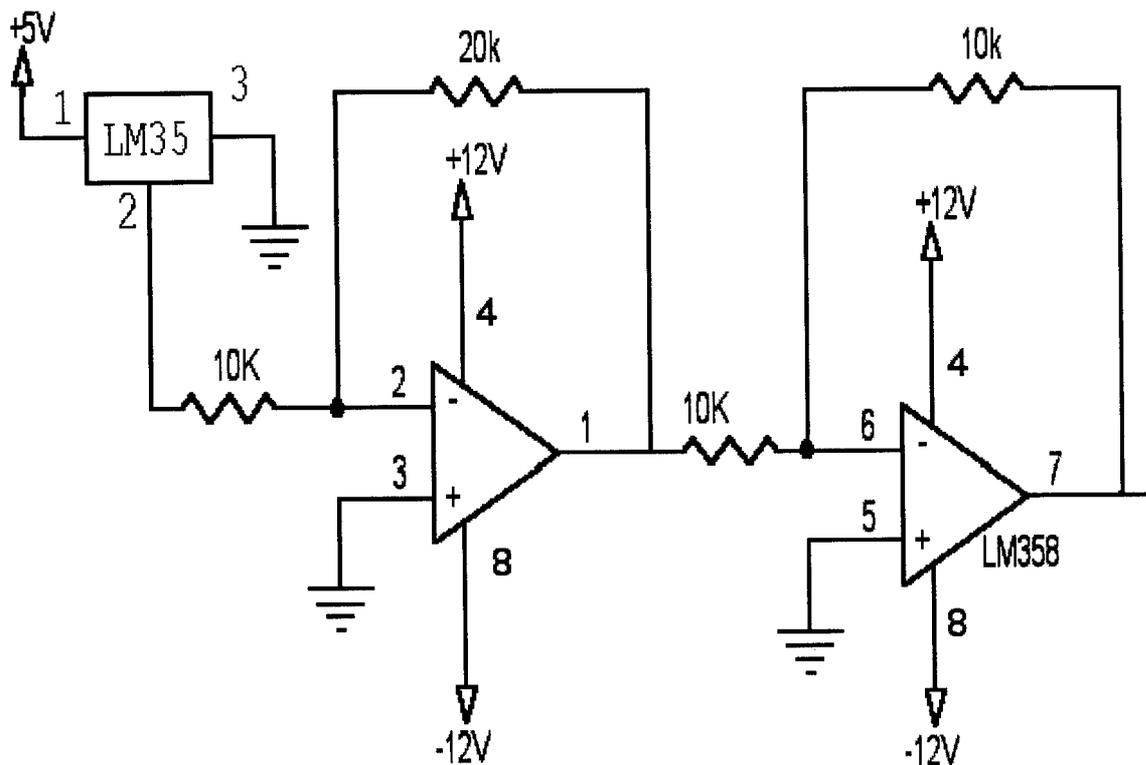
VOLTAGE AMPLIFIER:

The LM35 temperature sensor produces an output of 10mv, which is not sufficient to drive the ADC0804. The analog to digital converter requires 20mv to produce a 1-bit change. In order to interface the LM35 and ADC0804 we use inverting amplifier with a gain 2 and a second inverting amplifier with gain 1 is used to bring it back into phase. This analog output is fed to the ADC.

HEART BEAT SENSOR

Heart beat sensor is nothing but a photoelectric sensor .The photoelectric sensor used here is an infrared sensor. The infrared sensor consists of a pair of infrared transmitter and receiver. The infrared transmitter and receiver are placed such that the finger can be placed in between them.

WORKING:

The rays from the transmitter are focused onto a receiver that is placed at the opposite side. The receiver consists of an infrared detector that switches a transistor depending on the received signal. The amplitude of the output at the receiver end depends on the intensity of the light falling on the detector. The amplitude increases with the increase in the intensity.

Every time the heart pumps, blood it flows in the form of packets. Therefore maximum intensity of light is received in the interval between the pumping action and it decreases when the infrared ray passes through the blood packet. This decrease in the intensity of the received rays is due to the following properties of light in a medium

- ➤ Scattering
- ➤ Absorption
- ➤ Attenuation
- ➤ Reflection
- ➤ Refraction

These variations in the intensities are converted into pulses and is fed into the micro controller which is programmed to convert these pulses to heart beat.

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RINGER AND HOOK SWITCH RELAY

RINGER AND HOOK SWITCH RELAY

CIRCUIT DESCRIPTION:

The circuit shows the ring detector module. In presence of a ring the ac signal called jingle juices occurs, the neon lamp connected across the telephone lines glows. This light falls on the Light Detecting Resistor because of which the resistance of Light Detecting Resistor decreases. This makes the voltage at input of the timer to go below 2/3 Vcc and hence the 555 timer triggers and gives an interrupt to the micro controller indicating that the phase line is ringing and the connection to be established.

RINGER CIRCUIT

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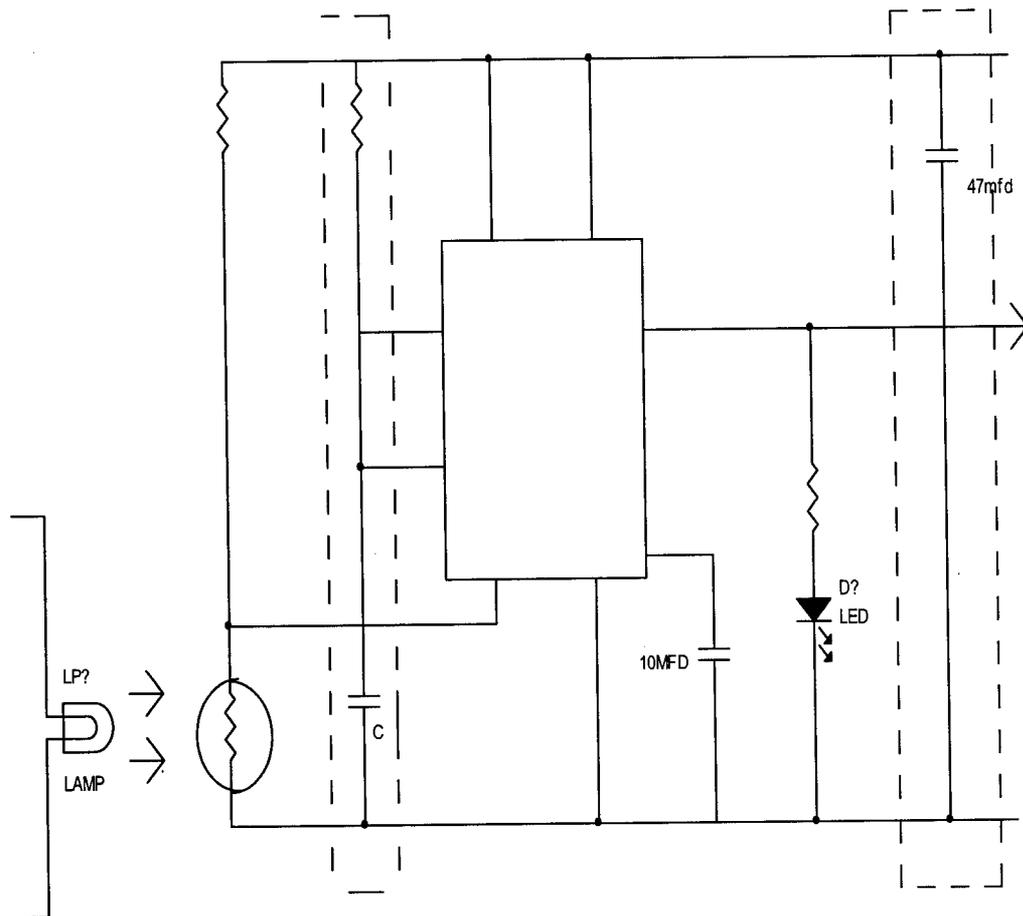
HOOK SWITCH RELAY:

The hook switch relay is a substitute for the cradle switch in the telephone. This relay is normally opened to receive a call, once a ring is detected the is established by closing the contacts and it is ready to receive a call.

The output from the micro controller is not sufficient enough to drive the 12V relay, so it is given through a switching transistor BC547.

RELAY CIRCUIT
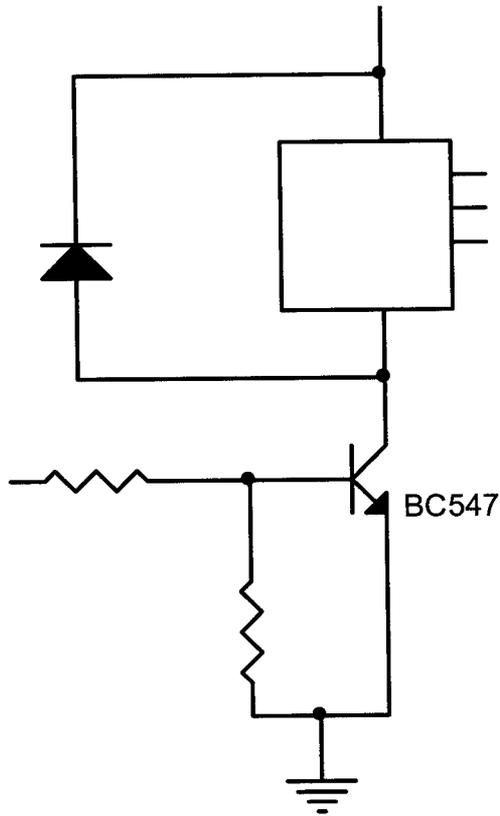
DTMF ENCODER FOR TELEPHONE

BASICS OF THE DTMF:

A signaling scheme was developed utilizing voice frequency tones and Implemented as a very reliable alternative to pulse dialing. This scheme is known as DTMF (Dual Tone Multi-Frequency), Touch-Tone™ or simply, tone dialing. As its acronym suggests, a valid DTMF signal is the sum of two tones, one from a low group (697-941Hz) and one from a high group (1209-1633Hz) with each group containing four individual tones. The tone frequencies were carefully chosen such that they are not harmonically related and that their inter modulation products result in minimal signaling impairment. This scheme allows for 16 unique combinations. Ten of these codes represent the numerals zero through nine, the remaining six (*, #, A, B, C, D) being reserved for special signaling. Most telephone keypads contain ten numeric push buttons, the asterisk (*) and octothorp (#). The buttons are arranged in a matrix, each selecting its low group tone from its respective row and its high group tone from its respective column. i.e. pressing '1' will send a tone made by adding 1209 Hz and 697 Hz to the other end of the line.

H1 = 1209 Hz H2 = 1336 Hz H3 = 1477 Hz H4 = 1633 Hz

L1 = 697 Hz [1] [2] [3] [A]

L2 = 770 Hz [4] [5] [6] [B]

LOW GROUP TONES L3 = 852 Hz [7] [8] [9] [C]

L4 = 941 Hz [*] [0] [#] [D]

LEGEND:

[ ] DTMF signal not available on a standard pushbutton telephone keypad

Telephone DTMF keypad matrix. Column H4 is normally not available on a telephone keypad and is reserved for special signalling.

DTMF CODING:

The DTMF coding scheme ensures that each signal contains one and only one component from each of the high and low groups. This significantly simplifies decoding because the composite DTMF signal may be separated with band pass filters, into its two single frequency components each of which may be handled individually. As a result DTMF coding has proven to provide a flexible signaling scheme of excellent reliability, hence motivating innovative and competitive decoder design.

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PIN CONFIGURATION

```
                    DIP, SOIC

          IN+ ▢1          20▢ V_DD
          IN- ▢2          19▢ SIGT
           GS ▢3          18▢ ESt
         V_REF ▢4         17▢ D3
          V_SS ▢5         16▢ D2
         OSC1 ▢6          15▢ D1
         OSC2 ▢7          14▢ D0
         TONE ▢8          13▢ IRQ/CP
          R/W ▢9          12▢ φ2
           CS ▢10         11▢ RSO
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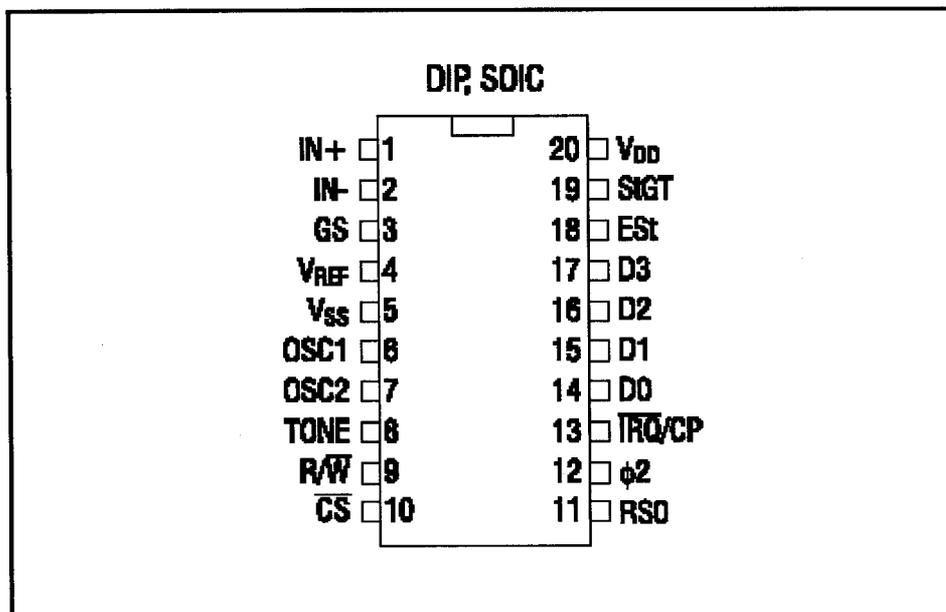
8880 DTMF ENCODER INTERNAL BLOCK DIAGRAM
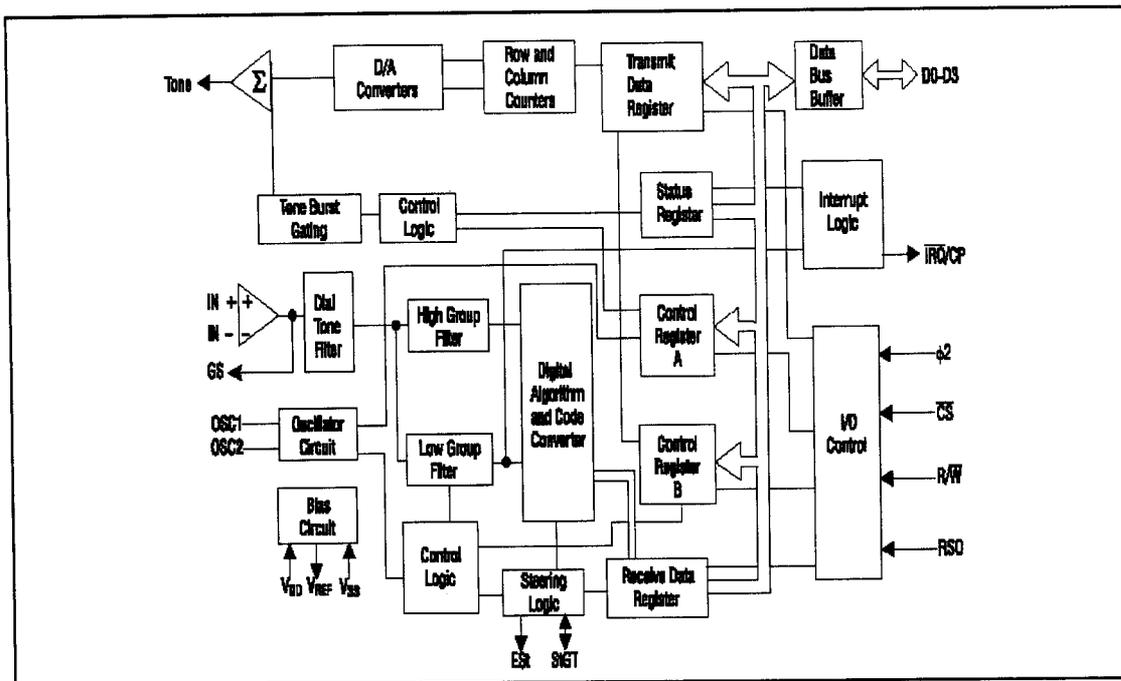
DTMF GENERATOR:

The 8880 encoder is capable of generating all 16 standard DTMF tone pairs with low distortion and high accuracy. All frequencies are derived from an external 3.58 MHz crystal. The sinusoidal waveforms for the individual tones are digitally synthesized using row and column programmable dividers and switched capacitor digital-to-analog converters. The row and column tones are mixed and filtered, providing a DTMF signal with low total harmonic distortion and high accuracy. To specify a DTMF signal, data conforming to the encoding format shown in Table must be written to the transmit data register. This is the same as the receiver output code. The individual tones that are generated (f_{LOW} and f_{HIGH}) are referred to as low-group and high-group tones. Typically, the high-group to low-group amplitude ratio (twist) is 2 dB to compensate or high-group attenuation on long loops.

TONE ENCODING

F$_{LOW}$	F$_{HIGH}$	Digit	D3	D2	D1	D0
697	1209	1	0	0	0	1
697	1336	2	0	0	1	0
697	1477	3	0	0	1	1
770	1209	4	0	1	0	0
770	1336	5	0	1	0	1
770	1477	6	0	1	1	0
852	1209	7	0	1	1	1
852	1336	8	1	0	0	0
852	1477	9	1	0	0	1
941	1336	0	1	0	1	0
941	1209	*	1	0	1	1
941	1477	#	1	1	0	0
697	1633	A	1	1	0	1
770	1633	B	1	1	1	0
852	1633	C	1	1	1	1
941	1633	D	0	0	0	0
0 = logic low, 1 = logic high						

DTMF DECODER FOR TELEPHONE

DECODING SEQUENCE:

An 8870 DTMF decoder receives the signal in its composite form, it is then split into its individual high and low frequency components. DTMF decoder separation of the low-group and high-group tones is achieved by applying the dual-tone signal to the inputs of two 9th-order switched capacitor band pass filters. The bandwidths of these filters correspond to the band enclosing the low-group and high-group tones. The filter section also incorporates notches at 350Hz and 440Hz, which provides excellent dial tone rejection. Each filter output is followed by a single order switched capacitor section which smoothes the signals prior to limiting. High-gain comparators perform signal limiting. These comparators are provided with a hysteresis to prevent detection of unwanted low-level signals and noise. The outputs of the comparators provide full-rail logic swings at the frequencies of the incoming tones.

The 8870 decoder uses a digital counting technique to determine the frequencies of the limited tones and to verify that these tones correspond to standard DTMF frequencies. A complex averaging algorithm is used to protect against tone simulation by extraneous signals (such as voice) while providing tolerance to small frequency variations.

The circuit is used in differential mode. The decoded output in the binary format is compatible with the voltage level of the micro controller to receive as a binary data. So the output of the decoder may be given to the ports of the micro controller. The data is given along with the strobe line to indicate a presence of a new data.

f_{LOW}	f_{HIGH}	KEY	TOE	Q_4	Q_3	Q_2	Q_1
697	1209	1	1	0	0	0	1
697	1336	2	1	0	0	1	0
697	1477	3	1	0	0	1	1
770	1209	4	1	0	1	0	0
770	1336	5	1	0	1	0	1
770	1477	6	1	0	1	1	0
852	1209	7	1	0	1	1	1
852	1336	8	1	1	0	0	0
852	1477	9	1	1	0	0	1
941	1209	0	1	1	0	1	0
941	1336	*	1	1	0	1	1
941	1477	#	1	1	1	0	0
697	1633	A	1	1	1	0	1
770	1633	B	1	1	1	1	0
852	1633	C	1	1	1	1	1
941	1633	D	1	0	0	0	0
-	-	ANY	0	Z	Z	Z	Z

APPLICATIONS:

The applications for DTMF signaling are tremendous and due to innovative technological advances its use is increasingly widespread. DTMF offers highly reliable, cost effective signaling solutions, which require no development effort on the user's part. The advent of single chip receivers has allowed many products that were previously not cost-effective to be manufactured in production quantities. DTMF signaling was originally designed for telephony signaling over voice quality telephone lines. This signaling technique has been applied to a multitude of control and data communications systems. All that is required is a voice quality communication channel with appropriate interfacing. The applications are limited only by one's imagination.

MICROCONTROLLER

MICROCONTROLLER

ATMEL 89C51 MICROCONTROLLER

INTRODUCTION

A Micro controller consists of a powerful CPU tightly coupled with memory RAM, ROM or EPROM), various I / O features such as Serial ports, Parallel Ports, Timer/Counters, Interrupt Controller, Data Acquisition interfaces-Analog to Digital Converter (ADC), Digital to Analog Converter (ADC), everything integrated onto a single Silicon Chip. The various devices can be used independently depending on the need and area of application for which it is designed. A microcomputer system requires memory to store a sequence of instructions making up a program, parallel port or serial port for communicating with an external system, timer / counter for control purposes like generating time delays, Baud rate for the serial port, apart from the controlling unit called the **Central Processing Unit.**

The major Features of 8-bit Micro controller **ATMEL 89C51**:

> 8 Bit CPU optimized for control applications
> Extensive Boolean processing (Single - bit Logic) Capabilities.
> On - Chip Flash Program Memory
> On - Chip Data RAM
> Bi-directional and Individually Addressable I/O Lines
> Multiple 16-Bit Timer/Counters
> Full Duplex UART
> Multiple Source / Vector / Priority Interrupt Structure
> On - Chip Oscillator and Clock circuitry.
> On - Chip EEPROM
> SPI Serial Bus Interface
> Watch Dog Timer

POWER MODES:

To exploit the power savings available in CMOS circuitry, ATMEL's Flash micro controllers have two software-invited reduced power modes.

They are

1. Idle mode
2. Power down mode.

IDLE MODE:

The CPU is turned off while the RAM and other on – chip peripherals continue operating. In this mode current drawn is reduced to about 15 percent of the current drawn when the device is fully active.

POWER DOWN MODE:

All on-chip activities are suspended while the on – chip RAM continues to hold its data. In this mode, the device typically draws less than 15 Micro Amps and can be as low as 0.6 Micro Amps.

POWER ON RESET:

When power is turned on, the circuit holds the RST pin high for an amount of time that depends on the capacitor value and the rate at which it charges. To ensure a valid reset, the RST pin must be held high long enough to allow the oscillator to start up plus two machine cycles. On power up, Vcc should rise within approximately 10ms. The oscillator start-up time depends on the oscillator frequency. For a 10 MHz crystal, the start-up time is typically 1ms.With the given circuit, reducing Vcc quickly to 0 causes the RST pin voltage to momentarily fall below 0V. However, this voltage is internally limited and will not harm the device.

MEMORY ORGANISATION

Logical separation of program and data memory

All ATMEL flash micro controllers have separate address spaces for program and data memory. The logical separation of the program and data memory allows the data memory to be accessed by 8 bit addresses, which is quickly stored and manipulated by am 8 bit CPU nevertheless 16 bit data memory addresses can also be generated through the DPTR register. Program memory can only be read. There can be up to 64K bytes of directly addressable program memory. The read strobe for external program memory is the Program Store Enable Signal (PSEN) Data memory occupies a separate address space from program memory. Up to 64K bytes of external memory can be directly addressed in the external data memory space. The CPU generates read and write signals, RD and WR, during external data memory accesses. External program memory and external data memory can be combined by a applying the RD and PSEN signal to the inputs of AND gate and using the output of the fate as the read strobe to the external program/data memory.

PROGRAM MEMORY:

The figure shows the map of the lower part of the program memory, after reset, the CPU begins execution from location 0000h. Each interrupt is assigned a fixed location in program memory. The interrupt causes the CPU to jump to that location, where it executes the service routine. External Interrupt 0 for example, is assigned to location 0003h. If external Interrupt 0 is used, its service routine must begin at location 0003h. If the Interrupt I is not used its service location is available as general-purpose program memory. The interrupt service locations are spaced at 8 byte intervals 0003h for External interrupt 0, 000Bh for Timer 0, 0013h for External interrupt 1,001Bh for Timer1, and so on.

Lower part of the program memory
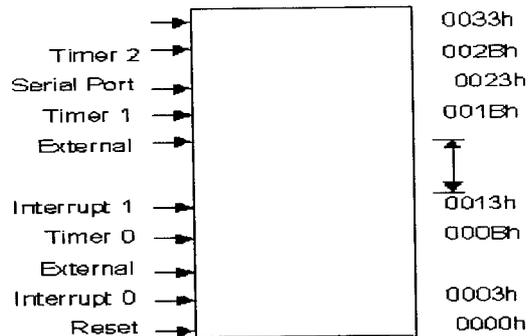
If an Interrupt service routine is short enough (as is often the case in control applications) it can reside entirely within that 8-byte interval. Longer service routines can use a jump instruction to skip over subsequent interrupt locations. If other interrupts are in use. The lowest addresses of program memory can be either in the on-chip Flash or in an external memory. To make this selection, strap the External Access (EA) pin to either Vcc or GND. For example, in the AT89C51 with 4K bytes of on-chip Flash, if the EA pin is strapped to Vcc, program fetches to addresses 0000h through 0FFFh are directed to internal Flash. Program fetches to addresses 1000h through FFFFh are directed to external memory.

DATA MEMORY:

The Internal Data memory is dived into three blocks namely,

 - ➢ The lower 128 Bytes of Internal RAM.
 - ➢ The Upper 128 Bytes of Internal RAM.
 - ➢ Special Function Register.

Internal Data memory Addresses are always 1 byte wide, which implies an address space of only 256 bytes. However, the addressing modes for internal RAM can in fact accommodate 384 bytes. Direct addresses higher than 7Fh access one memory space and indirect addresses higher than 7Fh access a different Memory Space. The lowest 32 bytes are grouped into 4 banks of 8 registers. Program instructions call out these registers as R0 through R7. Two bits in the Program Status Word (PSW) Select, which register bank, are in use. This architecture allows more efficient use of code space, since register instructions are shorter than instructions that use direct addressing.

The next 16-bytes of the above register banks form a block of bit addressable memory space. The micro controller instruction set includes a wide selection of single - bit instructions and this instruction can directly address the 128 bytes in this area. These bit addresses are 00h through 7Fh. either directs or indirect addressing can access all of the bytes in lower 128 bytes. Indirect addressing can only access the upper 128. The upper 128 bytes of RAM are only in the devices with 256 bytes of RAM. The Special Function Register includes Port latches, timers, peripheral controls etc., direct addressing can only access these register.

In general, all ATMEL micro controllers have the same SFRs at the same addresses in SFR space as the AT89C51 and other compatible micro controllers. However, upgrades to the AT89C51 have additional SFRs. Sixteen addresses in SFR space are both byte and bit Addressable. The bit Addressable SFRs are those whose address ends in 000B. The bit addresses in this area are 80h through FFh.

ADDRESSING MODES:

There are three types of addressing. They are
- Direct addressing-Nine variations.
- Indirect addressing- Nine variations.
- Indexed addressing- Nine variations.

DIRECT ADDRESSING:

In direct addressing, the operand is specified by an 8-bit address field in the instruction. Only internal data RAM and SFR's can be directly addressed.

INDIRECT ADDRESSING:

In Indirect addressing, the instruction specifies a register that contains the address of the operand. Both internal and external RAM can indirectly address. The address register for 8-bit addresses can be either the Stack Pointer or R0 or R1 of the selected register Bank. The address register for 16-bit addresses can be only the 16-bit data pointer register, DPTR.

INDEXED ADDRESSING:

Program memory can only be accessed via indexed addressing this addressing mode is intended for reading look-up tables in program memory. A 16 bit base register (Either DPTR or the Program Counter) points to the base of the table, and the accumulator is set up with the table entry number. Adding the accumulator data to the base pointer forms the address of the table entry in program memory. Another type of Indexed addressing is used in the "case jump" instructions. In this case the destination address of a jump instruction is computed as the sum of the base pointer and the accumulator data.

REGISTER INSTRUCTION:

The register banks, which contains registers R0 through R7, can be accessed by instructions whose op-codes carry a 3-bit register specification. Instructions that access the registers this way make efficient use of code, since this mode eliminates an address byte. When the instruction is executed, one of four banks is selected at execution time by the row bank select bits in PSW.

REGISTER - SPECIFIC INSTRUCTION:

Some Instructions are specific to a certain register. For example some instruction always operates on the Accumulator, so no address byte is needed to point OT. In these cases, the opcode itself points to the correct register. Instruction that rigger to Accumulator as A assemble as Accumulator - specific Opcode.

IMMEDIATE CONSTANTS:

The value of a constant can follow the opcode in program memory For example. MOV A, #100 loads the Accumulator with the decimal number 100. The same number could be specified in hex digit as 64h.

CPU TIMING:

A machine cycle consists of 6 states. Each stare is divided into a phase / half, during which the phase 1 clock is active and phase 2 half. Arithmetic and Logical operations take place during phase1 and internal register - to register transfer take place during phase 2.

PIN DIAGRAM OF ATMEL 89C51 MICROCONTROLLER

```
            P1.0 ⊏  1        40  ⊐ VCC
            P1.1 ⊏  2        39  ⊐ P0.0 (AD0)
            P1.2 ⊏  3        38  ⊐ P0.1 (AD1)
            P1.3 ⊏  4        37  ⊐ P0.2 (AD2)
            P1.4 ⊏  5        36  ⊐ P0.3 (AD3)
            P1.5 ⊏  6        35  ⊐ P0.4 (AD4)
            P1.6 ⊏  7        34  ⊐ P0.5 (AD5)
            P1.7 ⊏  8        33  ⊐ P0.6 (AD6)
             RST ⊏  9        32  ⊐ P0.7 (AD7)
       (RXD) P3.0 ⊏ 10       31  ⊐ EA/VPP
       (TXD) P3.1 ⊏ 11       30  ⊐ ALE/PROG
       (INT0) P3.2 ⊏ 12      29  ⊐ PSEN
       (INT1) P3.3 ⊏ 13      28  ⊐ P2.7 (A15)
        (T0) P3.4 ⊏ 14       27  ⊐ P2.6 (A14)
        (T1) P3.5 ⊏ 15       26  ⊐ P2.5 (A13)
        (WR) P3.6 ⊏ 16       25  ⊐ P2.4 (A12)
        (RD) P3.7 ⊏ 17       24  ⊐ P2.3 (A11)
           XTAL2 ⊏ 18        23  ⊐ P2.2 (A10)
           XTAL1 ⊏ 19        22  ⊐ P2.1 (A9)
             GND ⊏ 20        21  ⊐ P2.0 (A8)
```
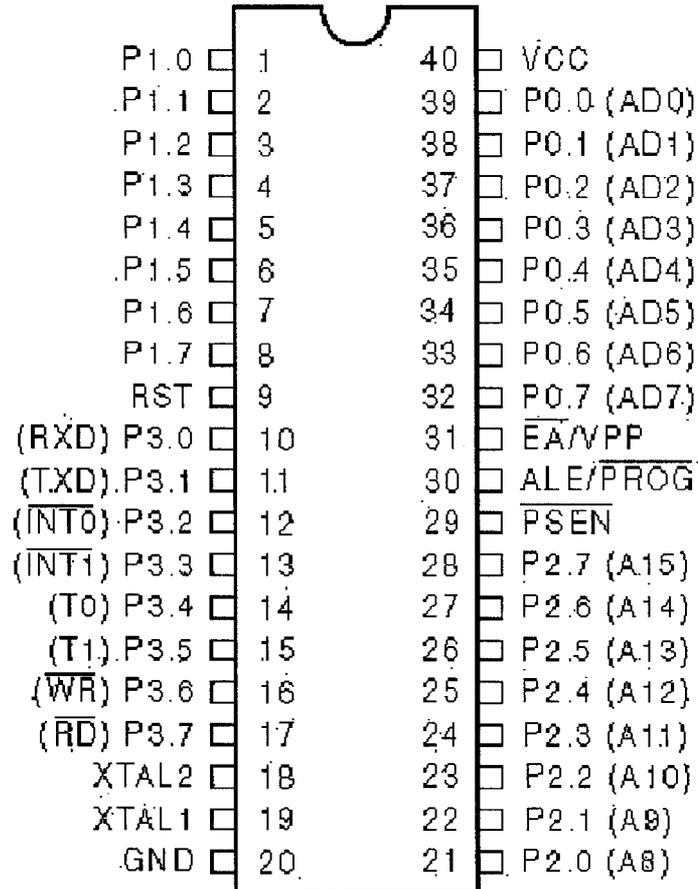
Pin Description:

VCC

Supply voltage.

GND

Ground.

Port 0

Port 0 is an 8-bit open-drain bi-directional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high impedance inputs. Port 0 may also be configured to be the multiplexed low order address/data bus during accesses to external program and data memory. In this mode P0 has internal pull-ups. Port 0 also receives the code bytes during Flash programming, and outputs the code bytes during program verification. External pull-ups are required during program verification.

Port 1

Port 1 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (IIL) because of the internal pull-ups. Port 1 also receives the low-order address bytes during. Flash programming and verification.

Port 2

Port 2 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (IIL) because of the internal pull-ups. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, it uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register. Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

Port 3

Port 3 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (IIL) because of the pull-ups. Port 3 also serves the functions of various special features of the AT89C51 as listed below:

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	INT0 (external interrupt 0)
P3.3	INT1 (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	WR (external data memory write strobe)
P3.7	RD (external data memory read strobe)

Port 3 also receives some control signals for Flash programming and verification.

RST

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

ALE/PROG

Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input (PROG) during Flash programming. In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory. If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or OVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the micro controller is in external execution mode.

PSEN

Program Store Enable is the read strobe to external program memory. When the AT89C51 is executing code from external program memory, PSEN is activated twice each machine cycle, except that two PSEN activations are skipped during each access to external data memory.

EA/VPP

External Access Enable. EA must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, EA will be internally latched on reset. EA should be strapped to VCC for internal program executions. This pin also receives the 12-volt programming enable voltage (VPP) during Flash programming, for parts that require 12-volt VPP.

XTAL1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

XTAL2

Output from the inverting oscillator amplifier.

RS232 CABLE

RS-232C SERIAL DATA STANDARD

In the 1960s as the use of time-share computer terminals became more widespread; modems were developed so that terminals could use phone lines to communicate with distant computers. As we stated earlier, modems and other devices used to send serial data are often referred to as data communication equipment or DCE. The terminals or computers that are sending or receiving the data are referred to as data terminal equipment or DTE. In response to the need for signal and handshake standards between DTE and DCE, the Electronic Industries Association (EIA) developed EIA standard RS-232C. This standard describes the functions of 25 signal and handshake pins for serial data transfer. It also describes the voltage levels. Impedance levels, rise and fall times, maximum bit rate, and maximum capacitance for these signal lines. Before we work our way through the 25 pin functions, we will take a brief look at some of the other hardware aspects of RS-232C.

RS-232C specifies 25 signal pins and it specifies that the DTE connector should be a male, and the DCE connector should be a female. A specific connector is not given, but the most commonly used connectors are the DB-25P male and the DB-25S female shown in figure, when you are wiring up these connectors. It is important to note the order in which the pins are numbered. The voltage levels for all RS-232C signals are as follows. A logic high, or mark, is a voltage between −3V and −15 V under load (-25 V no load). A logic low or space is a voltage between +3 V and +15 under load (+25 V no load). Voltage such as 12 V is commonly used. The output signal level usually swings between +12V and -12V. The "dead area" between +3v and -3v is designed to absorb line noise. In the various RS-232-like definitions this dead area may vary. For instance, the definition for V.10 has a dead area from +0.3v to -0.3v. Many receivers designed for RS-232 are sensitive to differentials of 1v or less.

DP9 PIN CONNECTOR
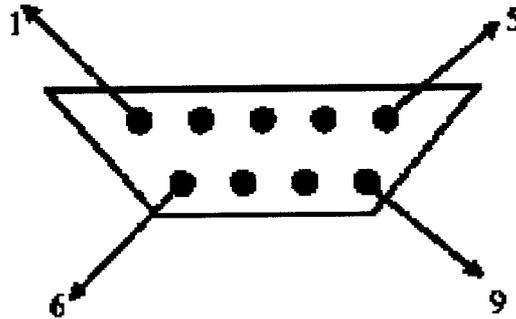
RS232 Pin Assignments	
Pin 1	Received Line Signal Detector (Data Carrier Detect)
Pin 2	Received Data
Pin 3	Transmit Data
Pin 4	Data Terminal Ready
Pin 5	Signal Ground
Pin 6	Data Set Ready
Pin 7	Request To Send
Pin 8	Clear To Send
Pin 9	Ring Indicator

PIN DESCRIPTION:

DTR (Data terminal ready):

When the terminal is turned on, after going through a self-test, it sends out signal DTR to indicate that it is ready for communication.

DSR (Data set ready):

When DCE is turned on and has gone through the self-test, it asserts DSR to indicate that it is ready to communicate.

RTS (Request to send):

When the DTE device (such as a pc) has a byte to transmit, it asserts RTS to signal the modem that it has a byte of data to transmit.

CTS (clear to send):

In response to RTS when the modem has room for storing the data it is to receive, it sends out signal CTS to the DTE (PC) to indicate that it can receive the data now.

DCD (data carrier detect):

The modem assert signal DCD to inform the DTE (PC) that a valid carrier has been detected and that contact between it and the other modem is established.

RI (ring indicator):

An output from the modem (DCE) and an input to a PC (DTE) indicates that the telephone is ringing. It goes on and off in synchronization with the ringing sound. While signals DTR and DSR are used by the pc and modem respectively, to indicate that they are alive and well, it is RTS and CTS that actually control the flow of data. RTS and CTS are also referred to as hardware control flow signals. This concludes the description of the 9 most important pins of the RS232 handshake signals plus TxD, RxD, and ground. ground is also referred to as SG (signal ground).
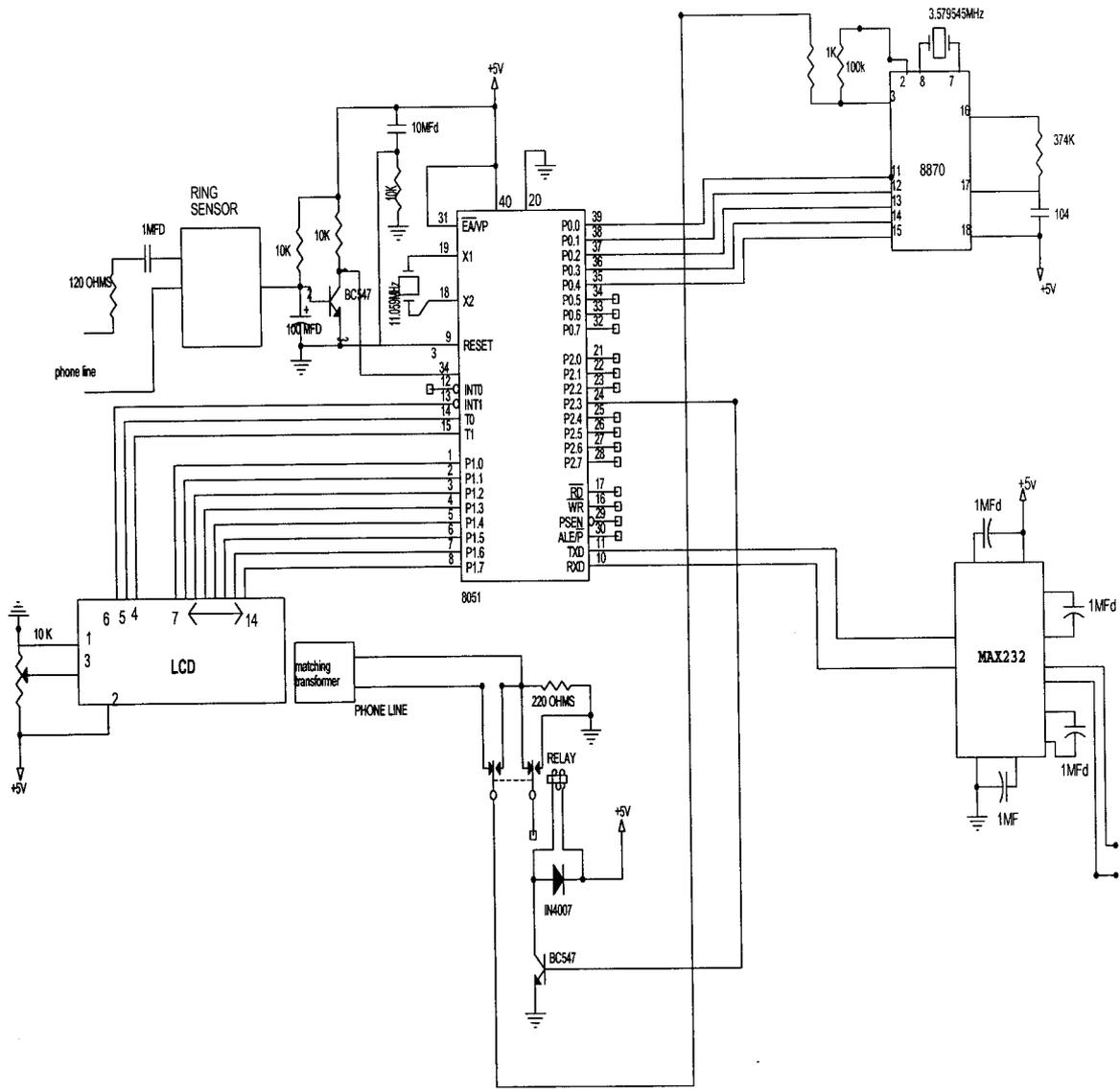
CIRCUIT DIAGRAM

CIRCUIT DIAGRAM

TRANSMITTER SECTION:

HEART PULSE THROUGH TELEPHONE LINE
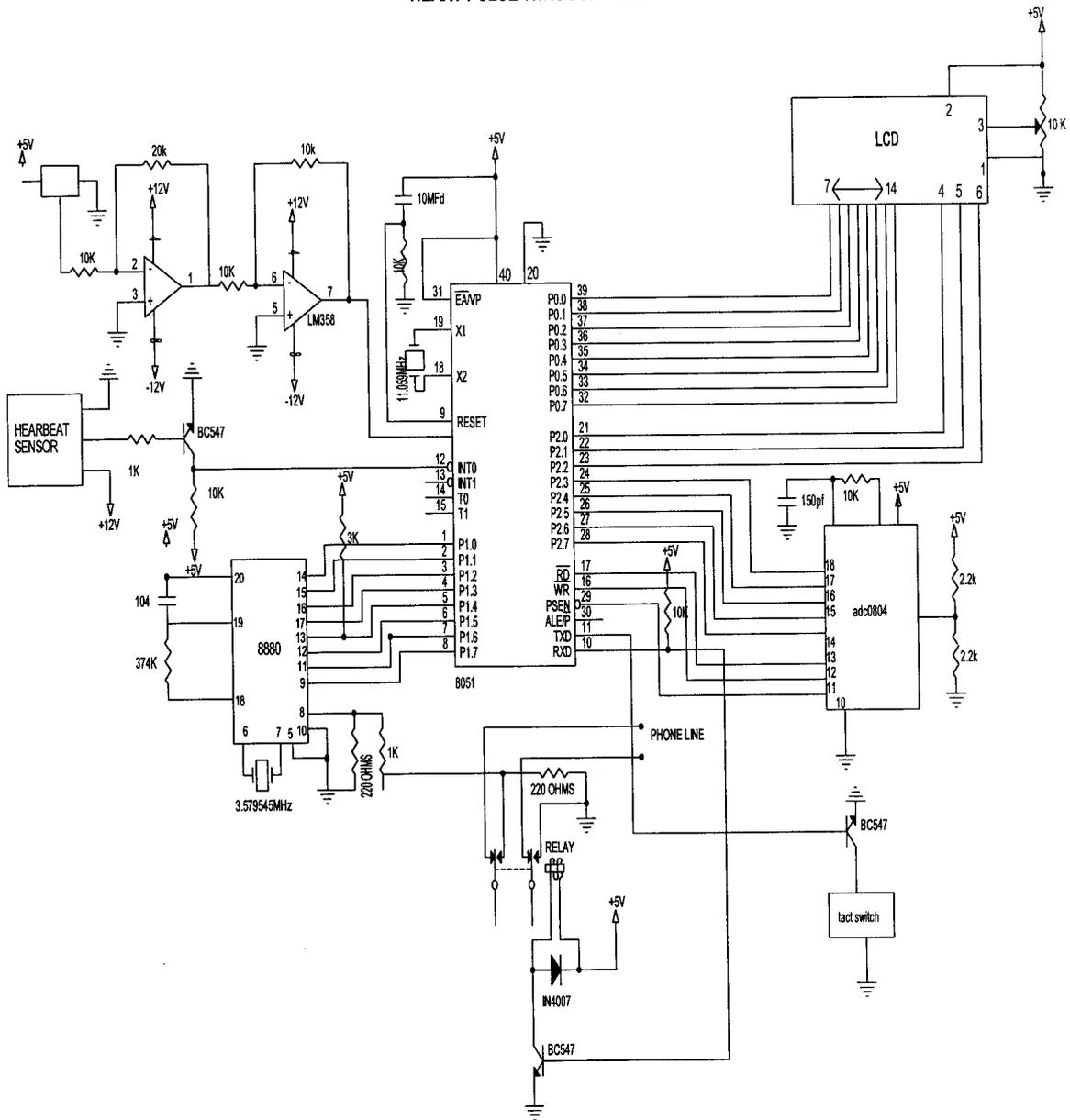
RECEIVER SECTION:

HEART PULSE THROUGH TELEPHONE LINE

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SOFTWARE

SOURCE CODE

PC INTERFACING PROGRAM:

```c
#include <bios.h>
#include <conio.h>
#include <stdio.h>
#include <dos.h>
#include <time.h>
#include<string.h>
#include<ctype.h>

#include<stdlib.h>
#include<process.h>

#define COM0  1
#define COM1  0 ////////////////

#define SETTINGS0 (_COM_9600| _COM_CHR8 | _COM_STOP1 |
_COM_NOPARITY)
#define SETTINGS1 (_COM_9600| _COM_CHR8 | _COM_STOP1 |
_COM_NOPARITY)

#define TRANS0 0x2f8
#define TRANS1 0x3F8 //2f8

unsigned char t1[8],i;
unsigned int ack,temp,t;
```

```c
void main()
{
                                    // initialize serial port
    _bios_serialcom(_COM_INIT,COM0,SETTINGS0);
    _bios_serialcom(_COM_INIT,COM1,SETTINGS1);
    clrscr();
    textcolor(BLACK);
    textbackground(CYAN);
        while(1)
          {
          ack=inportb(TRANS1);
          if(ack==0xaa)
              {
                t1[1]=ack;
                while(t1[1]==ack)
                 {
                  t1[1]=inportb(TRANS1);
                 }
              }
          else if(ack==0xab)
              {
                t1[2]=ack;
                while(t1[2]==ack)
                 {
                  t1[2]=inportb(TRANS1);
                 }
              }
```

```c
            else if(ack==0xac)
        {
         t1[3]=ack;
         while(t1[3]==ack)
          {
           t1[3]=inportb(TRANS1);
          }
        }
    else if(ack==0xad)
        {
         t1[4]=ack;
         while(t1[4]==ack)
          {
           t1[4]=inportb(TRANS1);
          }
        }
    else if(ack==0xae)
         {
         t1[5]=ack;
         while(t1[5]==ack)
          {
           t1[5]=inportb(TRANS1);
          }
         }
             /*


         t1[2]=ack=t1[1];
         while(t1[2]==ack)
          {
```

```c
     t1[2]=inportb(TRANS1);
     }
    t1[3]=ack=t1[2];
    while(t1[3]==ack)
     {
      t1[3]=inportb(TRANS1);
     }
    t1[4]=ack=t1[3];
    while(t1[4]==ack)
     {
      t1[4]=inportb(TRANS1);
     }
    t1[5]=ack=t1[4];
    while(t1[5]==ack)
     {
      t1[5]=inportb(TRANS1);
     }
   }      */

  temp=t1[4]<<4;
  temp=temp|t1[5];
  gotoxy(20,10);
  printf("TEMPERATURE  = %d  C          ",temp);

  gotoxy(20,15);
  printf("HEART BEAT   = %d" "%d" "%d        ",t1[1],t1[2],t1[3]);

  }
}
```

CONCLUSION

CONCLUSION

This system is designed for remote monitoring of a patients health. It detects the heart pulse and temperature. These signals are transmitted continuously to a remote monitoring station through a telephone line. Since the transmission of data is done through a telephone line the chances of error are minimal. Further as telephone networks are well established it can be implemented anywhere. Incase we make use of intercom's for transmission there are no call charges involved and hence the system turns out to be cost effective. This system was tested for all type of conditions and found reliable.

This project can be extended to monitor several patients at the same time. Further it could be designed to monitor various other parameters such as insulin levels, blood pressure and other medical parameters by providing appropriate sensors. Bi-directional data transmission can also be made possible.

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BIBLIOGRAPHY

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❖ www.microchip.com

❖ www.electronicsforu.com

APPENDIX

L7800
SERIES

## POSITIVE VOLTAGE REGULATORS

- OUTPUT CURRENT UP TO 1.5 A
- OUTPUT VOLTAGES OF 5: 5.2: 6: 8: 8.5: 9:
  12: 15: 18: 24V
- THERMAL OVERLOAD PROTECTION
- SHORT CIRCUIT PROTECTION
- OUTPUT TRANSITION SOA PROTECTION

DESCRIPTION

The L7800 series of three-terminal positive regulators is available in TO-220 ISOWATT220 TO-3 and D²PAK packages and several fixed output voltages. making it useful in a wide range of applications.These regulators can provide local on-card regulation. eliminating the distribution problems associated with single point regulation. Each type employs internal current limiting. thermal shut-down and safe area protection. making it essentially indestructible. If adequate heat sinking is provided. they can deliver over 1A output current. Although designed primarily as fixed voltage regulators. these devices can be used with external components to obtain adjustable voltages and currents.

TO-3   D²PAK

TO-220   ISOWATT220
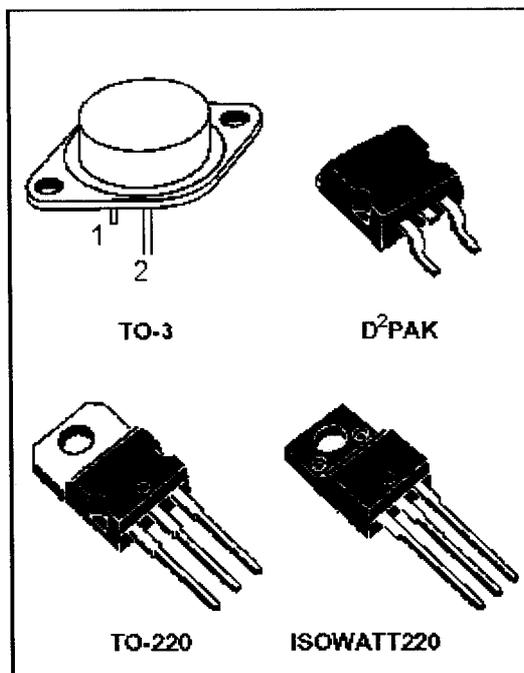
BLOCK DIAGRAM
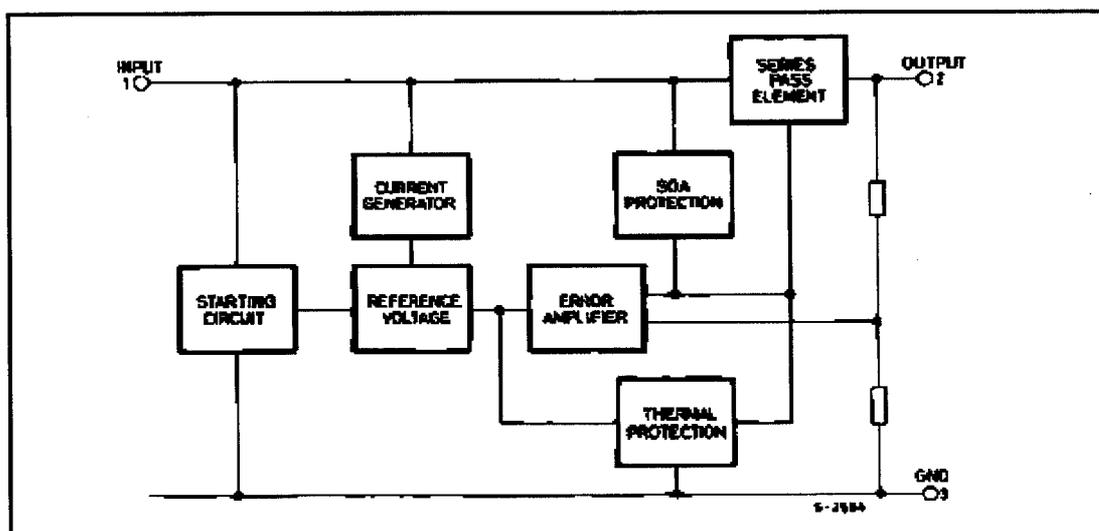
ELECTRICAL CHARACTERISTICS FOR L7805 (refer to the test circuits, T_j = -55 to 150 °C, V_i = 10V, I_o = 500 mA, C_i = 0.33 µF, C_o = 0.1 µF unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	T_j = 25 °C	4.8	5	5.2	V
V_o	Output Voltage	I_o = 5 mA to 1 A $P_o \le$ 15 W V_i = 8 to 20 V	4.65	5	5.35	V
ΔV_o*	Line Regulation	V_i = 7 to 25 V T_j = 25 °C V_i = 8 to 12 V T_j = 25 °C		3 1	50 25	mV mV
ΔV_o*	Load Regulation	I_o = 5 to 1500 mA T_j = 25 °C I_o = 250 to 750 mA T_j = 25 °C			100 25	mV mV
I_d	Quiescent Current	T_j = 25 °C			6	mA
ΔI_d	Quiescent Current Change	I_o = 5 to 1000 mA			0.5	mA
ΔI_d	Quiescent Current Change	V_i = 8 to 25 V			0.8	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5 mA		0.6		mV/°C
eN	Output Noise Voltage	B = 10Hz to 100KHz T_j = 25 °C			40	µV/Vo
SVR	Supply Voltage Rejection	V_i = 8 to 18 V f = 120Hz	68			dB
V_d	Dropout Voltage	I_o = 1 A T_j = 25 °C		2	2.5	V
R_o	Output Resistance	f = 1 KHz		17		mΩ
I_{sc}	Short Circuit Current	V_i = 35 V T_j = 25 °C		0.75	1.2	A
I_{scp}	Short Circuit Peak Current	T_j = 25 °C	1.3	2.2	3.3	A

ELECTRICAL CHARACTERISTICS FOR L7812 (refer to the test circuits, T_j = -55 to 150 °C, V_i = 19V, I_o = 500 mA, C_i = 0.33 µF, C_o = 0.1 µF unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	T_j = 25 °C	11.5	12	12.5	V
V_o	Output Voltage	I_o = 5 mA to 1 A $P_o \le$ 15 W V_i = 15.5 to 27 V	11.4	12	12.6	V
ΔV_o*	Line Regulation	V_i = 14.5 to 30 V T_j = 25 °C V_i = 16 to 22 V T_j = 25 °C			120 60	mV mV
ΔV_o*	Load Regulation	I_o = 5 to 1500 mA T_j = 25 °C I_o = 250 to 750 mA T_j = 25 °C			100 60	mV mV
I_d	Quiescent Current	T_j = 25 °C			6	mA
ΔI_d	Quiescent Current Change	I_o = 5 to 1000 mA			0.5	mA
ΔI_d	Quiescent Current Change	V_i = 15 to 30 V			0.8	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5 mA		1.5		mV/°C
eN	Output Noise Voltage	B = 10Hz to 100KHz T_j = 25 °C			40	µV/Vo
SVR	Supply Voltage Rejection	V_i = 15 to 25 V f = 120Hz	61			dB
V_d	Dropout Voltage	I_o = 1 A T_j = 25 °C		2	2.5	V
R_o	Output Resistance	f = 1 KHz		18		mΩ
I_{sc}	Short Circuit Current	V_i = 35 V T_j = 25 °C		0.75	1.2	A
I_{scp}	Short Circuit Peak Current	T_j = 25 °C	1.3	2.2	3.3	A

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

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National Semiconductor

LM320L/LM79LXXAC Series
3-Terminal Negative Regulators

General Description

The LM320L/LM79LXXAC dual marked series of 3-terminal negative voltage regulators features fixed output voltages of −5V, −12V, and −15V with output current capabilities in excess of 100mA. These devices were designed using the latest computer techniques for optimizing the packaged IC thermal/electrical performance. The LM79LXXAC series, even when combined with a minimum output compensation capacitor of 0.1 μF, exhibits an excellent transient response, a maximum line regulation of 0.07% V_O/V, and a maximum load regulation of 0.01% V_O/mA.

The LM320L/LM79LXXAC series also includes, as self-protection circuitry: safe operating area circuitry for output transistor power dissipation limiting, a temperature independent short circuit current limit for peak output current limiting, and a thermal shutdown circuit to prevent excessive junction temperature. Although designed primarily as a fixed voltage regulators, these devices may be combined with simple external circuitry for boosted and/or adjustable voltages and currents. The LM79LXXAC series is available in the 3-lead

TO-92 package, 8-lead SOIC package, and the 6-Bump micro SMD package. The LM320L series is available in the 3-lead TO-92 package.

For output voltage other than −5V, −12V and −15V, the LM137L series provides an output voltage range from 1.2V to 47V.

Features

■ Preset output voltage error is less than ±6% overload, line and temperature
■ Specified at an output current of 100mA
■ Easily compensated with a small 0.1μF output capacitor
■ Internal short-circuit, thermal and safe operating area protection
■ Easily adjustable to higher output voltages
■ Maximum line regulation less than 0.07% V_{OUT}/V
■ Maximum load regulation less than 0.01% V_{OUT}/mA
■ See AN-1112 for micro SMD considerations

Typical Applications

Fixed Output Regulator
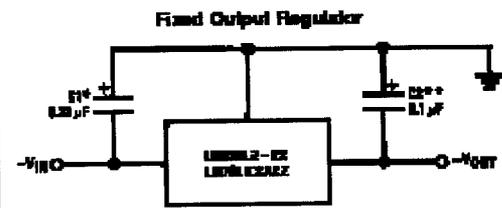
*Required if the regulator is located far from the power supply filter. A 1μF aluminum electrolytic may be substituted.

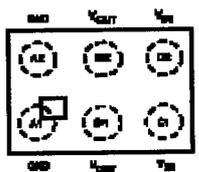**Required for stability. A 1μF aluminum electrolytic may be substituted.

Adjustable Output Regulator
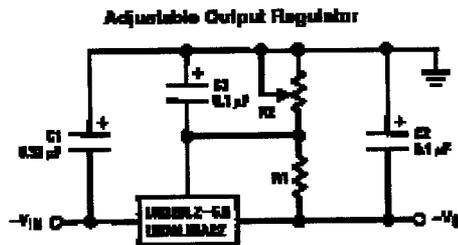
$−V_O = −5V − (5V/R1 + I_Q) × R2,$
$5V/R1 > 3 I_Q$

Connection Diagrams

6-Bump micro SMD

Bump Side Down

TO-92 Plastic Package (Z)

Bottom View

LM320L/LM79LXXAC

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Input Voltage

$V_O = -5V, -12V, -15V$ .... −35V

Internal Power Dissipation (Note 2) ... Internally Limited

Operating Temperature Range .... 0°C to +70°C
Maximum Junction Temperature .... +125°C
Storage Temperature Range .... −65°C to +150°C
Lead Temperature
(Soldering, 10 sec.) .... 230°C

Electrical Characteristics (Note 3)

$T_A = 0°C$ to +70°C unless otherwise noted.

	Output Voltage		−5V			−12V			−15V			
	Input Voltage (unless otherwise noted)		−10V			−17V			−20V			Units
Symbol	Parameter	Conditions	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_O	Output Voltage	$T_J = 25°C, I_O = 100mA$	−5.2	−5	−4.8	−12.5	−12	−11.5	−15.6	−15	−14.4	V
		$1mA \leq I_O \leq 100mA$ $V_{MIN} \leq V_{IN} \leq V_{MAX}$	−5.25 ($-20 \leq$		−4.75 $V_{IN} \leq -7.5$)	−12.6 ($-27 \leq$		−11.4 $V_{IN} \leq -14.6$)	−15.75 ($-30 \leq$		−14.25 $V_{IN} \leq -18$)	V
		$1mA \leq I_O \leq 40mA$ $V_{MIN} \leq V_{IN} \leq V_{MAX}$	−5.25 ($-20 \leq$		−4.75 $V_{IN} \leq -7$)	−12.6 ($-27 \leq$		−11.4 $V_{IN} \leq -14.6$)	−15.75 ($-30 \leq$		−14.25 $V_{IN} \leq -17.5$)	V
ΔV_O	Line Regulation	$T_J = 25°C, I_O = 100mA$		80			45			45		mV
		$V_{MIN} \leq V_{IN} \leq V_{MAX}$		($-20 \leq V_{IN} \leq -7.3$)			($-27 \leq V_{IN} \leq -14.6$)			($-30 \leq V_{IN} \leq -17.7$)		V
		$T_J = 25°C, I_O = 40mA$		80			45			45		mV
		$V_{MIN} \leq V_{IN} \leq V_{MAX}$		($-20 \leq V_{IN} \leq -7$)			($-27 \leq V_{IN} \leq -14.6$)			($-30 \leq V_{IN} \leq -17.6$)		V
ΔV_O	Load Regulation	$T_J = 25°C$ $1mA \leq I_O \leq 100mA$		50			100			125		mV
ΔV_O	Long Term Stability	$I_O = 100mA$		20			48			60		mV/khrs
I_Q	Quiescent Current	$I_O = 100mA$		2	6		2	6		2	6	mA
ΔI_Q	Quiescent Current Change	$1mA \leq I_O \leq 100mA$		0.3			0.3			0.3		
		$1mA \leq I_O \leq 40mA$		0.1			0.1			0.1		mA
		$I_O = 100mA$		0.25			0.25			0.25		mA
		$V_{MIN} \leq V_{IN} \leq V_{MAX}$		($-20 \leq V_{IN} \leq -7.5$)			($-27 \leq V_{IN} \leq -14.6$)			($-30 \leq V_{IN} \leq -18$)		V
V_n	Output Noise Voltage	$T_J = 25°C, I_O = 100mA$ $f = 10Hz - 10kHz$		40			88			120		µV
$\frac{\Delta V_{IN}}{\Delta V_O}$	Ripple Rejection	$T_J = 25°C, I_O = 100mA$ $f = 120Hz$	60			52			60			dB
	Input Voltage Required to Maintain Line Regulation	$T_J = 25°C, I_O = 100mA$		−7.3			−14.6			−17.7		V
		$I_O = 40mA$		−7.0			−14.5			−17.5		V

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits.

Note 2: Thermal resistance of Z package is 80°C/W θ_{JA}, 55°C/W θ_{JA}, at still air, and 85°C/W at 400 ft/min of air. The M package θ_{JA} is 160°C/W in still air. The maximum junction temperature shall not exceed 125°C on electrical parameters.

Note 3: To ensure constant junction temperature, low duty cycle pulse testing is used.

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LM35
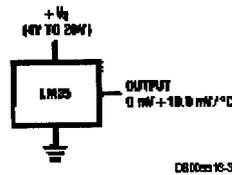# Precision Centigrade Temperature Sensors

General Description

The LM35 series are precision integrated-circuit temperature sensors, whose output voltage is linearly proportional to the Celsius (Centigrade) temperature. The LM35 thus has an advantage over linear temperature sensors calibrated in ˚ Kelvin, as the user is not required to subtract a large constant voltage from its output to obtain convenient Centigrade scaling. The LM35 does not require any external calibration or trimming to provide typical accuracies of ±¼˚C at room temperature and ±¾˚C over a full −55 to +150˚C temperature range. Low cost is assured by trimming and calibration at the wafer level. The LM35's low output impedance, linear output, and precise inherent calibration make interfacing to readout or control circuitry especially easy. It can be used with single power supplies, or with plus and minus supplies. As it draws only 60 µA from its supply, it has very low self-heating, less than 0.1˚C in still air. The LM35 is rated to operate over a −55˚ to +150˚C temperature range, while the LM35C is rated for a −40˚ to +110˚C range (−10˚ with improved accuracy). The LM35 series is available packaged in hermetic TO-46 transistor packages, while the LM35C, LM35CA, and LM35D are also available in the plastic TO-92 transistor package. The LM35D is also available in an 8-lead surface mount small outline package and a plastic TO-220 package.
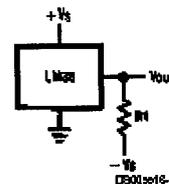
Features

- Calibrated directly in ˚ Celsius (Centigrade)
- Linear + 10.0 mV/˚C scale factor
- 0.5˚C accuracy guaranteeable (at +25˚C)
- Rated for full −55˚ to +150˚C range
- Suitable for remote applications
- Low cost due to wafer-level trimming
- Operates from 4 to 30 volts
- Less than 60 µA current drain
- Low self-heating, 0.08˚C in still air
- Nonlinearity only ±¼˚C typical
- Low impedance output, 0.1 Ω for 1 mA load

Typical Applications

FIGURE 1. Basic Centigrade Temperature Sensor
(+2˚C to +150˚C)

Choose R₁ = −V_S/50 µA
V_OUT=+1,500 mV at +150˚C
        = +250 mV at +25˚C
        = −550 mV at −55˚C

FIGURE 2. Full-Range Centigrade Temperature Sensor

M-8880 DTMF Transceiver

CLARE

Advanced CMOS technology for low power consumption and increased noise immunity

Complete DTMF transmitter/receiver in a single chip

Standard 6500/6800 series microprocessor port

Central office quality and performance

Adjustable guard time

Automatic tone burst mode

Call progress mode

Single +5 Volt power supply

20-pin DIP and SOIC packages

2 MHz microprocessor port operation

Inexpensive 3.58 MHz crystal

No continuous 2 clock required, only strobe

Applications include: paging systems, repeater systems/mobile radio, interconnect dialers, PBX systems, computer systems, fax machines, pay telephones, credit card verification

The M-8880 is a complete DTMF Transmitter/Receiver that features adjustable guard time, automatic tone burst mode, call progress mode, and a fully compatible 6500/6800 microprocessor interface. The receiver portion is based on the industry standard M-8870 DTMF Receiver, while the transmitter uses a switched-capacitor digital-to-analog converter for low-distortion, highly accurate DTMF signaling. Tone bursts can be transmitted with precise timing by making use of the automatic tone burst mode. To analyze call progress tones, a call progress filter can be selected by an external microprocessor.
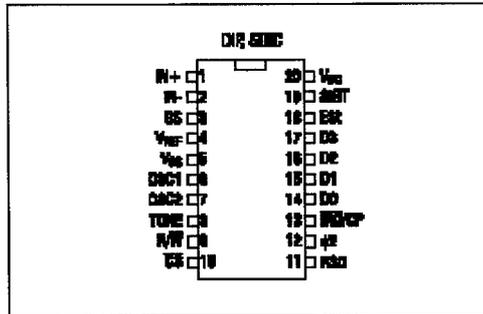

Figure 1 Pin Diagram

Functional Description

M-8880 functions consist of a high-performance DTMF receiver with an internal gain setting amplifier and a DTMF generator that contains a tone burst counter for generating precise tone bursts and pauses. The call progress mode, when selected, allows the detection of call progress tones. A standard 6500/6800 series microprocessor interface allows access to an internal status register, two control registers, and two data registers.

Input Configuration

The input arrangement consists of a differential input operational amplifier and bias sources (V_{REF}) for biasing the amplifier inputs at $V_{DD}/2$. Provisions are made for the connection of a feedback resistor to the op-amp output (GS) for gain adjust-
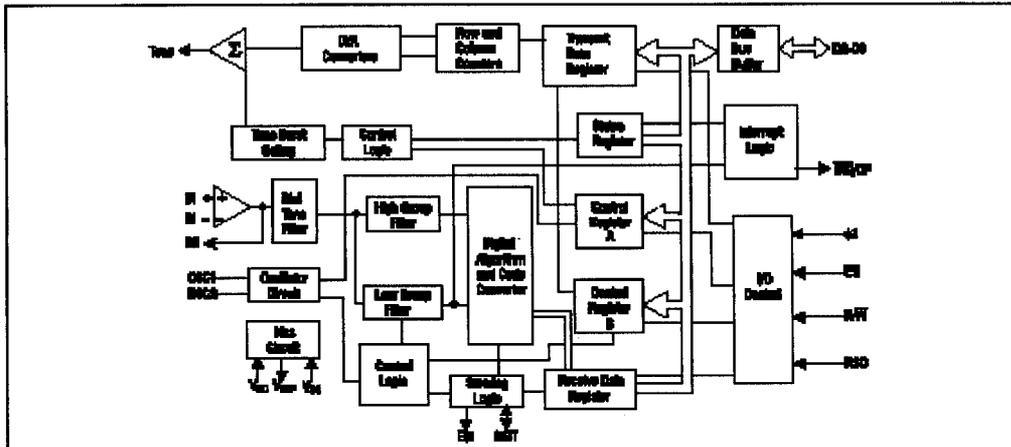

Figure 2 Block Diagram

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Table 12 AC Characteristics

PARAMETER	SYMBOL	MIN	TYP*	MAX	UNITS
Receive signal conditions					
Valid input signal levels (each tone of composite signal; Notes 1, 2, 3, 5, 8, 9)		-29 / 27.5	— / —	+1 / 8??	dBm / mVrms
Positive twist accept (Notes 2, 3, 8, 9)		—		8	dB
Negative twist accept (Notes 2, 3, 8, 9)		—		8	dB
Frequency deviation accept (Notes 2, 3, 5, 9)		±1.5% ±2 Hz	—	—	Nom.
Frequency deviation reject (Notes 2, 3, 8)		±3.5%	—	—	Nom.
Third tone tolerance (Notes 2, 3, 4, 5, 8, 10)		—	-16	—	dB
Noise tolerance (Notes 2, 3, 4, 5, 7, 8, 10)		—	-12	—	dB
Dial tone tolerance (Notes 2, 3, 4, 5, 8, 9, 11)		—	+22	—	dB
Call progress					
Lower frequency (@ -25 dBm) accept	f_{LA}	—	320	—	Hz
Upper frequency (@ -25 dBm) accept	f_{HA}	—	510	—	Hz
Lower frequency (@ -25 dBm) reject	f_{LR}	—	290	—	Hz
Upper frequency (@ -25 dBm) reject	f_{HR}	—	540	—	Hz
Receive timing					
Tone present detect time	t_{DP}	5	11	14	ms
Tone absent detect time	t_{DA}	0.5	4	8.5	ms
Tone duration accept (ref. Figure 12)	t_{REC}	—	—	40	ms
Tone duration reject (ref. Figure 12)	t_{REC}	20	—	—	ms
Interdigit pause accept (ref. Figure 12)	t_{ID}	—	—	40	ms
Interdigit pause reject (ref. Figure 12)	t_{IDD}	20	—	—	ms
Delay St to b3	t_{PStb3}	—	13	—	µs
Delay St to RX0—RX3	t_{PSRX}	—	8	—	µs
Transmit timing					
Tone burst duration (DTMF mode)	t_{BST}	50	—	52	ms
Tone pause duration (DTMF mode)	t_{PB}	50	—	52	ms
Tone burst duration (extended, call progress mode)	t_{BSTE}	100	—	104	ms
Tone pause duration (extended, call progress mode)	t_{PSE}	100	—	104	ms
Tone output					
High group output level (R_L = 10 kΩ)	V_{HOUT}	-8.1	—	-2.1	dBm
Low group output level (R_L = 10 kΩ)	V_{LOUT}	-8.1	—	-4.1	dBm
Pre-emphasis (R_L = 10 kΩ)	dB_P	0	2	3	dB
Output distortion (R_L = 10 kΩ, 3.4 kHz bandwidth)	THD	—	-25	—	dB
Frequency deviation (f = 3.5795 MHz)	f_D	—	±0.7	±1.5	%
Output load resistance	R_{LT}	10	—	50	kΩ
Microprocessor interface					
φ 2 cycle period	t_{CYC}	0.5	—	—	µs
φ2 high pulse width	t_{CH}	200	—	—	ns
φ2 low pulse width	t_{CL}	180	—		ns
φ2 rise and fall time	t_R, t_F	—	—	25	ns
Address, R/W hold time	t_{AH}, t_{RWH}	10	—	—	ns
Address, R/W setup time (prior to φ2)	t_{AS}, t_{RWS}	23	—	—	ns

N *National Semiconductor*

ADC0801/ADC0802/ADC0803/ADC0804/ADC0805
8-Bit μP Compatible A/D Converters

General Description

The ADC0801, ADC0802, ADC0803, ADC0804 and ADC0805 are CMOS 8-bit successive approximation A/D converters that use a differential potentiometric ladder—similar to the 256R products. These converters are designed to allow operation with the NSC800 and INS8080A derivative control bus with TRI-STATE® output latches directly driving the data bus. These A/Ds appear like memory locations or I/O ports to the microprocessor and no interfacing logic is needed.

Differential analog voltage inputs allow increasing the common-mode rejection and offsetting the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

Features

- Compatible with 8080 μP derivatives—no interfacing logic needed - access time - 135 ns
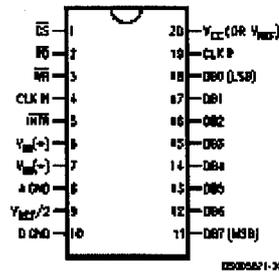- Easy interface to all microprocessors, or operates "stand alone"

- Differential analog voltage inputs
- Logic inputs and outputs meet both MOS and TTL voltage level specifications
- Works with 2.5V (LM336) voltage reference
- On-chip clock generator
- 0V to 5V analog input voltage range with single 5V supply
- No zero adjust required
- 0.3" standard width 20-pin DIP package
- 20-pin molded chip carrier or small outline package
- Operates ratiometrically or with 5 V_{DC}, 2.5 V_{DC}, or analog span adjusted voltage reference

Key Specifications

- Resolution   8 bits
- Total error $\pm\frac{1}{4}$ LSB, $\pm\frac{1}{2}$ LSB and ±1 LSB
- Conversion time   100 μs

Connection Diagram

ADC080X
Dual-In-Line and Small Outline (SO) Packages

CS—1		20—V_{CC} (OR V_{REF})
RD—2		19—CLK R
WR—3		18—DB0 (LSB)
CLK IN—4		17—DB1
INTR—5		16—DB2
V_{IN}(+)—6		15—DB3
V_{IN}(-)—7		14—DB4
A GND—8		13—DB5
V_{REF}/2—9		12—DB6
D GND—10		11—DB7 (MSB)

DS005671-30

See Ordering Information

Ordering Information

	TEMP RANGE	0°C TO 70°C	0°C TO 70°C	-40°C TO +85°C
ERROR	$\pm\frac{1}{4}$ Bit Adjusted			ADC0801LCN
	$\pm\frac{1}{2}$ Bit Unadjusted	ADC0802LCWM		ADC0802LCN
	$\pm\frac{1}{2}$ Bit Adjusted			ADC0803LCN
	±1 Bit Unadjusted	ADC0804LCWM	ADC0804LCN	ADC0805LCN/ADC0804LCJ
PACKAGE OUTLINE		M20B — Small Outline	N20A — Molded DIP	

www.national.com

HD44780U (LCD-II)

(Dot Matrix Liquid Crystal Display Controller/Driver)

HITACHI

Description

The HD44780U dot-matrix liquid crystal display controller and driver LSI displays alphanumerics, Japanese kana characters, and symbols. It can be configured to drive a dot-matrix liquid crystal display under the control of a 4- or 8-bit microprocessor. Since all the functions such as display RAM, character generator, and liquid crystal driver, required for driving a dot-matrix liquid crystal display are internally provided on one chip, a minimal system can be interfaced with this controller/driver.

A single HD44780U can display up to one 8-character line or two 8-character lines.

The HD44780U has pin function compatibility with the HD44780S which allows the user to easily replace an LCD-II with an HD44780U. The HD44780U character generator ROM is extended to generate 208 5 × 8 dot character fonts and 32 5 × 10 dot character fonts for a total of 240 different character fonts.

The low power supply (2.7V to 5.5V) of the HD44780U is suitable for any portable battery-driven product requiring low power dissipation.

Features

- 5 × 8 and 5 × 10 dot matrix possible
- Low power operation support:
  — 2.7 to 5.5V
- Wide range of liquid crystal display driver power
  — 3.0 to 11V
- Liquid crystal drive waveform
  — A (One line frequency AC waveform)
- Correspond to high speed MPU bus interface
  — 2 MHz (when $V_{cc} = 5V$)
- 4-bit or 8-bit MPU interface enabled
- 80 × 8-bit display RAM (80 characters max.)
- 9,920-bit character generator ROM for a total of 240 character fonts
  — 208 character fonts (5 × 8 dot)
  — 32 character fonts (5 × 10 dot)