DSP BASED UNIVERSAL MOTOR CONTROLLER

P-1148

PROJECT REPORT

Submitted by

SRIHARI.T	-2KEEE47
ANGAPPARAJ.K	-2KEEE02
LAKSHMI NARAYAN.R	-2KEEE18
AYYANNAN.S	-2KEEE06

Guided by

Mr.R.K.Pongiannan,M.E.

Senior Lecturer, Dept. of EEE

In partial fulfillment of the requirements for the

Award of the degree of BACHELOR OF ENGINEERING in ELECTRICAL AND ELECTRONICS ENGINEERING Branch of BHARATHIAR UNIVERSITY, COIMBATORE

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

KUMARAGURU COLLEGE OF TECHNOLOGY

COIMBATORE - 641 006

Estd-1984

ISO 9001:2000 Certified

2003 - 2004

Estd-1984

KUMARAGURU COLLEGE OF TECHNOLOGY

COIMBATORE - 641 006

ISO 9001:2000 Certified

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

CERTIFICATE

This is to certify that the project report entitled

DSP BASED UNIVERSAL MOTOR CONTROLLER

Is the bonafide work done by

_____

in partial fulfillment of the requirements for the Award of the degree of

Bachelor of Engineering In Electrical and Electronics Engineering Branch of

Bharathiar University, Coimbatore

_____

Guide

_____

Professor and Head

Date:

Certified that the candidate _____ *with*

University Register No. _____ *was examined in*

Project work Viva-Voce Examination on _____

_____

Internal Examiner

_____

External Examiner

ACKNOWLEDGEMENT

We express our deep sense of gratitude to **Dr.K.K.Padmanabhan,B.Sc.,(Engg).,M.Tech.,Ph.D.,** Principal, Kumaraguru College of Technology, Coimbatore, for providing facilities to carry out this project work.

With profound sense of gratitude and regards, we acknowledge with great pleasure the guidance and support extended by **Dr.T.Kameswaran,B.E,M.Sc.,(Engg),Ph.D.,MISTE,Sr.M.I.E.E.E.,F.I.E.**, Prof. and Head ,Department of Electrical and Electronics Engineering, for his valuable and continuous guidance, suggestions, constructive criticisms and persistent encouragement.

We also express our deep sense of respectful gratitude to our guide **Mr.R.K.Pongiannan M.E.,** Senior Lecturer, Department of Electrical and Electronics Engineering for his valuable guidance, keen suggestions, innovative ideas, inspiration, discussions, helpful criticisms and kind encouragement in all the phases of this project work. It had been indeed a great pleasure to work under his guidance.

We also very sincerely thank our **parents** and **friends** who have been very understanding and supportive throughout the entire course of this project. Without their constant encouragement and support this project would not have been possible.

SYNOPSIS

The unpredicted development in industrial drives over the past two decades has resulted from the process developments demanded by the automation industry. This development has been further accelerated due to increased speed of modern microprocessors, micro controllers, digital signal processors (DSP), complex programmable logic devices (CPLD), application specific integrated circuit (ASIC) technology and Field programmable gate array (FPGA) based control techniques. Digital controllers allow implementation of sophisticated operating algorithms, offering significant technical advantages due to their ability of fast processing of vast data, high operational flexibility, and ease of integration into automated industrial systems.

This project "***DSP BASED UNIVERSAL MOTOR CONTROLLER***" presents closed loop control of a Universal motor using DSP Controller. The control scheme is simple in architecture and thus facilitates the realization of the proposed DSP Controller. The proposed design scheme has been realized using the Texas Instruments TMS320C25 DSP. The speed of a Universal motor is controlled by adjusting the applied voltage through phase angle control. Using this system accurate speed control of the Universal motor over a wide range of speeds from 1000 rpm to 8500 rpm has been achieved. The designed DSP Controller IC is re-programmable, and thus provides efficient as well as flexible control and reduces the total size of the system.

This technique can be further improved by design of a sensor-less speed control system in which the running speed of the motor can be calculated by sensing the load current. This results in elimination of maintenance-prone mechanical coupling elements.

CONTENTS

CHAPTER 1

INTRODUCTION

Owing to the rapid development in industrial automation the Digital control of most of the main stream industrial drives have been realized. The Industrial AC drive control has been implemented with high performance low cost ASICs like microprocessors, micro controllers and Digital Signal Processors. But the area of automated control of the numerous motor driven appliances that operate in homes and businesses today has long been a neglected field in motor control. Most of these appliances lack a proper motor controller in order to run the motor more efficiently. This is due to the lack of affordable high-performance digital controllers which can control these motors. But with the development and mass production of low-cost Micro-controllers and DSPs, there has been a paradigm shift in the area of Motor control outside the industrial scenario. Particularly, the DSPs have paved the way toward efficient and accurate control of small sized motors.

Analog circuitry has been used to implement motor control in the past. But the design and implementation of analog control circuits for small sized motors is a time consuming and futile process. The adaptive capability of DSP is making it the technology of choice for many applications as the same controller can be used with many types of motors by changing the software part only with out any major changes to hardware.

1.1 Analog Vs Digital Control Systems:

Early solid state controls consisted of hardwired analog networks built around operational amplifiers. Analog controls offer two distinct advantages over digital systems:

- Higher speed control by processing input data in real time
- Higher resolution over wider bandwidths because of infinite sampling rates.

However, there are several drawbacks to analog systems:

- Aging and temperature can cause component variations,which in turn causes the system to need regular adjustment.
- Analog systems have more physical parts than digital systems, which reduces reliability and makes analog systems more difficult to design (component tolerance issues).
- Upgrades are difficult because the design is hardwired.

1.2 Benefits of Microcontrollers:

- Drift is eliminated since most functions are performed digitally.
- Upgrades are easily made in software.
- Part count is reduced because the microcontroller can handle several functions on-chip. Microcontrollers are good for systems that do not require high speed or precision.

1.3 Benefits of DSP-Based Control:

The TMS320C25 DSP includes the same advantages as the microcontroller but also offers higher speed, higher resolution, and capabilities to implement the math-intensive algorithms to lower the system cost. The high speed is attributable mainly to the dual bus of the Harvard architecture as well as single-cycle multiplication and addition instructions. One bus is used for data and the other is used for program instructions.

This saves time because each is utilized simultaneously. Traditionally, cost has been a potential disadvantage of the DSP solution, but this aspect has diminished with the continuing decline of DSP costs.

DSP controllers enable enhanced, real-time algorithms. The combination reduces the number of components and optimizes the design of silicon to achieve a system cost reduction. DSPs are capable of processing data at much faster rates than microcontrollers.

DSP-based controls offer the following additional benefits:

- Diagnostic monitoring achieved by the fast Fourier transform (FFT) of spectrum analysis. By observing the frequency spectrum of mechanical vibrations, failure modes can be predicted in early stages.
- Adaptive control by having the speed to monitor and control the system concurrently. A dynamic control algorithm adapts itself in real time to variations in system behavior.
- System cost reduction by an efficient control in all speed ranges, implying right dimensioning of power device circuits.
- Reduced harmonics using enhanced algorithms to meet easier requirements and reduce filter costs
- Reduce the number of look-up tables, which reduces the amount of memory needed
- Real-time generation of smooth, near-optimal reference profiles and move trajectories, which results in better performance.
- Single chip control system

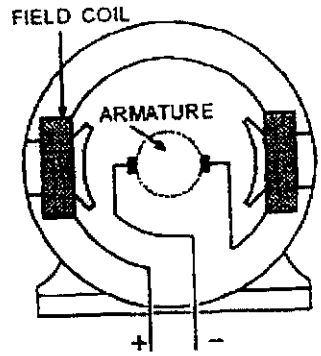
1.4 UNIVERSAL MOTOR:

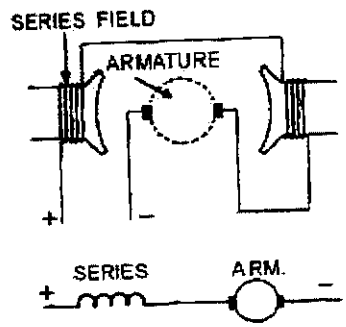
The universal motor is a rotating electric machine similar to a DC motor but designed to operate either from direct current or single-phase alternating current. It is essentially a dc series motor, with some differences in construction. In series motor, torque depends on the product of armature current And field flux.Reversal of the terminal voltage reverses both the armature current and field flux.Consequently torque remains in the same direction. Therefore, when fed from an AC source ,the series motor produces unidirectional torque.

A simple DC series motor does not operate well on AC. .Hysterisis and eddy current losses that occur in field poles and yoke reduce motor efficiency and increase thermal loading. Due to commutation excessive sparking at the commutator occurs.motor power factor is poor due to large inductance of field and armature.

Universal motor is specially constructed to solve these limitations.In addition to armature,field poles and yokes are also laminated to reduce eddy current losses. A compensating winding is used in series with armature to reduce armature inductance.

The stator and rotor windings of the motor are connected in series through the rotor commutator. Therefore the universal motor is also known as an AC series motor or an AC commutator motor.



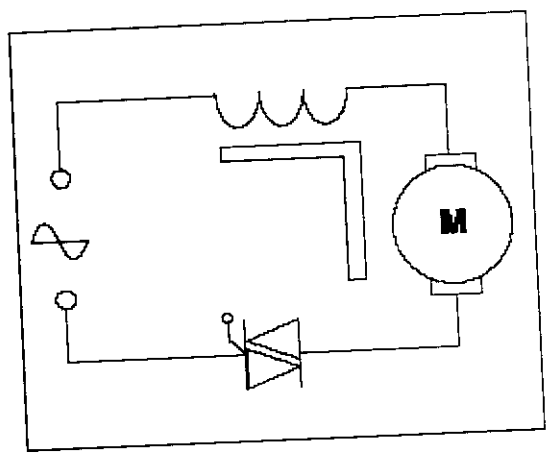


A series ac motor is the same electrically as a dc series motor. the left- hand rule is applied for the polarity of coils. the instantaneous magnetic polarities of the armature and field oppose each other, and motor action results. Now, reverse the current by reversing the polarity of the input. Note that the field magnetic polarity still opposes the armature magnetic polarity. This is because the reversal effects both the armature and the field. The ac input causes these reversals to take place continuously.

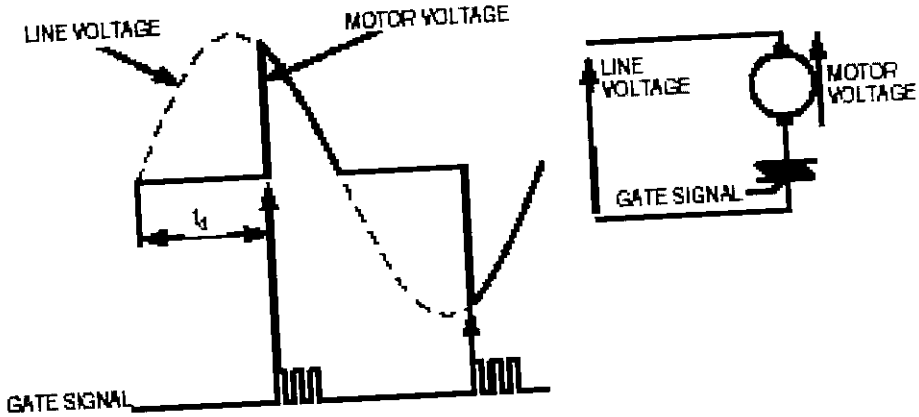
Universal motors operate at lower efficiency than either the ac or dc series motor. They are built in small sizes only. Universal motors do not operate on polyphase ac power.

Most universal motors are manufactured for use at speed in excess of 3000 rpm. Below this speed generally induction motor is considered. Because of high operating speeds, universal motor is much smaller in size compared to an induction or a low speed DC motor of identical rating.

In our project "***DSP based control of Universal Motor***", the digital signal processor is used for the closed loop control. A Universal motor may be operated either on direct or single-phase a.c.supply at approximately the same speed and output. Being a series-wound motor, it has high starting torque and a variable speed characteristic. In our project the speed of the Universal motor is controlled by controlling the applied voltage. Here the motor is run on 230 volts single phase a.c supply which is varied by phase angle controls implemented using a Triac (BT 139). To control the phase angle at which the Triac conducts, the trigger pulse given to the Triac should be varied, this is accomplished in an efficient and fast manner using the DSP (tms320c25). The speed of the motor is detected using a magnetic pick-up and given as input to the DSP in order to implement closed loop control.



Phase Angle control uses a low frequency switch to chop an AC sine wave. The firing angle of the switch is varied. The average voltage will be proportional the area under the sine wave. Thus, the average voltage is the integral from the firing angle to the zero crossing, the cosine of the firing angle. Phase Angle control provides a very inexpensive method to control the average voltage of an AC source.



CHAPTER 2

2.1 Introduction

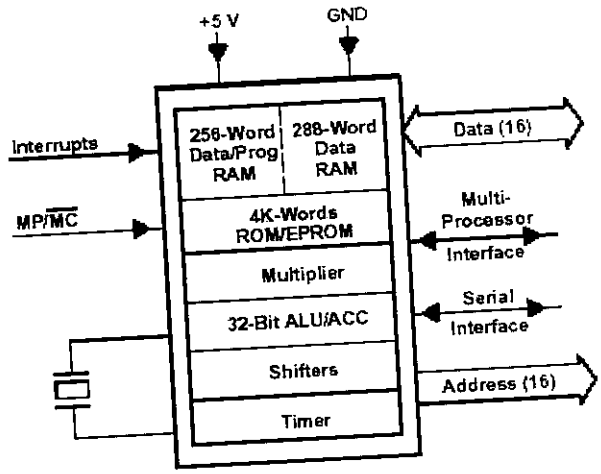
The TMS320 family of 16/32-bit single-chip digital signal processors combines the flexibility of a high-speed controller with the numerical capability of an array processor, thereby offering an inexpensive alternative to multichip bit-slice processors. The highly paralleled architecture and efficient instruction set provide speed and flexibility to produce a MOS microprocessor family that is capable of executing more than 12.5 MIPS (million instructions per section). The TMS320 family optimizes speed by implementing functions in hardware that other processors implement through microcode or software.

The **TMS320C25** is the second member of the TMS320 second generation. It is processed in CMOS technology, is capable of an instruction cycle time of 100 ns, and is pin-for-pin and object-code compatible with the TMS32020. The TMS320C25's enhanced feature set greatly increases the functionality of the device over the TMS32020. Enhancements included 24 additional instructions (133 total), eight auxiliary registers, an eight-level hardware stack, 4K words of on-chip program ROM, a bit-reversed indexed-addressing mode, and the low-power dissipation inherent to the CMOS process.

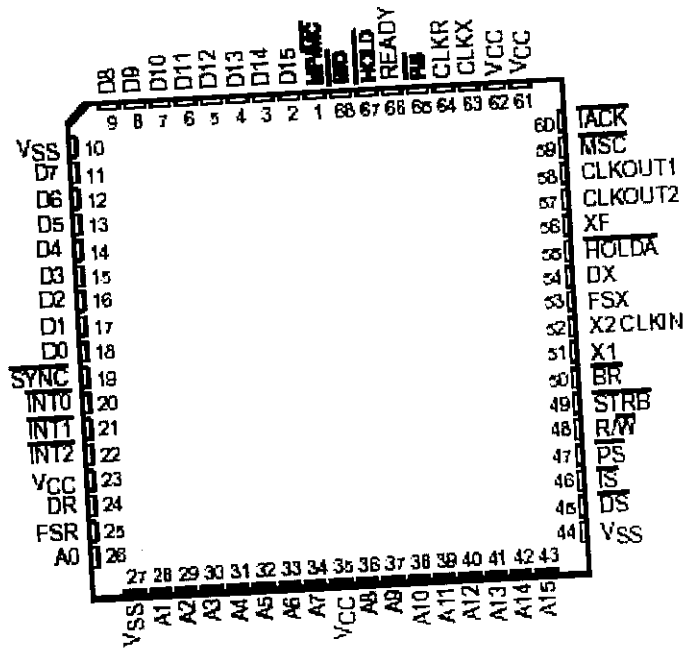
2.2 Key features of the TMS320C25

- 100-ns Instruction Cycle Time
- 4K Words of On-Chip Program ROM
- 544 Words of On-Chip RAM
- 128K Words of Total Program/DataMemory Space
- Wait States for Communications toSlower Off-Chip Memories
- Object-Code Compatible With the TMS32020
- Source-Code Compatible With TMS320C1x
- 24 Additional Instructions to SupportAdaptive Filtering, FFTs, and Extended- Precision Arithmetic
- Block Moves for Data/Program Management
- Single-Cycle Multiply/Accumulate Instructions
- Eight Auxiliary Registers With DedicatedArithmetic Unit
- Bit-Reversed Indexed-Addressing Mode for Radix-2 FFTS
- Double-Buffered Serial Port
- On-Chip Clock Generator
- Single 5-V Supply
- 68-to-28 Pin Conversion Adapter Socket
- CMOS Technology
- 68-Pin Grid Array (PGA) Package

2.3 Block Diagram



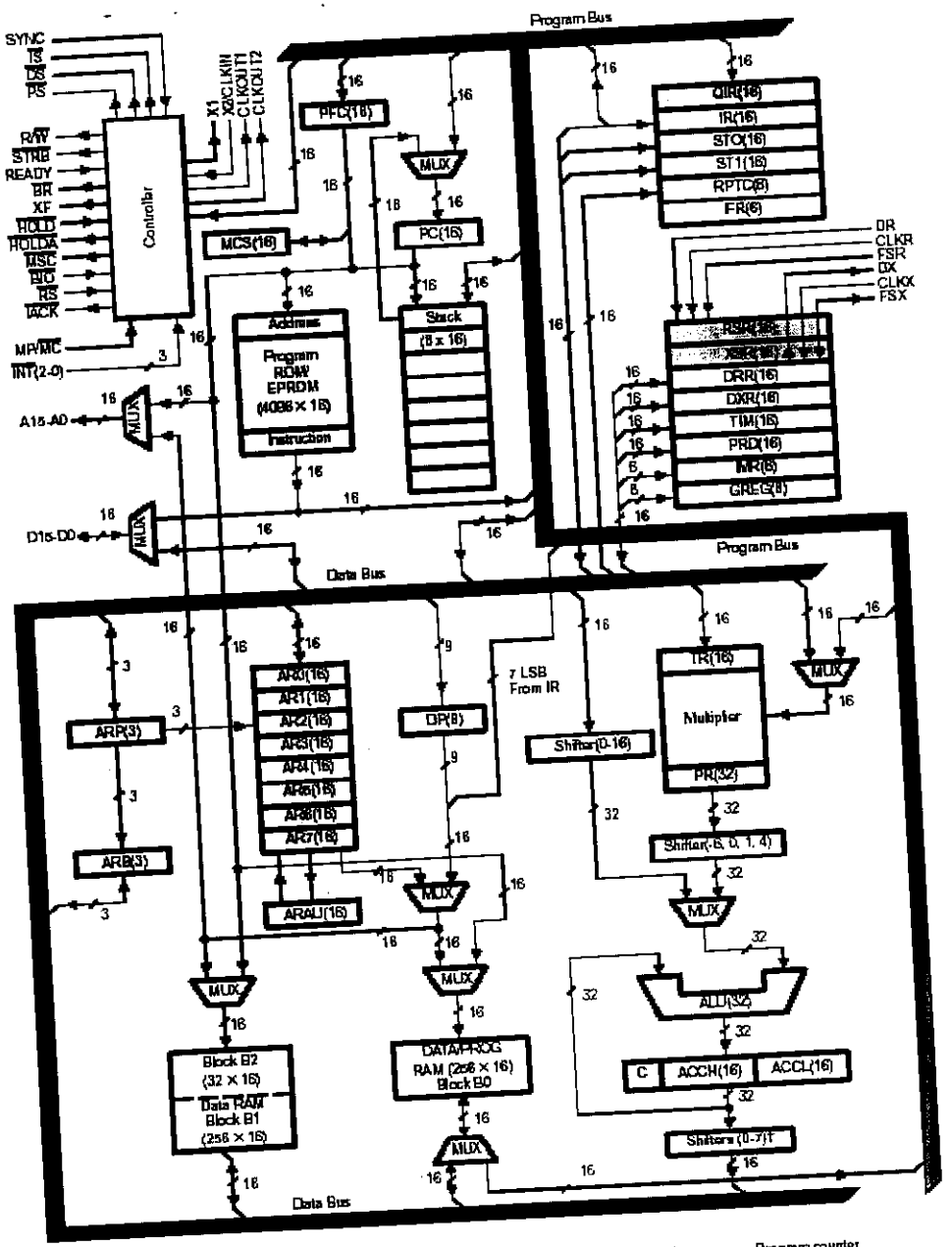
2.4 Pin Diagram



2.5 Architecture

The TMS320 family utilizes a modified Harvard architecture for speed and flexibility. In a strict Harvard architecture, program and data memory lie in two separate spaces, permitting a full overlap of instruction fetch and execution. The TMS320 family's modification of the Harvard architecture allows transfers between program and data spaces, thereby increasing the flexibility of the device. This modification permits coefficients stored in program memory to be read into the RAM, eliminating the need for a separate coefficient ROM. It also makes available immediate instructions and subroutines based on computed values. Increased throughput on the TMS320C2x devices for many DSP applications is accomplished by means of single-cycle multiply/accumulate instructions with a data move option, up to eight auxiliary registers with a dedicated arithmetic unit, and faster I/O necessary for data-intensive signal processing. The architectural design of the TMS320C2x emphasizes overall speed, communication, and flexibility in processor configuration. Control signals and instructions provide floating-point support, block-memory transfers, communication to slower off-chip devices, and multiprocessing implementations.

2.6 Functional Block Diagram



LEGEND:

ACCH	= Accumulator high	IFR	= Interrupt flag register	PC	= Program counter
ACCL	= Accumulator low	IMR	= Interrupt mask register	PFC	= Prefetch counter
ALU	= Arithmetic logic unit	IR	= Instruction register	RPTC	= Repeat instruction counter
ARAU	= Auxiliary register arithmetic unit MCS = Microcall stack			GREG	= Global memory allocation register
ARB	= Auxiliary register pointer buffer	QIR	= Queue instruction register	RSR	= Serial port receive shift register
ARP	= Auxiliary register pointer	PR	= Product register	XSR	= Serial port transmit shift register
DP	= Data memory page pointer	PRD	= Period register for timer	AR0-AR7	= Auxiliary registers
DRR	= Serial port data receive register TIM = Timer			ST0, ST1	= Status registers
DXR	= Serial port data transmit register	TR	= Temporary register	C	= Carry bit

2.7 Internal Architechture

The description of the basic building blocks are as follows:

2.7.1 32-bit ALU/accumulator

The 32-bit Arithmetic Logic Unit (ALU) and accumulator perform a wide range of arithmetic and logical instructions, the majority of which execute in a single clock cycle. The ALU executes a variety of branch instructions dependent on the status of the ALU or a single bit in a word. These instructions provide the following capabilities:

- Branch to an address specified by the accumulator
- Normalize fixed-point numbers contained in the accumulator
- Test a specified bit of a word in data memory

2.7.2 Scaling shifter

The TMS320C2x scaling shifter has 16-bit input connected to the data bus and a 32-bit output connected to the ALU. The scaling shifter produces a left shift of 0 to 16 bits on the input data, as programmed in the instruction.The LSBs of the output are filled with zeroes, and the MSBs may be either filled with zeroes or sign-extended, depending upon the status programmed into the SXM (sign-extension mode) bit of status register ST1.

2.7.3 16x 16-bit parallel multiplier

The 16x 16-bit hardware multiplier is capable of computing a signed or unsigned 32-bit product in a single machine cycle. The multiplier has the following two associated registers.

- A16-bit Temporary Register (TR) that holds one of the operands for the multiplier, and
- A 32-bit Product Register (PR) that holds the product.

2.7.4 Timer

The TMS320C2x provides a memory-mapped 16-bit timer for control operations. The on-chip timer (TIM) register is a down counter that is continuously clocked by CLKOUT1 on the TMS320C25. The timer is clocked by CLKOUT1/4 on the TMS32020. A timer interrupt (TINT) is generated every time the timer decrements to zero.

2.7.5 Memory control

The TMS320C25 provides a total of 544 16-bit words of on-chip data RAM, divided into three separate blocks (B0, B1, and B2). Of the 544 words, 288 words (blocks B1 and B2) are always data memory, and 256 words (block B0) are programmable as either data or program memory.

A data memory size of 544 words allows the TMS320C25 to handle a data array of 512 words (256 words if on-chip RAM is used for program memory), while still leaving 32 locations for intermediate storage. When using block B0 as program memory, instructions can be downloaded from external program memory into on-chip RAM and then executed.

2.7.6 Interrupts and Subroutines

The TMS320C2x has three external maskable user interrupts INT2-INT0, available for external devices that interrupt the processor. Internal interrupts are generated by the serial port (RINT and XINT), by the timer (TINT), and by the software interrupt (TRAP) instruction. Interrupts are prioritized with reset (RS) having the highest priority and the serial port transmit interrupt (XINT) having the lowest priority.

2.7.7 Multiprocessing

The flexibility of the TMS320C2x allows configurations to satisfy a wide range of system requirements and can be used as follows:

- A standalone processor
- A multiprocessor with devices in parallel
- A slave/host multiprocessor with global memory space
- A peripheral processor interfaced via processor-controlled signals to another device.

IMPLEMENTATION OF DSP BASED CONTROLLER

3.1.1 ALGORITHM:

Step 1: Start the process

Step 2: initialization of LCD with control words (0xc, 0x1) for left or right entry, clear RAM display

Step 3: check for three keys.

Step 4: if key 1 is high add 50 to reg. address and jump to step 3.else goto step 3

Step 5: if key 2 is high, subtract 50 to reg. address and jump to step 3.else goto Step 3.

Step 6: if key 3 is high, display running and enable timer interrupt

Step 7: check pulse from proximity sensor, for high pulse goto step 7, else goto Step 8.

Step 8: check low pulse, if low goto step 8 else goto step 9.

Step 9: add 1 to pulse register, goto step 7

3.1.2 TIMER ISR ALGORITHM:

Step 1: save stack pointer and status register

Step 2: if timer= 10 seconds , pulse = pulse * 6, goto step 3 else goto step 6

Step 3:display speed and compare with set speed.

Step 4: if speed greater than set speed, decrement DAC value by 5

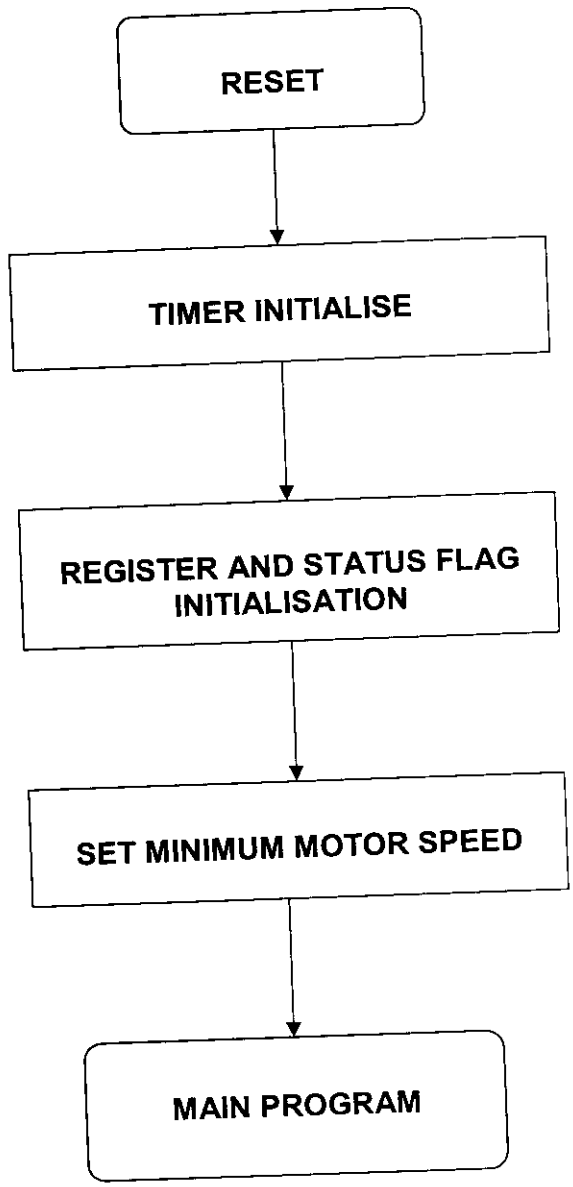
Step 5: else if speed is less than set speed, increment DAC value by 5.

clear pulse =0

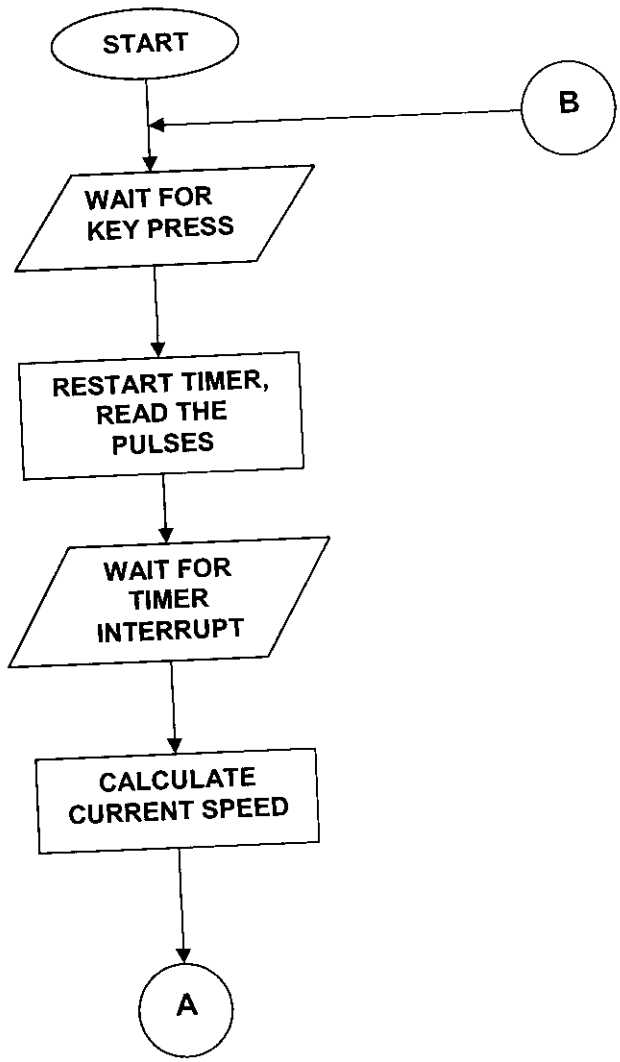
Step 6: store status register.

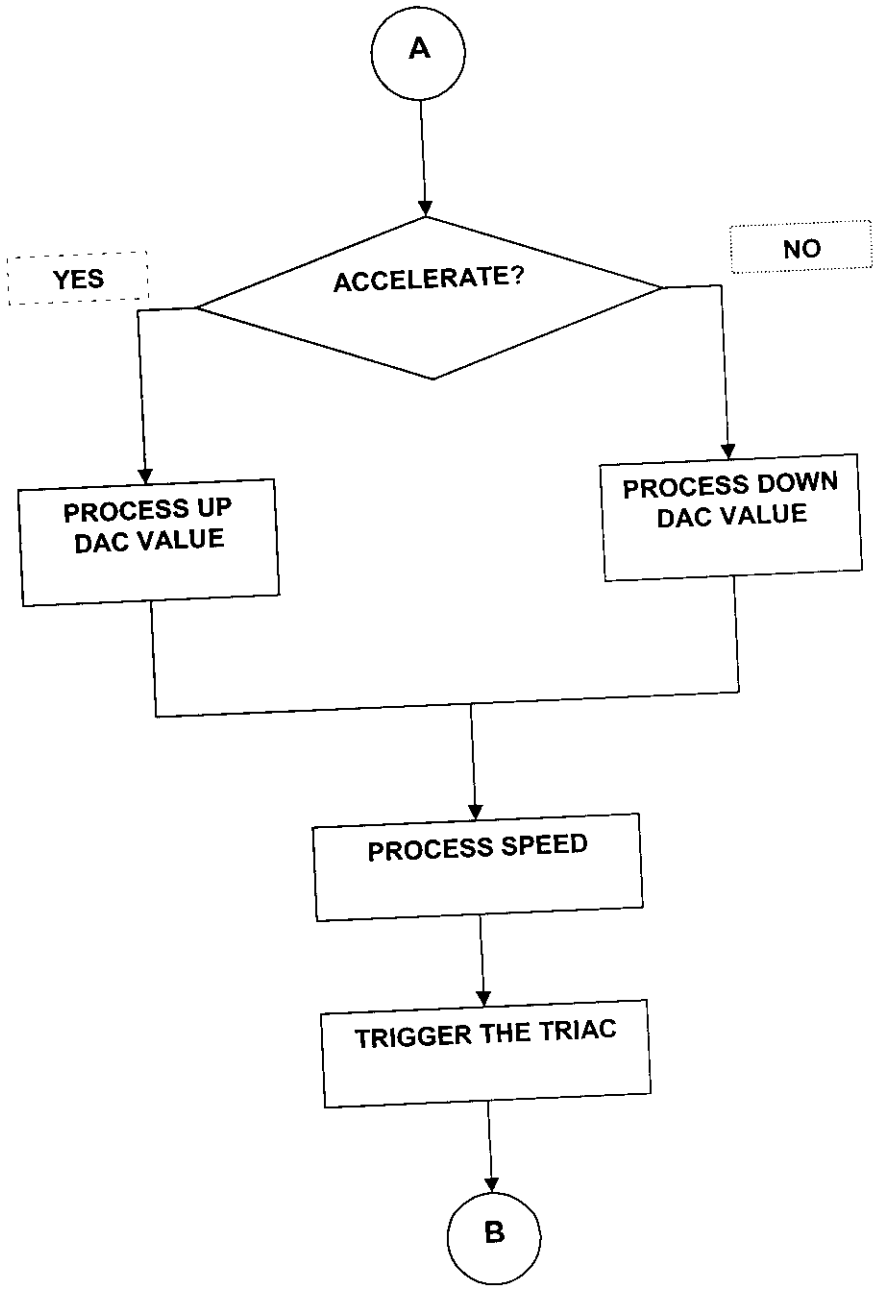
Step 7: return from interrupt routine.

3.1.3 POWER ON RESET FLOWCHART:



3.1.4 MAIN PROGRAM FLOWCHART:




A
ACCELERATE?
YES
NO
PROCESS UP DAC VALUE
PROCESS DOWN DAC VALUE
PROCESS SPEED
TRIGGER THE TRIAC
B

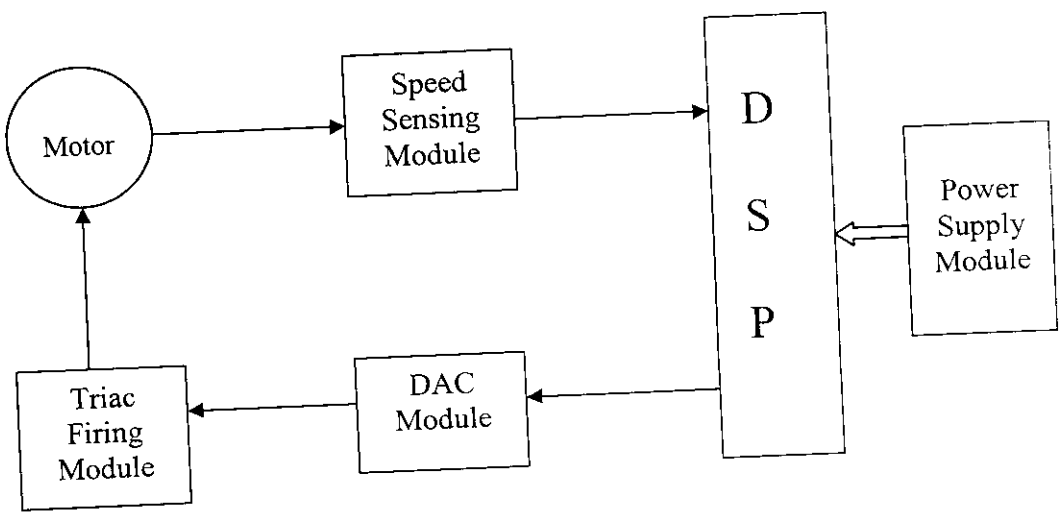
HARDWARE REALIZATION

3.2 Hardware Realization

The hardware realization of our project 'DSP BASED CONTROL OF UNIVERSAL MOTOR' consists of 4 modules. As one can see from the block diagram each and every module is separate from the rest and is integral to the functioning of the device. The modules have been fabricated keeping in mind the criteria of good efficiency, ease of construction and servicing.

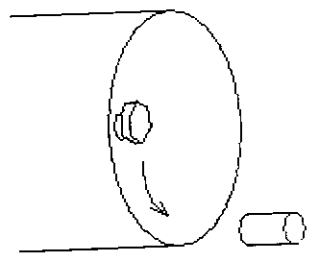
The four main modules are

i. Speed Sensing Module
ii. Power supply Module
iii. DAC Module
iv. Triac Firing Module



3.2.1 Speed Sensing Module

In order to detect motion, a sensor has to be able to detect two conditions, the presence or absence of a target. The target has to alternate so that the timing of alternation is proportional to the speed. Examples of this are found in sensing the sprocket teeth in a drive gear, a bolt installed in a conveyor roller, photo sensing products on a conveyor, or any repetitive motion.

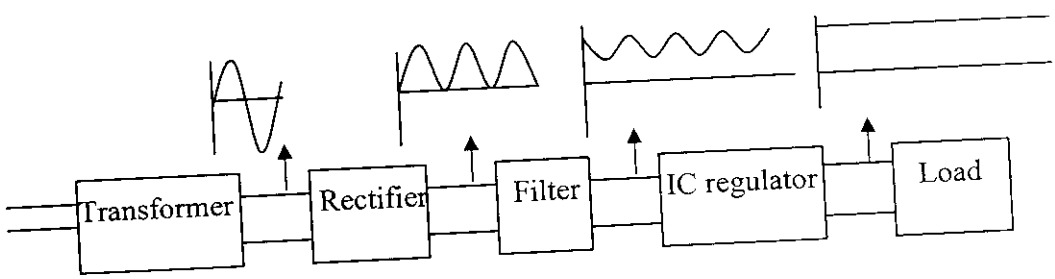


Speed is determined by comparing the timing of the measured pulses with what had been programmed during installation. The Speed Sentry keeps in memory a value that was learned during installation. It uses this "normal speed" to determine if the present speed has deviated from normal to the point of operating one of the alarm relays.

3.2.2.1 Introduction

Starting with an ac voltage, a steady dc voltage is obtained by rectifying the ac voltage, then filtering to a dc level, and finally, regulating to obtain a desired fixed dc voltage. The regulation is usually obtained from an IC voltage regulator unit, which takes a dc voltage and provides a somewhat lower dc voltage, which remains the same even if the input dc voltage varies, or the output load connected to the dc voltage changes.

A block diagram containing the parts of a typical power supply and the voltage at various points in the unit is shown in fig xxx. The ac voltage, typically 120 V rms, is connected to a transformer, which steps that ac voltage down to the level for the desired dc output. A diode rectifier then provides a full-wave rectified voltage that is initially filtered by a simple capacitor filter to produce a dc voltage. This resulting dc voltage usually has some ripple or ac voltage variation. A regulator circuit can use this dc input to provide a dc voltage that not only has much less ripple voltage but also remains the same dc value even if the input dc voltage varies somewhat, or the load connected to the output dc voltage changes. This voltage regulation is usually obtained using one of a number of popular voltage regulator IC units.

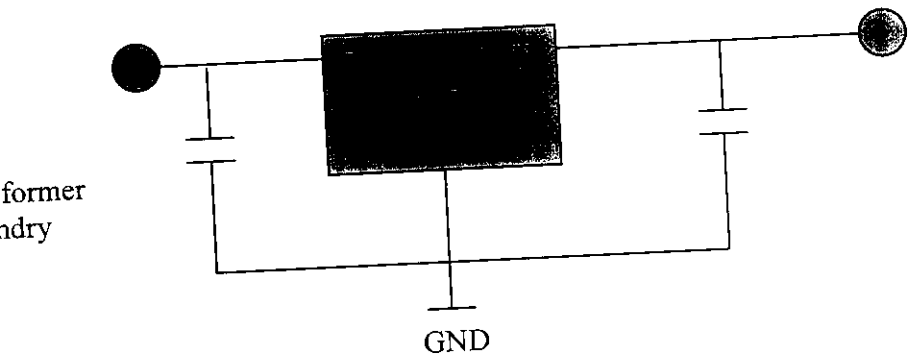


3.2.2.2 IC Voltage Regulators

Voltage regulators comprise a class of widely used ICs. Regulator IC units contain the circuitry for reference source, comparator amplifier, control device, and overload protection all in a single IC. Although the internal construction of the IC is somewhat different from that described for discrete voltage regulator circuits, the external operation is much the same. IC units provide regulation of either a fixed positive voltage, a fixed negative voltage, or an adjustably set voltage.

A power supply can be built using a transformer connected to the ac supply line to step the ac voltage to a desired amplitude, then rectifying that ac voltage, filtering with a capacitor and RC filter, if desired, and finally regulating the dc voltage using an IC regulator. The regulators can be selected for operation with load currents from hundreds of milli amperes to tens of amperes, corresponding to power ratings from milliwatts to tens of watts.

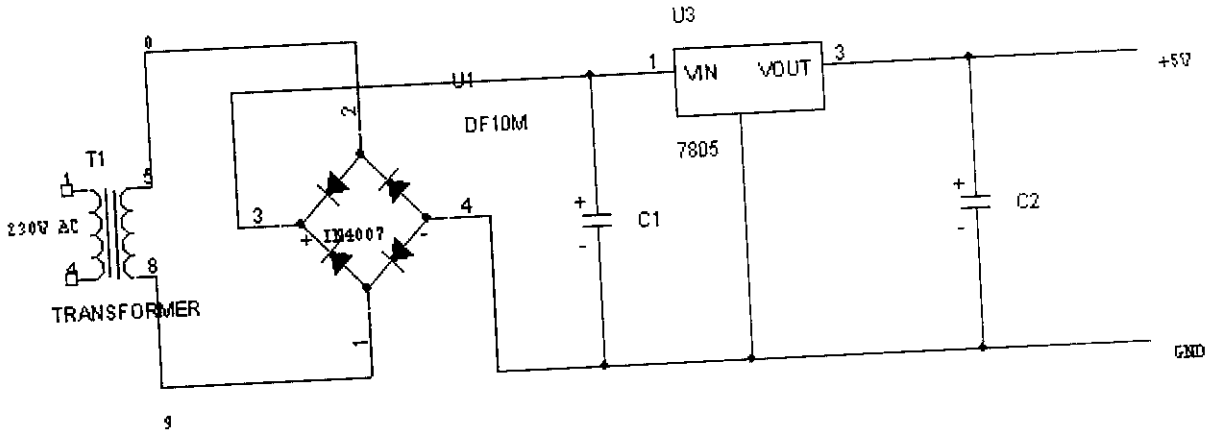
3.2.2.3 Fixed Positive Voltage Regulators:



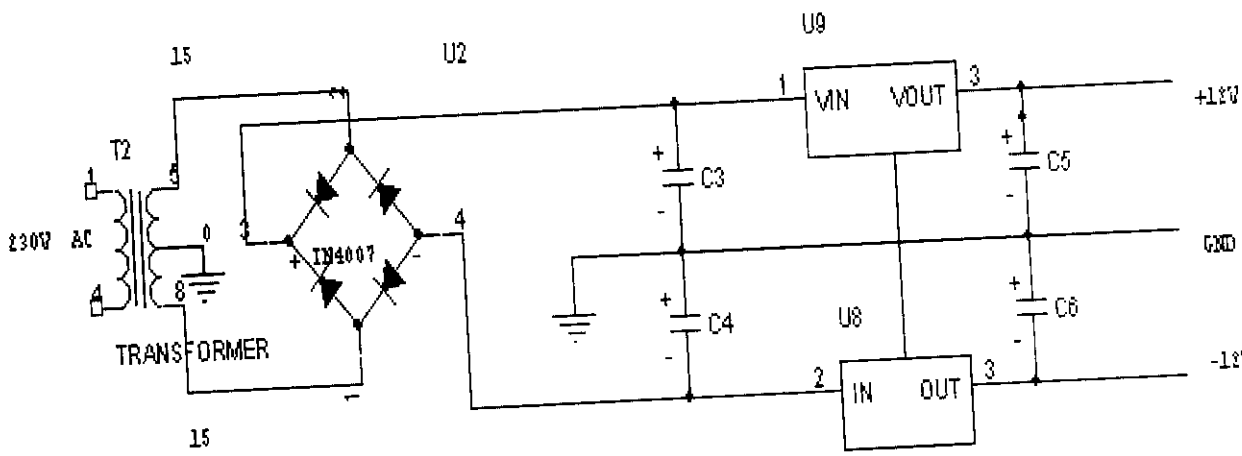
The series 78 regulators provide fixed regulated voltages from 5 to 24 V. Figure 19.26 shows how one such IC, a 7812, is connected to provide voltage regulation with output from this unit of +12V dc. An unregulated input voltage Vi is filtered by capacitor C1 and connected to the IC's IN terminal. The IC's OUT terminal provides a regulated + 12V which is filtered by capacitor C2 (mostly for any high-frequency noise). The third IC terminal is connected to ground (GND). While the input voltage may vary over some permissible voltage range, and the output load may vary over some acceptable range, the output voltage remains constant within specified voltage variation limits. These limitations are spelled out in the manufacturer's specification sheets.

3.2.2.4 Circuit Diagram:

+5 Volts Supply



+12V, -12V Supply



3.2.3 DAC Module

3.2.3.1 Introduction

The purpose of DAC is to convert a binary word to a proportional current or voltage. The characteristics of DAC are

i) Resolution:

The smallest analog increment corresponding to a 1 LSB converter change. It is determined by the number of bits in the input binary word. A converter with 8 binary inputs has 256 output levels, so its resolution is 1 part in 256. The resolution of an 8 bit converter is 0.39 percent.

ii) Monotonicity:

A monotonic function has a slope whose sign does not change. A monotonic DAC has an output that changes in the same direction for each increase in the input code. The converse is true for decreasing codes.

iii) *Offset error:*

The output voltage that exists when the input digital code is set to give an ideal output of zero volts. All the digital codes in the transfer curve are offset by the same value. Offset error is usually expressed in LSB's.

iv) settling time:

The time from a change in input code until a DAC's output signal remains within +/- ½ LSB of the final value.

v) Linearity:

It is a measure of how much the output ramp deviates from a straight line.

3.2.3.2 DAC CHIP 0800:

The DAC 0800 series are monolithic 8 bit high speed current output digital to analog converter (DAC) featuring typical setting time of 100ns. When used as a multiplying DAC, monotonic performance over a 40 to 1 reference current range is possible. The DAC 0800 series also features high compliance complementary current outputs to allow differential output voltages of 20V peak to peak with simple resistor loads. The reference to full scale current matching of better ±1LSB eliminates the need for full scale trims in most applications while the nonlinearities of better than ±0.1% over temperature minimizes system error accumulations.

The noise immune inputs of the DAC0800 series will accept TTL levels with the logic threshold pin, V_{lc} grounded. Simple adjustments of the V_{lc} potential will allow direct interface to all logic families. The performance and characteristics of the device are essentially unchanged over the full ±4.5V to ±18V power supply range; power dissipation is only 33mW with ±5V supplies and is independent of the logic input states.

Features:

- Fast setting output current 100ns
- Full scale error ±1 LSB
- Nonlinearity over temperature ±0.1%
- Full scale current drift ±10ppm/°C
- High output compliance ±10V to +18V
- Complementary current outputs
- Interface directly with TL, CMOS, PMOS, and others
- 2 quadrant wide range multiplying capability
- Wide power supply range ±4.5V to ±18V
- Low power consumption 33mW to ±5V

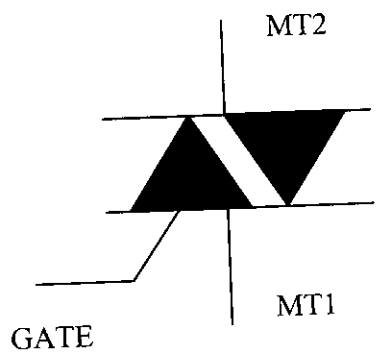
3.2.4 TRIAC Firing Module

3.2.4.1 INTRODUCTION:

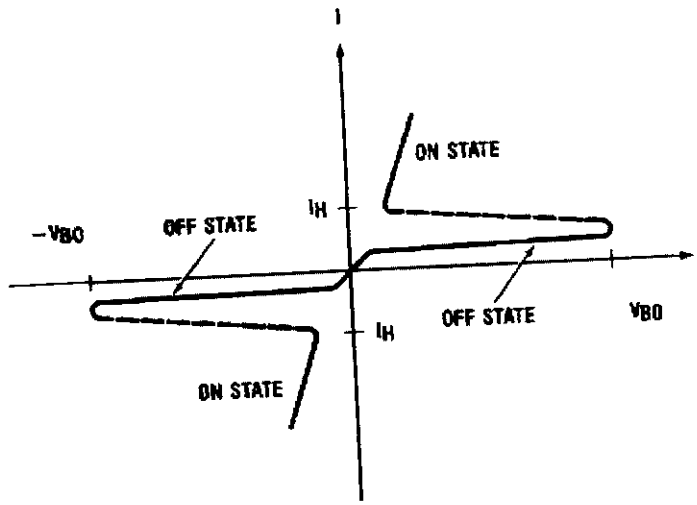
In the phase-angle application, the phase-angle control technique is used to adjust the voltage applied to the motor. A phase shift of the gate's pulses allows the effective voltage, seen by the motor, to be varied. The phase-angle drive requires just a triac.

3.2.4.2 BASIC TRIAC OPERATION:

A triac is basically a bidirectional switch which can be used to control AC power. In the high-impedance state, the triac blocks the principal voltage across the main terminals. By pulsing the gate or applying a steady state gate signal, the triac may be triggered into a low impedance state where conduction across the main terminals will occur. The gate signal polarity need not follow the main terminal polarity; however, this does affect the gate current requirements.

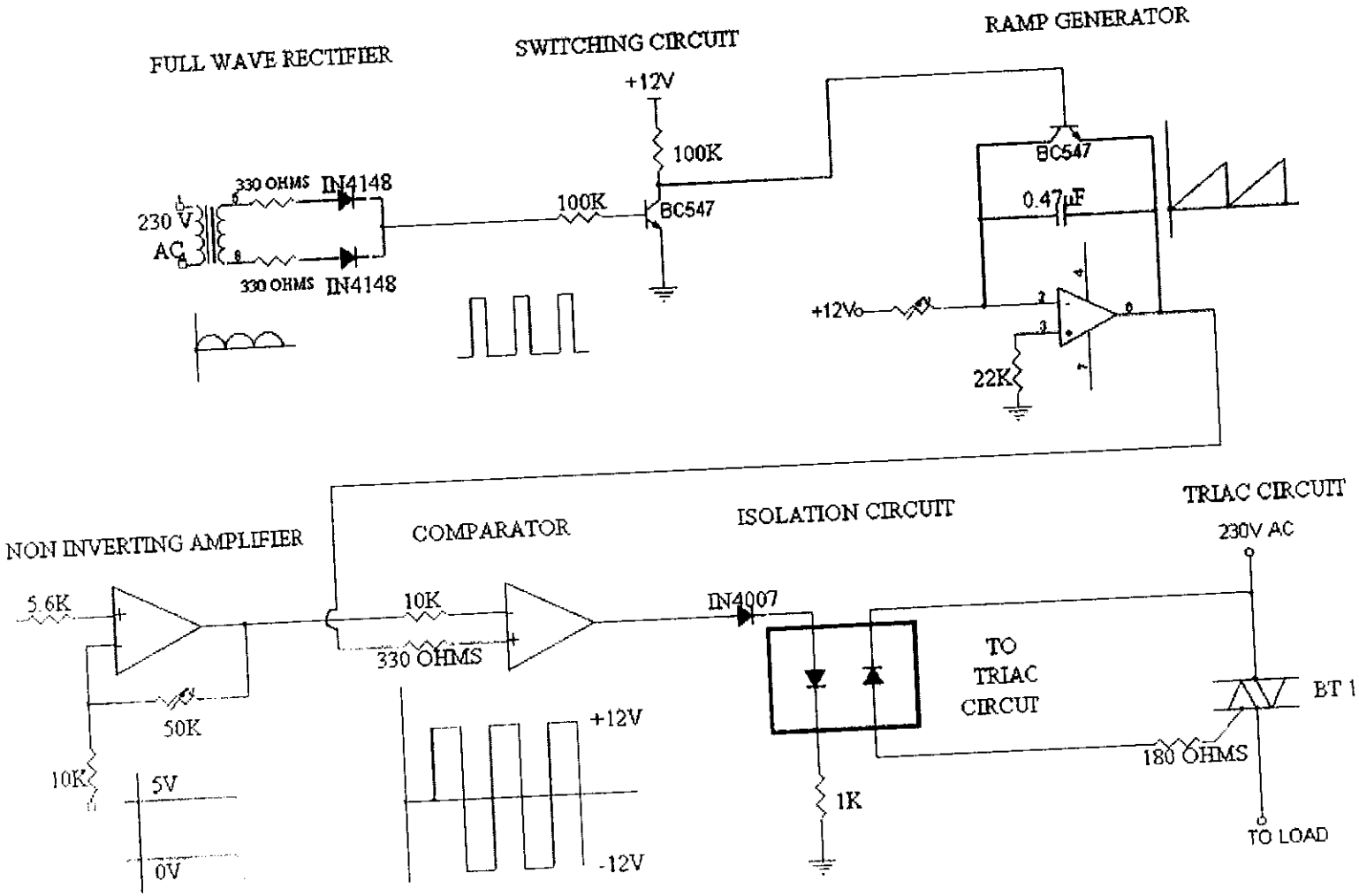


The break over voltage (VBO) is specified with the gate current (IGT) equal to zero. By increasing the gate current supplied to the triac, VBO can be reduced to cause the triac to go into the conduction or on state. Once the triac has entered the on state the gate signal need not be present to sustain conduction. The triac will turn itself off when the main terminal current falls below the minimum holding current required to sustain conduction (IH).



Voltage-Current Characteristics

After conduction occurs the main terminal current is independent of the gate current; however, due to the structure of the triac the gate trigger current is dependent on the direction of the main terminal current.


FULL WAVE RECTIFIER
SWITCHING CIRCUIT
RAMP GENERATOR
+12V
100K
330 OHMS
IN4148
230 V AC
330 OHMS
IN4148
100K
BC547
BC547
0.47µF
+12Vo
22K
NON INVERTING AMPLIFIER
COMPARATOR
ISOLATION CIRCUIT
TRIAC CIRCUIT
230V AC
5.6K
10K
330 OHMS
IN4007
50K
10K
5V
0V
+12V
-12V
TO
TRIAC
CIRCUT
1K
BT 1
180 OHMS
TO LOAD

3.2.4.3 OPERATION:

The rectified output is fed to the switching circuit, where the later output is employed for the ramp wave generation. The OP-AMP (IC 741) is operated in the integration mode for ramp wave output. The output voltage from the DSP is fed to the inverting amplifier before being fed to the comparator circuit. In the comparator operation the ramp wave is compared with the amplifier output ,resulting in the generation of the square wave. This output after being optically isolated is fed to the gate of the TRIAC for triggering.

Gate triggering signals should exceed the minimum rated trigger requirements as specified by the manufacturer. This is essential to guarantee rapid turn-on time and consistent operation from device to device. Triac turn-on time is primarily dependent on the magnitude of the applied gate signal. To obtain decreased turn-on times a sufficiently large gate signal should be applied.

Faster turn-on time eliminates localized heat spots within the pellet structure and increases triac dependability. Digital logic circuit, without large buffers, does not have the drive capabilities to efficiently turn on a triac. To insure proper operation in all firing situations, external trigger circuitry is used. Also, to prevent noise from disturbing the logic levels, AC/DC isolation or coupling techniques are utilized. Sensitive gate triacs which require minimal gate input signal and provide a limited amount of main terminal current may be driven directly.

3.2.4.4 ZERO VOLTAGE DETECTION:

In many applications it is advantageous to switch power at the AC line zero voltage crossing. In doing this, the device being controlled is not subjected to inherent AC transients. By utilizing this technique, greater dependability can be obtained from the switching device and the device being switched. It is also sometimes desirable to reference an event on a cyclic basis corresponding to the AC line frequency.

Depending on the load characteristics, switching times need to be chosen carefully to insure optimal performance. Triac controlled AC switching referenced to the AC 50 Hz line frequency enables precise control over the conduction angle at which the triac is fired. This enables the DSP to control the power output by increasing or decreasing the conduction angle in each half cycle. A wide variety of zero voltage detection circuits are available in various levels of sophistication.

TESTING AND RESULTS

3.3 TESTING:

In the following table the running speed of the motor for various inputs is given. The speed is tested over the entire range from 1500 rpm to 7500 rpm.

SET SPEED	RUNNING SPEED
1500	1420
2000	2130
2500	2400
3500	3600
4500	4612
7500	7490

RESULTS:

From the results we can see that the motor runs at the set speed with minimum deviation. Also the control is uniform from low speeds of 1500 rpm to the rated speed of 8000 rpm.

CONCLUSION

The new class of TMS320C25 DSP controller is becoming a viable option for cost sensitive applications. This controller has enough bandwidth and integrated on-chip power electronics peripherals to implement multiple function in a motor drive. Integrating multiple functions has reduced part count of the system .

This project titled " **DSP BASED CONTROL OF UNIVERSAL MOTOR**" produced the required speed according to the set speed and thus gave the expected results according to our design calculation.

Future enhancement can be made by the implementation of features such as motor speed or torque control, sensor monitoring, display control or soft start as well as protection.

A sensor-less speed control system in which the running speed of the motor can be calculated by sensing the load current results in elimination of maintenance-prone mechanical coupling elements.

The unused memory and some performance capacity are still available for other purposes.With the DSP controller an intelligent control approach is possible to reduce the overall system costs and to improve the reliability of the drive system.

BIBLIOGRAPHY

1) Mohammed,D. Figol, and Z.Yu, " **New generation DSP controllers provide cost effective motion control solutions,"** *PCIM*, vol. 24, no. 2, pp. 26-38,1998.
2) "**TMS320C1x/C2x/C2xx/C5x ASSEMBLY LANGUAGE TOOLS USER'S GUIDE**", Texas Instruments.,
3) '**Digital Signal Processing Solutions for Motor Control**' by Stefan Beierke,Texas Instruments.
4) **Digital Control Applications with the TMS320 Family**, Irfan Admed, 1991.
5) DSP, A Computer Based Approch, Sanjith.K.Mithra
6) Digital Signal Processor, R.V.Venkatraman
7) Fundamentals of Electrical Drives, Gopal K. Dubey
8) Electrical Machines, R . K. Rajput

APPENDIX I

January 1999

FAIRCHILD
SEMICONDUCTOR™

NMC27C64
65,536-Bit (8192 x 8) CMOS EPROM

General Description

The NMC27C64 is a 64K UV erasable, electrically reprogrammable and one-time programmable (OTP) CMOS EPROM ideally suited for applications where fast turnaround, pattern experimentation and low power consumption are important requirements.

The NMC27C64 is designed to operate with a single +5V power supply with ±10% tolerance. The CMOS design allows the part to operate over extended and military temperature ranges.

The NMC27C64Q is packaged in a 28-pin dual-in-line package with a quartz window. The quartz window allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written electrically into the device by following the programming procedure.

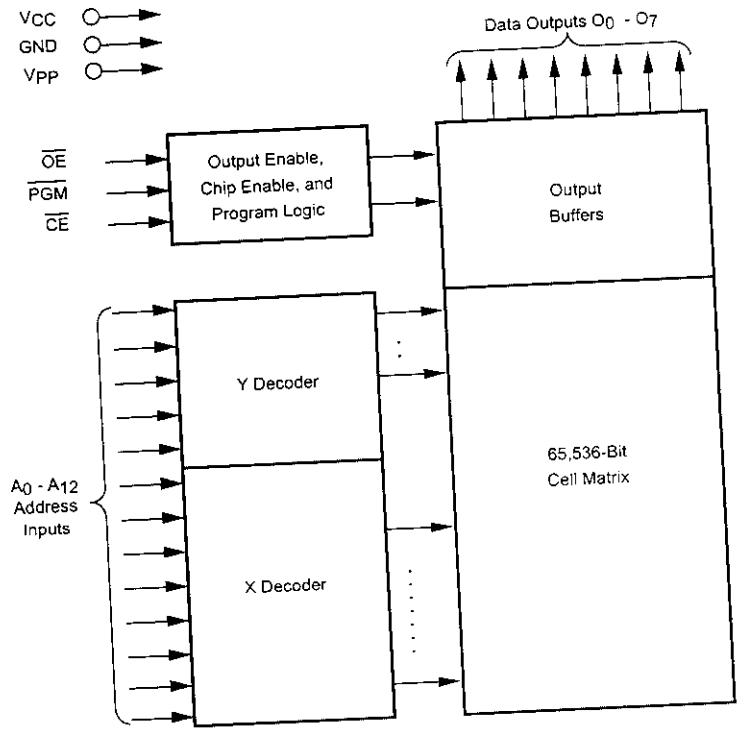
The NMC27C64N is packaged in a 28-pin dual-in-line plastic molded package without a transparent lid. This part is ideally suited for high volume production applications where cost is an important factor and programming only needs to be done once.

This family of EPROMs are fabricated with Fairchild's proprietary, time proven CMOS double-poly silicon gate technology which combines high performance and high density with low power consumption and excellent reliability.

Features

- High performance CMOS
  - —150 ns access time
- JEDEC standard pin configuration
  - —28-pin Plastic DIP package
  - —28-pin CERDIP package
- Drop-in replacement for 27C64 or 2764
- Manufacturers identification code

Block Diagram

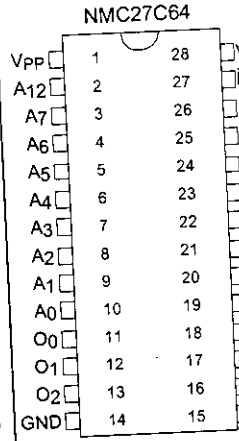


DS008634-1

Connection Diagram

27C512 27512	27C256 27256	27C128 27128	27C32 2732	27C16 2716
A15	VPP	VPP		
A12	A12	A12		
A7	A7	A7	A7	A7
A6	A6	A6	A6	A6
A5	A5	A5	A5	A5
A4	A4	A4	A4	A4
A3	A3	A3	A3	A3
A2	A2	A2	A2	A2
A1	A1	A1	A1	A1
A0	A0	A0	A0	A0
O0	O0	O0	O0	O0
O1	O1	O1	O1	O1
O2	O2	O2	O2	O2
GND	GND	GND	GND	GND

NMC27C64



27C16 2716	27C32 2732	27C128 27128	27C256 27256	27C512 27512
		VCC	VCC	VCC
		PGM	A14	A14
VCC	VCC	A13	A13	A13
A8	A8	A8	A8	A8
A9	A9	A9	A9	A9
VPP	A11	A11	A11	A11
OE	OE/VPP	OE	OE	OE/VPP
A10	A10	A10	A10	A10
CE/PGM	CE	CE	CE/PGM	CE
O7	O7	O7	O7	O7
O6	O6	O6	O6	O6
O5	O5	O5	O5	O5
O4	O4	O4	O4	O4
O3	O3	O3	O3	O3

DS008634-2

Note: Socket compatible EPROM pin configurations are shown in the blocks adjacent to the NMC27C64 pins.

Pin Names

A0–A12	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0–O_7	Outputs
$\overline{PGM}$	Program
NC	No Connect
V_{PP}	Programming Voltage
V_{CC}	Power Supply
GND	Ground

Commercial Temperature Range V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C64Q, N 150	150
NMC27C64Q, N 200	200

Extended Temp Range (-40°C to +85°C) V_{CC} = 5V ±10%

Parameter/Order Number	Access Time (ns)
NMC27C64QE, NE200	200

Absolute Maximum Ratings (Note 1)

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages except A9 with Respect to Ground (Note 10)	+6.5V to -0.6V
All Output Voltages with Respect to Ground (Note 10) V_{CC}	+1.0V to GND -0.6V
V_{PP} Supply Voltage and A_9 with Respect to Ground During Programming	+14.0V to -0.6V
V_{CC} Supply Voltage with Respect to Ground	+7.0V to -0.6V
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 sec.)	300°C
ESD Rating (Mil Spec 883C, Method 3015.2)	2000V

Operating Conditions (Note 7)

Temperature Range	
NMC27C64Q 150, 200	0°C to +70°C
NMC27C64N 150, 200	
NMC27C64QE 200	-40°C to +85°C
NMC27C64NE 200	
V_{CC} Power Supply	+5V ±10%

READ OPERATION

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND			10	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$			10	µA
I_{CC1} (Note 9)	V_{CC} Current (Active) TTL Inputs	$\overline{CE} = V_{IL}$, f=5 MHz Inputs = V_{IH} or V_{IL}, I/O = 0 mA		5	20	mA
I_{CC2} (Note 9)	V_{CC} Current (Active) CMOS Inputs	$\overline{CE}$ = GND, f = 5 MHz Inputs = V_{CC} or GND, I/O = 0 mA		3	10	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE} = V_{IH}$		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$		0.5	100	µA
I_{PP}	VPP Load Current	$V_{PP} = V_{CC}$		10	µA	
V_{IL}	Input Low Voltage		-0.1		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} +1	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA			0.45	V
V_{OH1}	Output High Voltage	I_{OH} = -400 µA	2.4			V
V_{OL2}	Output Low Voltage	I_{OL} = 0 µA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = 0 µA	V_{CC} - 0.1			V

AC Electrical Characteristics

Symbol	Parameter	Conditions	NMC27C64				Units
			150		200, E200		
			Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$ $\overline{PGM} = V_{IH}$		150		200	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$, $\overline{PGM} = V_{IH}$		150		200	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$, $\overline{PGM} = V_{IH}$		60		60	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$, $\overline{PGM} = V_{IH}$	0	60	0	60	ns
t_{CF}	$\overline{CE}$ High to Output Float	$\overline{OE} = V_{IL}$, $\overline{PGM} = V_{IH}$	0	60	0	60	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$ $\overline{PGM} = V_{IH}$	0		0		ns

Capacitance TA = +25˚C, f = 1 MHz (Note 2) NMC27C64Q

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	6	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	9	12	pF

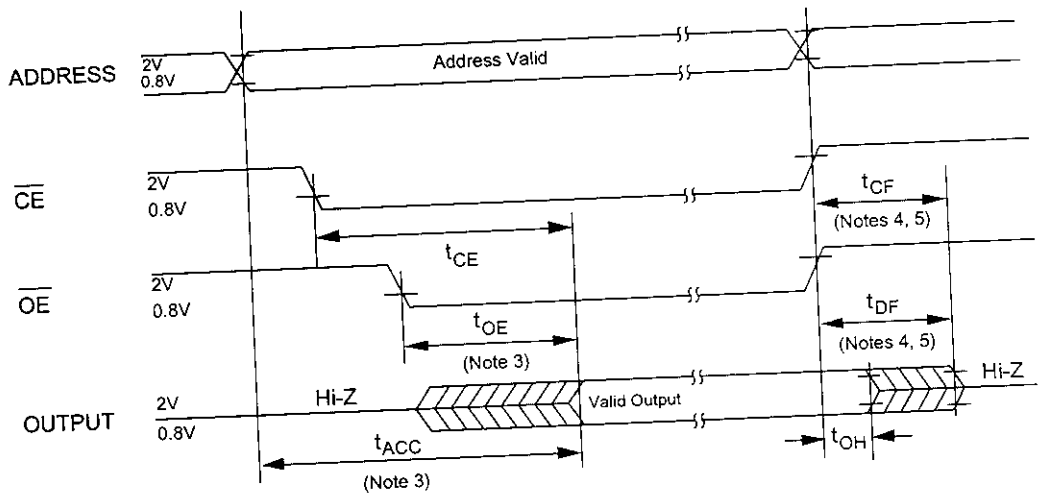
Capacitance TA = +25˚C, f = 1 MHz (Note 2) NMC27C64N

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	5	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	10	pF

AC Test Conditions

Output Load	1 TTL Gate and C_L = 100 pF (Note 8)
Input Rise and Fall Times	≤5 ns
Input Pulse Levels	0.45V to 2.4V
Timing Measurement Reference Level	
Inputs	0.8V and 2V
Outputs	0.8V and 2V

AC Waveforms (Note 6) (Note 9)



Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: This parameter is only sampled and is not 100% tested.

Note 3: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 4: The t_{DF} and t_{CF} compare level is determined as follows:
High to TRI-STATE ®, the measured V_{OH1} (DC) - 0.10V;
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V.

Note 5: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 6: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that at least a 0.1 µF ceramic capacitor be used on every device between V_{CC} and GND.

Note 7: The outputs must be restricted to V_{CC} + 1.0V to avoid latch-up and device damage.

Note 8: 1 TTL Gate: I_{OL} = 1.6 mA, I_{OH} = -400 µA.
C_L: 100 pF includes fixture capacitance.

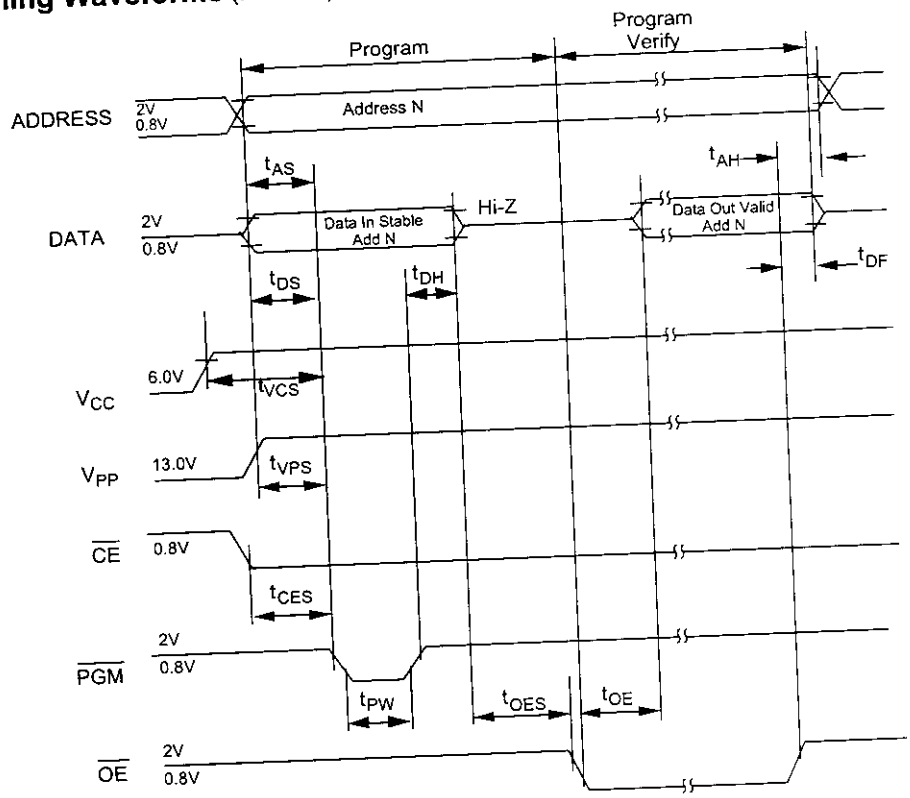
Note 9: V_{PP} may be connected to V_{CC} except during programming.

Note 10: Inputs and outputs can undershoot to -2.0V for 20 ns Max.

Programming Characteristics (Note 11) (Note 12) (Note 13) (Note 14)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Setup Time		2			µs
t_{OES}	$\overline{OE}$ Setup Time		2			µs
t_{CES}	$\overline{CE}$ Setup Time		2			µs
t_{DS}	Data Setup Time		2			µs
t_{VPS}	V_{PP} Setup Time		2			µs
t_{VCS}	V_{CC} Setup Time		0			µs
t_{AH}	Address Hold Time		2			µs
t_{DH}	Data Hold Time		0		130	ns
t_{DF}	Output Enable to Output Float Delay	$\overline{CE} = V_{IL}$	0.45	0.5	0.55	ms
t_{PW}	Program Pulse Width				150	ns
t_{OE}	Data Valid from $\overline{OE}$	$\overline{CE} = V_{IL}$			30	mA
I_{PP}	V_{PP} Supply Current During Programming Pulse	$\overline{CE} = V_{IL}$ $\overline{PGM} = V_{IL}$			10	mA
I_{CC}	V_{CC} Supply Current		20	25	30	°C
T_A	Temperature Ambient		5.75	6.0	6.25	V
V_{CC}	Power Supply Voltage		12.2	13.0	13.3	V
V_{PP}	Programming Supply Voltage		5			ns
t_{FR}	Input Rise, Fall Time			0.0	0.45	V
V_{IL}	Input Low Voltage		2.4	4.0		V
V_{IH}	Input High Voltage		0.8	1.5	2.0	V
t_{IN}	Input Timing Reference Voltage		0.8	1.5	2.0	V
t_{OUT}	Output Timing Reference Voltage					

Programming Waveforms (Note 13)



Note 11: Fairchild's standard product warranty applies to devices programmed to specifications described herein.

Note 12: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The EPROM must not be inserted into or removed from a board with voltage applied to V_{PP} or V_{CC}.

Note 13: The maximum absolute allowable voltage which may be applied to the V_{PP} pin during programming is 14V. Care must be taken when switching the V_{PP} supply to prevent any overshoot from exceeding this 14V maximum specification. At least a 0.1 µF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Note 14: Programming and program verify are tested with the interactive Program Algorithm, at typical power supply voltages and timings.

March 1998

FAIRCHILD SEMICONDUCTOR™

DM74LS244
Octal 3-STATE Buffers/Line Drivers/Line Receivers

General Description

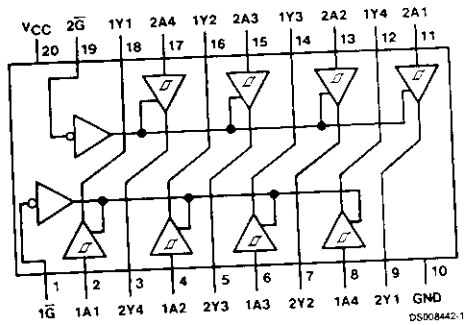
These buffers/line drivers are designed to improve both the performance and PC board density of 3-STATE buffers/drivers employed as memory-address drivers, clock drivers, and bus-oriented transmitters/receivers. Featuring 400 mV of hysteresis at each low current PNP data line input, they provide improved noise rejection and high fanout outputs and can be used to drive terminated lines down to 133Ω.

Features

- 3-STATE outputs drive bus lines directly
- PNP inputs reduce DC loading on bus lines
- Hysteresis at data inputs improves noise margins
- Typical I_{OL} (sink current)
  - 54LS 12 mA
  - 74LS 24 mA
- Typical I_{OH} (source current)
  - 54LS −12 mA
  - 74LS −15 mA
- Typical propagation delay times
  - Inverting 10.5 ns
  - Noninverting 12 ns
- Typical enable/disable time 18 ns
- Typical power dissipation (enabled)
  - Inverting 130 mW
  - Noninverting 135 mW

Connection Diagram

Dual-In-Line Package



Order Number 54LS244DMQB, 54LS244FMQB, 54LS244LMQB, DM74LS244WM or DM74LS244N
See Package Number E20A, J20A, M20B, N20A or W20A

Function Table

Inputs		Output
$\overline{G}$	A	Y
L	L	L
L	H	H
H	X	Z

L = Low Logic Level
H = High Logic Level
X = Either Low or High Logic Level
Z = High Impedance

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V	54LS	−55°C to +125°C
Input Voltage	7V	DM74LS	0°C to +70°C
Operating Free Air Temperature Range		Storage Temperature Range	−65°C to +150°C

Recommended Operating Conditions

Symbol	Parameter	54LS244			DM74LS244			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−12			−15	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions			Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA					−1.5	V
HYS	Hysteresis ($V_{T+} - V_{T-}$) Data Inputs Only	V_{CC} = Min			0.2	0.4		V
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OH} = −1 mA		DM74	2.7			V
		V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OH} = −3 mA		54LS/DM74	2.4	3.4		
		V_{CC} = Min, V_{IH} = Min, V_{IL} = 0.5V, I_{OH} = Max		54LS/DM74	2			
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IL} = Max, V_{IH} = Min	I_{OL} = 12 mA	54LS/DM74			0.4	V
			I_{OL} = Max	DM74			0.5	
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = Max, V_{IL} = Max, V_{IH} = Min	V_O = 2.7V				20	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied		V_O = 0.4V				−20	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max	V_I = 7V (DM74)				0.1	mA
			V_I = 10V (54LS)				20	μA
I_{IH}	High Level Input Current	V_{CC} = Max	V_I = 2.7V				−200	μA
I_{IL}	Low Level Input Current	V_{CC} = Max	V_I = 0.4V		−0.5		−225	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)		54LS	−50			
				DM74	−40			
I_{CC}	Supply Current	V_{CC} = Max, Outputs Open	Outputs High			13	23	mA
			Outputs Low			27	46	
			Outputs Disabled			32	54	

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

at V_{CC} = 5V, T_A = 25°C

Symbol	Parameter	Conditions	54LS Max	DM74LS Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 45 pF, R_L = 667Ω	18	18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	C_L = 45 pF, R_L = 667Ω	18	18	ns
t_{PZL}	Output Enable Time to Low Level	C_L = 45 pF, R_L = 667Ω	30	30	ns
t_{PZH}	Output Enable Time to High Level	C_L = 45 pF, R_L = 667Ω	23	23	ns
t_{PLZ}	Output Disable Time from Low Level	C_L = 5 pF, R_L = 667Ω	25	25	ns
t_{PHZ}	Output Disable Time from High Level	C_L = 5 pF, R_L = 667Ω	18	18	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 150 pF, R_L = 667Ω		21	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	C_L = 150 pF, R_L = 667Ω		22	ns
t_{PZL}	Output Enable Time to Low Level	C_L = 150 pF, R_L = 667Ω		33	ns
t_{PZH}	Output Enable Time to High Level	C_L = 150 pF, R_L = 667Ω		26	ns

Note 4: 54LS Output Load is C_L = 50 pF for t_{PLH}, t_{PHL}, t_{PZL} and t_{PZH}.

FAIRCHILD SEMICONDUCTOR™

September 1983
Revised February 1999

MM74HC273
Octal D-Type Flip-Flops with Clear

General Description

The MM74HC273 edge triggered flip-flops utilize advanced silicon-gate CMOS technology to implement D-type flip-flops. They possess high noise immunity, low power, and speeds comparable to low power Schottky TTL circuits. This device contains 8 master-slave flip-flops with a common clock and common clear. Data on the D input having the specified setup and hold times is transferred to the Q output on the LOW-to-HIGH transition of the CLOCK input. The CLEAR input when LOW, sets all outputs to a low state.

Each output can drive 10 low power Schottky TTL equivalent loads. The MM74HC273 is functionally as well as pin compatible to the 74LS273. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 18 ns
- Wide operating voltage range
- Low input current: 1 µA maximum
- Low quiescent current: 80 µA (74 Series)
- Output drive: 10 LS-TTL loads

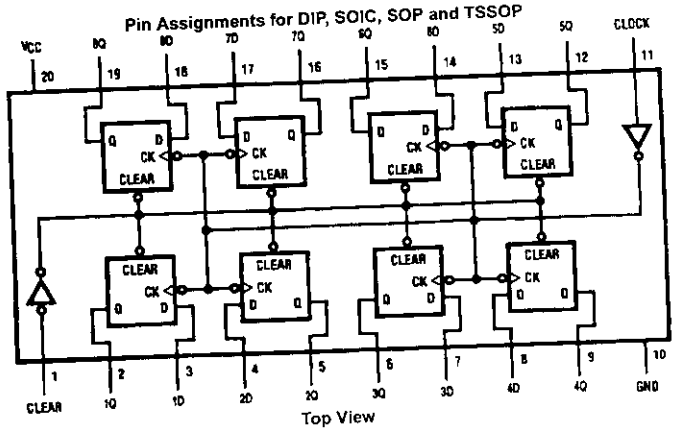
Ordering Code:

Order Number	Package Number	Package Description
MM74HC273M	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-153, 0.300" Wide
MM74HC273SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC273MTC	MTC20	20-Lead thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC273N	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram

Pin Assignments for DIP, SOIC, SOP and TSSOP



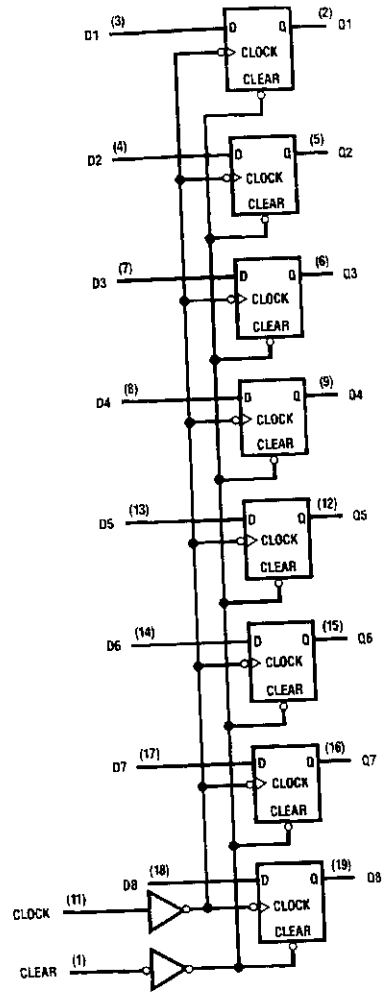
Truth Table

(Each Flip-Flop)

Inputs			Outputs
Clear	Clock	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

H = HIGH Level (Steady State)
L = LOW Level (Steady State)
X = Don't Care
↑ = Transition from LOW-to-HIGH level
Q_0 = The level of Q before the indicated steady state input conditions were established

Logic Diagram



Absolute Maximum Ratings (Note 1)

(Note 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering 10 seconds)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC input or Output Voltage			
(V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)	−40	+85	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C.

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	T_A = −40 to 85°C	T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum HIGH Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum LOW Level Input Voltage		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum HIGH Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 20$ μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \le 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum LOW Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 20$ μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 4$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8	80	160	μA

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

V_{CC} = 5V, T_A = 25°C, C_L = 15 pF, $t_r = t_f$ = 6 ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Output		18	27	ns
t_{PHL}	Maximum Propagation Delay, Clear to Output		18	27	ns
t_{REM}	Minimum Removal Time, Clear to Clock		10	20	ns
t_s	Minimum Setup Time Data to Clock		10	20	ns
t_H	Minimum Hold Time Clock to Data		-2	0	ns
t_W	Minimum Pulse Width Clock or Clear		10	16	ns

AC Electrical Characteristics

C_L = 50 pF, $t_r = t_f$ = 6 ns (unless otherwise specified)

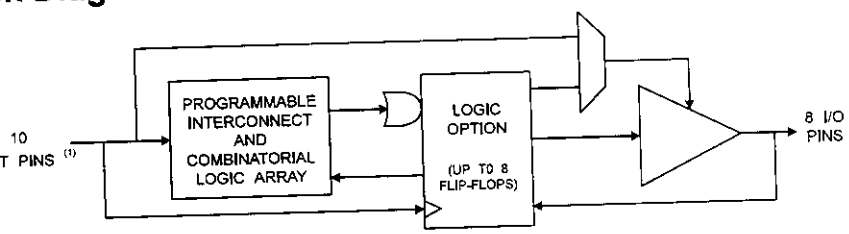
Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	T_A = −40 to 85°C	T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency		2.0V	16	5	4	3	MHz
			4.5V	74	27	21	18	MHz
			6.0V	78	31	24	20	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Output		2.0V	38	135	170	205	ns
			4.5V	14	27	34	41	ns
			6.0V	12	23	29	35	ns
t_{PHL}	Maximum Propagation Delay, Clear to Output		2.0V	42	135	170	205	ns
			4.5V	19	27	34	41	ns
			6.0V	18	23	29	35	ns
t_{REM}	Minimum Removal Time Clear to Clock		2.0V	0	25	32	37	ns
			4.5V	0	5	6	7	ns
			6.0V	0	4	5	6	ns
t_s	Minimum Setup Time Data to Clock		2.0V	26	100	125	150	ns
			4.5V	7	20	25	30	ns
			6.0V	5	17	21	25	ns
t_H	Minimum Hold Time Clock to Data		2.0V	−15	0	0	0	ns
			4.5V	−6	0	0	0	ns
			6.0V	−4	0	0	0	ns
t_W	Minimum Pulse Width Clock or Clear		2.0V	34	80	100	120	ns
			4.5V	11	16	20	24	ns
			6.0V	10	14	18	20	ns
t_r, t_f	Maximum Input Rise and Fall Time, Clock		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V	28	75	95	110	ns
			4.5V	11	15	19	22	ns
			6.0V	9	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per flip-flop)		45				pF
C_{IN}	Maximum Input Capacitance			7	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

res

- ry-standard Architecture
- nulates Many 20-pin PALs®
- ow-cost Easy-to-use Software Tools
- speed Electrically-erasable Programmable Logic Devices
- ns Maximum Pin-to-pin Delay
- ower - 100 µA Pin-controlled Power-down Mode Option
- and TTL Compatible Inputs and Outputs
- O Pin Keeper Circuits
- nced Flash Technology
- eprogrammable
- 00% Tested
- reliability CMOS Process
- 0 Year Data Retention
- 00 Erase/Write Cycles
- ,000V ESD Protection
- 00 mA Latchup Immunity
- mercial and Industrial Temperature Ranges
- -in-line and Surface Mount Packages in Standard Pinouts
- Compliant

k Diagram



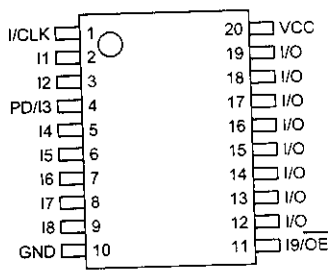
1. Includes optional PD control pin.

Configurations

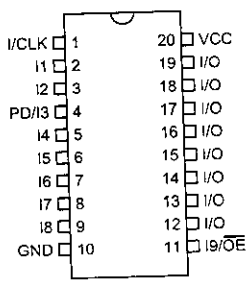
nouts Top View

Name	Function
	Clock
	Logic Inputs
	Bidirectional Buffers
	Output Enable
C	+5V Supply
	Power-down

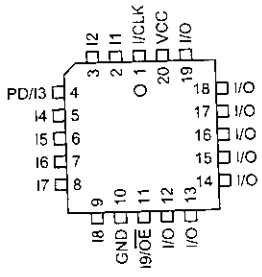
TSSOP



DIP/SOIC



PLCC



High-performance EE PLD

ATF16V8C

Rev. 0425G–08/99

ription

F16V8C is a high-performance EECMOS Program-
Logic Device that utilizes Atmel's proven electrically-
e Flash memory technology. Speeds down to 5 ns
00 µA pin-controlled power-down mode option are
. All speed ranges are specified over the full 5V ±
nge for industrial temperature ranges; 5V ± 5% for
rcial range 5-volt devices.

TF16V8C incorporates a superset of the generic
ctures, which allows direct replacement of the 16R8
and most 20-pin combinatorial PLDs. Eight outputs
ch allocated eight product terms. Three different modes of operation, configured automatically with software, allow highly complex logic functions to be realized.

The ATF16V8C can significantly reduce total system power, thereby enhancing system reliability and reducing power supply costs. When pin 4 is configured as the power-down control pin, supply current drops to less than 100 µA whenever the pin is high. If the power-down feature isn't required for a particular application, pin 4 may be used as a logic input. Also, the pin keeper circuits eliminate the need for internal pull-up resistors along with their attendant power consumption.

olute Maximum Ratings*

erature Under Bias	-40°C to +85°C
ge Temperature	-65°C to +150°C
e on Any Pin with Respect to Ground	-2.0V to +7.0V[1]
ge on Input Pins Respect to Ground g Programming	-2.0V to +14.0V[1]
amming Voltage with ect to Ground	-2.0V to +14.0V[1]

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V DC, which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} + 0.75V DC, which may overshoot to 7.0V for pulses of less than 20 ns.

and AC Operating Conditions

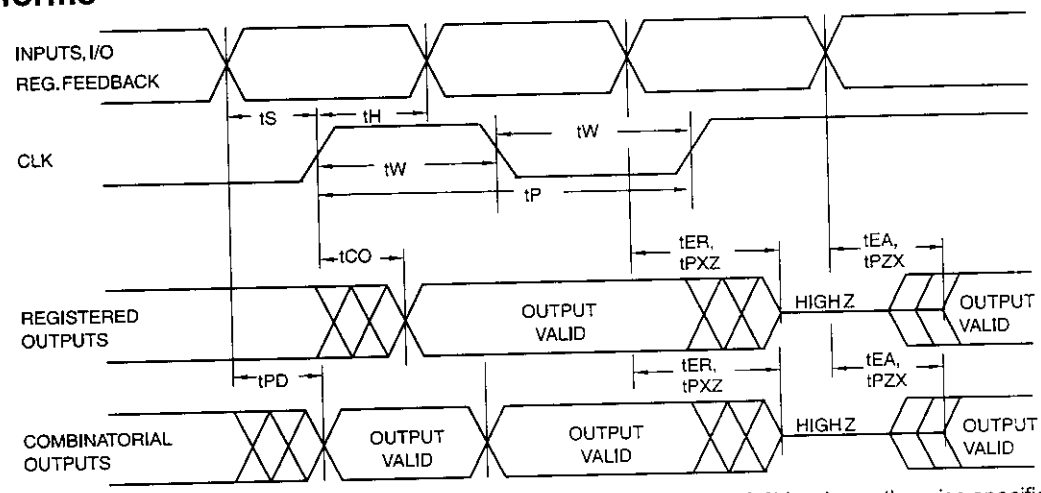
	Commercial	Industrial
ating Temperature (Ambient)	0°C - 70°C	-40°C - 85°C
Power Supply	5V ± 5%	5V ± 10%

haracteristics

	Parameter	Condition		Min	Typ	Max	Units
	Input or I/O Low Leakage Current	$0 \le V_{IN} \le V_{IL}$ (Max)				-10.0	µA
	Input or I/O High Leakage Current	$3.5 \le V_{IN} \le V_{CC}$				10.0	µA
	Power Supply Current, Standby	15 MHz, V_{CC} = Max, V_{IN} = 0, V_{CC}, Outputs Open	Com.			115	mA
			Ind.			130	mA
	Power Supply Current, Power-down Mode	V_{CC} = Max, V_{IN} = 0, V_{CC}	Com.		10	100	µA
			Ind.		10	105	µA
	Output Short Circuit Current	V_{OUT} = 0.5V; V_{CC} = 5V; T_A = 25°C				-150	mA
	Input Low Voltage	Min < V_{CC} < Max		-0.5		0.8	V
	Input High Voltage			2.0		V_{CC} + 1	V
	Output Low Voltage	V_{CC} = Min; All Outputs I_{OL} = 24 mA	Com., Ind.			0.5	V
	Output High Voltage	V_{CC} = Min I_{OL} = -4.0 mA		2.4			V
	Output Low Current	V_{CC} = Min	Com.	24.0			mA
			Ind.	12.0			mA
	Output High Current	V_{CC} = Min	Com., Ind.	-4.0			mA

1. All I_{CC} parameters measured with outputs open.

Waveforms



1. Timing measurement reference is 1.5V. Input AC driving levels are 0.0V and 3.0V, unless otherwise specified.

haracteristics

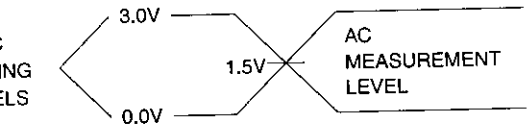
ol	Parameter	-5		-7		Units
		Min	Max	Min	Max	
	Input or Feedback to Non-Registered Output	1	5	3	7.5	ns
	Clock to Feedback		3		3	ns
	Clock to Output	1	4	2	5	ns
	Input or Feedback Setup Time	3		5		ns
	Input Hold Time	0		0		ns
	Clock Period	6		8		ns
	Clock Width	3		4		ns
	External Feedback $1/(t_S + t_{CO})$		142		100	MHz
	Internal Feedback $1/(t_S + t_{CF})$		166		125	MHz
	No Feedback $1/(t_P)$		166		125	MHz
	Input to Output Enable – Product Term	2	6	3	9	ns
	Input to Output Disable – Product Term	2	5	2	9	ns
	$\overline{OE}$ pin to Output Enable	2	5	2	6	ns
	$\overline{OE}$ pin to Output Disable	1.5	5	1.5	6	ns

ver-down AC Characteristics(1)(2)(3)

bol	Parameter	-5		-7		Units
		Min	Max	Min	Max	
	Valid Input Before PD High	5.0		7.5		ns
H	Valid $\overline{OE}$ Before PD High	0		0		ns
H	Valid Clock Before PD High	0		0		ns
X	Input Don't Care After PD High		5.0		7.5	ns
X	$\overline{OE}$ Don't Care After PD High		5.0		7.5	ns
X	Clock Don't Care After PD High		5.0		7.5	ns
V	PD Low to Valid Input		5.0		7.5	ns
V	PD Low to Valid $\overline{OE}$		15.0		20.0	ns
V	PD Low to Valid Clock		15.0		20.0	ns
V	PD Low to Valid Output		20.0		25.0	ns

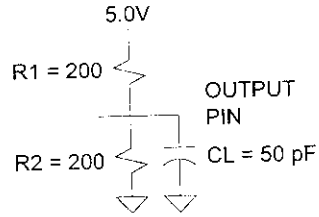
s: 1. Output data is latched and held.
2. HI-Z outputs remain HI-Z.
3. Clock and input transitions are ignored.

Test Waveforms and urement Levels:



1.5 ns (10% to 90%)

Output Test Loads:



Capacitance[1]

Hz, T = 25°C

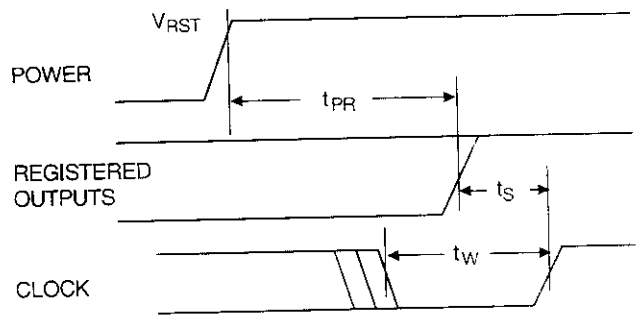
	Typ	Max	Units	Conditions
	5	8	pF	V_{IN} = 0V
	6	8	pF	V_{OUT} = 0V

1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

er-up Reset

TF16V8C's registers are designed to reset during -up. At a point delayed slightly from V_{CC} crossing all registers will be reset to the low state. As a result, gistered output state will always be high on power-up. eature is critical for state machine initialization. ver, due to the asynchronous nature of reset and the tainty of how V_{CC} actually rises in the system, the ng conditions are required:

- he V_{CC} rise must be monotonic, from below 0.7V,
- ter reset occurs, all input and feedback setup nes must be met before driving the clock term gh, and
- he signals from which the clock is derived must emain stable during t_{PR}.



Parameter	Description	Typ	Max	Units
t_{PR}	Power-up Reset Time	600	1,000	ns
V_{RST}	Power-up Reset Voltage	3.8	4.5	V

r-down Mode

F16V8C includes an optional pin controlled power-eature. Device pin 4 may be configured as the down pin. When this feature is enabled and the lown pin is high, total current consumption drops to n 100 µA. In the power-down mode, all output data rnal logic states are latched and held. All registered mbinatorial output data remains valid. Any outputs vere in a HI-Z state at the onset of power-down will at HI-Z. During power-down, all input signals except wer-down pin are blocked. The input and I/O pin circuits remain active to insure that pins do not float erminate levels. This helps to further reduce system

.on of the power-down option is specified in the V8C logic design file. The logic compiler will include otion selection in the otherwise standard 16V8 fuse file. When the power-down feature is not spec- the design file, pin 4 is available as a logic input, and s no power-down pin. This allows the ATF16V8C to grammed using any existing standard 16V8 fuse file.

Some programmers list the JEDEC-compatible 16V8C (No PD used) separately from the non-JEDEC compatible 16V8CEXT. (EXT for extended features.)

stered Output Preload

TF16V8C's registers are provided with circuitry to oading of each register with either a high or a low. eature will simplify testing since any state can be l into the registers to control test sequencing. A C file with preload is generated when a source file ectors is compiled. Once downloaded, the JEDEC file d sequence will be done automatically by approved mmers.

urity Fuse Usage

gle fuse is provided to prevent unauthorized copying ATF16V8C fuse patterns. Once programmed, fuse and preload are inhibited. However, the 64-bit User ture remains accessible.

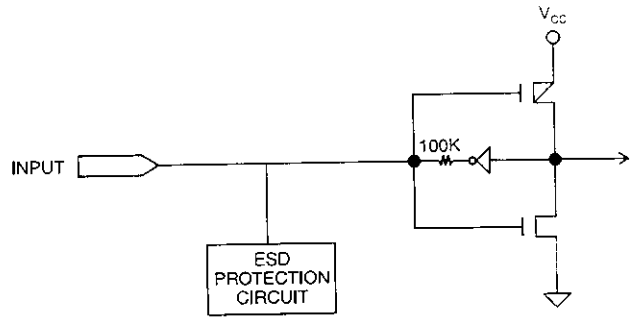
ecurity fuse will be programmed last, as its effect is diate.

ut and I/O Pin Keeper Circuits

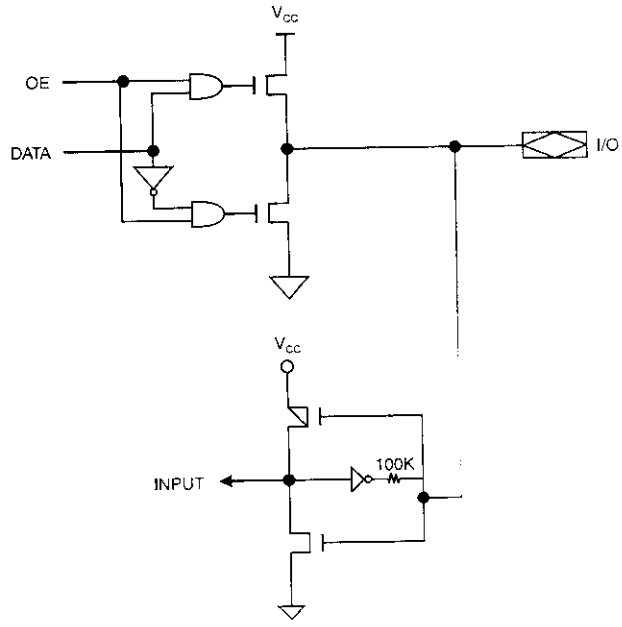
ATF16V8C contains internal input and I/O pin keeper s. These circuits allow each ATF16V8C pin to hold its ous value even when it is not being driven by an external source or by the device's output buffer. This helps insure that all logic array inputs are at known, valid logic levels. This reduces system power by preventing pins from floating to indeterminate levels. By using pin keeper circuits rather than pull-up resistors, there is no DC current required to hold the pins in either logic state (high or low).

These pin keeper circuits are implemented as weak feedback inverters, as shown in the Input Diagram below. These keeper circuits can easily be overdriven by standard TTL- or CMOS-compatible drivers. The typical overdrive current required is 40 µA.

Input Diagram



I/O Diagram



;ional Logic Diagram Description

gic Option and Functional Diagrams describe the '8C architecture. Eight configurable macrocells can igured as a registered output, combinatorial I/O, atorial output, or dedicated input.

F16V8C can be configured in one of three different Each mode makes the ATF16V8C look like a differ- ice. Most PLD compilers can choose the right mode tically. The user can also force the selection by sup- he compiler with a mode selection. The determining would be the usage of register versus combinatorial and dedicated outputs versus outputs with output control.

TF16V8C universal architecture can be programmed late many 20-pin PAL devices. These architectural subsets can be found in each of the configuration modes described in the following pages. The user can download the listed subset device JEDEC programming file to the PLD programmer, and the ATF16V8C can be configured to act like the chosen device. Check with your programmer manufacturer for this capability.

Unused product terms are automatically disabled by the compiler to decrease power consumption. A Security Fuse, when programmed, protects the content of the ATF16V8C. Eight bytes (64 fuses) of User Signature are accessible to the user for purposes such as storing project name, part number, revision, or date. The User Signature is accessible regardless of the state of the Security Fuse.

piler Mode Selection

	Registered	Complex	Simple	Auto Select
., Atmel-ABEL	P16V8R	P16V8C	P16V8AS	P16V8
With PD ENABLE	P16V8PDR[1]	P16V8PDC[1]	P16V8PD[1]	P16V8PDS[1]
., Atmel-CUPL	G16V8MS	G16V8MA	G16V8AS	G16V8A
With PD ENABLE	G16V8CPMS	G16V8CPMA	G16V8CPAS	G16V8CP
ViC	GAL16V8_R[2]	GAL16V8_C7[2]	GAL16V8_C8[2]	GAL16V8
AD-PLD	"Registered"	"Complex"	"Simple"	GAL16V8A
esigner	P16V8R	P16V8C	P16V8C	P16V8A
rio/Atmel-Synario	NA	NA	NA	ATF16V8C ALL
With PD ENABLE	NA	NA	NA	ATF16V8C (PD) ALL[1]
go-PLD	G16V8R	G16V8C	G16V8AS	G16V8

1. Please call Atmel PLD Hotline at (408) 436-4333 for more information.
2. Only applicable for version 3.4 or lower.

ocell Configuration

e compilers support the three different OMC modes ent device types. These device types are listed in e below. Most compilers have the ability to automat- elect the device type, generally based on the usage and output enable ($\overline{OE}$) usage. Register n the device forces the software to choose the reg- mode. All combinatorial outputs with $\overline{OE}$ controlled product term will force the software to choose the x mode. The software will choose the simple mode en all outputs are dedicated combinatorial without trol. The different device types listed in the table used to override the automatic device selection by ware. For further details, refer to the compiler soft- anuals.

using compiler software to configure the device, the ust pay special attention to the following restrictions mode.

stered mode pin 1 and pin 11 are permanently con- as clock and output enable, respectively. These nnot be configured as dedicated inputs in the regis- node.

plex mode pin 1 and pin 11 become dedicated and use the feedback paths of pin 19 and pin 12 tively. Because of this feedback path usage, pin 19 12 do not have the feedback option in this mode.

ple mode all feedback paths of the output pins are via the adjacent pins. In doing so, the two inner most ins 15 and 16) will not have the feedback option as ins are always configured as dedicated combinato- tput.

16V8C Registered Mode

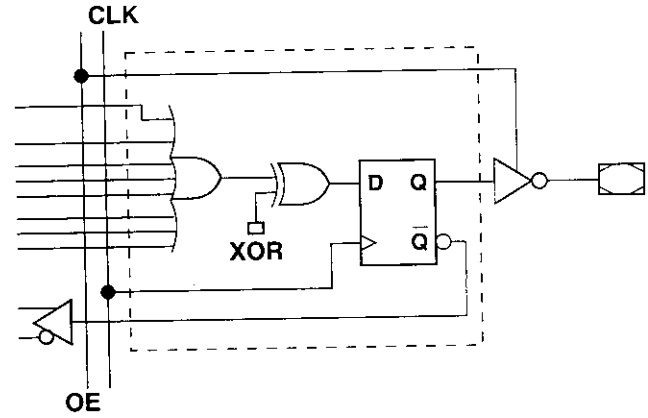
Device Emulation/PAL Replacement

egistered mode is used if one or more registers are ed. Each macrocell can be configured as either a reg- d or combinatorial output or I/O, or as an input. For a ered output or I/O, the output is enabled by the $\overline{OE}$ nd the register is clocked by the CLK pin. Eight ct terms are allocated to the sum term. For a combi- al output or I/O, the output enable is controlled by a ct term, and seven product terms are allocated to the erm. When the macrocell is configured as an input, tput enable is permanently disabled.

egister usage will make the compiler select this mode. ollowing registered devices can be emulated using ode:

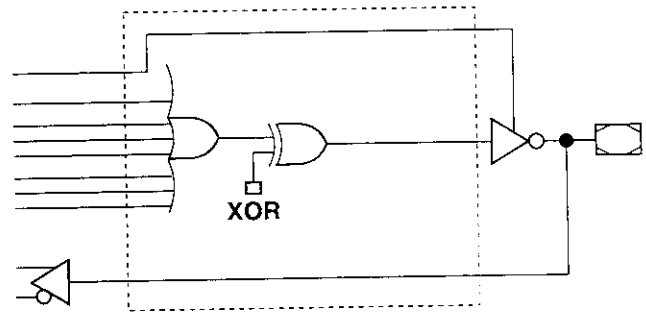
16RP8
16RP6
16RP4

Registered Configuration for Registered Mode(1)(2)



Notes:
1. Pin 1 controls common CLK for the registered outputs.
   Pin 11 controls common $\overline{OE}$ for the registered outputs.
   Pin 1 and Pin 11 are permanently configured as CLK and $\overline{OE}$.
2. The development software configures all the architecture control bits and checks for proper pin usage automatically.

Combinatorial Configuration for Registered Mode(1)(2)



Notes:
1. Pin 1 and Pin 11 are permanently configured as CLK and $\overline{OE}$.
2. The development software configures all the architecture control bits and checks for proper pin usage automatically.

Functional Description

DEVICE OPERATION

The six modes of operation of the NMC27C64 are listed in Table 1. It should be noted that all inputs for the six modes are at TTL levels. The power supplies required are V_{CC} and V_{PP}. The V_{PP} power supply must be at 12.75V during the three programming modes, and must be at 5V in the other three modes. The V_{CC} power supply must be at 6V during the three programming modes, and at 5V in the other three modes.

Read Mode

The NMC27C64 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. The programming pin ($\overline{PGM}$) should be at V_{IH} except during programming. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of OE , assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

The sense amps are clocked for fast access time. V_{CC} should therefore be maintained at operating voltage during read and verify. If V_{CC} temporarily drops below the spec. voltage (but not to ground) an address transition must be performed after the drop to insure proper output data.

Standby Mode

The NMC27C64 has a standby mode which reduces the active power dissipation by 99%, from 55 mW to 0.55 mW. The NMC27C64 is placed in the standby mode by applying a CMOS high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tying

Because NMC27C64s are usually used in larger memory arrays, Fairchild has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

1. the lowest possible memory power dissipation, and
2. complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recomended that $\overline{CE}$ (pin 20) be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 22) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 14V on pin 1 (V_{PP}) will damage the NMC27C64.

Initially, all bits of the NMC27C64 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be presented in the data word. A "0" cannot be changed to a "1" once the bit has been programmed.

The NMC27C64 is in the programming mode when the V_{PP} power supply is at 12.75V and $\overline{OE}$ is at V_{IH}. It is required that at least a 0.1 µF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

For programming, $\overline{CE}$ should be kept TTL low at all times while V_{PP} is kept at 12.75V.

When the address and data are stable, an active low, TTL program pulse is applied to the $\overline{PGM}$ input. A program pulse must be applied at each address location to be programmed. The NMC27C64 is programmed with the Fast Programming Algorithm shown in Figure 1. Each address is programmed with a series of 100 µs pulses until it verfies good, up to a maximum of 25 pulses. Most memory cells will program with a single 100 µs pulse. The NMC27C64 must not be programmed with a DC signal applied to the PGM input.

Programming multiple NMC27C64s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled NMC27C64s may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{PGM}$ input programs the paralleled NMC27C64s. If an application requires erasing and reprogramming, the NMC27C64Q UV erasable PROM in a windowed package should be used.

TABLE 1. Mode Selection

Pins / Mode	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	V_{PP} (1)	V_{CC} (28)	Outputs (11–13, 15–19)
Read	V_{IL}	V_{IL}	V_{IH}	5V	5V	D_{OUT}
Standby	V_{IH}	Don't Care	Don't Care	5V	5V	Hi-Z
Output Disable	Don't Care	V_{IH}	V_{IH}	5V	5V	Hi-Z
Program	V_{IL}	V_{IH}		13V	6V	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	13V	6V	D_{OUT}
Program Inhibit	V_{IH}	Don't Care	Don't Care	13V	6V	Hi-Z

Functional Description (Continued)

Program Inhibit

Programming multiple NMC27C64s in parallel with different data is also easily accomplished. Except for $\overline{CE}$ all like inputs (including $\overline{OE}$ and $\overline{PGM}$) of the parallel NMC27C64 may be common. A TTL low level program pulse applied to an NMC27C64's $\overline{PGM}$ input with $\overline{CE}$ at V_{IL} and V_{PP} at 13.0V will program that NMC27C64. A TTL high level $\overline{CE}$ input inhibits the other NMC27C64s from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 13.0V. V_{PP} must be at V_{CC}, except during programming and program verify.

MANUFACTURER'S IDENTIFICATION CODE

The NMC27C64 has a manufacturer's identification code to aid in programming. The code, shown in Table 2, is two bytes wide and is stored in a ROM configuration on the chip. It identifies the manufacturer and the device type. The code for the NMC27C64 is "8FC2", where "8F" designates that it is made by Fairchild Semiconductor, and "C2" designates a 64k part.

The code is accessed by applying 12V ± 0.5V to address pin A9. Addresses A1–A8, A10–A12, $\overline{CE}$, and $\overline{OE}$ are held at V_{IL}. Address A0 is held at V_{IL} for the manufacturer's code, and at V_{IH} for the device code. The code is read out on the 8 data pins. Proper code access is only guaranteed at 25°C ± 5°C.

The primary purpose of the manufacturer's identification code is automatic programming control. When the device is inserted in a EPROM programmer socket, the programmer reads the code and then automatically calls up the specific programming algorithm for the part. This automatic programming control is only possible with programmers which have the capability of reading the code.

ERASURE CHARACTERISTICS

The erasure characteristics of the NMC27C64 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å – 4000Å range.

After programming, opaque labels should be placed over the NMC27C64's window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

The recommended erasure procedure for the NMC27C64 is exposure to short wave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 15W-sec/cm^2.

The NMC27C64 should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of 4.) Lamps lose intensity as they age. When a lamp is changed, the distance has changed or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by voltage transitions on input pins. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated V_{CC} transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that at least a 0.1 µF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, at least a 4.7 µF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of the PC board traces.

TABLE 2. Manufacturer's Identification Code

Pins	A0 (10)	O7 (19)	O6 (18)	O5 (17)	O4 (16)	O3 (15)	O2 (13)	O1 (12)	O0 (11)	Hex Data
Manufacturer Code	V_{IL}	1	0	0	0	1	1	1	1	8F
Device Code	V_{IH}	1	1	0	0	0	0	1	0	C2