

SPEED CONTROL OF MOTOR USING CELLULAR PHONE

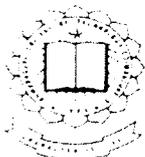
PROJECT REPORT

P-1150

Submitted by
ANANTHALAKSHMI. H
BETSY THOMAS.
KAVITHA. S.
LAAVANYA. S.

Guided by
Mr. S. TITUS, M.E.,
Lecturer, Dept. of EEE.

In partial fulfillment of the requirements for the award of the degree of
BACHELOR OF ENGINEERING in
ELECTRICAL AND ELECTRONICS ENGINEERING
branch of **BHARATHIAR UNIVERSITY, COIMBATORE**



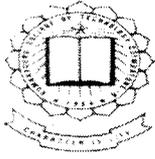
Estd-1984

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING
KUMARAGURU COLLEGE OF TECHNOLOGY
COIMBATORE - 641 006



ISO 9001:2000
Certified

2003- 2004



Estd-1984

KUMARAGURU COLLEGE OF TECHNOLOGY
COIMBATORE - 641 006
DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING



ISO 9001:2000
Certified

CERTIFICATE

This is to certify that the project report entitled
SPEED CONTROL OF MOTOR USING CELLULAR PHONE
is the bonafide work done by

ANANTHALAKSHMI.H-2KEEEE01
BETSY THOMAS-2KEEEE08
KAVITHA.S-2KEEEE15
LAAVANYA.S-2KEEEE17

*in partial fulfillment of the requirements for the Award of the degree
of Bachelor of Engineering In Electrical and Electronics Engineering
Branch of Bharathiar university, Coimbatore for 2003-04.*


GUIDE
Date: 10/03/04.


HEAD OF DEPARTMENT

Certified that the candidate _____ with
University Register No. _____ was examined in
Project work Viva-Voce Examination on 12-3-04.


Internal Examiner


External Examiner

Acknowledgement

ACKNOWLEDGEMENT

We are indebted to **Dr. K. K. PADMANABHAN, B.Sc. (Engg.), M.Tech., Ph.D., M.I.S.T.E., F.I.E., Principal**, Kumaraguru College of Technology for providing us the facilities to complete this project successfully.

We sincerely thank our Head of the Department **Dr. T. M. KAMESWARAN, B.E., M.Sc., (Engg), Ph.D., MISTE, Sr. M.I.E.E.E., F.I.E.**, for his invaluable suggestions and encouragement.

We place on record our gratitude to **Asst. Prof. V. Duraisamy, M.E, M.I.S.T.E, A.M.I.E, M.S.S.I. Project Co-ordinator** for his invaluable suggestions and assistance.

We thank our Guide **Mr. S. Titus, M.E., M.I.S.T.E.**, for his valuable guidance and technical expertise that aided us in completing our project.

We would be failing in our duty if we don't thank all the department staff, lab technicians who in their own way encouraged and supported us in our project.

And last but not the least we want to thank family and friends who have been our pillar of support at all times.

Synopsis

SYNOPSIS

This project aims to integrate both the fields of electrical and electronics in keeping with the true spirit of the course of which we are a part of "SPEED CONTROL OF MOTOR USING CELLULAR PHONE" as the name suggests is committed to speed control of motor. On the activation of the call from a cellular phone to the phone connected to the circuit the speed of the motor is controlled or altered by directly keying the speed in the dial pad of the phone. To detect this we have made use of the DTMF decoder. The control set up for the model is provided by the 89C51 micro controller. The speed is controlled using SCR. The speed of the motor is obtained by the proximity sensor which in turn is displayed on a LCD display.

The main intention behind this project is to obtain speed control of the motor from a remote place and the idea behind this project is harbinger of many of the sophisticated techniques that can be built on this idea.

Contents

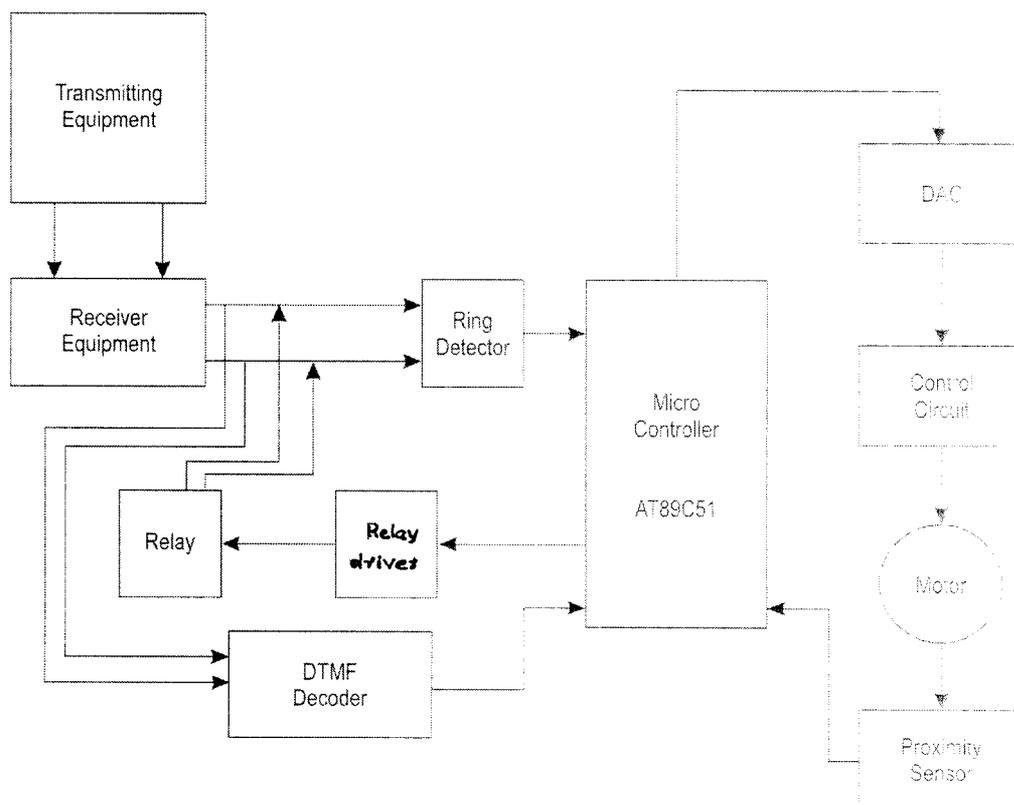
CONTENTS

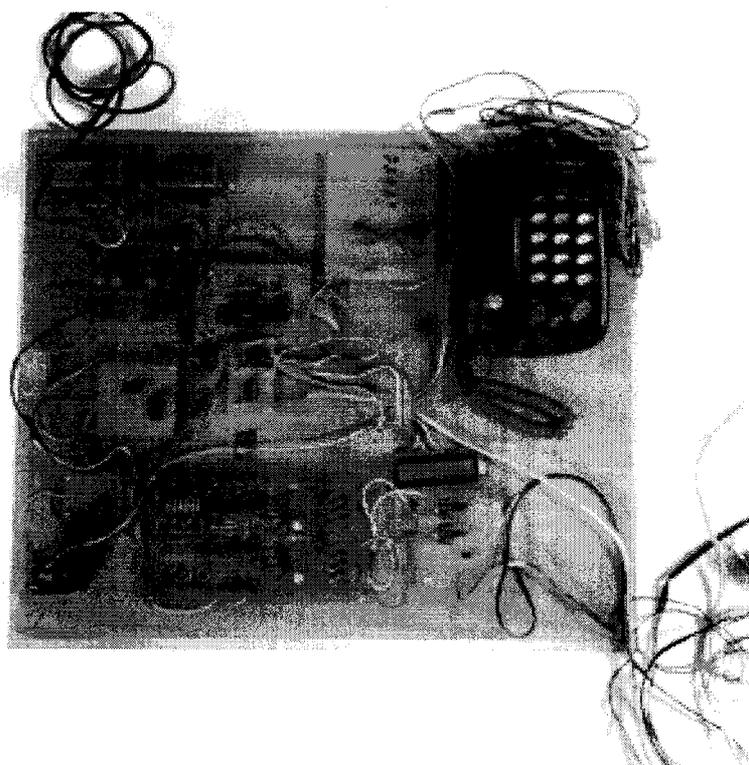
	Certificate	ii
	Acknowledgment	iv
	Synopsis	vi
	Contents	viii
1	Introduction	
	1.1 Block Diagram	2
2	Hardware Details	
	2.1 Overall Circuit Diagram	7
	2.2 Power Supply	8
	2.3 Ring Detector	11
	2.4 Microcontroller	13
	2.4 DTMF Decoder	25
	2.5 Relay	30
	2.6 DAC	31
	2.7 Control Circuit	35
	2.9 Universal Motor	38
3	Software Details	
	3.1 Program	41
4	Project Module	54
5	Conclusion	56
	Appendix	
	Bibliography	

INTRODUCTION :

Most modern gadgets used on a day to day basis are motor driven appliances. In keeping up with the speed of the modern world it only makes sense to automate the control of these gadgets to our convenience and a more sophisticated improvement is -control of these gadgets from a remote place. With the advent of telecommunication especially cellular phone, conquering time and space has only been made easier. So thus taking this into account we have ventured in controlling the speed of motor by a phone call to a telephone connected to the circuit.

GENERAL BLOCK DIAGRAM :





TRANSMISSION AND RECEIVER EQUIPMENT :

The transmission equipment is the cellular phone from which the call is being made. The receiver equipment is the phone that is connected to the circuit.

RING DETECTOR :

The ring detector counts the number of rings and sends the information of the same to the microcontroller. The number of rings can be manipulated by appropriate software programming. In our case we have fixed the number of rings to be five. After the fifth ring the ring detector sends a signal to the microcontroller.

MICROCONTROLLER :

The micro controller that we have used is ATMEL 89C51. The microcontroller is the main control circuit.

RELAY DRIVER:

The microcontroller on receiving the signal from the ring detector after the fifth ring activates the relay which in turn lifts the hook off thus connecting the incoming call.

DTMF :

Once the call has been connected the user has to key in the desired speed in the dial pad of the phone from which he/she is dialing. These signals are converted to digital signals by the **DUAL TONE MULTI FREQUENCY DECODER**. We have used DTMF decoder 8870 for the same.

DAC :

The digital signals are sent to the microcontroller from which they are conveyed to the DAC to be converted into analog signals by DAC-0800. This signal corresponds to the difference between the running speed and the speed keyed in.

SCR CONTROL :

The analog signals from the DAC are passed on to the SCR control circuit which provide voltage control to the motor.

MOTOR :

This is the motor whose speed is being controlled. This motor could be a part of any modern day gadget or it could be a motor in its very sense. The type of motor can be changed according to the need of the situation. In our case we have used a UNIVERSAL MOTOR.

PROXIMITY SENSOR :

The proximity sensor is the speed sensing device which is connected to the motor. This is senses the running speed of the motor thus providing closed loop control to the project. This speed is considered the bench mark or base level from which the difference between the new speed is calculated. The output of the proximity sensor is connected to the microcontroller.

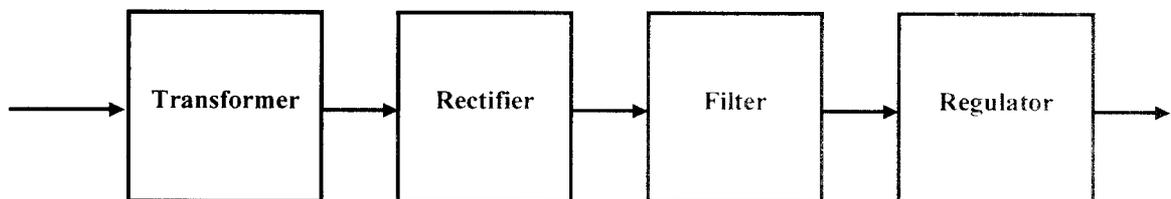
Hardware Details

POWER SUPPLY UNIT

The power supply circuits are built using filters, rectifiers and voltage regulators. Starting with an ac voltage, a steady dc voltage is obtained by rectifying the ac voltage, then filtering to a dc level, and finally regulating to obtain a desired fixed dc voltage. The regulation is usually obtained from an IC voltage regulator unit, which takes a dc voltage and provides a somewhat lower dc voltage, which remains the same even if the input dc voltage varies, or load connected to the output changes.

A.C. voltage typically 230V rms is connected to a transformer which steps that AC voltage down to the level of the desired AC voltage. A diode rectifier then provides a full-wave rectified voltage that is initially filtered by a simple capacitor filter to produce a DC voltage. This resulting DC voltage usually has some ripple or AC voltage variations. A regulator circuit can use this DC input to provide DC voltage that not only has much less ripple voltage but also remains in the same DC value even if the DC voltage varies or the load connected to the output changes.

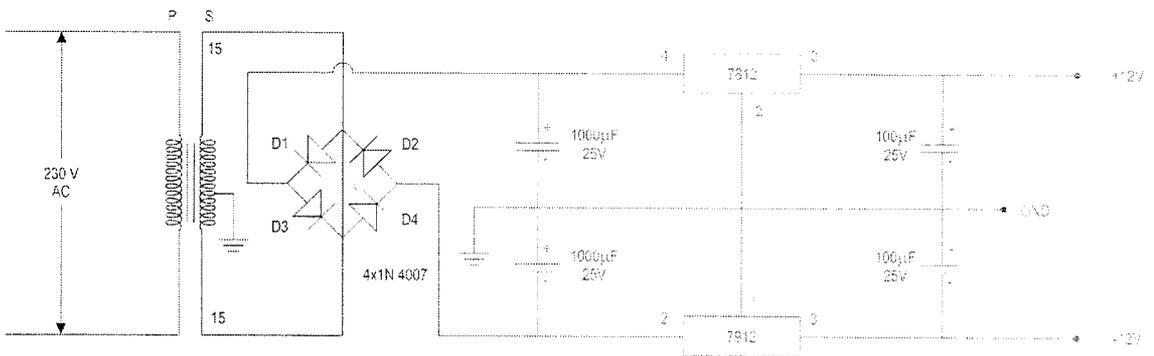
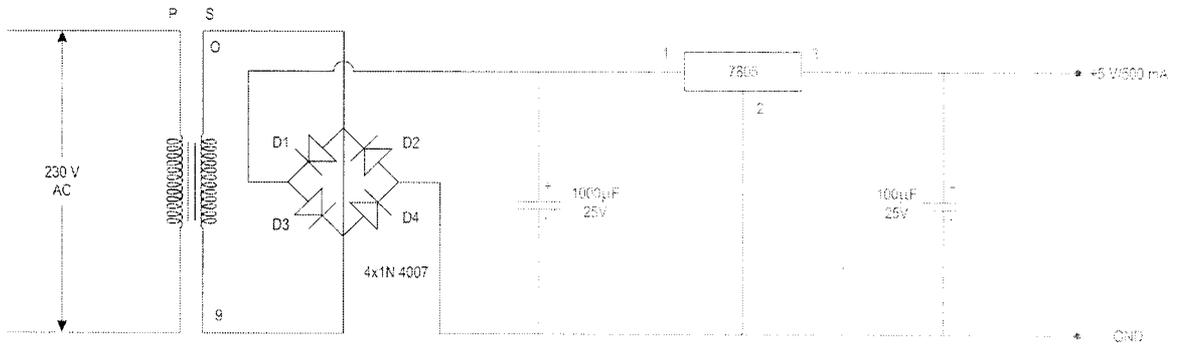
BLOCK DIAGRAM :



TRANSFORMER :

A transformer is a static device in which electric power in one circuit is transformed into electric power of the same frequency in another circuit. It can raise or lower the voltage in a circuit but with a corresponding decrease or increase in current. It works by the principle of mutual induction. In our project we are using step down transformer for providing a necessary supply for the electronic circuits and we are using a 15-0-15 center tapped transformer.

POWER SUPPLY



RECTIFIER :

The DC level obtained from a sinusoidal input can be improved 100% using a process called full-wave rectification. It uses 4 diodes in a bridge configuration. From the basic bridge configuration we see that two diodes (say D2 & D3) are conducting while the other two diodes (D1 & D4) are in "off" state during the positive of the input. Accordingly for the negative of the input the conducting diodes are D1 & D4. Thus the polarity across the load is the same.

FILTER :

The filter circuit used here is the capacitor filter circuit where a capacitor is connected at the rectifier output, and a DC is obtained across it. The filtered waveform is essentially a DC voltage with negligible ripples, which is ultimately fed to the load.

REGULATOR :

The output voltage from the capacitor is more filtered and finally regulated. The voltage regulator is a device, which maintains the output voltage constant irrespective of the change in supply variations, load variations and temperature changes. Here we use two fixed voltage regulators namely LM 7812, LM 7805 and LM7912. The IC 7812 is a +12V regulator, IC 7912 is a -12V regulator and IC 7805 is a +5V regulator.

RING DETECTOR

The circuit for the ring detector is shown in the figure 1. The capacitor C1 acts as a filter for the incoming AC signal. This AC signal is fed to the diode 1N4007, which acts as a rectifier. Resistors R1 and R2 are used for current limiting purposes. The base resistor R3 prevents the high current from reaching the transistor BC547 i.e. it prevents the transistor from getting damaged. The resistor R5 is used for signal boosting.

Initially the capacitor C2 is in the charged condition. When the ring signal is given as the input the transistor becomes ON and the capacitor C2 discharges, which in turn helps in triggering the timer 555. Depending upon R6 and C3 the timer is oscillated and a pulse is generated at the output. Thus the ring detector detects the number of ring pulses. The number of ring pulses can be set according to our need using software and an electromagnetic relay is used for hook switch release.

555 TIMER is used in the ring detector circuit. It is a highly stable device for getting accurate time delay or oscillation. A single 555 TIMER can provide time delay ranging from microseconds to hours.

The 555 TIMER can be used with supply voltage in the range of +5V to +18V and can drive load upto 200mA. It is compatible with both TTL and CMOS logic circuits. Because of the wide range of supply voltage the 555 TIMER are versatile and are easy to use in various applications.

RING DETECTOR

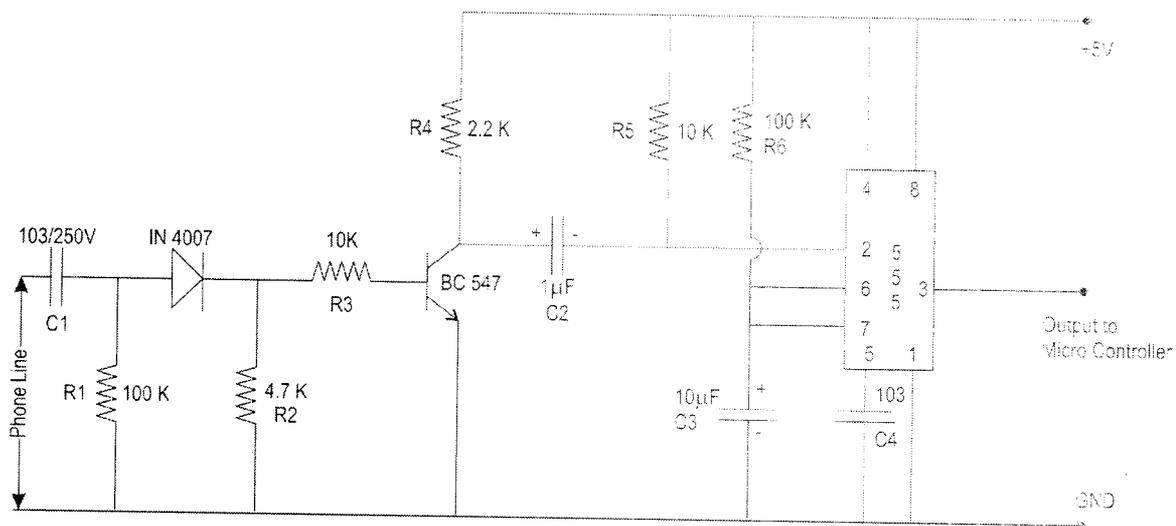


Fig. 1

MICROCONTROLLER

INTRODUCTION :

A microcontroller consist of a microprocessor coupled with memory RAM, ROM or EPROM, and various input/output features such as serial ports, parallel ports, timers/counters, interrupt controller, data acquisition interfaces-analog to digital converter(ADC),digital to analog converter (DAC), everything integrated onto a single silicon chip. A microcontroller may not have all the above mentioned features. Depending upon the application its design and features may vary.

The microcontroller we are using in our project is 89C51, manufactured by Atmel. This microcontroller has inbuilt 4K bytes of flash ROM,256 bytes of RAM, 32 I/O lines and 6 vectored interrupts.

FEATURES OF 89C51 :

- 8 Bit CPU- optimized for control applications
- Extensive Boolean processing (Single-bit Logic) Capabilities.
- On - Chip Flash Program Memory
- On - Chip Data RAM
- Bi-directional and Individually Addressable I/O Lines
- Multiple 16-Bit Timer/Counters
- Full Duplex UART
- Multiple Source / Vector / Priority Interrupt Structure
- On - Chip Oscillator and Clock circuitry.
- On - Chip EEPROM
- SPI Serial Bus Interface
- Watch Dog Timer

MEMORY ORGANIZATION:

The Atmel Flash micro controllers have separate address spaces for program and data memory. The logical separation of program and data memory allows the data memory to be accessed by 8 bit addresses, which can be more quickly stored and manipulated by an 8 bit CPU. Nevertheless 16 Bit data memory addresses can also be generated through the DPTR register.

Program memory can only be read. There can be up to 64K bytes of directly addressable program memory. The read strobe for external program memory is the Program Store Enable Signal (PSEN).

Data memory occupies a separate address space from program memory. Up to 64K bytes of external memory can be directly addressed in the external data memory space. The CPU generates read and write signals during external data memory access. External program memory and external data memory can be combined by applying the RD and PSEN signals to the inputs of AND gate and using the output of the gate as the read strobe to the external program/data memory.

PROGRAM MEMORY :

After reset, the CPU begins execution from location 0000h. Each interrupt is assigned a fixed location in program memory. The interrupt causes the CPU to jump to that location, where it executes the service routine. The interrupt service locations are spaced at 8 byte intervals. If an Interrupt service routine is short enough (as is often the case in control applications) it can reside entirely within that 8-byte interval. Longer service routines can use a jump instruction to skip over subsequent interrupt locations, if other interrupts are in use. The lowest addresses of program memory can be either in the on-chip Flash or in an external memory. To make this selection, strap the External Access (EA) pin to either V_{cc} or GND.

DATA MEMORY :

The Internal Data memory is divided into three blocks namely:

- The lower 128 Bytes of Internal RAM.
- The Upper 128 Bytes of Internal RAM.
- Special Function Register.

Internal Data memory Addresses are always 1 byte wide, which implies an address space of only 256 bytes. However, the addressing modes for internal RAM can in fact accommodate 384 bytes. Direct addresses higher than 7Fh access one memory space, and indirect addresses higher than 7Fh access a different Memory Space.

The lowest 32 bytes are grouped into 4 banks of 8 registers. Program instructions call out these registers as R0 through R7. Two bits in the Program Status Word (PSW) select which register bank is in use. This architecture allows more efficient use of code space since register instructions are shorter than instructions that use direct addressing.

The next 16-bytes above the register banks form a block of bit addressable memory space. The microcontroller instruction set includes a wide selection of single - bit instructions and this instruction can directly address the 128 bytes in this area. These bit addresses 00h through 7Fh which can be either directly or indirectly addressed can access all of the bytes in lower 128 bytes. Indirect addressing can only access the upper 128 bytes.

The Special Function Register includes Port latches, timers, peripheral controls etc. Direct addressing can only access these registers. Sixteen addresses in SFR space are both byte and bit addressable.

ADDRESSING MODES :

DIRECT ADDRESSING :

In direct addressing, the operand is specified by an 8-bit address field in the instruction. Only internal data RAM and SFR's can be directly addressed.

INDIRECT ADDRESSING :

In Indirect addressing, the instruction specifies a register that contains the address of the operand. Both internal and external RAM can be indirectly addressed.

The address register for 8-bit addresses can be either the Stack Pointer or R0 or R1 of the selected register Bank. The address register for 16-bit addresses can be only the 16-bit data pointer register, DPTR.

INDEXED ADDRESSING :

Program memory can only be accessed via indexed addressing. This addressing mode is intended for reading look-up tables in program memory. A 16 bit base register (either DPTR or the Program Counter) points to the base of the table and the accumulator is set up with the table entry number. Adding the accumulator data to the base pointer forms the address of the table entry in program memory.

Another type of indexed addressing is used in the " case jump " instructions. In this case the destination address of a jump instruction is computed as the sum of the base pointer and the accumulator data.

REGISTER INSTRUCTION:

The register banks which contains registers R0 through R7, can be accessed by instructions whose opcodes carry a 3-bit register specification. Instructions that access the registers this way make efficient use of code since this mode eliminates an address byte. When the instruction is executed, one of four banks is selected at execution time by the row bank select bits in PSW.

REGISTER - SPECIFIC INSTRUCTION :

Some Instructions are specific to a certain register. For example some instructions always operates on the Accumulator. In these cases the opcode itself points to the correct register.

IMMEDIATE CONSTANTS :

The value of a constant can follow the opcode in program memory. For example `MOV A, #100` loads the Accumulator with the decimal number 100. The same number could be specified in hex digit as 64h.

PROGRAM STATUS WORD:

CY	AC	F0	RS1	RS0	OV	-	P
PSW7	PSW6	PSW5	PSW4	PSW3	PSW2	PSW1	PSW0

PSW0 :

Parity of accumulator- set by hardware to 1 if it contains an odd number of 1s, otherwise it is reset to 0.

PSW1 :

User definable flag.

PSW2 :

Overflow flag set by arithmetic operations.

PSW3 :

Register bank select.

PSW4 :

Register bank select.

PSW5 :

General purpose flag.

PSW6 :

Auxiliary carry flag -Receives carry out from Bit 1 of addition operands.

PSW7 :

Carry flag- Receives carry out from Bit 1 of ALU operands.

The Program Status Word contains status bits that reflects the current state of the CPU. The PSW resides in SFR space. The PSW contains the carry bit, the auxillary carry (for BCD operations), the two - register bank select bits, the overflow flag, a parity bit and two user definable status flags.

The carry bit, in addition to serving as a carry bit in arithmetic operations also serves the as the "Accumulator" for a number of Boolean operations .The bits RS0 and RS1 select one of the four register banks. A number of instruction registers are there in the RAM locations as R0 through R7.The status of the RS0 and RS1 bits at execution time determines which of the four banks is selected.

The Parity bit reflect the number of 1s in the accumulator. P=1 if the accumulator contains odd number of 1s, and P=0 if the accumulator contains even number of 1s. Thus, the number of 1s in the accumulator plus P is always even. Two bits in the PSW are uncommitted and can be used as general-purpose status flags.

INTERRUPTS :

The AT89C51 provides 5 interrupt sources: Two External interrupts two-timer interrupts and a serial port interrupt. The External Interrupts INT0 and INT1 can each either be level activated or transition - activated, depending on bits IT0 and IT1 in Register TCON. The Flags that actually generate these interrupts are the IE0 and IE1 bits in TCON. When the service routine is vectored to hardware it clears the flag that generated an external interrupt only if the interrupt is transition - activated. If the interrupt was level - activated, then the external requesting source (rather than the on-chip hardware) controls the requested flag. Tf0 and Tf1 generate the Timer 0 and Timer 1 Interrupts, which are set by a rollover in their respective Timer/Counter register (except for Timer 0 in Mode 3). When a timer interrupt is generated, the on-chip hardware clears the flag that generated it. The logical OR of RI and TI generate the serial port Interrupt. Neither of these flag is cleared by hardware when the service routine is vectored to. In fact, the service routine normally must determine whether RI or TI generated the interrupt and the bit must be cleared in software.

IE: Interrupt Enable Register

EA	-	ET2	ES	ET1	EX1	ET0	EX0
----	---	-----	----	-----	-----	-----	-----

Enable bit = 1 enabled the interrupt

Enable bit = 0 disables it.

Symbol	Position	Function
EA	IE	Global enable / disable all interrupts. If EA = 0, no interrupt will be Acknowledge If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
-	IE.6	Undefined / reserved
ET2	IE.5	Timer 2 Interrupt enable Bit
ES	IE.4	Serial Port Interrupt enabled bit.
ET1	IE.3	Timer 1 Interrupt enable bit.
EX1	IE.2	External Interrupt 1 enable bit.
ET0	IE.1	Timer 0 Interrupt enable bit.
EX0	IE.0	External Interrupt 0 enable bit.

PIN DESCRIPTION:

VCC-Supply voltage

GND-Ground

Port 0:

Port 0 is an 8-bit open-drain bi-directional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs.

Port 0 may also be configured to be the multiplexed with low-order address/data bus during access to external program and data memory. In this mode P0 has internal pullups.

Port 0 also receives the code bytes during Flash programming, and outputs the code bytes during program verification. External pullups are required during program verification.

Port 1:

Port 1 is an 8-bit bi-directional I/O port with internal pullups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}) because of the internal pullups. Port 1 also receives the low-order address bytes during flash programming and verification.

Port 2:

Port 2 is an 8-bit bi-directional I/O port with internal pullups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses. In this application, it uses strong internal pull-ups when emitting 1s.

During accesses to external data memory that use 8-bit addresses, Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during flash programming and verification.

Port 3:

Port 3 is an 8-bit bi-directional I/O port with internal pullups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pullups. Port 3 also receives some control signals for flash programming and verification. Port 3 also serves the functions of various special features of the AT89C51 which are listed below.

Port Pin Alternate Functions:

P3.0 RXD (serial input port)

P3.1 TXD (serial output port)

P3.2 INT0 (external interrupt 0)

P3.3 INT1 (external interrupt 1)

P3.4 T0 (timer 0 external input)

P3.5 T1 (timer 1 external input)

P3.6 WR (external data memory write strobe)

P3.7 RD (external data memory read strobe)

RST:

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

ALE/PROG:

Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input (PROG) during flash programming. In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clock purposes. However one ALE pulse is skipped during each access to external data memory. If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

PSEN:

Program Store Enable is the read strobe to external program memory. When the AT89C51 is executing code from external program memory, PSEN is activated twice each machine cycle, except that two PSEN activations are skipped during each access to external data memory.

EA/VPP:

External Access Enable. EA must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. However, if lock bit 1 is programmed, EA will be internally latched on reset. EA should be strapped to V_{CC} for internal program executions. This pin also receives the 12-volt programming enable voltage (V_{PP}) during flash programming, for parts that require 12-volt V_{PP}.

XTAL1:

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

XTAL2:

Output from the inverting oscillator amplifier

OSCILLATOR AND CLOCK CIRCUIT:

XTAL1 and XTAL2 are the input and output respectively of an inverting amplifier which is intended for use as a crystal oscillator, in the frequency range of 1.2 Mhz to 12 Mhz. XTAL2 also the input to the internal clock generator.

To drive the chip with an internal oscillator, XTAL1 and XTAL2 is grounded. Since the input to the clock generator is divided by two flipflops there are no requirements on the duty cycle of the external oscillator signal. However, minimum high and low times must be observed.

The clock generator divides the oscillator frequency by 2 and provides a low phase clock signal to the chip. The phase 1 signal is active during the first half to each clock period and the phase 2 signals are active during the second half of each clock period.

MODES OF OPERATION :

IDLE MODE:

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special functions registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

It should be noted that when idle is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

POWER-DOWN MODE :

In the power-down mode, the oscillator is stopped, and the instruction that invokes power-down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the power-down mode is terminated. The only exit from power-down is a hardware reset. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before VCC is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

DTMF

The DTMF decoder decodes DTMF signals. DTMF stands for **dual-tone-multiple-frequency** and it is audible sound that can be heard when we press a key on the telephone keypad. The telephone network is designed to carry voice, but usually many other tasks are assigned to it to perform. For example, when we dial a number, the telephone has to communicate that number with the telephone company. Moreover, often we have to press telephone button in response to questions we are asked by interactive telephone systems, entering our account number, accessing answering machine, enquiring about account balance etc. So whenever we press the buttons of touch-tone phones the numbers are turned into tones. The method of turning numbers into tones is called DTMF signaling.

DTMF signaling converts the digits into tones that can travel over telephone network and carry information. The DTMF decoder decodes DTMF signals and represents them in a sequence of four bits. That means our system receives the DTMF signals as sinusoidal signal and converts them to binary numbers.

DTMF was originally developed to allow sending control information (dialed numbers) across the telephone network. The telephone network has a bandwidth of approx. 300 to 3400 Hz, suitable for voice communications. Any control tones would also need to be in this range and had to work regardless of whether voice was present or not. A single tone or frequency could have been used. However, if voice was present, it would interfere with the control tones, making them useless.

To overcome this a scheme was developed whereby two tones or frequencies were combined to represent each control code or number. A total of seven tones were needed to represent the digits normally found on a telephone keypad, namely 0-9, * and #. An eighth tone was added so that some extra digits were available for use. These are commonly labeled ABCD. These eight tones

were divided into two groups of four tones each, a low-frequency group and a high-frequency group.

The second harmonic of the low frequency group falls between the high-frequency tones. Third harmonics and above are outside the range of the high-frequency tones and are not a problem. A valid tone pair has to meet the following criteria:

- Only one tone per group allowed
- Start of each tone must be less than 5ms apart
- Both tones must last at least 40ms
- Each tone must be within 2% of the center frequency
- The tone levels must be within 6dB of each other.

All of these features make it extremely unlikely that voice will accidentally generate valid DTMF tones. This has meant that DTMF is now used for much more than just sending dialed numbers across the telephone network

It is not easy to detect and recognize DTMF with satisfactory precision. Often, dedicated integrated circuits are used. It is rather complicated, so it is used only marginally. Most often, a MT 8870 or compatible circuit would be used.

The MT8870 is a complete DTMF receiver integrating both the bandsplit filter and digital decoder functions. The filter section uses switched capacitor techniques for high and low group filters. The decoder uses digital counting techniques to detect and decodes all 16 DTMF tone-pairs into a 4-bit code. External component count is minimized by on chip provision of a differential input amplifier, clock oscillator and latched three-state bus interface.

Features of DTMF decoder

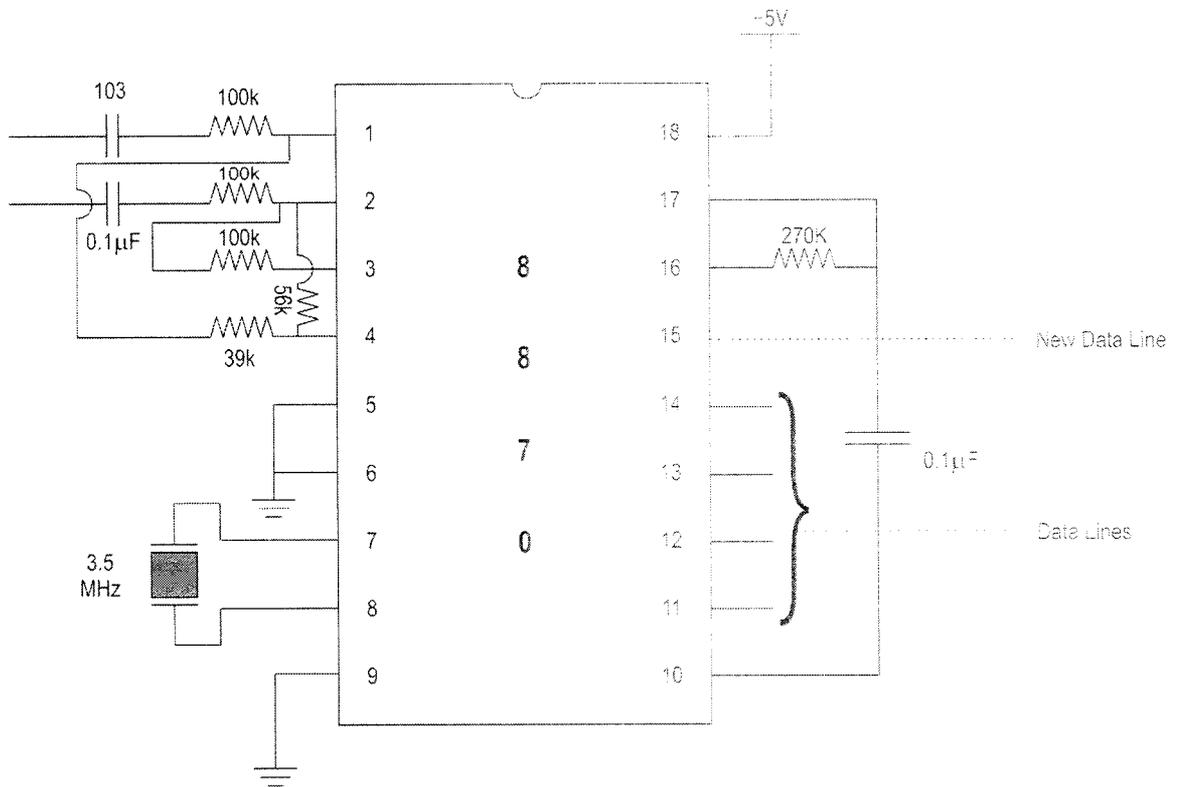
- Complete DTMF Receiver
- Low power consumption

- Internal gain setting amplifier
- Adjustable guard time
- Central office quality
- Power-down mode
- Inhibit mode
- Backward compatible with MT8870C/MT8870C-1

Typical Applications for DTMF decoders

- Paging systems
- Repeater systems/mobile radio
- Credit card systems
- Remote control
- Personal computers
- Telephone answering machine

DTMF



Pins and Tone Decoding Table of the DTMF Decoder Chip

DTMF Chip: M-8870-01

Number of pins: 18

Each pin with its connection:

Pin 1 (IN+): Non-inverting input.

Pin 2 (IN-): Inverting input.

Pin 3 (GS): Gain Select.

Pin 4 (Vref): Reference voltage output (normally $V_{dd}/2$).

Pin 5 (IC): Grounded.

Pin 6 (IC): Grounded.

Pin 7 (OSC1): Clock input. Clock source, 3.57MHz crystal, connected between this pin and OSC2.

Pin 8 (OSC2): Clock output. Clock source, 3.57MHz crystal, connected between this pin and OSC1.

Pin 9 (Vss): Negative power supply (normally connected to ground).

Pin 10 (OE): Tri-stable output enable (input).

Pin 11 – Pin 14 (Q1 – Q4): Tri- data output.

Pin 15 (StD): Delay steering output.

Pin 16 (Est): Early steering output.

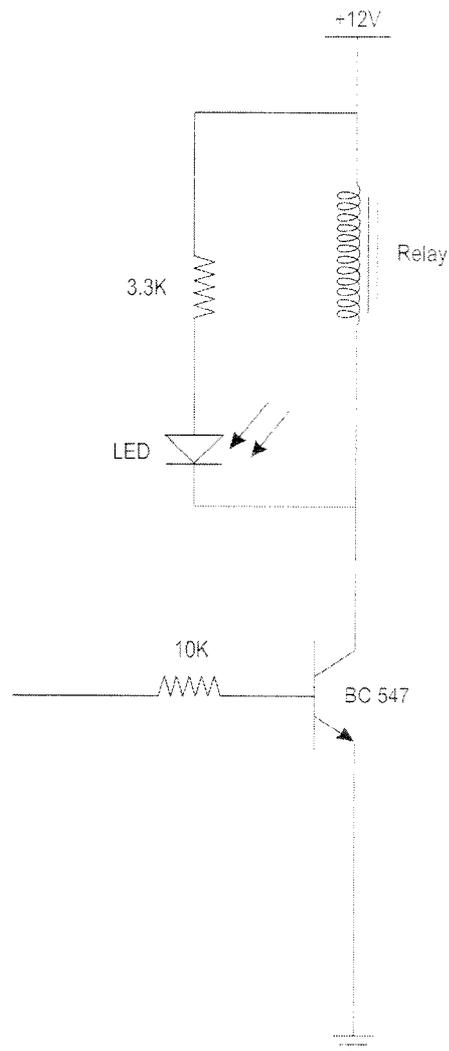
Pin 17 (St/GT): Steering input/guard time output.

Pin 18 (Vdd): Positive power supply, 5V.

RELAY

Relays are electromagnetic switches, which provide contact between two mechanical elements. Relays have a coil and provides DPDT action as an output. In general, relays provide potential free contacts which can be used for universal functions like DC, AC voltage switching and to control bigger electrical switchgears.

The electromagnetic relay consists of a core around which a coil is wound. When the coil is energized the core becomes magnetized and the armature placed near the core is attracted to it and the contact is made. When there is no power supply, demagnetization of the core occurs and the contact is removed.



DIGITAL TO ANALOG CONVERTER (DAC)

INTRODUCTION :

The purpose of DAC is to convert a binary word to a proportional current or voltage. The characteristics of DAC are:

i) Resolution :

Resolution is the smallest analog increment corresponding to a 1 LSB converter change. It is determined by the number of bits in the input binary word. A converter with 8 binary inputs has 256 output levels, so its resolution is 1 part in 256. The resolution of an 8 bit converter is 0.39 percent.

ii) Monotonicity :

A monotonic function has a slope whose sign does not change. A monotonic DAC has an output that changes in the same direction for each increase in the input code. The converse is true for decreasing codes.

iii) Offset error :

Offset error is the output voltage that exists when the input digital code is set to give an ideal output of zero volts. All the digital codes in the transfer curve are offset by the same value. Offset error is usually expressed in LSB's.

iv) Settling time :

The time from a change in input code until a DAC's output signal remains within $\pm \frac{1}{2}$ LSB of the final value.

v) Linearity:

It is a measure of how much the output ramp deviates from a straight line.

The DAC applications with computer:

- i) In Compact audio disk player 13 or 14 bit DAC converter is used to convert the binary data read off the disk by a laser to an analog audio signal.
- ii) The speech synthesizer IC's contain a DAC to convert stored binary data for words into analog audio signals.

DAC CHIP 0800 :

The DAC 0800 series are monolithic 8 bit high speed current output digital to analog converter (DAC) featuring typical setting time of 100ns. When used as a multiplying DAC, monotonic performance over a 40 to 1 reference current range is possible. The DAC 0800 series also features high compliance complementary current outputs to allow differential output voltages of 20V peak to peak with simple resistor loads. The reference to full scale current matching of better $\pm 1\text{LSB}$ eliminates the need for full scale trims in most applications while the nonlinearities of better than $\pm 0.1\%$ over temperature minimizes system error accumulations.

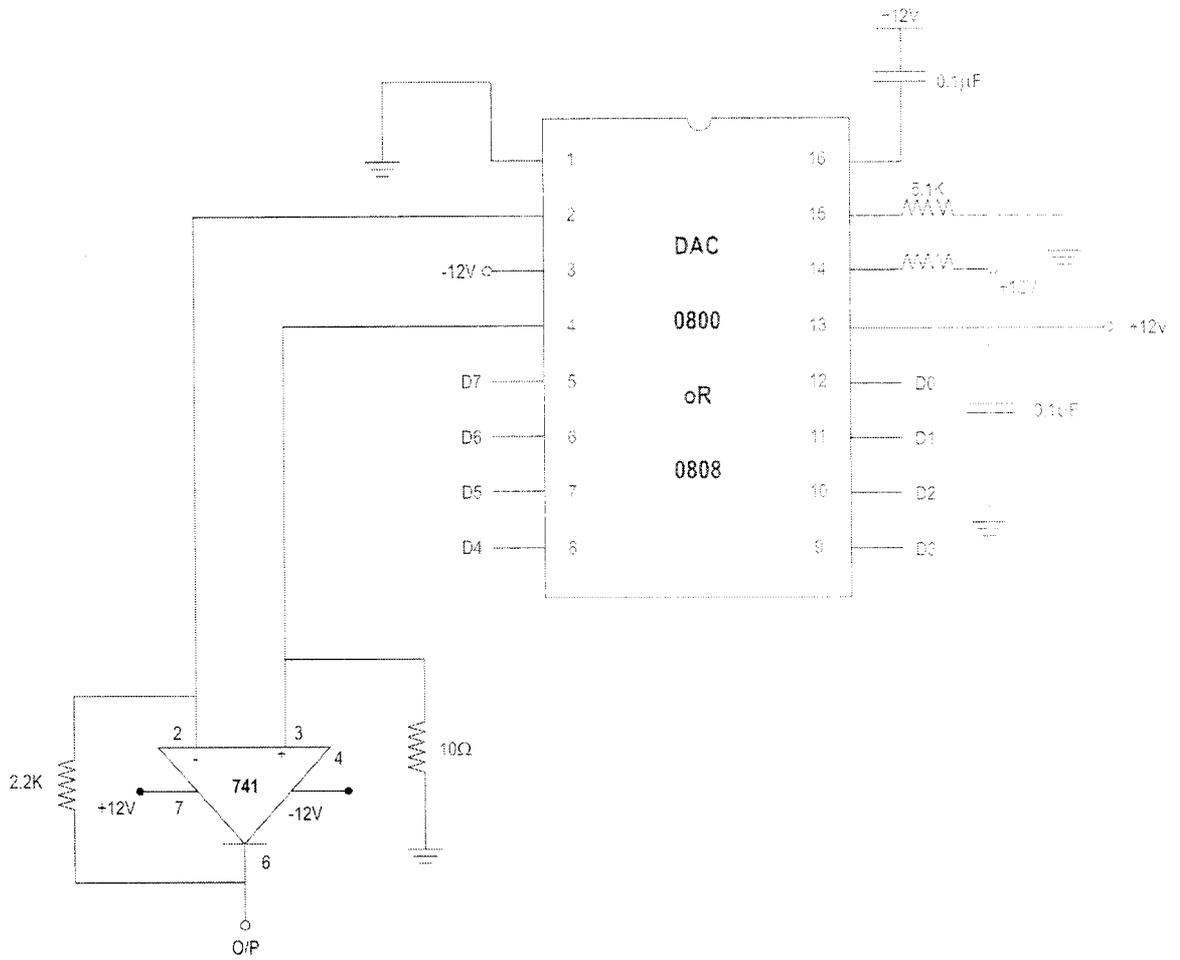
The noise immune inputs of the DAC0800 series will accept TTL levels with the logic threshold pin, V_{IC} grounded. Simple adjustments of the V_{IC} potential will allow direct interface to all logic families. The performance and characteristics of the device are essentially unchanged over the full $\pm 4.5\text{V}$ to $\pm 18\text{V}$ power supply range; power dissipation is only 33mW with $\pm 5\text{V}$ supplies and is independent of the logic input states.

Features :

- Fast setting output current
- Full scale error
- Nonlinearity over temperature
- Full scale current drift
- High output compliance
- Complementary current outputs

- Interface directly with TL, CMOS, PMOS, and others
- 2 quadrant wide range multiplying capability
- Wide power supply range
- Low power consumption
- Low cost

DAC



CONTROL CIRCUIT

This circuit is used for speed control and for on-off control. It is the high voltage section. Depending upon the firing pulses from the control section, SCRs are fired such that controlled output voltage is obtained from the half and fully controlled bridges. Single-phase 230V supply is transformed into 30V using center tapped transformer and it is given to full wave rectifier. The output of the rectifier is given to the base of the NPN transistor BC547. The collector is supplied +12V DC and the emitter is grounded.

The output of the transistor comprises of +12V on-off pulses of equal time period. It is given to the base of another NPN transistor BC547. Its emitter and collector are connected across the capacitor of an op-amp integrator –12V DC. The output of the integrator is a saw tooth waveform and it is given to the comparator. A dc voltage from micro controller unit is given to the amplifier and the output of the amplifier is given to the comparator.

The comparator compares these two signals and produces rectangular pulses, which is given to the pulse transformer which in turn triggers the gate of the SCR circuit.

INTEGRATOR :

The circuit in which the output voltage waveform is the integral of the input voltage waveform is the integrator. In our project, integrator circuit is obtained using a basic inverting op-amp 741 configuration by replacing the feedback resistor R_f by a capacitor C_f .

Then the output voltage will be

$$V_o = -1/R_1 C_1 \int V_i dt$$

The input voltage V_i given is –12V dc. The capacitor terminals are shunted with the transistors emitter and collector. The output of the integrator will be positive ramp signal.

AMPLIFIER :

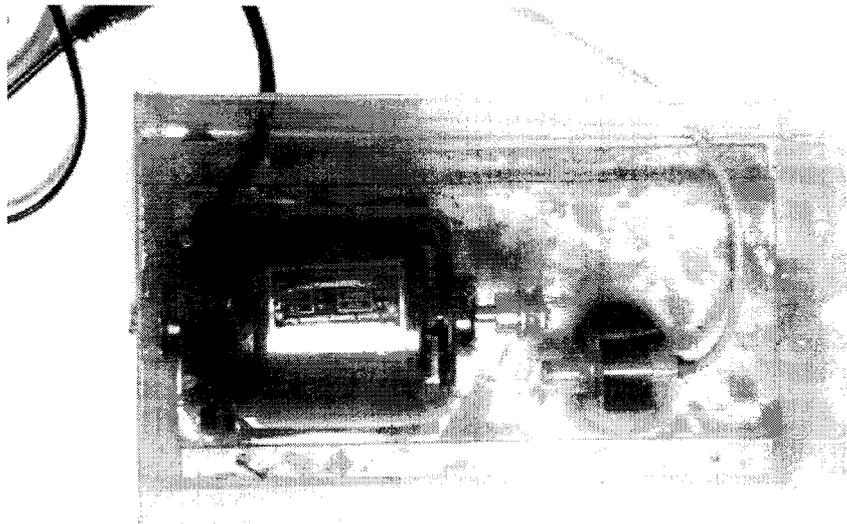
In our circuit, the amplifier is used to amplify the output dc signal from DAC circuit of the micro controller unit. It is an op-amp 741 inverting amplifier. The output of this amplifier is given to the comparator.

COMPARATOR :

A comparator is a circuit, which compares the signals applied at its inputs. In our circuit, op-amp 741 is used as comparator. The ramp signal of the integrator is given to the non-inverting terminal. The dc signal of the amplified form of output of DAC circuit is given to the inverting terminal. This circuit produces rectangular pulses as output.

UNIVERSAL MOTORS

- Fractional-horsepower series motors that are adapted for use on either D.C. or A.C. circuits of a given voltage are called universal motors.
- The universal motor is designed for commercial frequencies from 60 cycles down to D.C.(zero frequency),and for voltage from 250V to 1.5V. A commercial universal motor may have a somewhat weaker series field and more armature conductors than a D.C. series motor of equivalent horsepower. It is manufactured in ratings up to $\frac{3}{4}$ H.P., particularly for sewing machines and vacuum cleaners.
- Like all series motors, the no load speed of the universal motor is universally high.



ADVANTAGES :

- High speed from above 3600r.p.m. to around 25,000 r.p.m.
- High power output.
- High torque at low and intermediate speeds to carry a particularly severe load.
- Variable speed by adjustable governor, by line voltage or specially by modern pulse techniques.

DISADVANTAGES :

- Increased service requirement due to use of brushes and commutators.
- Relatively high noise level at high speeds.
- Moderate to severe radio and television interference due to brush sparking.
- Requirement of careful balancing to avoid vibrations.
- Requirement of reduction gearing in most portable tools.

Software Details

```

#include<reg51.h>
void lcd_dis(unsigned char*,unsigned char);
void lcd_init();
void clock();
void clock1();
void delay1();
sbit rw=P2^1;
sbit rs=P2^0;
sbit en=P2^2;
void dth();
void delay();
void htd();
void display();
void chk_speed();
void nkey_chk();
void del();
void compare();
void disr();
void htdx();
sbit ring=P3^5;
sbit ndata=P3^4;
sbit hs=P3^6;
sbit spul=P3^7;
unsigned char ringcount,i,dtmf,arr[12],cx0,c1,c2,c3,c4,u,x,y,z,j;
unsigned int sp,speed,set_value;
unsigned char idreg,a,c,e,f,g,h,k=0,m=0,reg,mode;
unsigned int ik,b,d;
unsigned char c1x,a1x,b1x,p,cx,e1,g1,h1,m1=0xcc;
main()
{
hs=0;
lcd_init();
P0=0x80;
clock();

```

```

delay1();
lcd_dis("Telephone Operat",16);
P0=0xc0;
clock();
delay1();
lcd_dis("Motor controller",16);
delay1();
ring=1;
ndata=1;
hs=0;
delay();
P1=80;
P2=P0=0;
del();
del();
del();
EA=1;
ET0=1;
TH0=0;
TL0=0;
TMOD=0x01;
TR0=1;
while(1)
{
I1:
    chk_speed();

```

```

    if(ring==1)
    {goto l1;}
l2:
    chk_speed();
    if(ring==0)
    {goto l2;}
    ringcount++;
    disr();
    if(ringcount==5)
    {
        ringcount=0;
        hs=1;
xx:
        chk_speed();
        if(ndata==0)
        {goto xx;}
yy:
        chk_speed();
        if(ndata==1)
        {goto yy;}
        dtmf=P3&0x0f;
        del();
        if(dtmf==0x01)
        {
            TR0=0;
            nkey_chk();
            TR0=1;
goto xx;
        }
        if(dtmf==0x02)
        {
            TR0=1;
            hs=0;
goto l1;

```

```

    }
    goto xx;
}
}
}
void timer0(void) interrupt 1
{
    TR0=0;
    reg++;
    if(reg==0x10)
    {
        reg=0;
        speed=sp*30;
        if(speed>8500)
        {
            speed=8500;
        }
        htd();
        display();
        compare();
        sp=0;
    }
    TH0=0;
    TL0=0;
    TR0=1;
}
void dth()
{
    set_value=(1000*arr[0])+(100*arr[1])+(10*arr[2])
              +(1*arr[3]);
}
void nkey_chk()
{
    P0=0xc0;

```

```

clock();
delay1();
lcd_dis("DTMF CODE: ",12);
P0=m1;
clock();
aa:
if(ndata==0)
{goto aa;}
bb:
if(ndata==1)
{goto bb;}
dtmf=P3&0x0f;
del();
if(dtmf==0x0a)
{dtmf=0x00;}
P0=dtmf+0x30;
clock1();
m1++;
arr[m]=dtmf;
m++;
if(m==4)
{
m1=0xcc;
m=0;
dth();
htdx();
display();
goto cont;
}
goto aa;
cont:
;
}
void chk_speed()

```

```

{
  if(k==0)
  {
    if(spul==0)
    {
      k=1;
      goto retr1;
    }
  }
  if(k==1)
  {
    if(spul==1)
    {
      k=0;
      sp++;
      goto retr1;
    }
  }
retr1:
;
}
void htd()
{
  a=speed/10000;
  b=speed%10000;
  c=b/1000;
  d=b%1000;
  e=d/100;
  f=d%100;
  g=f/10;
  h=f%10;
}
void htdx()
{

```

```

    a=set_value/10000;
    b=set_value%10000;
    c=b/1000;
    d=b%1000;
    e=d/100;
    f=d%100;
    g=f/10;
    h=f%10;
}
void compare()
{
    if(speed>set_value)
    {
        if(P1==0x00)
        {
            P1=0x00;
            goto retr;
        }
        P1--;
    }
    if(speed<set_value)
    {
        if(P1==0xff)
        {
            P1=0xff;
            goto retr;
        }
        P1++;
    }
retr:
;
}
void del()
{

```

```
for(ik=0;ik<=30000;ik++)
{
}
void delay()
{
for(j=0x00;j<=0xfe;j++)
{
}
}
```

```
void display()
{
    P0=0x80;
    clock();
    P0='S';
    clock1();
    P0='P';
    clock1();
    P0='E';
    clock1();
    P0='E';
    clock1();
    P0='D';
    clock1();
    P0=': ';
    clock1();
    P0=a+0x30;
    clock1();
    P0=c+0x30;
    clock1();
    P0=e+0x30;
    clock1();
    P0=g+0x30;
    clock1();
}
```



```

P0=0x45;
clock();
delay1();
}
void clock()
{
rs=0;
rw=0;
en=1;
delay1();
en=0;
delay1();
}
void clock1()
{
rs=1;
rw=0;
en=1;
delay1();
en=0;
delay1();
}
void lcd_dis(unsigned char *mess,unsigned char n)
{
for(i=0;i<n;i++)
{
P0=mess[i];
clock1();
delay1();
}
}
void delay1()
{
for(j=0x00;j<0xfe;j++)

```

```

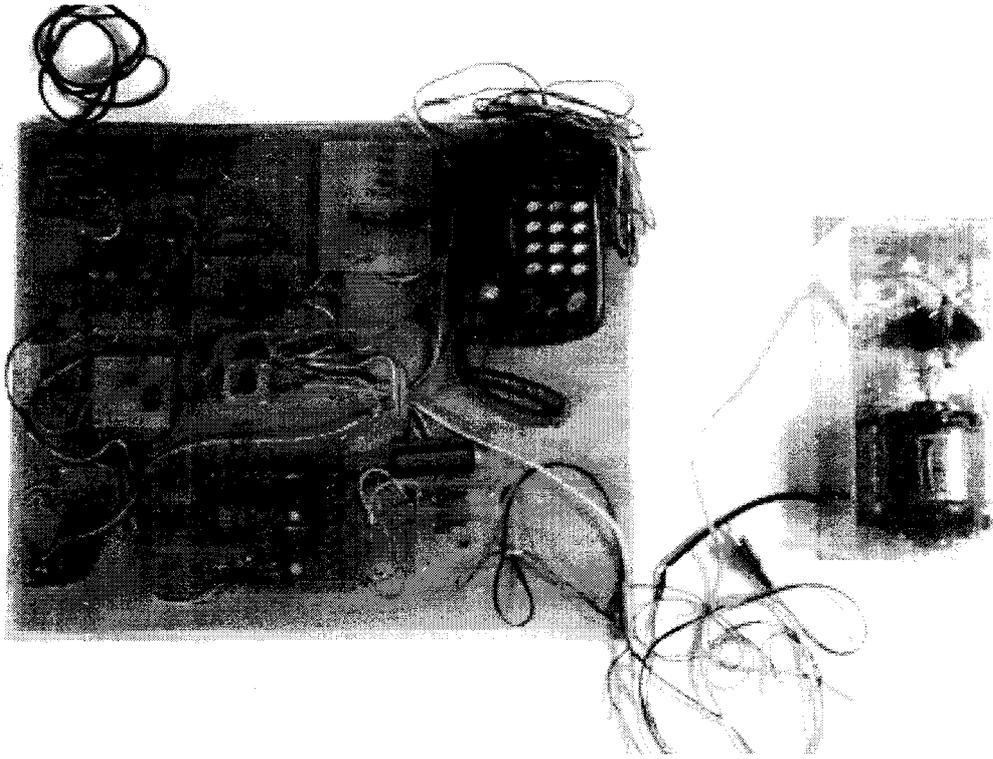
}
}
void disr()
{
P0=0x80;
clock();
P0='R';
clock1();
P0='i';
clock1();
P0='n';
clock1();
P0='g';
clock1();
P0=' ';
clock1();
P0='C';
clock1();
P0='o';
clock1();
P0='u';
clock1();
P0='n';
clock1();
P0='t';
clock1();
P0=': ';
clock1();
P0=ringcount+0x30;
clock1();
P0=' ';
clock1();
P0=' ';
clock1();
}

```

```
P0=' ';  
clock1();  
P0=' ';  
clock1();  
P0=' ';  
clock1();  
P0=' ';  
clock1();  
}
```

Project Module

PROJECT MODULE



Conclusion

CONCLUSION

Explaining the concept of control of motor using telecommunication and having tested the same we have successfully completed the project. Although we have not dealt in detail with the various methods of speed control, we have covered the phenomenon in the best possible manner.

The difficulties that we experienced were “sensitivity” or rather difficulty in obtaining exact values of speed due to incoming voltage fluctuation and also instances of power failure. In the further expansion of the project it could be dealt to a greater nuance and obtained in a more precise manner.

Living in a world as ours where speed and ever increasing sophistication in control of equipments is advancing at a tremendous this project is definitely a break through in the field of speed control.

This project would serve its purpose where machines are placed at inaccessible heights or extreme conditions. Apart from this it would find tremendous application in day to day gadgets too.

APPENDIX

TECHNICAL SPECIFICATIONS OF SCR:

Incoming supply	:	230v AC, single phase, 50Hz
Supply current	:	maximum 16A
Maximum temperature	:	80 degrees
Control section firing angle	:	10 to 180 degrees
Fuse rating (for control section)	:	1A

Features

- Compatible with MCS-51™ Products
- 4K Bytes of In-System Reprogrammable Flash Memory
 - Endurance: 1,000 Write/Erase Cycles
- Fully Static Operation: 0 Hz to 24 MHz
- Three-level Program Memory Lock
- 128 x 8-bit Internal RAM
- 32 Programmable I/O Lines
- Two 16-bit Timer/Counters
- Six Interrupt Sources
- Programmable Serial Channel
- Low-power Idle and Power-down Modes

Description

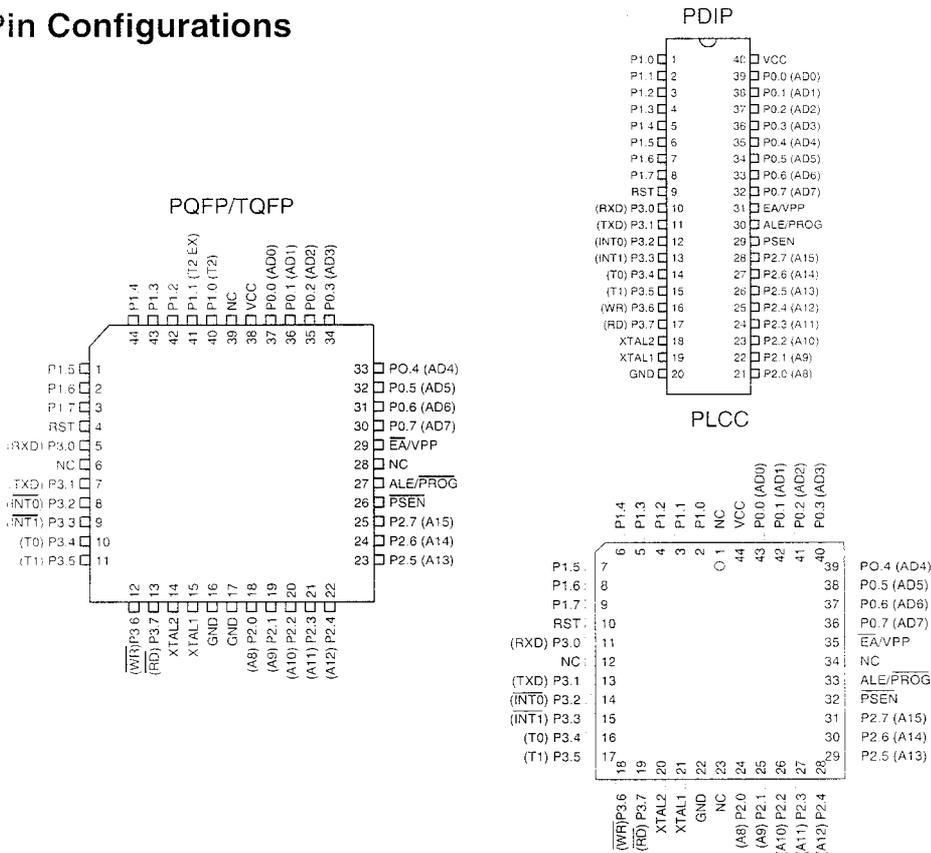
The AT89C51 is a low-power, high-performance CMOS 8-bit microcomputer with 4K bytes of Flash programmable and erasable read only memory (PEROM). The device is manufactured using Atmel's high-density nonvolatile memory technology and is compatible with the industry-standard MCS-51 instruction set and pinout. The on-chip Flash allows the program memory to be reprogrammed in-system or by a conventional nonvolatile memory programmer. By combining a versatile 8-bit CPU with Flash on a monolithic chip, the Atmel AT89C51 is a powerful microcomputer which provides a highly-flexible and cost-effective solution to many embedded control applications.

Pin Configurations



8-bit Microcontroller with 4K Bytes Flash

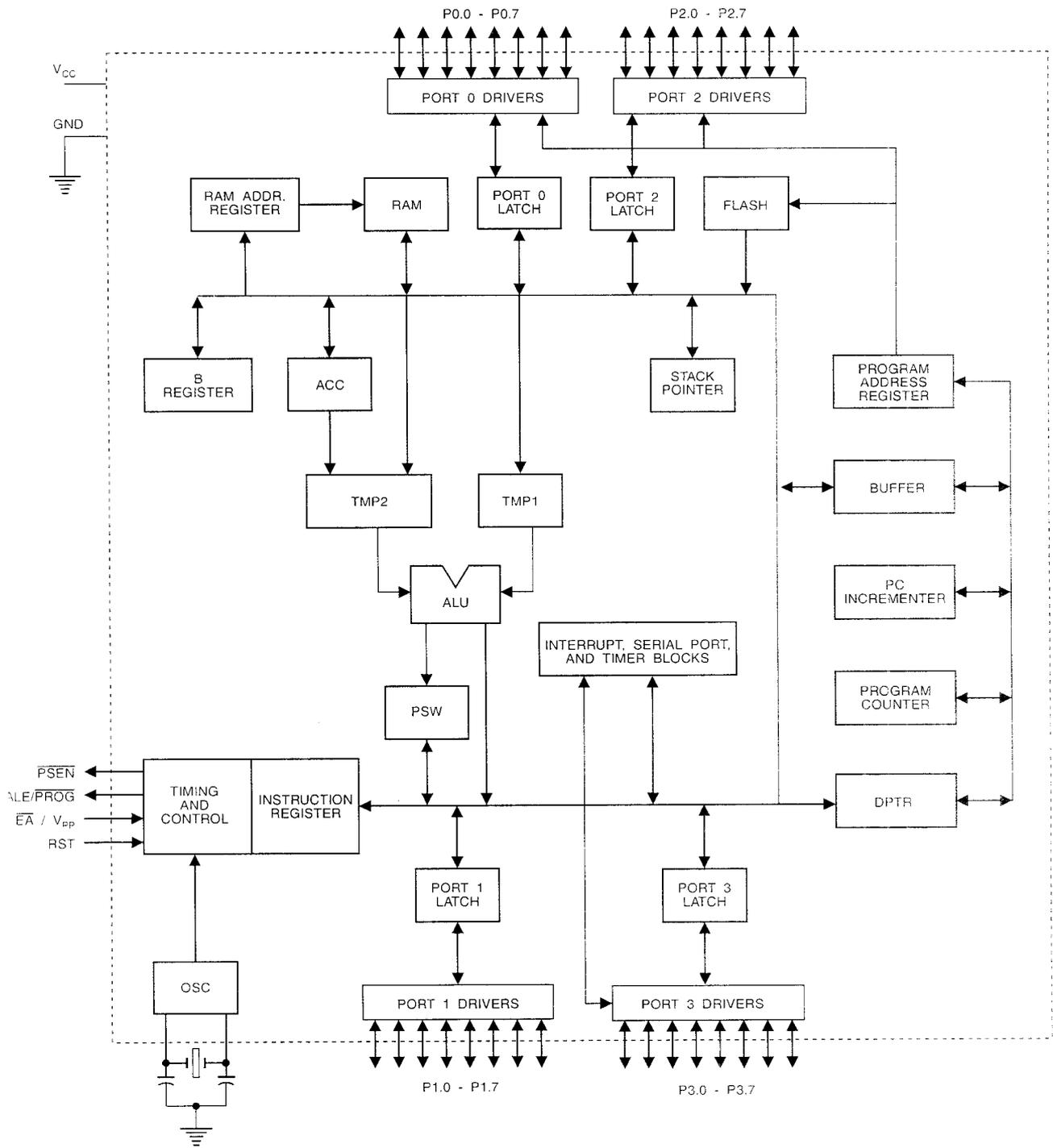
AT89C51



Rev. 0265G-02/00



Block Diagram



DAC0800/DAC0802 8-Bit Digital-to-Analog Converters

General Description

The DAC0800 series are monolithic 8-bit high-speed current-output digital-to-analog converters (DAC) featuring typical settling times of 100 ns. When used as a multiplying DAC, monotonic performance over a 40 to 1 reference current range is possible. The DAC0800 series also features high compliance complementary current outputs to allow differential output voltages of 20 V_{p-p} with simple resistor loads as shown in Figure 1. The reference-to-full-scale current matching of better than ±1 LSB eliminates the need for full-scale trims in most applications while the nonlinearities of better than ±0.1% over temperature minimizes system error accumulations.

The noise immune inputs of the DAC0800 series will accept TTL levels with the logic threshold pin, V_{LC}, grounded. Changing the V_{LC} potential will allow direct interface to other logic families. The performance and characteristics of the device are essentially unchanged over the full ±4.5V to ±18V power supply range; power dissipation is only 33 mW with ±5V supplies and is independent of the logic input states.

The DAC0800, DAC0802, DAC0800C and DAC0802C are a direct replacement for the DAC-08, DAC-08A, DAC-38C, and DAC-08H, respectively.

Features

- Fast settling output current: 100 ns
- Full scale error: ±1 LSB
- Nonlinearity over temperature: ±0.1%
- Full scale current drift: ±10 ppm/°C
- High output compliance: -10V to +18V
- Complementary current outputs
- Interface directly with TTL, CMOS, PMOS and others
- 2 quadrant wide range multiplying capability
- Wide power supply range: ±4.5V to ±18V
- Low power consumption: 33 mW at ±5V
- Low cost

Typical Applications

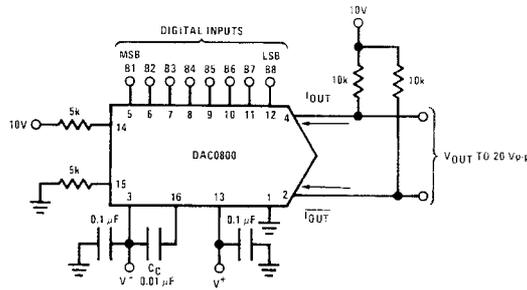


FIGURE 1. ±20 V_{p-p} Output Digital-to-Analog Converter (Note 5)

Ordering Information

Non-Linearity	Temperature Range	Order Numbers				
		J Package (J16A) (Note 1)	N Package (N16E) (Note 1)	SO Package (M16A)		
±0.1% FS	0°C ≤ T _A ≤ +70°C	DAC0802LCJ	DAC-08HQ	DAC0802LCN	DAC-08HP	DAC0802LCM
±0.19% FS	-55°C ≤ T _A ≤ +125°C	DAC0800LJ	DAC-08Q			
±0.19% FS	0°C ≤ T _A ≤ +70°C	DAC0800LCJ	DAC-08EQ	DAC0800LCN	DAC-08EP	DAC0800LCM

Note 1: Devices may be ordered by using either order number.

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V^+ - V^-$)	$\pm 18V$ or $36V$
Power Dissipation (Note 3)	500 mW
Reference Input Differential Voltage (V14 to V15)	V^- to V^+
Reference Input Common-Mode Range (V14, V15)	V^- to V^+
Reference Input Current	5 mA
Logic Inputs	V^- to V^+ plus $36V$
Analogue Current Outputs ($V_S = -15V$)	4.25 mA
ESD Susceptibility (Note 4)	TBD V

Storage Temperature	-65 C to +150 C
Lead Temp. (Soldering, 10 seconds)	
Dual-In-Line Package (plastic)	260 C
Dual-In-Line Package (ceramic)	300 C
Surface Mount Package	
Vapor Phase (60 seconds)	215 C
Infrared (15 seconds)	220 C

Operating Conditions (Note 2)

	Min	Max	Units
Temperature (T_A)			
DAC0800L	-55	+125	C
DAC0800LC	0	+70	C
DAC0802LC	0	+70	C

Electrical Characteristics

The following specifications apply for $V_S = \pm 15V$, $I_{REF} = 2$ mA and $T_{MIN} \leq T_A \leq T_{MAX}$ unless otherwise specified. Output characteristics refer to both I_{OUT+} and I_{OUT-} .

Symbol	Parameter	Conditions	DAC0802LC			DAC0800L/ DAC0800LC			Units
			Min	Typ	Max	Min	Typ	Max	
	Resolution		8	8	8	8	8	8	Bits
	Monotonicity		8	8	8	8	8	8	Bits
	Nonlinearity				± 0.1			± 0.18	%FS
t_s	Settling Time	To $\pm 1/2$ LSB, All Bits Switched "ON" or "OFF", $T_A = 25^\circ C$		100	135				ns
		DAC0800L				100	135		ns
		DAC0800LC				100	150		ns
t_{PLH} , t_{PHL}	Propagation Delay Each Bit All Bits Switched	$T_A = 25^\circ C$		35	60		35	60	ns
				35	60		35	60	ns
TCI_{FS}	Full Scale Tempco			± 10	± 50		± 10	± 50	ppm/C
V_{OC}	Output Voltage Compliance	Full Scale Current Change $< 1/2$ LSB, $R_{OUT} > 20$ M Ω Typ	-10		18	-10		18	V
I_{FS1}	Full Scale Current	$V_{REF} = 10.000V$, $R14 = 5.000$ k Ω $R15 = 5.000$ k Ω , $T_A = 25^\circ C$	1.984	1.992	2.000	1.94	1.99	2.04	mA
I_{FS3}	Full Scale Symmetry	$I_{FS4} - I_{FS2}$		± 0.5	± 4.0		± 1	± 8.0	μA
I_{ZS}	Zero Scale Current			0.1	1.0		0.2	2.0	μA
I_{FS1+}	Output Current Range	$V^- = -5V$ $V^- = -8V$ to $-18V$	0	2.0	2.1	0	2.0	2.1	mA
			0	2.0	4.2	0	2.0	4.2	mA
V_{IL}	Logic Input Levels Logic "0"	$V_{LC} = 0V$			0.8			0.8	V
V_{IH}	Logic "1"		2.0			2.0			V
I_{IL}	Logic Input Current Logic "0"	$V_{LC} = 0V$ $-10V \leq V_{IN} \leq +0.8V$		-2.0	-10		-2.0	-10	μA
I_{IH}	Logic "1"	$2V \leq V_{IN} \leq +18V$		0.002	10		0.002	10	μA
V_{IS}	Logic Input Swing	$V^- = -15V$	-10		18	-10		18	V
V_{THR}	Logic Threshold Range	$V_S = \pm 15V$	-10		13.5	-10		13.5	V
I_{IS}	Reference Bias Current			-1.0	-3.0		-1.0	-3.0	μA
dI/dt	Reference Input Slew Rate	(Figure 11)	4.0	8.0		4.0	8.0		mA/ μs
$PSS_{I_{FS+}}$	Power Supply Sensitivity	$4.5V \leq V^+ \leq 18V$		0.0001	0.01		0.0001	0.01	%/%
$PSS_{I_{FS-}}$		$-4.5V \leq V^- \leq -18V$		0.0001	0.01		0.0001	0.01	%/%
		$I_{REF} = 1$ mA							

Electrical Characteristics (Continued)

The following specifications apply for $V_S = \pm 15V$, $I_{REF} = 2\text{ mA}$ and $T_{MIN} \leq T_A \leq T_{MAX}$ unless otherwise specified. Output characteristics refer to both I_{OUT} and I_{OUT} .

Symbol	Parameter	Conditions	DAC0802LC			DAC0800L/ DAC0800LC			Units
			Min	Typ	Max	Min	Typ	Max	
I ⁺ I ⁻	Power Supply Current	$V_S = \pm 5V$, $I_{REF} = 1\text{ mA}$		2.3	3.8		2.3	3.8	mA
				-4.3	-5.8		-4.3	-5.8	mA
		$V_S = 5V$, $-15V$, $I_{REF} = 2\text{ mA}$		2.4	3.8		2.4	3.8	mA
				-6.4	-7.8		-6.4	-7.8	mA
I ⁺ I ⁻	Power Supply Current	$V_S = \pm 15V$, $I_{REF} = 2\text{ mA}$		2.5	3.8		2.5	3.8	mA
				-6.5	-7.8		-6.5	-7.8	mA
P _D	Power Dissipation	$\pm 5V$, $I_{REF} = 1\text{ mA}$		33	48		33	48	mW
		$5V$, $-15V$, $I_{REF} = 2\text{ mA}$		108	136		108	136	mW
		$\pm 15V$, $I_{REF} = 2\text{ mA}$		135	174		135	174	mW

Note 2: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

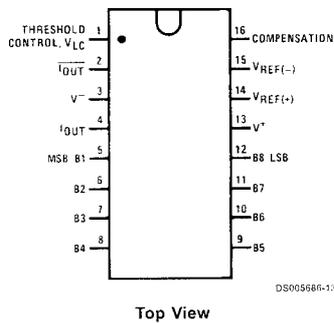
Note 3: The maximum junction temperature of the DAC0800 and DAC0802 is 125°C. For operating at elevated temperatures, devices in the Dual-In-Line J package must be derated based on a thermal resistance of 100°C/W, junction-to-ambient, 175°C/W for the molded Dual-In-Line N package and 100°C/W for the Small Outline M package.

Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 5: Pin-out numbers for the DAC080X represent the Dual-In-Line package. The Small Outline package pin-out differs from the Dual-In-Line package.

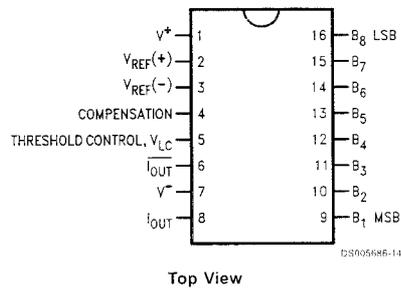
Connection Diagrams

Dual-In-Line Package



Top View

Small Outline Package



Top View

See Ordering Information

Bibliography

BIBLIOGRAPHY

REFERENCE :

- Linear Integrated Circuits - D.ROY CHOUDHURY &SHAIL JAIN.
- Electric Machines I&II - J.B.GUPTA
- Electric Machines - RAJPUT.R.K.
- Electric drives - VEDAM SUBRAMANIAM
- www.fairchildsemi.com
- www.eu.atmel.com
- www.microchip.com