Processor Controlled Command Recognizer

Project Report

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Under the Guidance of

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Certificate

This is to certify that the Report entitled

Processor Controlled Command Recognizer

has been submitted by

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In partial fulfilment for the award of Bachelor of Engineering in Electronics and Communication Engineering Branch of Bharathiar University, Coimbatore-641 046 during the academic year 1991-92.

Guide

Head of the Department

Certified that the candidate was Examined by us in the project work Viva-voce Examination held on .... and the University Register Number was ....

Internal Examiner

External Examiner

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Last but not the least we thank our Lab technicians for their valuable help rendered to us.

SYNOPSIS

The processor controlled command recognizer (PCCR), is likely to be used much more often in situations where a person's hands are busy, where a worker's eyes must remain fixed ona display or a measuring instrument.

This system is based on the idea that the number of times the audio signal cro sses a particular level in unit time can be a measure of repetitiveness.

In PCCR, a microphone is used to convert human speech into electrical signals, the signal patterns are then transmitted to the processor where they are compared to a dictionary of patterns that have been previously placed in the storage. When a closed match is found, the word is recognized and the processor then produces the appropriate output.

INTRODUCTION

1.1. Speech production:

In normal speech production, the chest cavity expands and contracts to force air from the lungs out through the trachea past the glottis.

If the vocal cords are tensed, as for voiced sounds like vowels, they will vibrate in the mode of a relaxation oscillator, modulating the air into discrete puffs or pulses. If the cords are spread apart, the air stream passes through the glottis and is unaffected. The air stream passes through the pharynx cavity, past the tongue and depending on the position of the trap door velum, through the mouth and/or nasal cavity.

The air stream is explelled at either the mouth or nose, or both, and is perceived as speech. In the case of unvoiced sounds like 's' as in snow or 'p' as in pit, the vocal cords are spread apart (no voicing) and one of two conditions prevails. Either a turbulent flow is produced as the air passes a narrow constriction in the vocal trait (as is s) or a brief transient exitation occurs following a build up of pressure behind a point of total closure along the tract (as in p). As the various articulators (example lips, tongue, jaw, velum) change position during continuous speech, the shapes of the

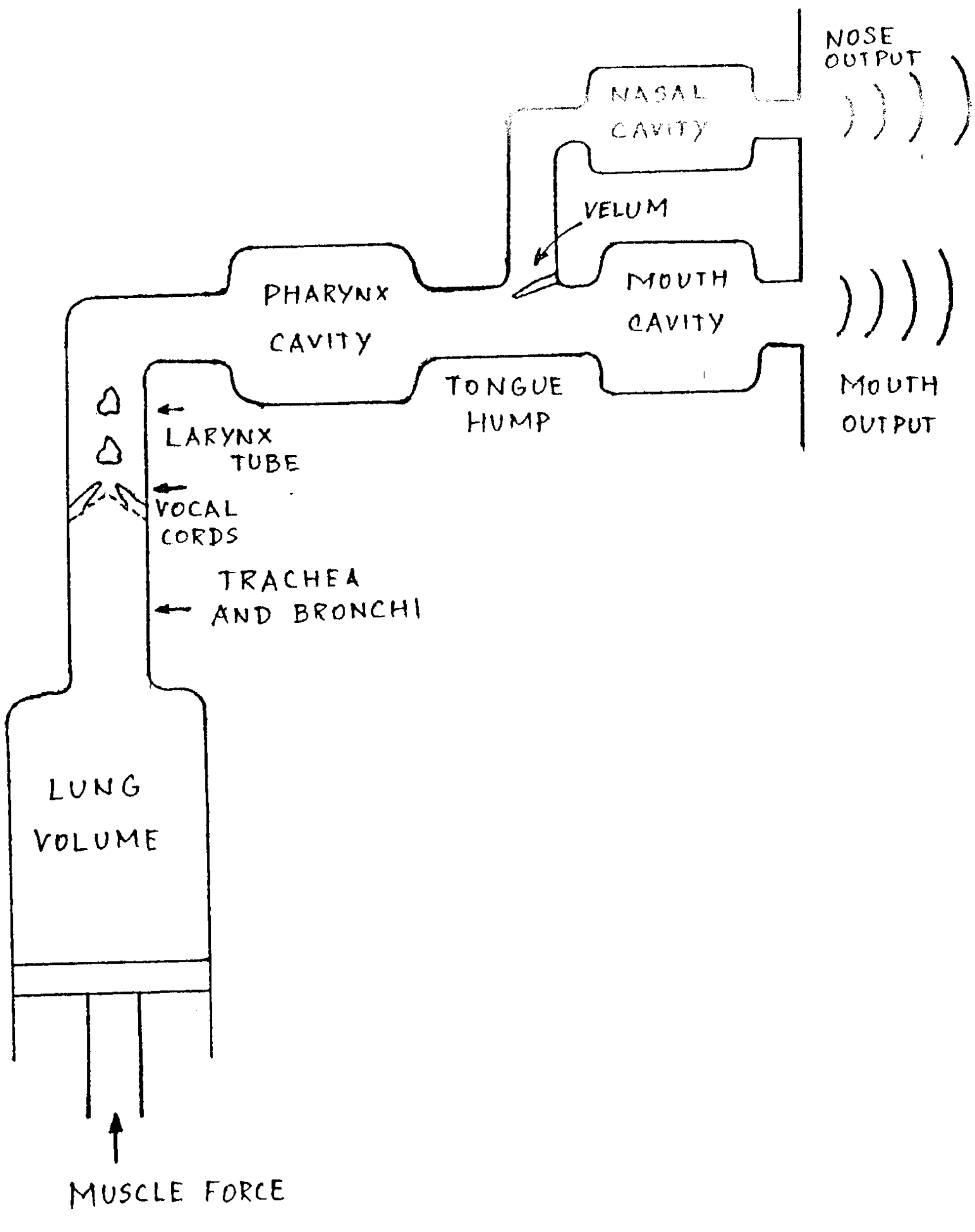


Fig. 1.1. SCHEMATIC DIAGRAM OF THE HUMAN SPEECH PRODUCTION MECHANISM

various cavities change drastically.

1.2. Voice recognition:

Basically the voice recognizer is of two types,

i) User dependent

ii) User independent

In the first system, recognition is achieved by comparing speech patterns of a person with his/her patterns stored previously. It is extremely important that the present speech is identical to the one stored initially to serve as a reference. It means that conditions such as stress in the voice and back ground noise and greately offset both accuracy & reliability.

Speaker independent system donot require speech patterns of the user to serve as a reference. Instead, speech is compared to the same reference speech patterns irrespective of the user. The reference speech patterns is made by using speech created by large groups of people saying the same word.

The recognizer converts speech to data which is stored in memory for later use. The set of data patterns created for one speaker is known as template.

Our project PCCR is strictly confined to user dependent system, that is it can be used by speaker only ofter training the recongnizer with his/her particular voice patterns.

PCCR should be operated in two modes

i) Learn mode

ii) Processing mode.

1.2.1. Learn mode:

In the learn mode the software is used to first train the unit. To do this the operator says the first desired word, the program samples the word and the digital information is stored in a memory location this creates a TEMPLATE for the desired word.

1.2.2. Processing word:

In the recognition mode the spoken word is converted into digital information and this value for the spoken word are compared with the template stored in the memory, and the best match is assumed to be the correct word. Each word can direct of processor to perform a disired operation such as turning on lights, opening the door etc.....

2. SYSTEM AND ITS OPERATION

2.1. Operating Principle:

The operation is mainly based on the idea that the number of times the audio signal crosses a particular level in unit time can be measure of repetitiveness.

The voice signals which are amplified by a low noise amplifier are fed to a zero crossing detector. The zero crossing detector converts the analog signals into a square wave output, which is then perfectly shaped by the pulse shaping circuit. The output thus obtained is the digital information required for processing purpose.

Counting Process:

The counting of the output pulses from pulse shaping circuit is done by using the programmable interval timer /counter 8253.

Initially a value is set in the counter and whenever a counter get enabled it starts, decrementing from the stored value. The counter gets enabled for a fixed interval of time whenever a word is spoken. The software then retrieves the decremented value from the counter and then subtracts from the initial set value of the counter, this gives the exact number of pulses generated for a particular command.

Creation of template:

A software routine is used to store the number of pulses for the particular word in a memory location which is the required template for that desired word. These templates are created in the learn mode operation.

Recognition of the word:

Recognition is done in the processing mode of operation. In this mode, the speech command is converted to a data pattern in much the same way as described above. However this time the processor matches the present patterns with those stored, to find the closest match.

PROCESSOR CONTROLLED COMMAND RECOGNISER

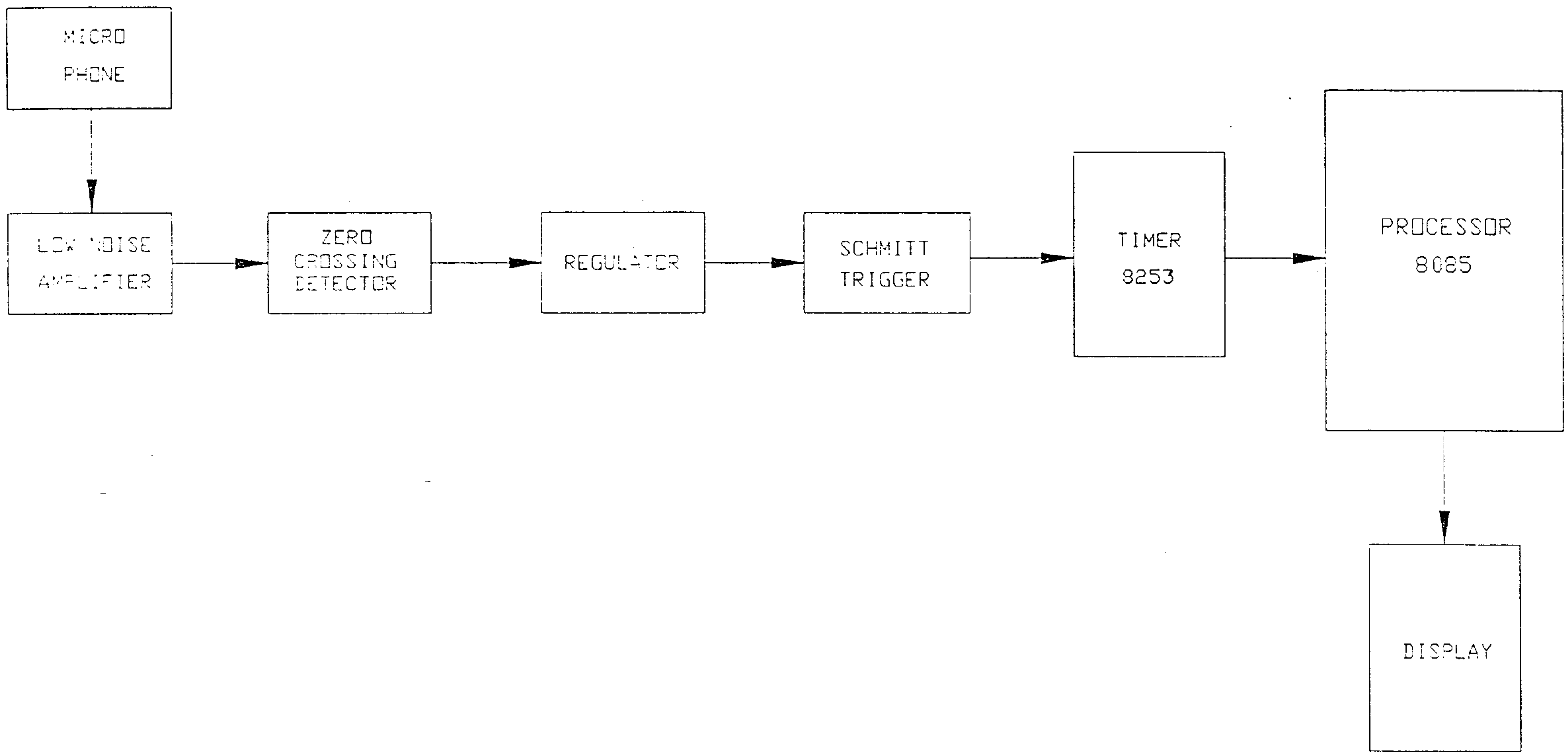


FIG : 2.2 BLOCK DIAGRAM

2.2. Block Diagram:

The block diagram of PCCR is presented in fig 2.2

2.2.1. Explanation:

PCCR is developed on the basis of the following blocks,

The blocks are,

- Microphone
- Low noise amplifier
- Zero crossing detector
- Clipper
- Regulator
- Pulse shaping circuit.

Microphone:

Microphone is a device that converts variation is sound pressure (sound waves) into correlated electrical currents (or) voltages i.e sound wave to electrical wave transducer.

Microphones serves two principle purposes. First they are used for converting music or speech into electrical signals which are transmistted (or) processed in some manner, and then reproduced. Second, they serve as measuring instruments, converting acoustic signals in to electrical signals which actuate indicating meters.

Depending upon the nature of the operational force obtained from sound pressure to drive diaphragm, microphones are pressure-operated, pressure-gradient, or phase-shift operated. This determines whether the microphone will accept or discriminate against sounds from a particular direction.

Microphone used in the circuit is a condenser microphone with a sensitivity of 5.5mv/pa in the voice prequency range.

Sensitivity or open circuit voltage response of microphone is the voltage output for a sound pressure input of one microbar i.e. 74db re 0.0002 microbar.

MICROPHONE SPECIFICATIONS

Type	=	Omni directional Electret
Frequency range	=	100 - 1500hz
Sensitivity	=	5.5mv/pa
Impedance	=	500 ohms (Lo-z)
Cable	=	6mtrs.
Battery	=	1.5v

Low noise amplifier:

LM 381 is used for the amplification of low level signals. It is a low noise dual preamplifier. Each of the two amplifiers is completely independent, with individual internal power supply decoupler - regulator, providing 120dB supply rejection and 60dB channel seperation.

The amplifier is designed for a gain of 60dB in the voice frequency range. This amplified voice signals are then fed to a zero crossing detector.

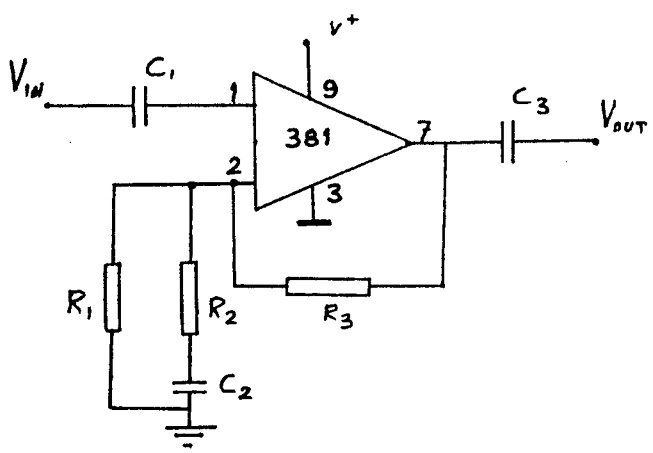


Fig. 2.3. LOW NOISE AMPLIFIER

$R_1 = 9.6\,k\Omega$

$R_2 = 40\,\Omega$

$R_3 = 40\,k\Omega$

$C_1 = 0.01\,\mu f$

$C_2 = 100\,\mu f$

$C_3 = 0.01\,\mu f$

Zero crossing detector:

The zero crossing detector is nothing but a comparator with zero reference voltage. The circuit is constructed using dual op-amp IC358. This IC has a typical application of operating with a positive bias alone.

The diodes D1, & D2 are clamping diodes. These are placed inverse-parallel across the input terminals of the comparator to limit the difference input voltage V_{id} to approximately ± 0.7V. This helps prevent possible damage to the amplifier.

Because of the extremely high A_{oc}, this input voltage range is more than adequate to drive the output into saturation.

Ressistor R_1, serves as a current limiter, preventing the input voltage source from being damaged when either of the diodes goes into conduction.

Ressistor R_2 is used to help null out biascurrent induced offset voltage & is made = R_1. Due to the slewrate problems, the output of this fed to a pulse shaping circuit to get a perfect shape of the pulses.

Clippers:

Clippers are also known as limiters, amplitude selector (or) slicers. Clippers have the ability to "clip" off a portion of the input signals without distorting the ramaining part of the alternating wave form.

Clippers are used to select for transmission a part of an arbitrary waveform which lies above (or) below same particular reference level.

Depending on the orientation of the diode the positive or negative region is "Clipped" off. In our circuit shunt clipper is used to clip off the negative alternation in the waveform.

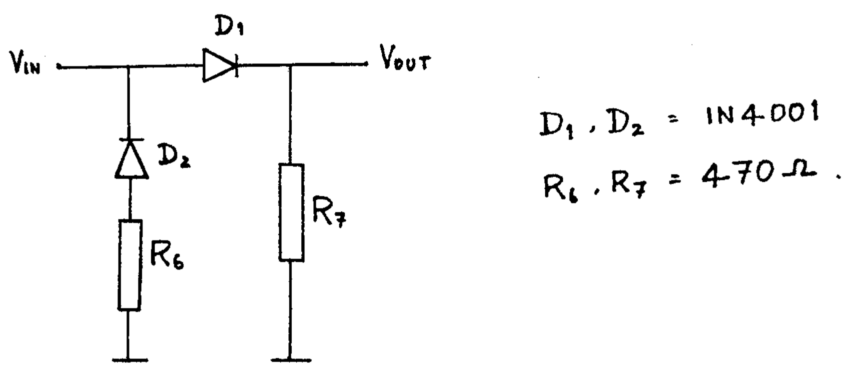


Fig. 2.4 CLIPPER

Regulator:

A regulator is used to reduce the output level to 5V which is compatible for microprocessor operation..

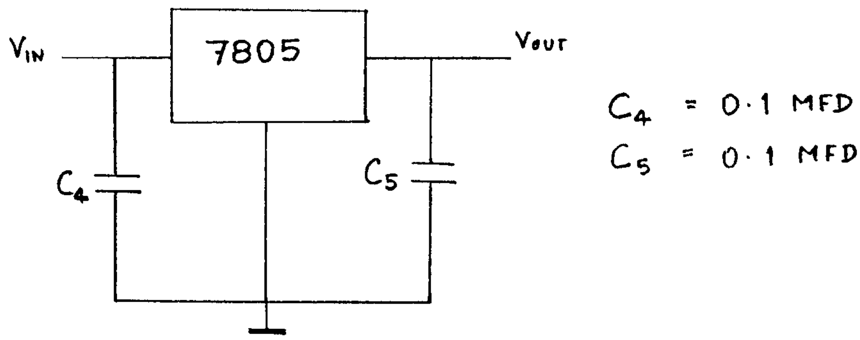


Fig.2,5 REGULATOR

ZERO CROSSING DETECTOR

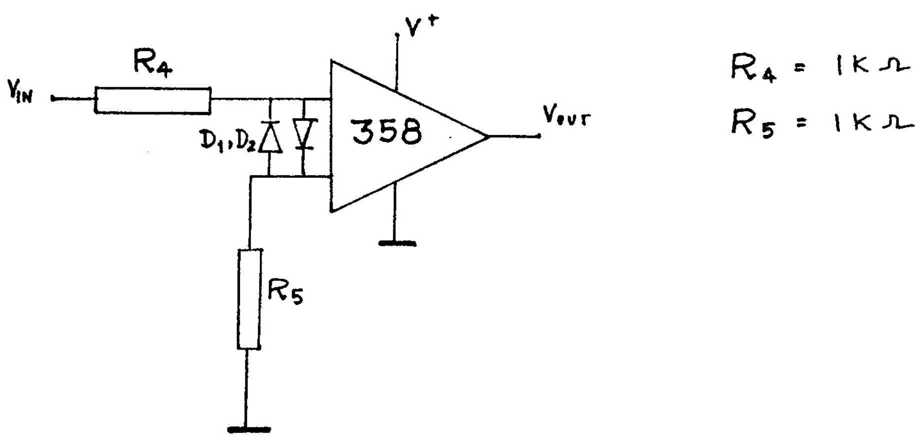


Fig.2.6. ZERO CROSSING DETECTOR

Schmitt trigger:

Pulse shaping circuit:

The pulse shaping circuit used here is a schmitt trigger. The clipped waveform from the clipper is fed to a schmitt NAND gate connected in the invertor mode.

IC 74LS 132: is used for this purpose. It is a quad dual input schmitt NAND gate. The characteristics of 74132 is described in the hardware details section.

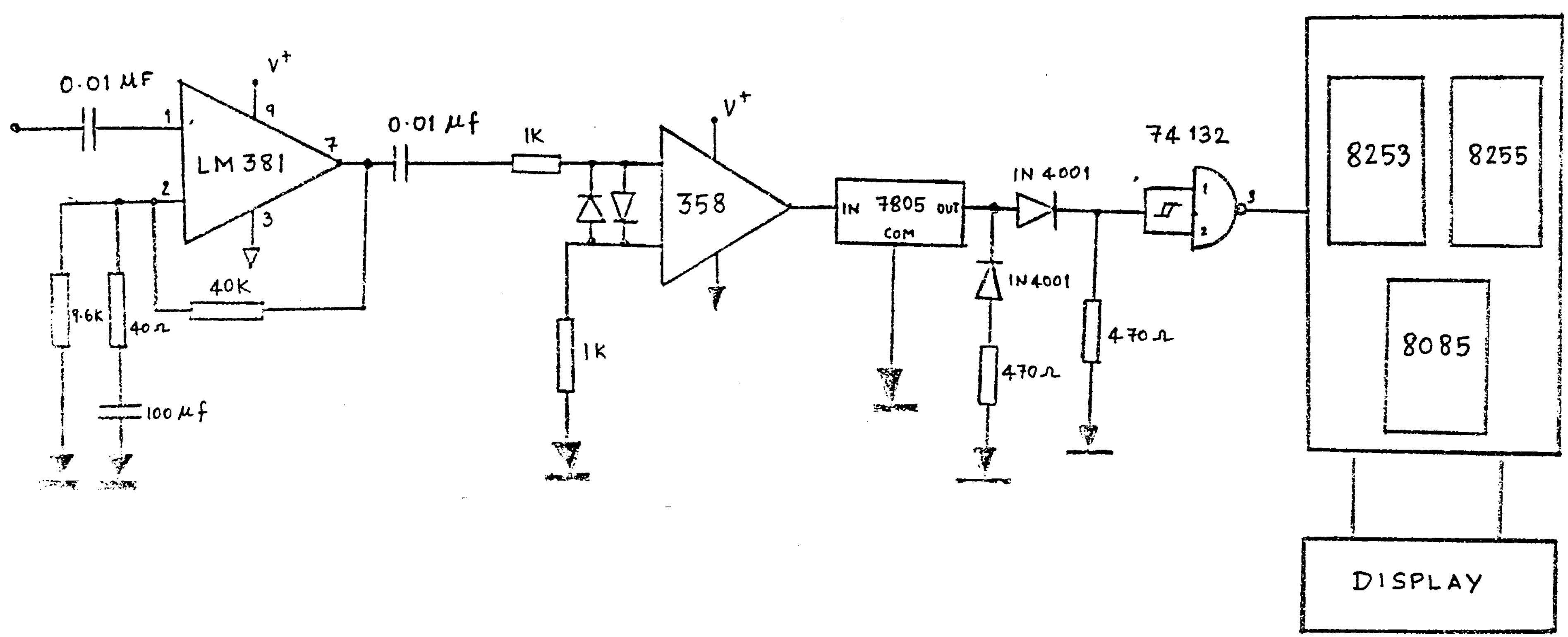


Fig.3.1. CIRCUIT DIAGRAM OF PCCR

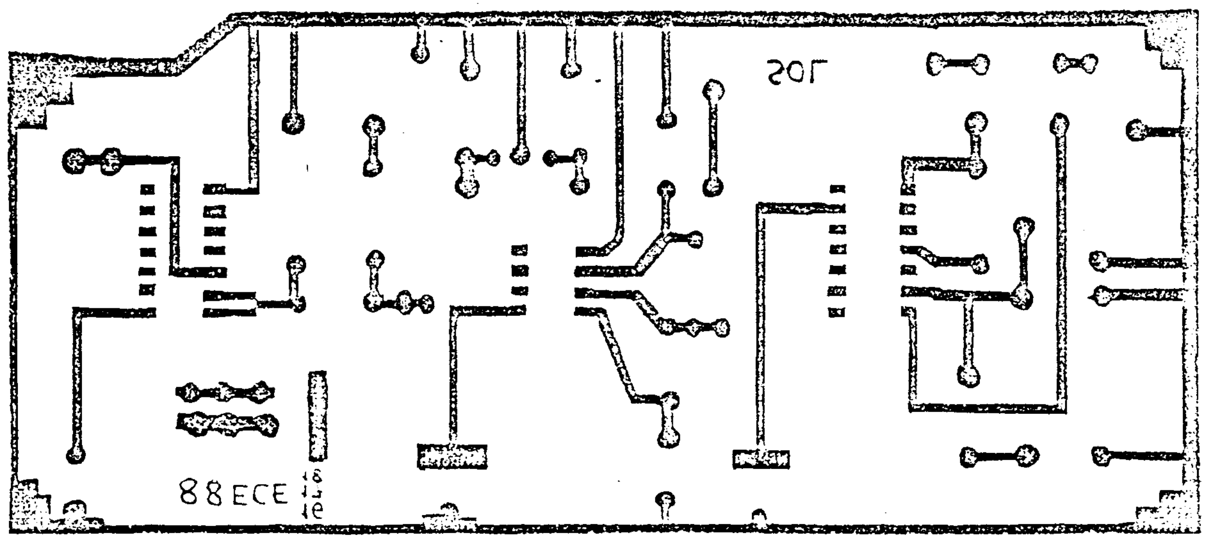
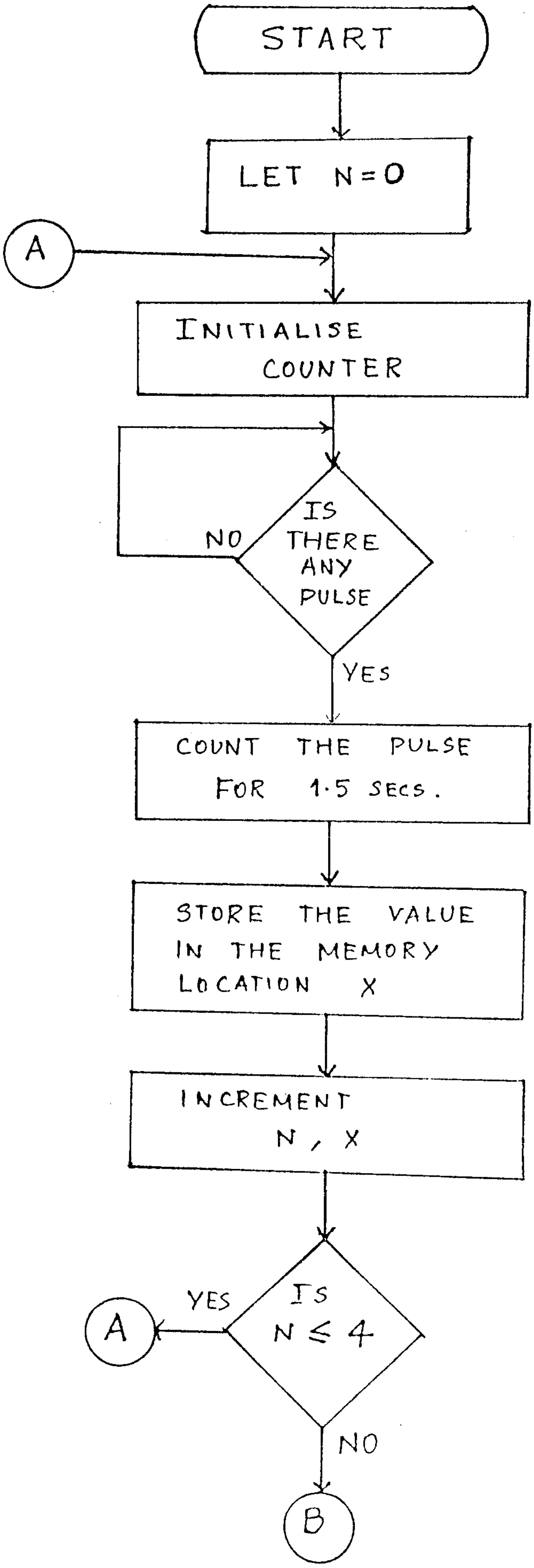
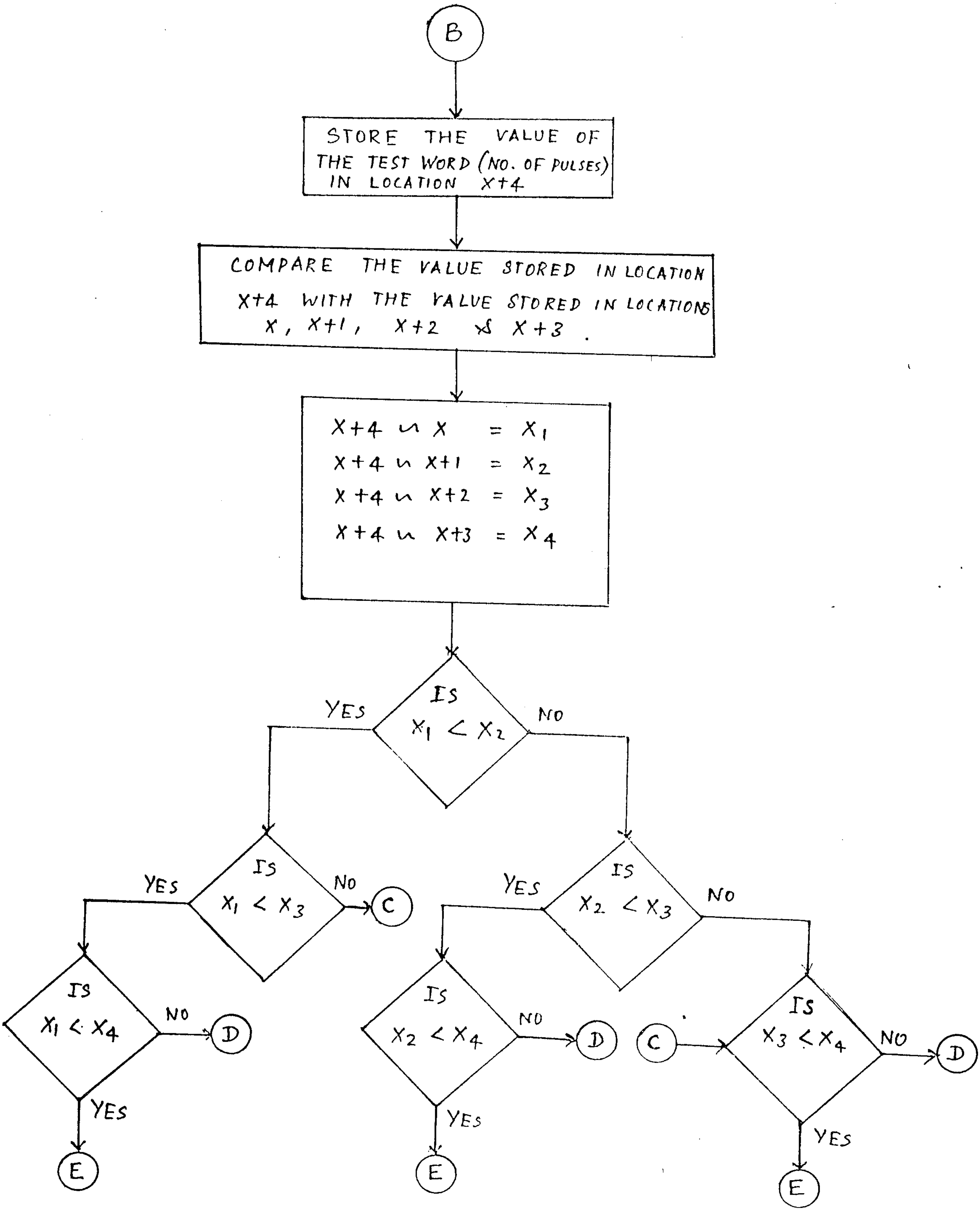


Fig.3.2. PCB LAYOUT OF VOICE DIGITIZER


START
LET N=0
A
INITIALISE COUNTER
IS THERE ANY PULSE
NO
YES
COUNT THE PULSE FOR 1·5 SECS.
STORE THE VALUE IN THE MEMORY LOCATION X
INCREMENT N, X
IS N ≤ 4
YES
A
NO
B


B
STORE THE VALUE OF THE TEST WORD (NO. OF PULSES) IN LOCATION X+4
COMPARE THE VALUE STORED IN LOCATION X+4 WITH THE VALUE STORED IN LOCATIONS X, X+1, X+2 & X+3.
X+4 ~ X = X1
X+4 ~ X+1 = X2
X+4 ~ X+2 = X3
X+4 ~ X+3 = X4
IS X1 < X2
YES
NO
IS X1 < X3
YES
NO
C
IS X2 < X3
YES
NO
IS X1 < X4
NO
D
YES
E
IS X2 < X4
NO
D
YES
E
C
IS X3 < X4
NO
D
YES
E

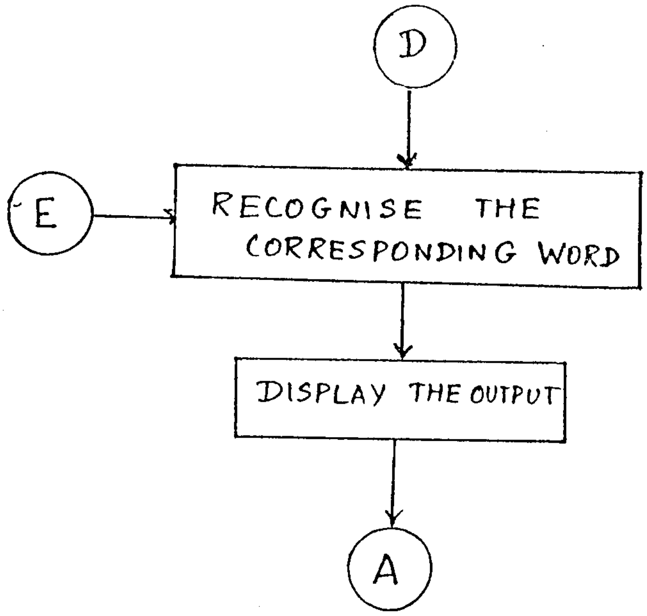


Fig.4.1. FLOW CHART FOR PCCR

4.2. PROGRAM LISTING

ADDRESS	LABEL	MNEMONIC	OPCODE	OPERAND
8000		LXI SP 9F00	31	00 9F
8003		LXIB 8500	01	00 85
8006		MVI H 05	26	05
8008		MVI A, BO	3E	BO
800A		OUT 13	D3	13
800C	loop-0	MVI A, EE	3E	EE
800E		OUT 12	D3	12
8010		MVI A, EE	3E	EE
8012		OUT 12	D3	12
8014	loop-1	MVI A, 80	3E	80
8016		OUT 13	D3	13
8018		IN 12	DB	12
801A		MOV E,A	5F	
801B		SUI E9	D6	E9
801D		JNC loop-1	D2	14, 80
8020		CALL DELAY	CD	50 81
8023		MVI A, 80	3E	80
8025		OUT 13	D3	13
8027		IN 12	DB	12
8029		MOV E,A	5F	
802A		IN 12	DB	12
802C		MOV D,A	57	
802D		MVI A,EE	3E	EE
802F		SUB E	93	
8030		STAX B	02	
8031		MVI A,EE	3E	EE
8033		SBB D	9A	

ADDRESS	LABEL	MNEMONIC	OPCODE	OPERAND
8034		INX B	03	
8034		STAX B	02	
8036		INX B	03	
8037		DCR H	25	
8038		JNZloop -0	C2	0C, 80

COMPARISION:

803B		LXIB 9000	01	00 90
803E		MVI D, 04	16	04
8040		LXIH 8500	21	00 85
8043	loop-3	PUSH D	D%	
8044		MOV E, M	5E	
8045		INX H	23	
8046		MOV D,M	56	
8047		PUSH H	E5	
8048		LHLD 8508	2A	08 85
804B		LDA 8509	3A	09 85
804E		SUB D	92	
804F		JC loop-3	DA	5A 80
8052		JNZ loop-4	C2	5B 80
8055		LDA 8508	3A	08 85
8056		SUB E	93	
8057		JNC loop-4	D2	5B 80
80 5A	loop-3	XCHG	EB	

ADDRESS	LABEL	MNEMONIC	OPCODE	OPERAND
805B	loop-4	MOV A,L	7D	
805C		SUB E	93	
805D		STAX B	02	
805E		MOV A,H	7C	
805F		SBB D	9A	
8060		INX B	03	
8061		STAX B	02	
8062		POP H	E1	
8063		INX H	23	
8064		INX B	03	
8065		POP D	D1	
8066		DCR D	15	
8067		JNZ loop-2	C2	43, 80

RECOGNITION:

806A		MVI B,01	06	01
806C		MVI C, 01	0E	01
806E		LXIH 9000	21	00 90
8070		MOV E, M	5E	
8071		INX H	23	
8072		MOV D, M	56	
8073	loop-5	INX H	23	
8074		INR C	0C	
8075		MOV A,C	79	
8076		CPI 05	FE	

ADDRESS	LABEL	MNEMONIC	OPCODE	OPERAND
8077		JZ loop-6	CA	8E 80
807A		MOV A, M	7E	
807B		SUB E	93	
807C		INX H	23	
807D		MOC A, M	7E	
807E		SBB D	9A	
807F		JNC loop-5	D2	73 80
8082		DCX H	2B	
8083		PUSH H	E5	
8084		MOV E, M	5E	
8085		POP H	E1	
8086		INX H	23	
8087		PUSH H	E5	
8088		MOV D,M	56	
8089		POP H	E1	
808A		MOV B,C	41	
808B		JMP loop-5	C3	73, 80
808E	loop-6	MOV A,B	78	
808F		STA 9008	32	08 90
8092		MVI H, 01	26	01
8094		LXIB 8508	01	08 85
DISPLAY:				
8097		LDA 9008	3A	08 90
809A		MOV B, A	47	
809B		MVI A, 04	3E	04

ADDRESS	LABEL	MNEMONIC	OPCODE	OPERAND
809D		CMP B	B8	
809E		JNZ loop-7	C2	0B 81
8101		MVI A, 80	3E	80
8103		OUT C1	D3	C1
8105		MVI A, 66	3E	66
8107		OUT C0	D3	C0
8108		JMP	C3	34, 81
810B	loop-7	MVI A, 03	3E	03
810C		CMP B	B8	
810D		JNZ loop-8	C2	1B 81
8110		MVI A 80	3E	80
8112		OUT C1	D3	C1
8114		MVI A, F4	3E	F4
8116		OUT C0	D3	C0
8118		JMP	C3	34, 81
811B	loop-8	MVI A,02	3E	02
811D		CMP B	B8	
811E		JNZ loop-9	C2	2C 81
8121		MVI A 80	3E	80
8123		OUT C1	D3	C1
8125		MVI A, B5	3E	B5
8127		OUT C0	D3	C0
8129		JMP	C3	34, 81
812C	loop-9	MVI A 80	3E	80
812E		OUT C1	D3	C1

ADDRESS	LABEL	MNEMONIC	OPCODE	OPERAND
8130		MVI A, 60	3E	60
8132		OUT C0	D3	C0
8134		JMP loop-0	C3	0C 80
DELAY:				
8150		MVI D,04	16	04
8152	loop-10	LXIB FFFF	01	FF FF
8155	loop-11	DCX B	0B	
8156		MOV A,C	79	
8157		ORA B	B0	
8158		JNZ loop-11	C2	55 81
815B		DCR D	15	
815C		JNZ loop-10	C2	52 81
815F		RET	C9	

5.1 8085 - PROCESSOR

The host processor (8085) is an 8 bit general purpose microprocessor capable of addressing 64K of memory. The device has forty pins, requires +5 volt power supply and can operate with a 3 MHz single phase clock. The figure 5.1.1 shows the logic pinout of the 8085 microprocessor. All the signals have been classified into six groups.

* Address bus
* Data bus
* Control and status signal
* Power supply and frequency signals.
* Interrupts and peripheral initiated signals
* Serial Input/Output ports.

Address Bus

The 8085 has eight signal lines A_{15} - A_8 which are unidirectional and used as the high order address bus unlike their counterparts the lines AD_0 - AD_7 which are bidirectional and are used in a multiplexed mode for transmission of address as well as data.

Multiplexed Address/Data bus

As explained earlier the signal lines AD_7 - AD_0 are bidirectional and they serve a dual purpose. These are used as the low order address bus as well as the data bus. During the earlier part of the cycle, these lines are used as the low order address bus. In the later part of the cycle, these lines are used as the data bus.

Control and status signals

The control and status signals used up by the 8085 or as follows:

* ALE - Address Latch Enable:- This signal is used primarily to latch the low order address from the multiplexed bus and generate a separate set of eight address lines that is from A_7 - A_0.

* $\overline{RD}$ - Read:- This signal indicates that the selected Input/Output or memory device is to be read and data are available on that data bus.

* $\overline{WR}$ - Write:- This signal indicates that the data on the data bus is to be written into a selected memory on Input/Output location.

* $IO/\overline{M}$ This differentiates between input/output and memory operations. When high it indicates the former and when low the latter.

* S_1 ON S_0 : These status signals, similar to $IO/\overline{M}$ can identify various operations.

The operations and associated states signals are listed in the Table 5.1.1.

Table 5.1.1. 8085 Machine Cycle Status and Control Signals

Machine Cycle	$IO/\overline{M}$	Status S_1	S_0	Control Signals
Opcode Fetch	0	1	1	$\overline{RD}$ = 0
Memory Read	0	1	0	$\overline{RD}$ = 0
Memory Write	0	0	1	$\overline{WR}$ = 0
I/O Read	1	1	0	$\overline{RD}$ = 0
I/O Write	1	1	0	$\overline{WR}$ = 0
Interrupt Acknowledge	1	1	1	$\overline{INTA}$ = 0
Halt	Z	0	0	
Hold	Z	X	X	$\overline{RD}$, $\overline{WR}$ = Z and $\overline{INTA}$ = 1
Reset	Z	X	X	

NOTE : Z = Tri-state (high impedance)
X = Unspecified

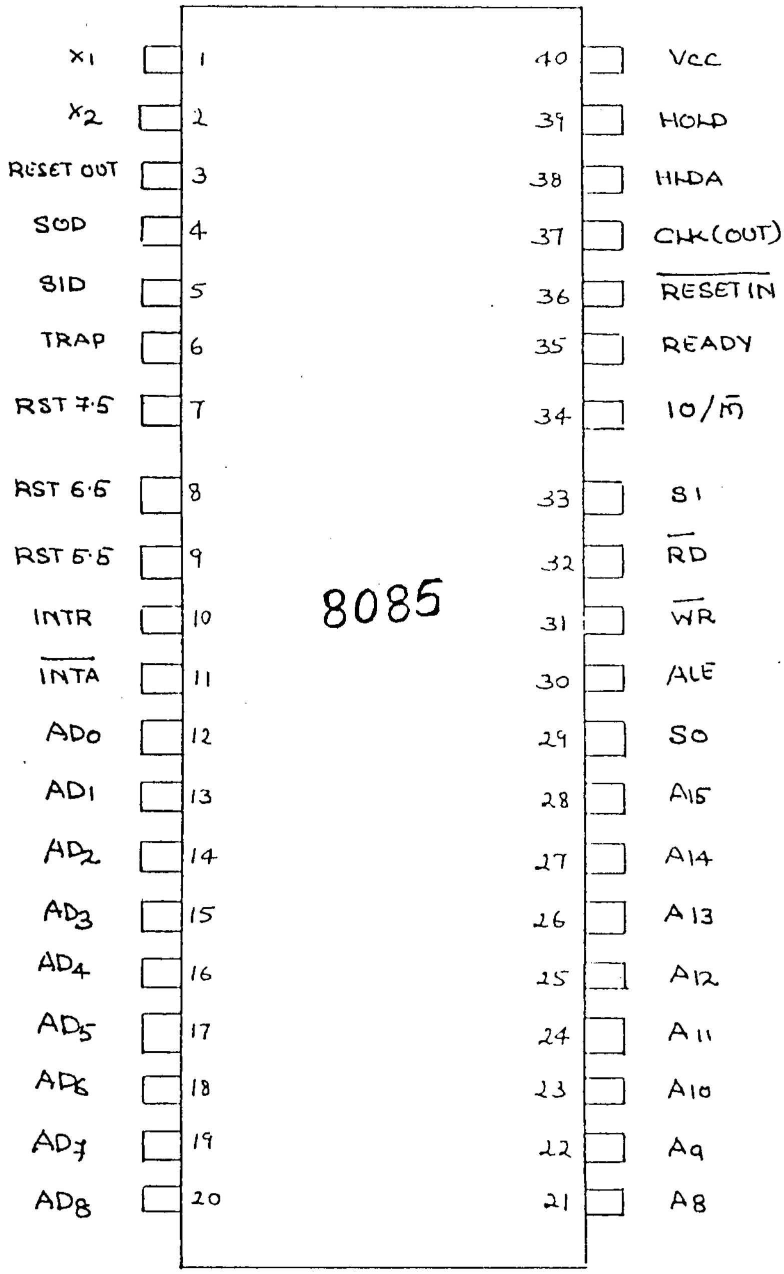


FIG. 5.1.1. PIN-OUT OF 8085

Power Supply and Clock Frequency

- V_{cc} + 5 volt power supply
- V_{ss} - Ground reference.
- X_1, X_2 A crystal (or RC, LC n/w) is connected at these two pins. The frequency is internally divided by two, to operate a system at 3 mHz, the crystal should have a frequency of 6 mHz.
- CLK (OUT) - Clock output. This signal can be used as the system clock for other devices.

Interrupts and Externally Initiated Operations

The 8085 has five interrupt signal that can be used to interrupt a program execution.

INTR - Interrupt Request

$\overline{\text{INTA}}$ - IOnterrupt Acknowledge.

The other signals are RESET, HOLD and READ. These are described as shown in Table 5.1.2.

Table 5.1.2. 8085 Interrupts and Externally Initiated Signals

*	INTR (Input)	Interrupt Request : This is used as a general-purpose interrupt; it is similar to the INT signal of the 8080 A
*	$\overline{\text{INTA}}$ (Output)	Interrupt Acknowledge : This is used to acknowledge an interrupt.
*	RST 7.5 (Inputs) RST 6.5 RST 5.5	Restart Interrupts : These are vectored interrupts and transfer the program control to specific memory locations. They have higher priorities than the INTR interrupt. Among these three, the priority order is 7.5, 6.5, and 5.5.
*	TRAP (Input)	This is a nonmaskable interrupt and has the highest priority.
*	HOLD (Input)	This signal indicates that a peripheral such as a DMA (Direct Memory Access) controller is requesting the use of the address and data buses.
*	HLDA (Output)	Hold Acknowledge : This signal acknowledges the HOLD request.
*	READY (Input)	This signal is used to delay the microprocessor Read or Write cycles until a slow responding peripheral is ready to send or accept data. When this signal goes low, the microprocessor waits for an integral number of clock cycles until it goes high.

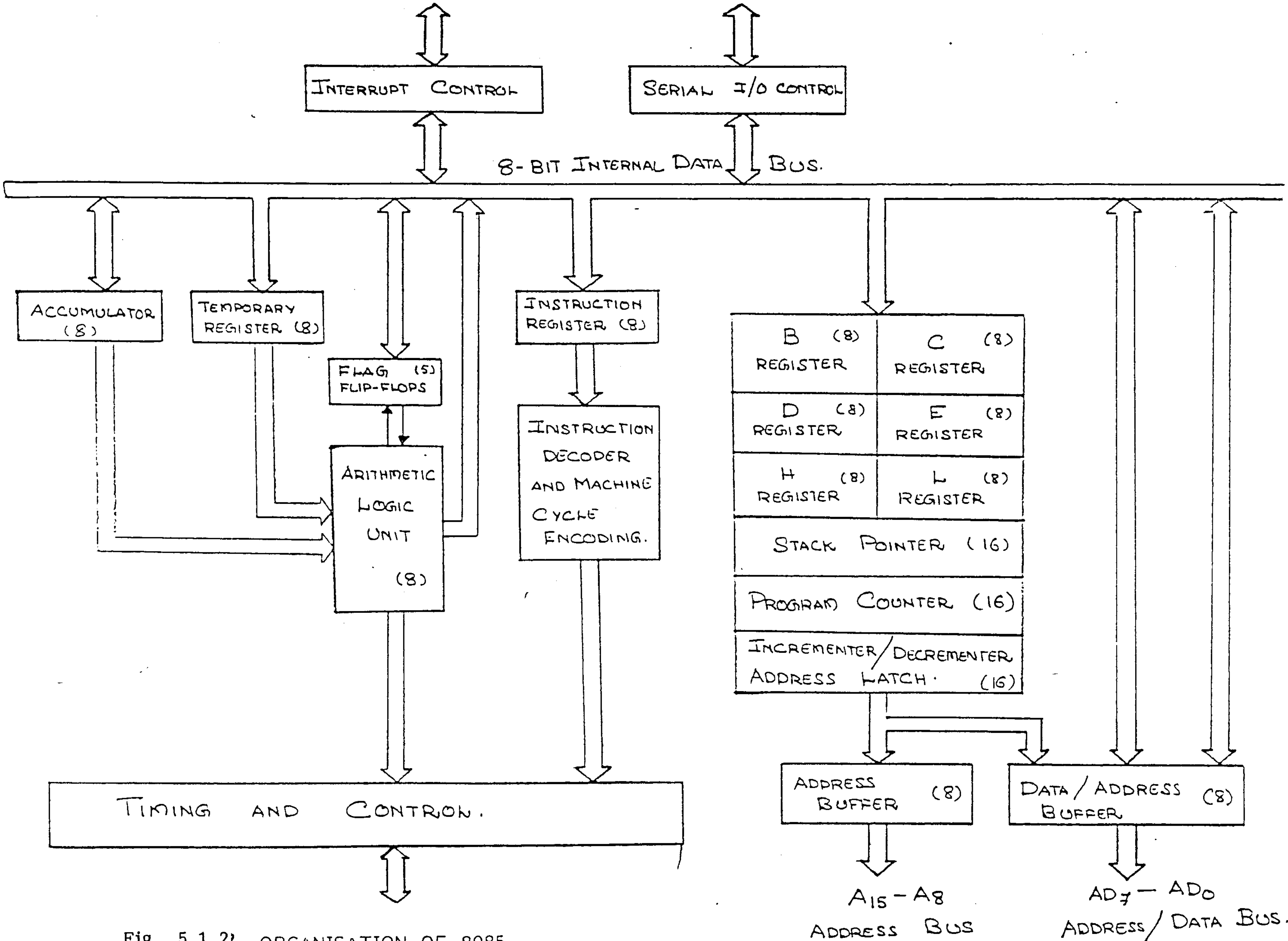


Fig. 5.1.2l ORGANISATION OF 8085

Serial I/O Ports

The 8085 has two signals to implement the serial transmission :

SID - Serial Input Data

SOD - Serial Output Data.

5.1.1 Organization of 8085

The registers used in the organization of 8085 can be understood by with the help of the block diagram provided in Fig. 5.1.2. There is one 8-bit register known as the accumulator which is used in various arithmetic and logical operations. There are six general purpose 8-bit registers that can be used by a programmer for a variety of purposes. These are labelled as B, C, D, E, H and L. There are used either individually or in pains; these are explained as the basis of the table.

Register Pair	Bit Pattern
B - C	00
D - E	01
H - L	10
SP*	11

Codes of General Purpose Registers

Register	Code
A (ACC)	111
B	000
C	001
D	010
E	011
H	100
L	101

In program counter is a 16-bit register used by the 8085 to keep track of the address of the instruction that has to executed next. This is another 16-bit register, known as the stack printer used to maintain a stack in memory. A set of five flip-flops, one-bit registers serve as flags.

5.2 (A) Parallel Peripheral Interface

This is used as a programmable parallel I/O device. This is used to transfer data under various conditions from simple input/output to interrupt input/output. This is flexible, versatile and economical. This is an important general purpose input/output device used with almost any microprocessor.

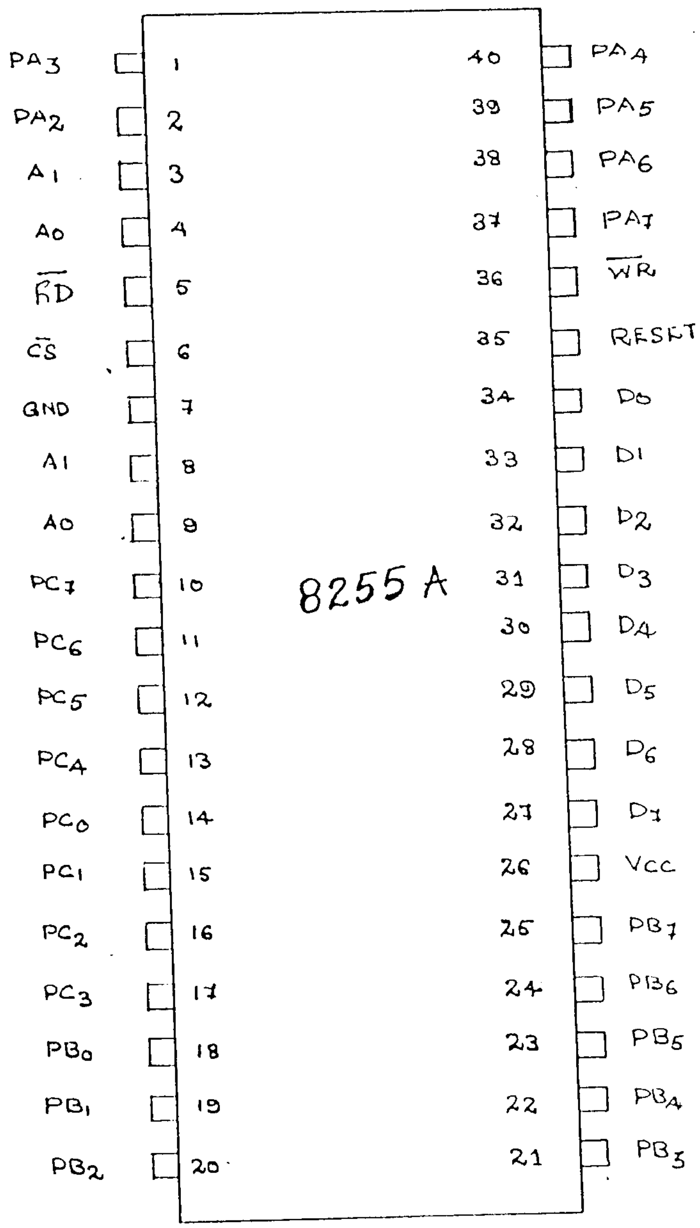


Fig. 5.2.1. PINOUT DIAGRAM OF 8255 A

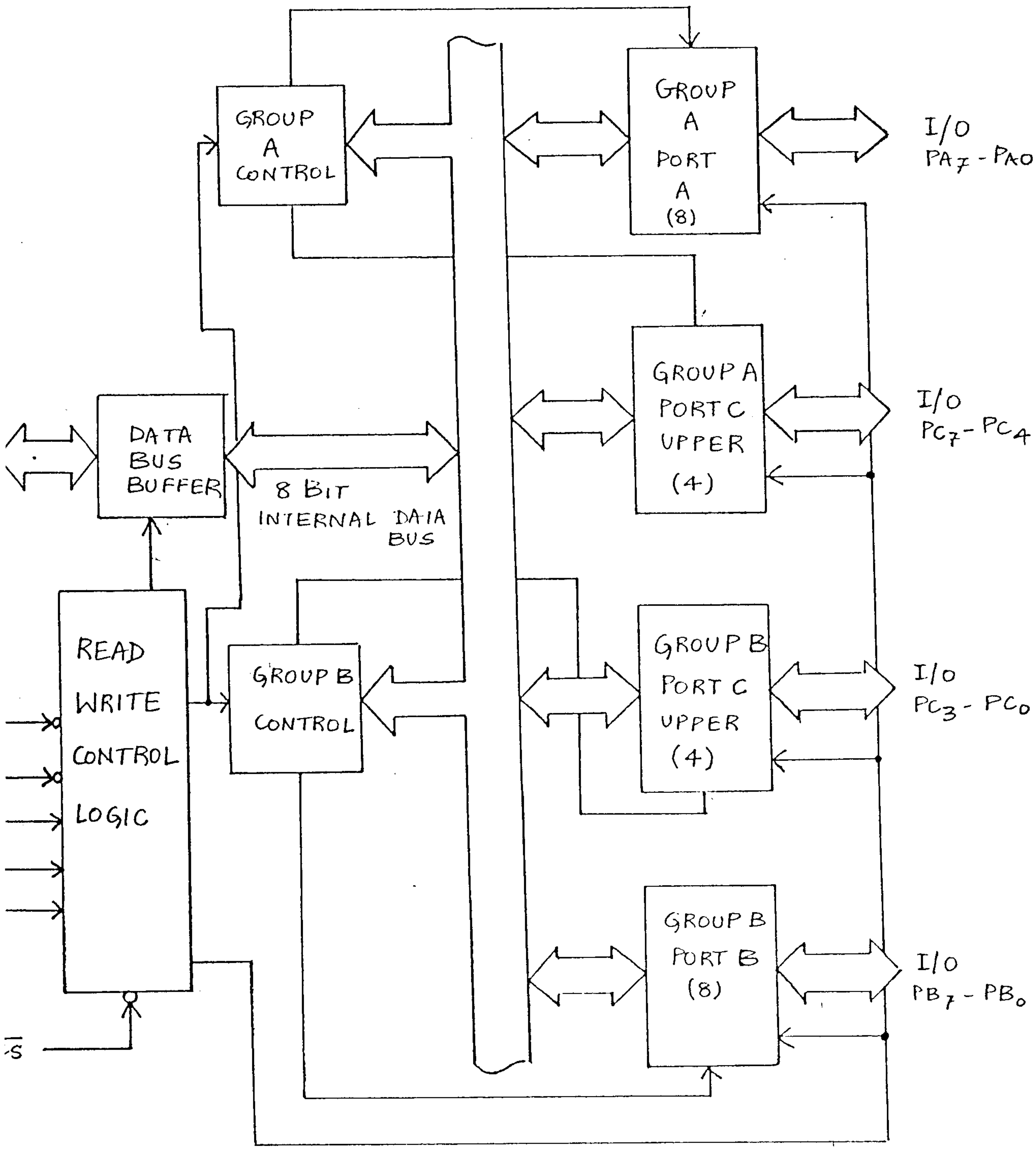


Fig. 5.2.2. SCHEMATIC OF 8255 (A)

8255 (A)

This has 24 I/O pins grouped primarily in two 8-bit parallel ports A and B with the remaining 8 bits as port C. The 8 bits of port C can be used as or be grouped in two 4 bit ports. C UPPER (CU), C LOWER (CL). The functions of the ports are defined by writing a control word in the control register.

The figure 5.2.1. and 5.2.2 shows all the functions of the 8255 A, classified according to two nodes Bit set/Reset (BSR) mode and the I/O mode. The BSR mode is used to set or reset the bits in port C. The I/O mode is further divided into 3 modes; Mode 0, Mode 1 and Mode 2.

In mode 0, all ports function as simple Input/Output ports. Mode 1 is a handshake mode whereby ports A and/or B use bits from Port C as handshake signals. In the handshake mode, two types of Input/Output data transfer can be implemented. Status check and interrupt. In mode 2, port A can be set up for bidirectional data transfer using handshake signals from port C and port B can be set up either in mode 0 or mode 1.

5.2.1 Control Logic

The control section hs 6 lines and their functions are as follows :

This "Enables" the system. A software timer is started to count down for a specific period of time after which the signal input is cut off by disabling the gate. The output of the cascaded counters is read into the host system through the ports A and B of the interface. This final counter value is the "feature" of the present utterance and hence is passed on to the feature template matching software.

* $\overline{RD}$ (READ) - This control signal enables the read operation. When the signal is low, the microprocessor reads data from a selected input/output port of 8255 A.

* $\overline{WR}$ (WRITE) - This control signal enables the write operation. When the signal is low, the microprocessor writes into a selected input/output port on the control register.

* RESET (RESET) - Active high signal, it clears the control register and sets all ports in the input mode.

* $\overline{CS}$, A_0 and A_1 - These are device select signals. Chip select $\overline{CS}$ is connected to a decoded address and A_0 and A_1 are generally connected to the microprocessor address lines A0 and A_1 respectively.

$\overline{CS}$	A_1	A_0	Selected
0	0	0	Port A
0	0	1	Port B
0	1	0	Port C
0	1	1	Control Register
1	X	X	8255 is not selected.

5.2.2 Control Word

Figure (5.2.3) shows a register called the control register. The contents of the control register is called the control word specifying an input/output function for each port. This register can be accessed to write a control word. When A_0 and A_1 are at logic. At this time, the register a not accessible for a read operation.

Bit D_7 of the control register specifies either the input function or the Bit set/Reset function. If bit D_7 = 1, bits D_6-D_0 determine input functions in various modes. If bit D_7 = 0, port C operates in the Bit set/Reset mode. The BSR control word does not affect the function of the Port A and B.

To communicate with peripherals through the 8255 A, the following 3 steps are required.

1. Determine the addresses of port A, B and C of the control register according to the chip select logic and address lines A_0 and A_1.
2. Write a control word in the control register.
3. write Input/Output instructions to communicate with the peripherals through ports A, B and C.

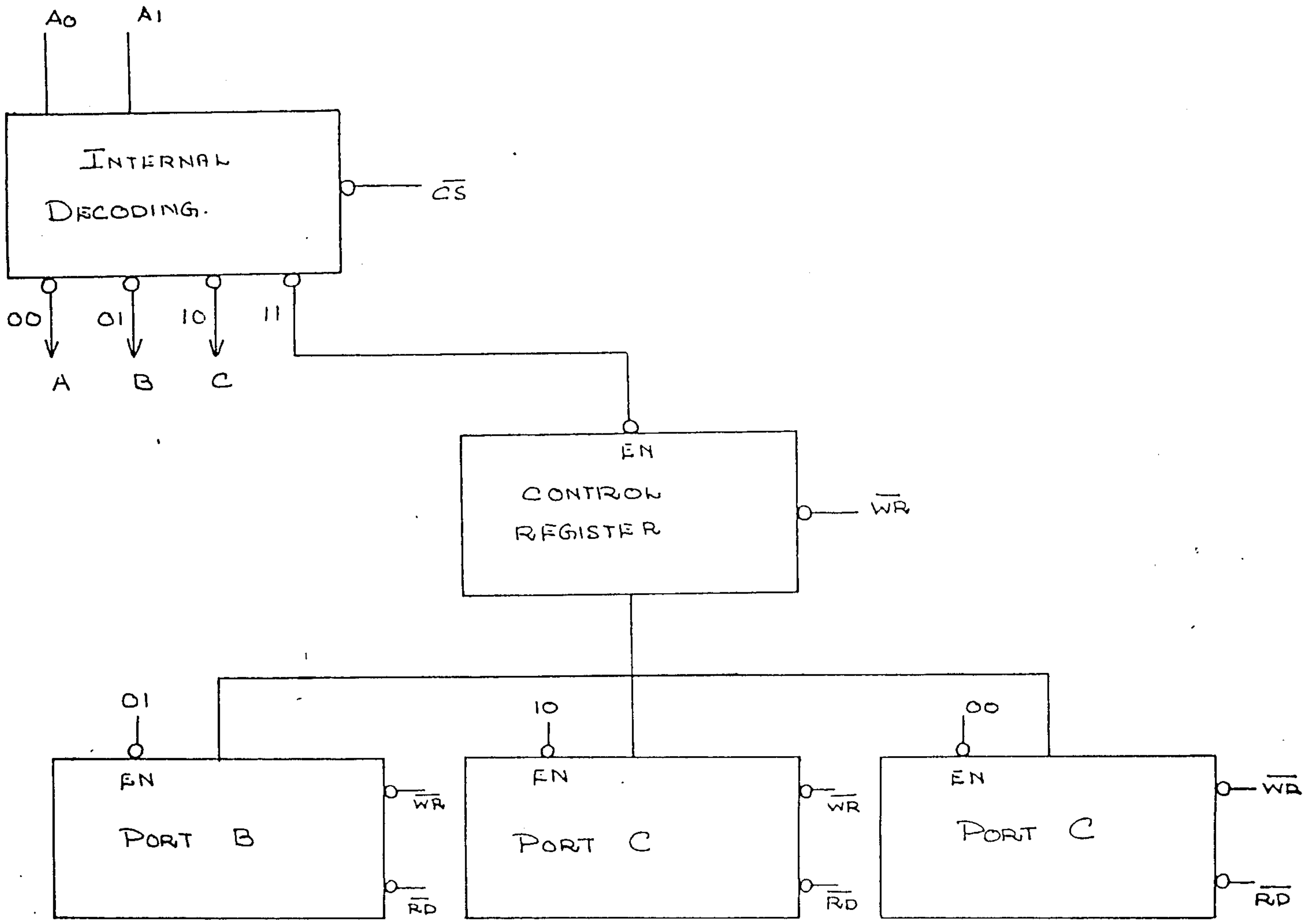


FIG. 5.2.3 CONTROL LOGIC FOR I/O PORTS OF 8255 A

5.2 Programmable Interval Timer (8253)

The 8253 Programmable Interval Timer/Counter generates accurate time delays and can be used for applications such as a real-time clock, an event counter, a digital one-shot, a square wave generator, and a complex waveform generator.

The unique features of the 8253 are 1) 3 Independent 16-bit counters 2) Input clock from DC to 2 MHz 3) Programmable counter modes and 4) Count binary or BCD. It is packaged in a 24

8253 PROGRAMMABLE INTERVAL TIMER

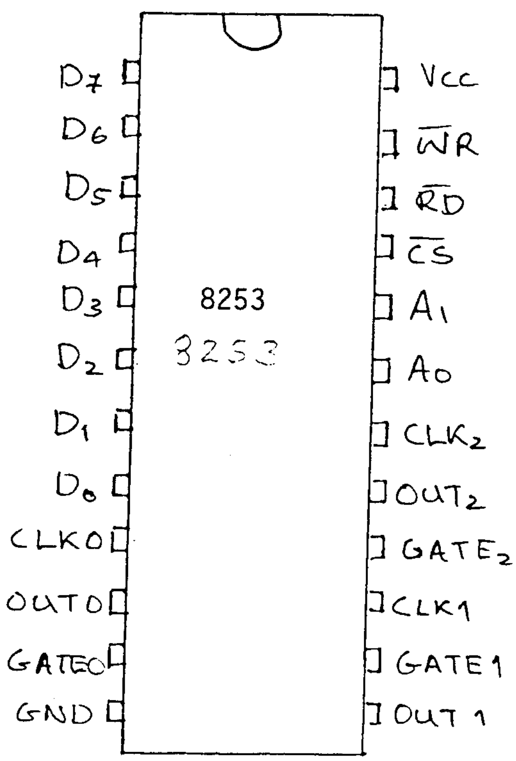


Fig.5.3.1 PROGRAMMABLE INTERVAL TIMER

pin DIP and requires a single +5V power supply. To operate a counter, a 16 bit count is loaded in its register and on command, it begins to decrement the count until it reaches 0. At the end of the count, it generates a pulse that can be used to interrupt the MPU. A count can be read by the MPU while the counter is decrementing.

BLOCK DIAGRAM OF THE 8253

It includes three counters (0, 1 and 2), a data, bus buffer, Read/Write control logic, and a control register. Each counter has two input signals - clock (CLK) and GATE - and an output signal - OUT.

DATA BUS BUFFER

The tri-state, 8 bit, bidirectional buffer is connected to the databus of the MPU.

CONTROL LOGIC

The control section has five signals : $\overline{RD}$ (Read), $\overline{WR}$ (Write), CS (Chip Select), and the address lines A0 and A1. In the peripheral I/O mode, the $\overline{RD}$ and $\overline{WR}$ signals are connected to $\overline{IOR}$ and $\overline{IOW}$, respectively. In memory mapped I/O, these are connected to $\overline{MEMR}$ (Memory Read) and $\overline{MEMW}$ (Memory Write). Address

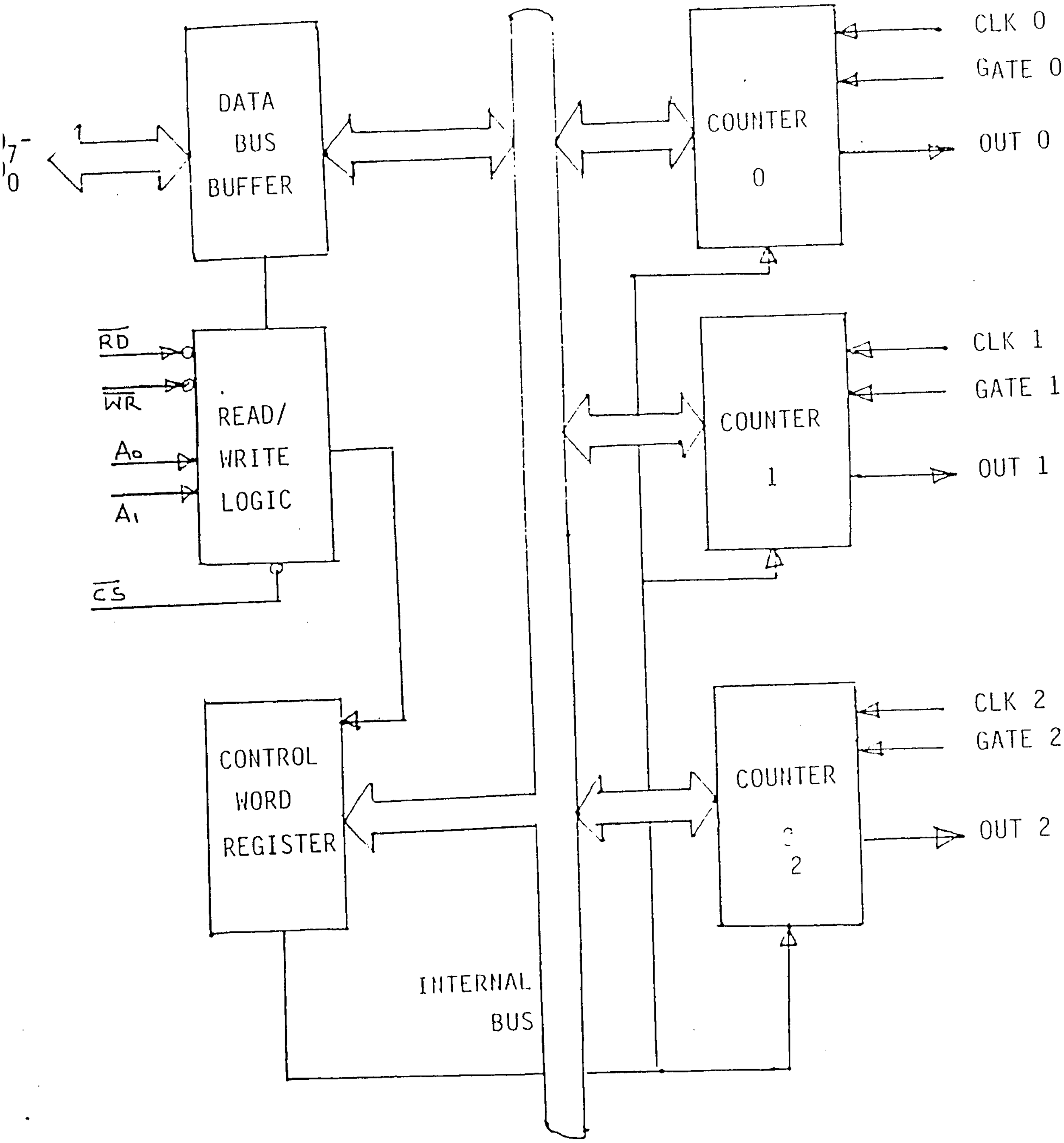


Fig.5.3.2. BLOCK DIAGRAM OF 8253 PROGRAMMABLE INTERVAL TIMER

lines A0 and A1 of the MPU are usually connected to lines A0 and A1 of the 8253, and CS is tied to a decoded address. The control word register and counters are selected according to the signals on lines A0 and A1, as shown below :

A1	A0	Selection
0	0	Counter 0
0	1	Counter 1
1	0	Counter 2
1	1	Control Register

CONTROL WORD REGISTER

This register is accessed when lines A0 and A1 are logic 1. It is used to write a command word which specifies the counter to be used, its mode, and either a Read or a Write operation. However, the control word register is not available for a Read operation.

MODE

The 8253 can operate in six different modes, as shown. The gate of a counter is used either to disable on enable counting.

PROGRAMMING THE 8253

The 8253 can be programmed to provide various types of output through write operations or to check a count while counting through Read operations. The details are as given below :

WRITE OPERATIONS

To intialise a counter, the following steps are necessary 1) Write a control word into control register. 2) Load the low-order byte of a count in the counter register. 3) Load the high order byte of a count in the counter register.

8253 CONTROL WORD FORMAT

D7	D6	D5	D4	D3	D2	D1	D0
SC		R/L			M		C

7	6	Select counter	5	4	Read/ Load	D_3	D_2	D_1	Mode	Code
0	0	0	0	0	LC	0	0	0	0	0=binary
0	1	1	0	1	LSB	0	0	1	1	1 = BCD
1	0	2	1	0	MSB	x	1	0	2	
1	1	illegal	1	1	LSB,	x	1	1	3	
					MSB	1	0	0	4	
						1	0	1	5	

READ OPERATIONS

In some applications, especially in event counters, it is necessary to read the value of the count in progress. This can be done by either of two methods. One method involves reading a count after inhibiting the counter to be read. The second method involves reading a count while the count is in progress. In the first method, counting is stopped by controlling the gate input or the clock input of the selected counter and two I/O read operations are performed by the MPU. The first I/O operations reads the low-order byte, and the second I/O operation reads the high-order byte.

In the second method an appropriate control word is written into the control register to latch a count in the O/P latch and two I/O read operations are performed by the MPU.

CONCLUSION

PCCR accept only a small vocabulary and a single speaker. These are well with in the capabilities of present day recognisers. One solution to the limited vocabularies is to provide for the most frequently used words, which are capable of handling a huge vocabulary. To include new words we could delete the unused words among the original of words and these make romm for the newly encounted ones.

The other question which arises is the futility of a speaker dependent system. As most office systems and other applications are used only by a few people, a speaker - ddependent mode of use is apt for the surroundings. The complexity which arises so that of embiquity due to voice levels of the speaker.

A possible compromise is a system which various speaker - dependent templates for these words which need to be edited.

PCCR is yet another addition tot he vast expanding group of speech recognizers. This is not a conclusion but a begining for new horizons is speech system.

APPLICATIONS

The use of speech recognition is expected to follow the adoption of computers in various areas of human activity. The patential uses of speech recognition can be illustrated as

* Domestic appliance system
* Office applications.
* Industrial applications.
* Transport applications.
* Medical applications.
* Application in public service.
* Military applications.
* Aids for handicapped.

7.1 DOMESTIC APPLIANCE SYSTEM

This system controls the operation of domestic appliances through voice. When the speaker uses the name of any particular device, the device is activated immediately. These devices can be controlled as desired by giving further commands.

An elementary block diagram of the said system is shown in Fig. 7.1.2. along with the figure showing the actual set up.

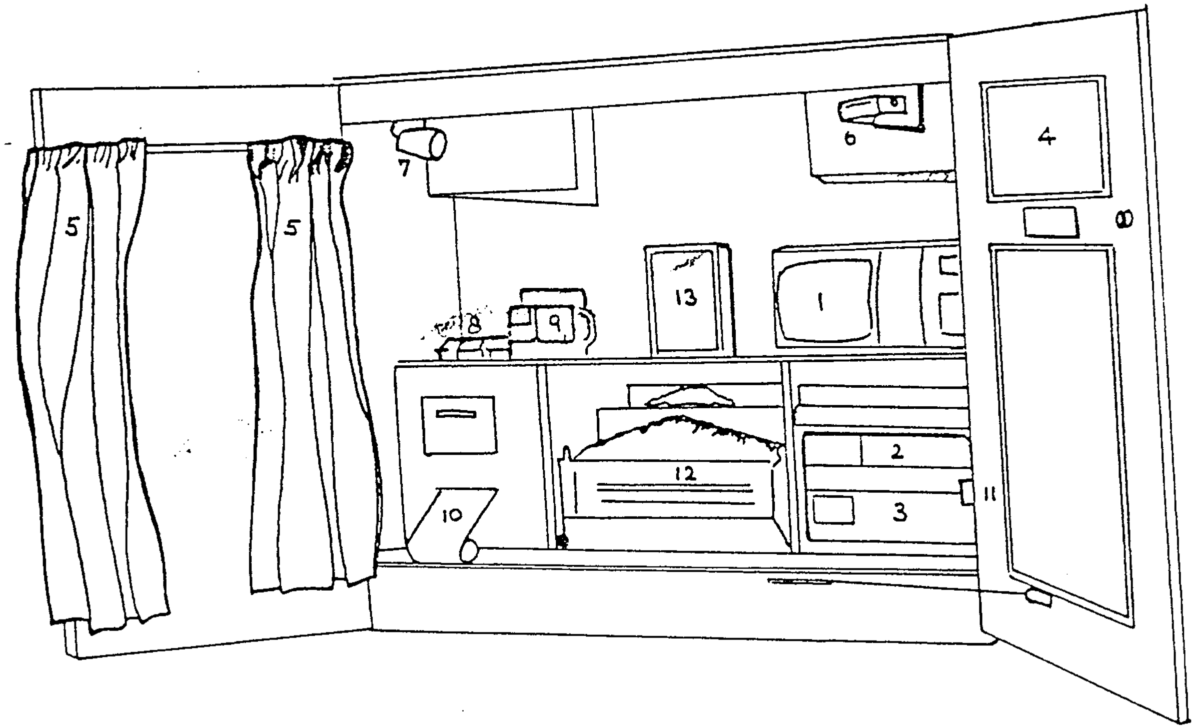


FIG. 7.1.1 VOICE ACTIVATED DOMENSTIC APPLIANCE SYSTEM

(1). Turn the television on and off. Change channels, select teletext, adjust the volume. (2) Turn the radio on and off and select stations (3) Play, Fast Forward and rewind the casette player (4) open and close the door. (5) Open and close the curtains (6) Control a security camera (7) Turn lights on and off (8) Activate the telephone and dial numbers (9) Turn on the Teasmaid (10) Accept dictation and print a letter (11) Activate an Alaram signal (12) Control an electric fire (13) Speak foreign languages.

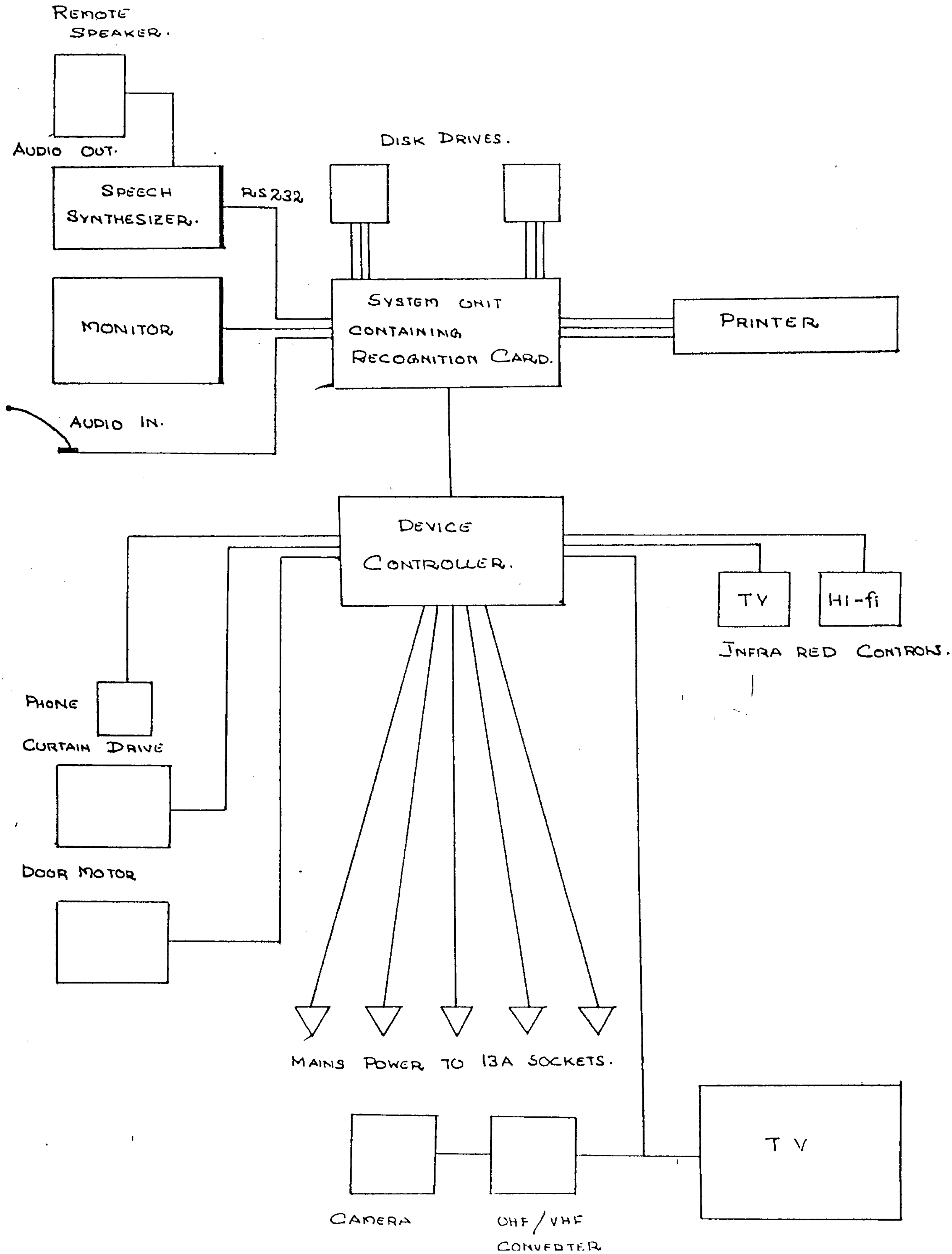


Fig.7.1.2. BLOCK DIAGRAM OF VOICE ACTIVATED APPLIANCE SYSTEM

This system when constructed by voice input systems of St.IVES. U.K. which made use of Apple II system with 2 a asynchronous communication cards a floppy drive , silenttype printer, votrax synthesizer, scott recognition card and a device controller. We do not explain the detailed working of the system as it is beyond the scope of this text.

7.1.2. Office Applications

In the office, voice-controlled telephone-answering machines are much used. The incoming calls could be directed to the appropriate extensionseither by number or name. It would also be possible to reprogram the exchange by voice so that the calls are temporarily diverted during adbsences or meetings in other toom.

The main current-use of computers in office and for work. Processing and data applications. A machine which could type an utterance spoken into it would revolutionise office which is the dream of designers.

7.1.3 Industrial Applications

Due to the diversity of industrial processes, many applications of speech recognisers have not yet been conceived whereas some applications have already been tested. An example for this is computer-controller machine loads which are programmed by means of a key board.

Another use of speech recognisers is in inspection and quality control. The process of detecting the fault and noting it down, which all constitutes a manual job can be executed with the help of voice-activated systems. Speech recognition has been used in industry for materials handling. Articles on a conveyor handling. Articles on a conveyor belt - can be routed to appropriate destination by controlling the sorting mechanism by voice.

7.1.4 Transport Applications

There are two main areas of applications of speech recognition relating to transport those which involve the driver and those which affect the consumer. A flight management system is are important application for voice controlled systems. Another areas of emphasis for speech recognisers in the field of avionics is in training of air-traffic controllers.

The other area of application concerning transport is in booking and time table inquiries. With the use of speech recognisers any traveller with a telephone could have direct access to the reservation system.

7.1. 5 Medical Applications

There are a number of areas of medicine where speech-recognition systems might find application. These might patients, doctors, or laboratory applications. Machines could be built which would indicate those patients who should undergo further medical tests. Systems could be developed which could be used for self-diagnosis.

7.1.6. Applications in Public Service

One of the earliest applications of speech recognition was in the postal service. Parcels were sorted by one man picking up a parcel and reading the distination from the label Another potential use of speech recognition in public services is in police work. Because of the mobile nature of police palrats immediate access to databases by voice over a radio link could save valuable time and improve efficiency.

7.1.7. Military Applications

The potential use of speech recognition in combat air craft is similar to its use in civil plane. In warships speech recognition could be used to control weapon systems from the bridge. It is advantageous for the captain to control the helm, interrogate the

Speech can be used to assist astronauts in space. The use of speech recognition will make accurate key strokes easier especially while moving in bulky space suits.

7.1.8 Aids for Handicapped

Many of the uses mentioned above, will provide a relief to the handicapped. The control of home appliances by voice could greatly add to the comfort and enjoyment of life by people with paralysed limbs. A means of converting speech into writing would aid the deaf.

A system can be used for training deaf people in speech production. The missing auditory feedback could be applied by visual means. A good deal of mobility could be restored to people with paralysed limbs. If they were supplied with a motorised wheel chair controlled by voice.

As the use of computers becomes more widespread, the penalty for not being able to do so will become greater. People with inprecise control of their hands find it difficult to operate keyboards, but the use of speech may circumvent this difficult.

8. FUTURE TREND

One of the principle developments planned on this system is to evaluate the input signal after it has been separated into more than one frequency band. The input signal will be fed into three band pass filters, typically and the number of crossings will be noted down each band and the average distance calculated. This will give a much more accurate result. Alternatively, the total time frame can be divided into two or more parts and the crossings in each time slice be recorded separately. Calculation of distance for each of these divisions and averaging the corresponding deviations can give more accuracy. Calculation of the power of the signal can also be incorporated.

8.1.1 Speech Recognition

Speech recognition is being used extensively in various avenues and many more are opening up. With advent of advanced techniques such as fast fourier transfer, filter bank techniques and linear predictive coding, great accuracy has become possible.

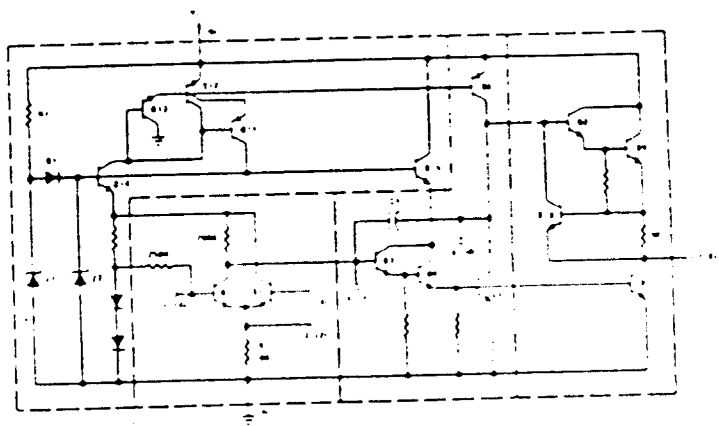
Also the VLSI technology has made it possible to integrate an entire recognition system as a single integrated circuit chip. As time goes by, the costs of these silicon based semiconductor devices will go down as can already be seen, and the use of speech based devices is foreseen to be most widespread. Let "Listener" be a modest stepping stone in this endeavour.

National Semiconductor

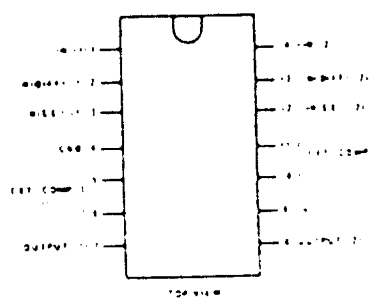
Absolute maximum ratings

Supply voltage	+40 V
Power dissipation (note 1)	715 mW
Operating temperature range	0°C to 70°C
Storage temperature range	−65°C to +150°C
Lead temperature (Soldering, 10 sec)	300°C

schematic and connection diagrams



Dual-In-Line Package



National Semiconductor

electrical characteristics $T_A = 25°C$, $V_{CC} = 14V$, unless otherwise stated.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Voltage Gain	Open Loop (Differential Input), f = 100 Hz		160,000		V/V
	Open Loop (Single Ended), f = 100 Hz		320,000		V/V
Supply Current	V_{CC} 9 to 40V, $R_L = \infty$		10		mA
Input Resistance					
(Positive Input)			100		kΩ
(Negative Input)			200		kΩ
Input Current					
(Negative Input)			0.5		μA
Output Resistance	Open Loop		150		Ω
Output Current	Source		8		mA
	Sink		2		mA
Output Voltage Swing	Peak to Peak		$V_{CC} - 2$		V
Unity Gain Bandwidth			15		MHz
Power Bandwidth	20 V_{p-p} (V_{CC} = 24V)		75		kHz
Maximum Input Voltage	Linear Operation			300	mVrms
Supply Rejection Ratio	f = 1 kHz		120		dB
Channel Separation	f = 1 kHz		60		dB
Total Harmonic Distortion	60 dB Gain, f = 1 kHz		0.1		%
Total Equivalent Input Noise	R_S = 600Ω, 10 – 10,000 Hz (Single Ended Input, Flat Gain Circuit, A_V = 1000)				
LM381A			0.5	0.7	μVrms
LM381			0.5	1.0	μVrms

Note 1: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 175°C/W junction to ambient.

National Semiconductor

DM54ALS132/DM74ALS132 Quad 2-Input NAND Gates with Schmitt Trigger Inputs

General Description

This device contains four independent gates, each of which performs the logic NAND function. Each input has hysteresis which increases the noise immunity and transforms a slowly changing input signal to a fast changing, jitter-free output.

Features

- Switching specifications at 50 pF
- Switching specifications guaranteed over full temperature and V_{CC} range
- Advanced oxide-isolated, ion-implanted Schottky TTL process
- Functionally and pin-for-pin compatible with Schottky and low power Schottky TTL counterparts
- Improved AC performance over Schottky and low power Schottky counterparts

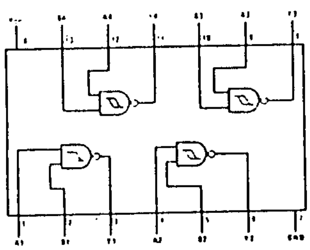
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



TL/F/6707-1

DM54ALS132 (J) DM74ALS132 (N)

Function Table

$Y = \overline{AB}$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = high logic level
L = low logic level

Recommended Operating Conditions

Symbol	Parameter	DM54ALS132 Min	DM54ALS132 Typ	DM54ALS132 Max	DM74ALS132 Min	DM74ALS132 Typ	DM74ALS132 Max	Units
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{T+}	Positive-Going Input Threshold Voltage (Note 2)	1.4		2	1.4		2	V
V_{T-}	Negative-Going Input Threshold Voltage (Note 2)	0.7		1.2	0.8		1.2	V
Hys	Input Hysteresis (Note 2)	0.5			0.5			V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

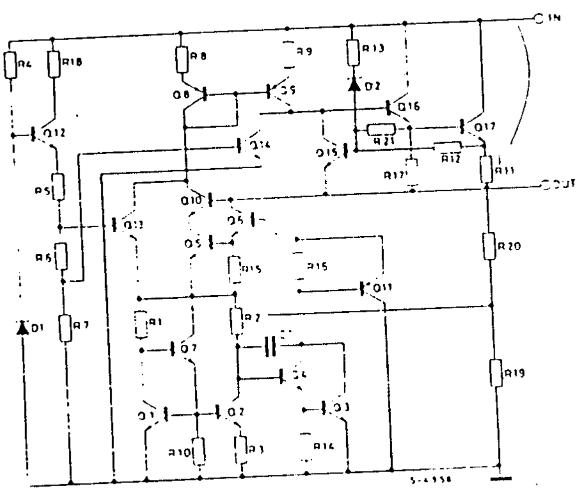
Symbol	Parameter	Conditions		Min	Typ (Note 3)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, $V_I = V_{T-Min}$	DM54	$V_{CC}-2$	3.4		V
			DM74	$V_{CC}-2$	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, $V_I = V_{T+Max}$	DM54		0.25	0.4	V
			DM74		0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	V
I_{T+}	Input Current at Positive-Going Threshold	V_{CC} = 5V, $V_I = V_{T+}$			0.03		mA
I_{T-}	Input Current at Negative-Going Threshold	V_{CC} = 5V, $V_I = V_{T-}$			0.034		mA
I_I	Input Current at Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = Max, V_O = 2.25V		−30		−112	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max				8	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max				8	mA

Note 2: V_{CC} = 5V.

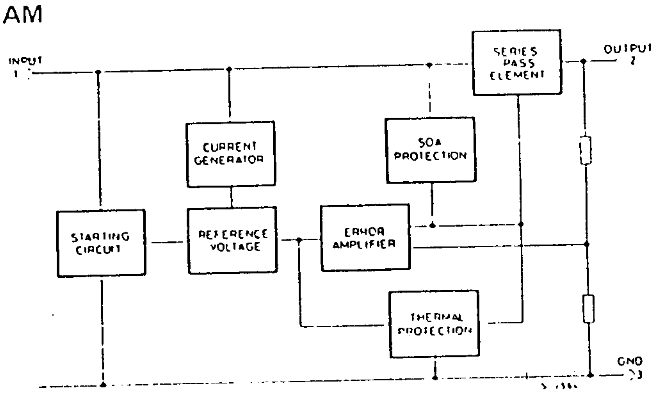
Note 3: All typicals are at V_{CC} = 5V, T_A = 25°C.

μA7800 Series 3-Terminal Positive Voltage Regulators

SCHEMATIC DIAGRAM



BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS L7805AC (V_i = 10V, I_o = 1A, T_j = 0 to 125°C unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit
V_o	Output voltage	T_j = 25°C	4.9	5	5.1	V
V_o	Output voltage	I_o = 5mA to 1A, Po ≤ 15W V_i = 7.5 to 20V	4.8	5	5.2	V
ΔV_o*	Line regulation	V_i = 7.5 to 25V, I_o = 500 mA V_i = 8 to 12V V_i = 8 to 12V, T_j = 25°C V_i = 7.3 to 20V, T_j = 25°C		7 10 2 7	50 50 25 50	mV mV mV mV
ΔV_o*	Load regulation	I_o = 5mA to 1A I_o = 5mA to 1.5A, T_j = 25°C I_o = 250 to 750 mA		25 25 8	100 100 50	mV mV mV
I_d	Quiescent current	T_j = 25°C		4.3	6 6	mA mA
ΔI_d	Quiescent current change	V_i = 8 to 25V, I_o = 500mA V_i = 7.5 to 20V, T_j = 25°C I_o = 5mA to 1A			0.8 0.8 0.5	mA mA mA
SVR	Supply voltage rejection	V_i = 8 to 18V, f = 120Hz I_o = 500mA		68		dB
V_d	Dropout voltage	I_o = 1A T_j = 25°C		2		V
e_N	Output noise voltage	f = 10Hz to 100KHz, T_{amb} = 25 C		10		µV/V_o
R_o	Output resistance	f = 1KHz		17		mΩ
I_{sc}	Short circuit current	T_{amb} = 25°C V_i = 35V		0.2		A
I_{scp}	Short circuit peak current	T_j = 25°C		2.2		A
$\frac{\Delta V_o}{\Delta T}$	Output voltage drift			−1.1		mV/°C

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

National Semiconductor

.M158/LM258/LM358, LM158A/LM258A/LM358A .ow Power Dual Operational Amplifiers

3eneral Description

The LM158 series consists of two independent, high ;ain, internally frequency compensated operational am-)lifiers which were designed specifically to operate from single power supply over a wide range of voltages.)peration from split power supplies is also possible and he low power supply current drain is independent of the nagnitude of the power supply voltage.

\pplication areas include transducer amplifiers, dc gain)locks and all the conventional op amp circuits which ıow can be more easily implemented in single power upply systems. For example, the LM158 series can be lirectly operated off of the standard +5 V_{DC} power upply voltage which is used in digital systems and will asily provide the required interface electronics without equiring the additional ±15 V_{DC} power supplies.

Jnique Characteristics

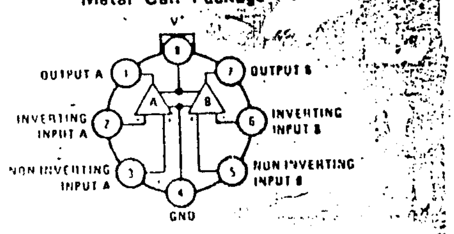
- In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.
- The unity gain cross frequency is temperature compensated.
- The input bias current is also temperature compensated.

\dvantages

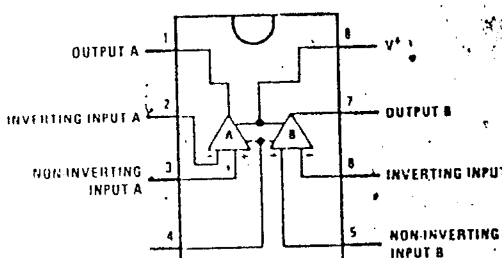
- Eliminates need for dual supplies
- Two internally compensated op amps in a single package

Connection Diagrams (Top Views)

Metal Can Package



Order Number LM158AH, LM158H, LM258AH, LM258H, LM358AH or LM358H
See NS Package H08C



Order Number LM358AN, LM358N or LM2904N
See NS Package N08B

PART I : SPECIFICATIONS

1. CPU : Intel 8085A CPU Operating at 3.072 MHz Clock Rate.

2. ROM : (Read Only Memory)
   Provision to accomadate ROM upto 8K

   Address : 0000 - 0FFF for 4K Bytes (2732)

   OR 0000 - 1FFF for 8K Bytes (2764)

3. RAM : (Random Access Memory)

   Provision to accomadate 8K RAM.

   Address: 6000 - 67FF when using 6116 (2k)

   6000 - 7FFF when using 6264 (8K)

4. PERIPHERALS: 1) 24 I/o lines using 8255.

   Address: A0H - A3H

   2. Three number of 16 bit Timers/counters using 8253.

   Address: E0H - E3H

   3. Keyboard/Display controller using 8279. Facility to interface 64+2 keys and 16 digits of seven Segment Displays

   Address: C0H for Data

   C1H for Command.

5. BUFFERING : All Address, Data and Control and other important lines are properly buffered before termination at 50 pin FRC header.

6. TERMINATION :

1. 24 I/O lines of 8255 brought out on a seperate 26 pin FRC Header.

2. All interfacing lines of 8279 are brought out on a seperate 26 pin FRC Header.

3. Clock, Gate and output lines of Three timers/counters of 8253 are brought out on a 9 pin FRC header.

4. Complete buffered bus is brought out on a 50 pin FRC header.

7. SYSTEM POWER REQUIREMENT : +5V, Less than 500 MA.

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8. Communication standard Distionary - Martin H. Weik.