Multi Function Frequency Meter
with
Additional Prescaler Facility

A PROJECT REPORT
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Certificate

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Multi Function Frequency Meter with Additional Prescaler Facility

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THE AUTHORS

SYNOPSIS

The multi-function frequency meter is an advanced, versatile and user - configurable test instrument capable of accurate measurement of frequency, frequency ratio and time interval. In addition to all this, it can be used as a period and event counter.

The multi-function test instrument described here is based on the 8-digit counter/timer IC Type ICM 7226 B from Intersil (GE/RCA). This chip combines all the functions expected from a good and versatile counter, and requires a very few external components. The chip handles frequency measurement from DC to 10 MHz. A prescaler circuit in addition, when connected extends the usable frequency range from 10 MHz to well over 1.2 GHz.

It also handles period measurement from 0.5 μs to 10 s, unit counting up to 10 million events, frequency ratio measurement and time interval measurement. The inputs of the proposed instrument can accept a wide range of alternating (analogue) voltages as well as digital pulses at TTL or CMOS levels.

CONTENTS

CHAPTER - I

INTRODUCTION

The multi function frequency meter is very much useful for communication purposes.

The word "frequency" is one of the most important words used and it is also the very common word used in communications.

In its basic electrical sense, the term "Communications" refers to the sending, receiving and processing of information by electrical means.

Frequency is defined as "the number of events per time interval".

There are different frequency ranges (ie. Band-width) which are also called bands or channels which are used for different communicatin purposes. These frequency ranges are listed in the Table-1.

The ICM 7226 is a fully integrated Universal counter and LED display driver.

TABLE : 1 : CLASSIFICATION OF RADIO BANDS

Frequency Range	Wave length	Name	Application
30 Hz to 300 Hz	10 Mm to 1 Mm	Extremely low fre- quency (ELF)	Sub-surface communication
3 KHz to 30 KHz	100 Km to 10 Km	Very low frequency (VLF)	Surface wave and sky wave communication
30 KHz to 300 KHz	10 Km to 1 Km	Low frequ- (LF)	Surface wave & sky wave communications standard time and frequency broadcasts and Radio Navigation
300 KHz to 3MHz	1 Km to 100 m	Medium frequency (MF)	Ground wave for short dista- nces, ionospheric wave for longer distances
3 MHz to 30 MHz	100 m to 10 m	High fre- quency (HF)	used for short wave radio communication
30 MHz to 300 MHz	10 m to 1m	Very high frequency (VHF)	TV receivers & FM pro/agation space wave propagation
300 MHz to 3GHz	1 m to 10 cm	Ultra high frequency (UHF)	only possible line of sight radio communica- and broadcast service
3 GHz to 30 GHz	10 cm to 1 cm	Super high frequency (SHF)	Space wave communication is possible, radar communication,
30 GHz to 300 GHz	1 cm to 1 mm	Extreamly high frequency (EHF)	satellite communication & microwave line of sight communication is also possible

The counter inputs accept a maximum frequency of 10 MHz in "frequency" and "unit Counter" modes and 2MHz in all the other modes. Both inputs are digital inputs. For "Period" and "time-interval", the 10MHz time base gives a 0.1 μsec resolution. In "Period average" and "time interval average", the resolution can be in the nano second range. In the "frequency" mode, we can select accumulation time of 10 ms, 100 ms, 1 S and 10 S. There is a 0.2 sec interval between measurement in all ranges. Control signals are provided to enable gating and storing of prescaler data.

CHAPTER - II

CIRCUIT DESCRIPTION

The circuit diagram of the multifunction frequency meter is given in Figure 1. It shows the ICM 7226 B - IC along with an outline of the simple peripheral circuitary needed to obtain an complete instrument. A prescalar for extending the input frequency range to 1.2 GHz will be discussed in the forth comming chapter of this project report.

The ICM 7226 B has an internal time base circuitary, display decoders, segment and digit drivers. The block diagram of ICM 7226 B is shown in Figure 2. And its pin configuration is shown in figure 3.

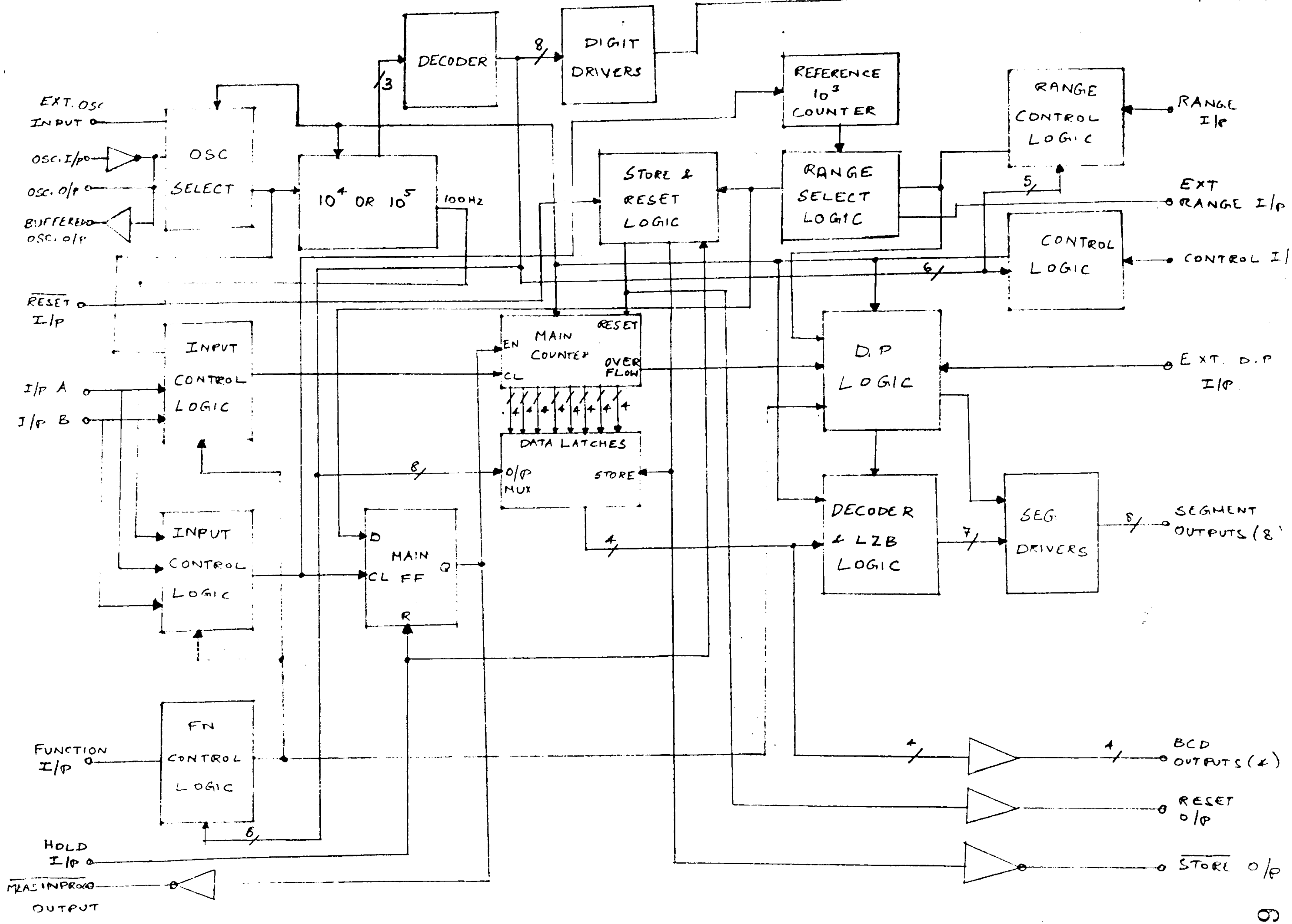
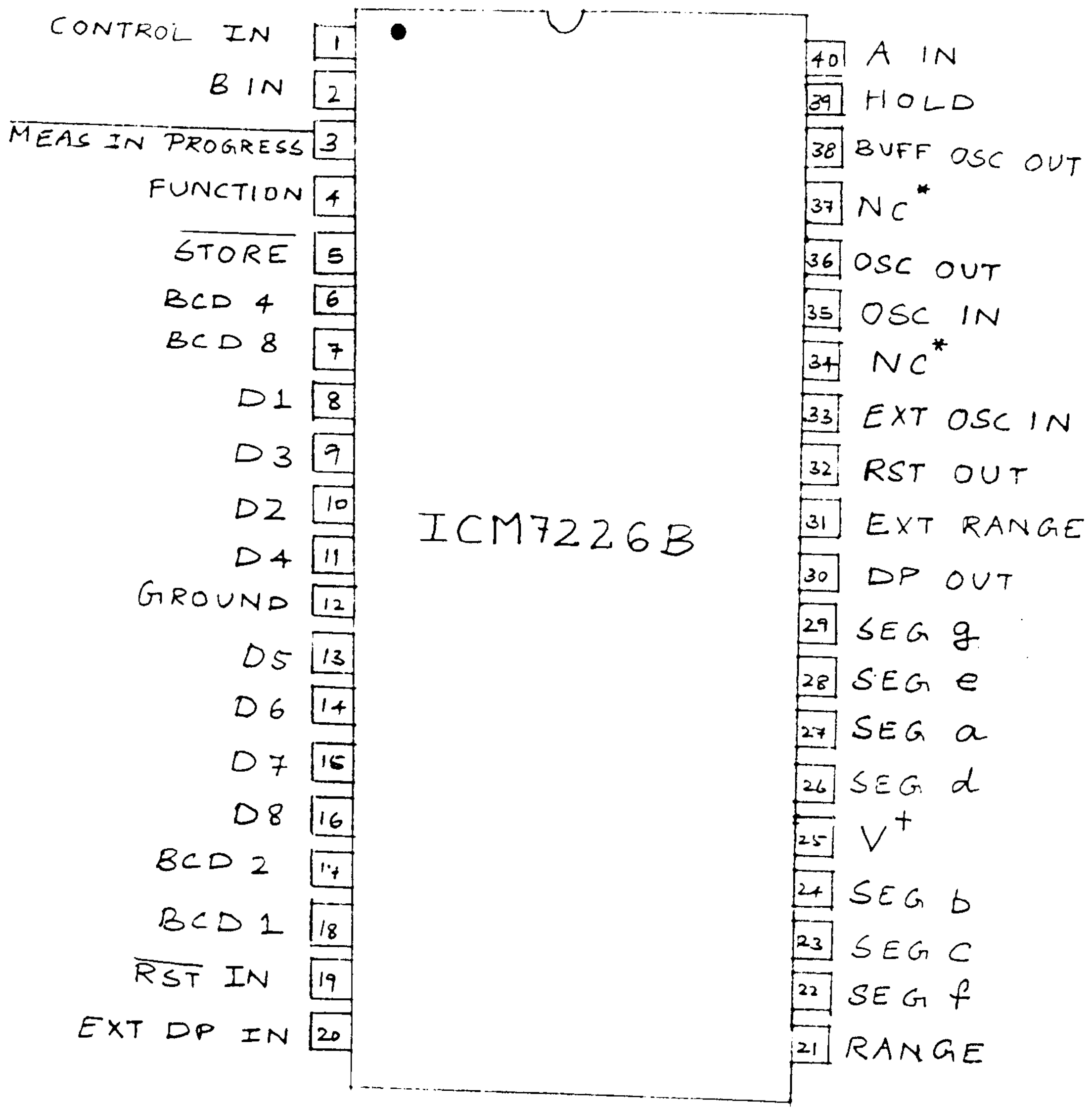


FIGURE : 2 :- BLOCK DIAGRAM OF ICM7226

2.1 BLOCK DIAGRAM OF ICM 7226 B :

As shown in figure.2 we can see that the ICM 7226 B has the different blocks such as the main counter block, two input control logic blocks, a function control logic block, an oscillaton select block, decoder and digits drivers block, a reference 10^3 counter, range control logic block, range select logic block, data latches block, decimal point logic blocks, decoder and LZB logic block and segment drivers block. The different inputs and outputs are also shown in the block diagram.

The different input and outputs are the different pins of the ICM 7226 B. Different opamps and op amp inverters are also shown at the different input and output pins. These are used for the proper operation of Universal counter IC. The different pin numbers are also shown at the different points of the block diagram. Though the block diagram looks a bit complicated, the operation of the circuit is very easy tounderstand.



*For maximum frequency stability, connect to V^+ or GND

FIGURE:3 :- PIN CONFIGURATION OF ICM7226B

2.2 PIN CONFIGURATION OF ICM 7226 B :

The figure.3 shows the pin configuration of the 8-digit counter/timer IC Type ICM 7226 B. This IC is a 40 pin IC. The different functions of the 40 pins are shown in the figure.3. The important pins of the IC are described below.

INPUTS A & B :

The signal to be measured is applied to INPUT A in frequency, period, unit counter, frequency ratio and time interval modes. The other input signal to be measured is applied to INPUT B in frequency ratio and time interval. f_A should be higher than f_B during frequency ratio.

Both inputs are digital inputs with a typical switching threshold of 2.0 V at $V^+ = 5.0$ V and input impedance of 250 KΩ. For optimum performance, the peak to peak input signal should be at least 50% of the supply voltage and centered about the switching voltage, when these inputs are being driven from TTL logic, it is desirable to use a pull up resistor. The circuit counts high to low transitions at both inputs.

The table:2 shows the functions selected by each digit for these inputs.

TABLE:2 MULTIPLEXED INPUT CONTROL

	FUNCTION	DIGIT
FUNCTION INPUT PIN 4	Frequency	D_1
	Period	D_8
	Frequency Ratio	D_2
	Time Interval	D_5
	Unit Counter	D_4
	Oscillator Frequency	D_3
RANGE INPUT PIN 21	0.01 Sec/1 Cycle	D_1
	0.1 Sec/10 Cycles	D_2
	1 Sec/100 Cycles	D_3
	10 Sec/1K Cycles	D_4
	Enable External Range Input	D_5
CONTROL INPUT PIN 1	Blank Display	D_4 & Hold
	Display Test	D_8
	1MHZ Select	D_2
	External Oscillator Enable	D_1
	External Decimal Point Enable	D_3
	Test	D_5
EXTERNAL DECIMAL POINT INPUT, PIN 20	Decimal Point is Output for Same Digit. That is Connected to This Input.	

NOTE :-

The amplitude of the input should not exceed the supply by more than 0.3V otherwise, the circuit may be damaged.

MULTIPLEXED INPUTS :

The FUNCTION, RANGE, CONTROL and EXTERNAL DECIMAL POINT inputs are time multiplexed to select the input function desired. This is acheived by connecting the appropriate digit driven output to the inputs. The input function, range and control inputs must be stable during the last half of each digit output (typically 125 μsec). The multiplex inputs are active high for the common anode ICM 7226 A, and active low for the common cathode ICM 7226 B. Here since we used ICM 7226 B, the multiplex inputs are active low.

Noise on the multiplex inputs can cause improper operation. This is particularly true when the unit counter mode of operation is selected, since charges in voltage on the digit drivers can be capacitively coupled thro the LED diodes to the multiplex inputs. For maximum noise immunity a 10 KΩ resistor should be placed in series with the multiplex inputs.

CONTROL INPUTS :

Display Test - All segments are enabled continuously, giving a display of all 8's with decimal points. The display will be blanked if display off is selected at the same time.

Display off - To enable the display off mode it is necessary to tie D_4 to the CONTROL input and have the HOLD input at V^+. The chip will remain in this mode until HOLD is switched low. While in the display off mode, the segment and digit driver outputs are open and the oscillator continues to run (with a typical supply current of 1.5 mA with a 10 MHz crystal) but no measurements are made. In addition, signals applied to the multiplexed inputs have no effect. A new measurements is initiated after the HOLD input goes low. (This mode does not operate when functioning as a unit counter).

1MHz select - The 1MHz select mode allows use of a 1MHz crystal with the same digit multiplex rate and time between measurements as a 10 MHz crystal. The internal decimal point is also shifted one digit to the right in period and time interval, since the least significant digit will be in, 1µsec increments rather than 0.1µsec.

External Oscillator Enable - In this mode, the EXT ernal OSCillator INput is used, rather than the on-chip oscillator, for the Time base and Main Counter inputs in period and time interval modes. The on-chip oscillator will continue to function when the external oscillator is selected but have no effect on circuit operation.

The external oscillator input frequency must be greater than 100 KHz or the chip will reset itself and enable the on-chip oscillator. Connect external oscillator to both OSC IN (Pin 35) and EXT OSC IN(Pin 33), on provide crystal for "default" oscillation, to aviod hang-up problems.

External Decimal Point Enable - when external point is enabled, a decimal point will be displayed whenever the digit driver connected to the EXTERNAL DECIMAL POINT pin is active. Leading Zero Blanking will be disabled for all digits following the decimal point. Test Mode - This is a special mode used only in high speed production testing and serves no other purpose.

RANGE INPUT :

The range input selects whether the measurement is mode for 1,10,100 or 1000 counts of the reference counter, or if the EXTernal RANGE INput determines the measurement time. In all functional modes except unit counter, a change in the RANGE input will stop the measurement in progress, without updating the display and initiate a new measurement. This prevents an erroneous first reading, after the RANGE input is changed.

FUNCTION INPUT :

Six functions can be selected. They are: Frequency, Period, Time interval, Unit Counter, Frequency Ratio and Oscillator Frequency.

These functions select which signal is counted into the main counter and which signal is counted by the reference counter. In time interval, a flip flop is set first by a 1-->0 transition at INPUT A and then reset by a 1 --> 0 transition at input B.

The oscillator is gated into the Main Counter during the time the flip flop is set. A change in the FUNCTION input will stop the measurement in progress without updating the display and then initiate a new measurement. This prevents an erroneous first reading after the FUNCTION input is changed. If the main counter overflows, an overflow indication is output on the Decimal Point Output during D_8.

EXTERNAL DECIMAL POINT INPUT :

When the external decimal point is selected, this input is active. Any of the digits, except D_8, can be connected to this point. D_8 should not be used since it will override the overflow output and leading zeros will remain unblanked after the decimal point.

HOLD Input - Except in the unit counter mode, when the hold input is at V^+, any measurement in progress (before $\overline{STORE}$ goes low) is stopped, the main counter is reset and the chip is held ready to initiate a new measurement as soon as HOLD goes low. The latches which hold the main counter data are not updated, so the last complete measurement is displayed. In unit counter mode when HOLD Input is at V^+, the counter is not stopped or reset, but the display is forzen at that instantaneous value. When HOLD goes low the count continues from the new value in the counter.

$\overline{RESET}$ Input - The $\overline{RESET}$ Input resets the main counter, stops any measurement in progress and enables the main counter latched, resulting in an all zero output. A capacitor to ground will prevent any hang-ups on power-up.

EXTernal RANGE Input - The EXTernal RANGE Input is used to select other ranges than those provided on the chip. Figure . 4. shows the relationship between $\overline{\text{MEASurementIN PROGRESS}}$ and a EXTernal RANGE Input.

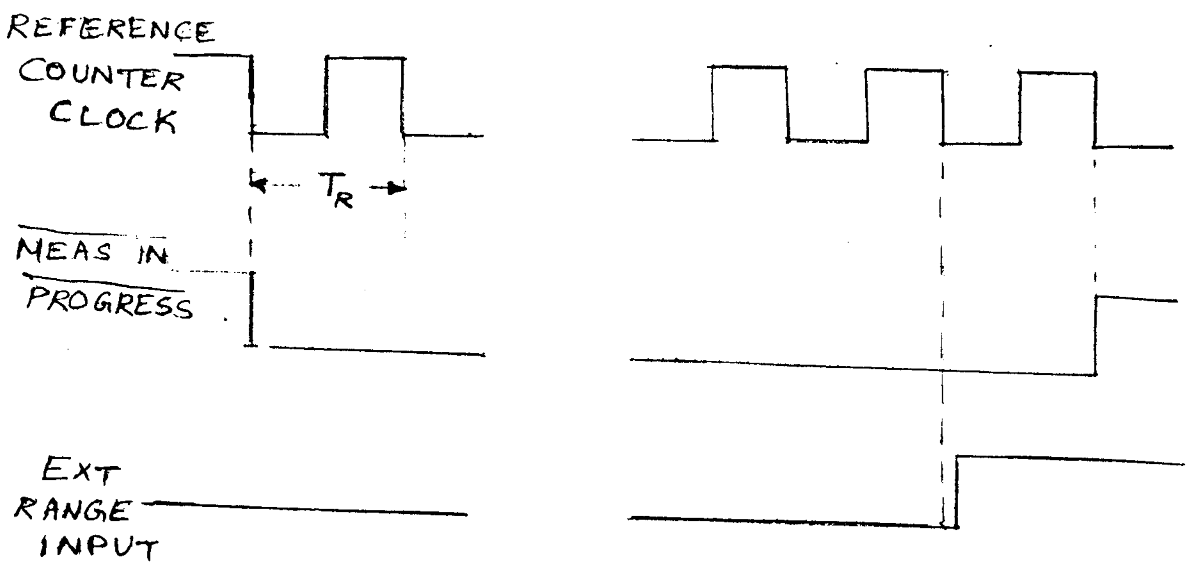


FIG.4: Ext Range input to end of measurement in Progress

MEASUREMENT IN PROGRESS, STORE ND RESET Outputs - These Outputs are provided to facilitate external interfacing. Figure .5 shows the relationship between these signals during the time between measurements. All three outputs can drive a low power schottky TTL load. The MEASUREMENT IN PROGRESS Output can directly drive one ECL load, if the ECG device is powered from the same power supply as the ICM 7226.

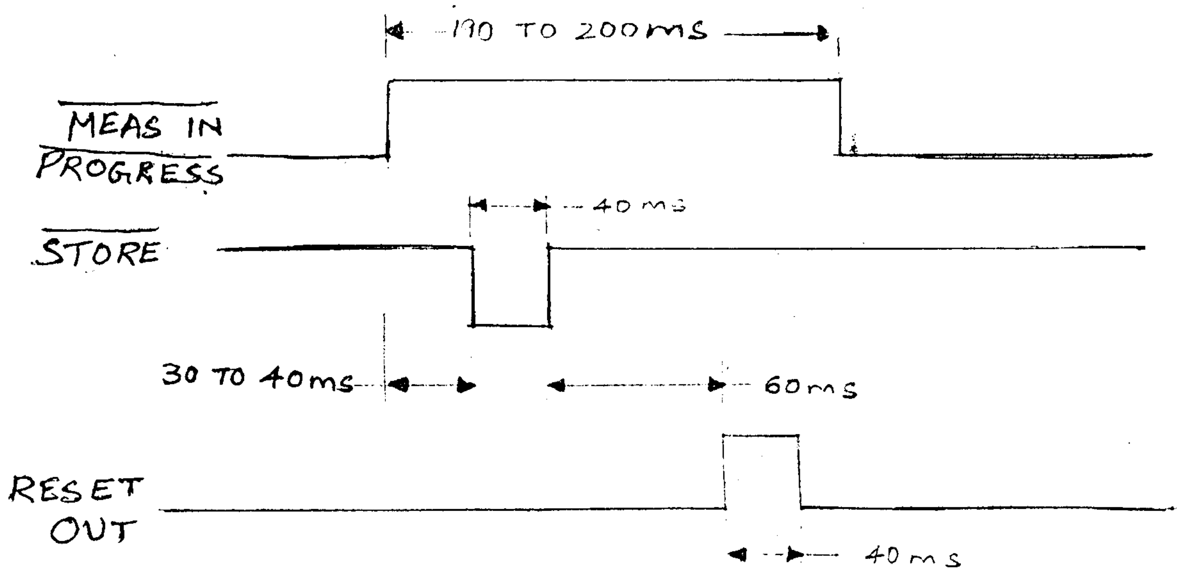


FIG.5: RESET OUT, STORE and MEASUREMENT IN PROGRESS outputs between Measurements

BCD Outputs - The BCD representation of each digit output is available at the BCD outputs. The negative going (ICM 7226B - Common Cathode) digit drivers lag the BCD data by 2 to 6 microseconds; the leading edge of the digit drive signal should be used to externally latch the BCD data. Each BCD output will drive one low power Schottky TTL load and when interfacing low power Schottky TTL latches, it is necessary to use 1KΩ pull down resistors on the TTL inputs for optimum results. The display is multiplexed form MSD to LSD. Leading zero blanking has no effect on the BCD outputs.

BUFFered OSCillator OUTput - The BUFFered OSCillator OUTput has been provided to enable use of the chip oscillator signal without loading the oscillator itself. This output will drive one low power schottky TTL load. Care should be taken to minimize capacitive loading on this pin.

CHAPTER - III

INDIVIDUAL DESCRIPTION OF EACH PART

3.1. THE 8-DIGIT READ-OUT :

The 8-digit read out is shown in figure:6. It is composed of common cathode LED displays multiplexed at 500Hz and a duty factor of 0.122 per digit. Leading (non-significant) zeroes are blanked when the meter is set to frequency measurement in μsec.LED D_9 indicates an overflow condition, i.e., the counter is "full" and all digits read 9.

The decimal point and leading zero blanking have been implemented for right hand decimal point displays; zeroes following the decimal point will not be blanked. Leading zero blanking will also be disabled if the main counter over flows.

To increase the light output from the displays, V^+ can be increased to 6.0 V, but however care is taken to see that maximum power and current ratings are not exceeded.

LD1 --- LD8 = HD11070 ≈ TL 313

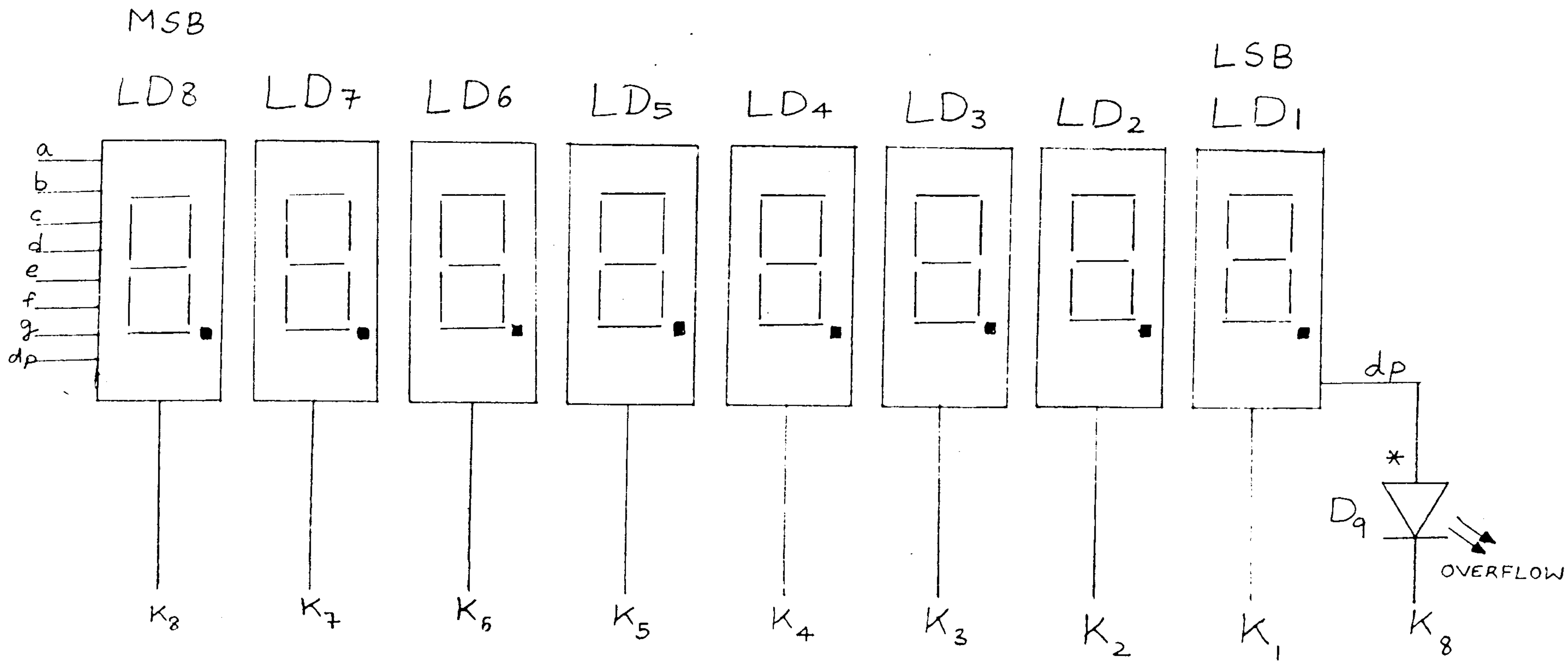


FIG. 6:- THE 8-DIGIT READ OUT

The Segment and Digit outputs in the ICM 7226 B is not directly compatible with either TTL or CMOS logic. Therefore, level shifting with discrete transistors should be used to use these outputs with discrete transistors. External latching should also be done on the leading edge of the digit signal.

3.2. OPTIONAL CONNECTIONS :

The counter, IC_3, has an on-chip time base oscillator which operates at 10 MHz (X_1). It is possible to use a 1 MHz quartz crystal provided S_8 is closed. The 1 MHz select mode allows use of a 1 MHz crystal with the same digit multiplex rate and time between measurements as a 10 MHz crystal. The internal decimal point is also shifted one digit to the right in period and time interval, since the least significant digit will be in 1μs increments rather than 0.1μs.

Similarly, S_7 makes it possible to apply an external clock signal of 100 KHz or more to pin 33. We have to connect external oscillator to both OSC IN (Pin 35) and EXT OSC IN (Pin 33), or provide crystal for "default" oscillator, to avoid hang-up problems.

When switch S_6 is closed, the position of the decimal point on the display is controlled externally via the respective input, pin 20. The decimal point can thus be positioned as required for the prescaler used. Leading zero blanking will be disabled for all digits following the decimal point. These External decimal point, External Oscillator and the 1 MHz select options are connected to ICM 7226 B as shown in the figure 7.

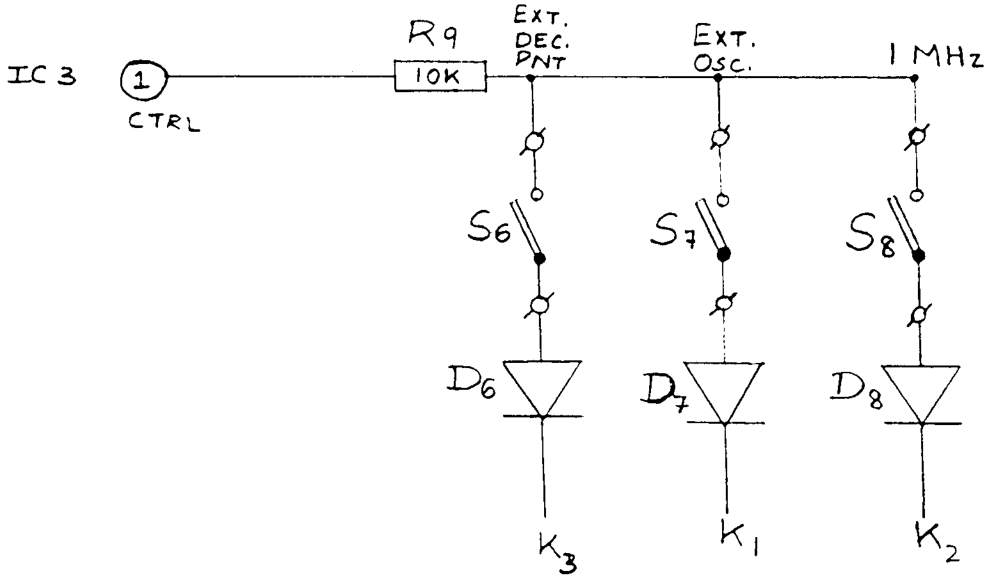


FIGURE. 7: OPTIONAL CONNECTIONS

Switches S_6-S_7-S_8 and the associated diodes, D_6-D_7-D_8 are intended for the above options on the frequency meter and may be omitted when the relevant function is not required. It is, ofcourse also possible to replace the switches with wire links for permanent operation in a particular mode.

3.3. EXTERNAL DECIMAL POINT AND $\overline{\text{RESET}}$ INPUTS :

The functions of the External Decimal Point input and the RESET input of the IC_3 - ICM 7226 B can be explained with the help of figure 8.

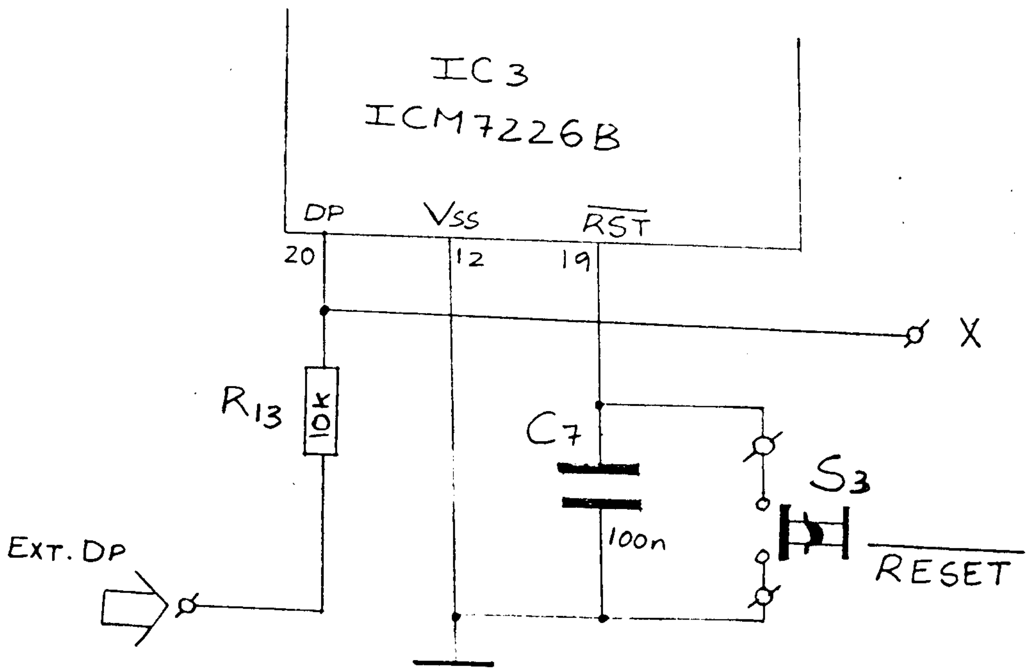


FIGURE. 8: EXT. DP AND RESET INPUTS

When the external decimal point is seleted, this input is active. Any of the digits, except D_8, can be connected to this point. D_8 should not be used since it will over ride the over flow output and leading zeros will remain unblanked after the decimal point.

The counter's internal circuits and hence the read-out-can be cleared at all times by pressing the RESET key S_3. Capacitor C_7 is connected in parallel with S_3 to prevent hang-up's at power on. A push button is fitted on the front panel for this switch S_3. The $\overline{\text{RESET}}$ Input resets the main counter, stops any measurement in progress, and enables the main counter latches, resulting in all zero output.

3.4. INPUTS A AND B :

The maximum input frequency applied to input A of the instrument is 10 MHZ in the frequency and unit count modes, and 2 MHz in the other modes. The input B is only used for measuring frequency ratios and time intervals. The frequency of the signal which is applied to the input A should be higher than that which is applied to the input B. Similiarly, the pulse transition on input A should occur before that on input B. When the inputs are being driven from TTL logic, we use a pullup resistor of 330Ω. The circuit counts high to low transistions at both inputs.

At the inputs A and B, some protective networks are fitted before connecting the inverters. These are shown in the the figure 9 and 10.

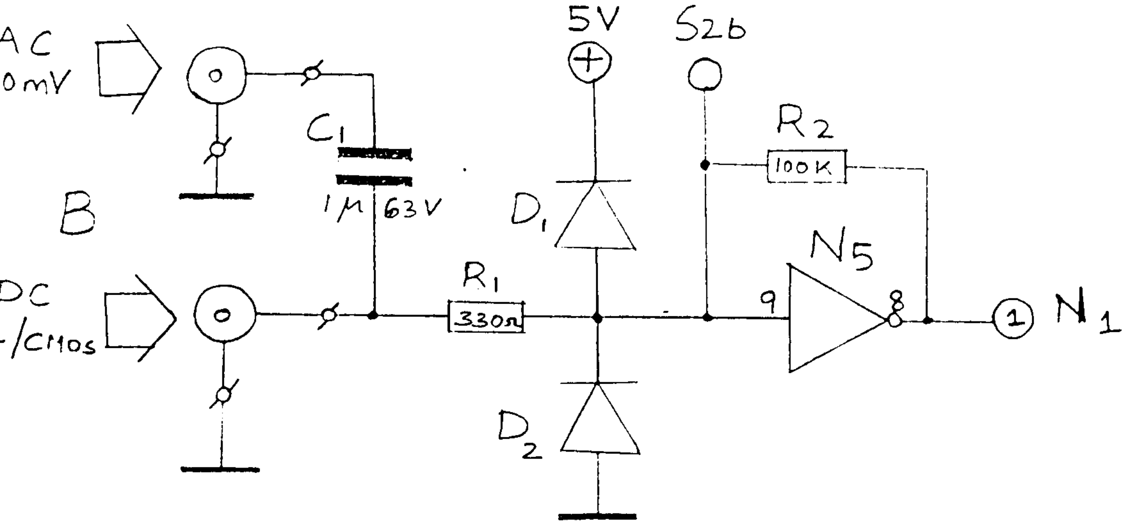


FIGURE. 9 : INPUT B

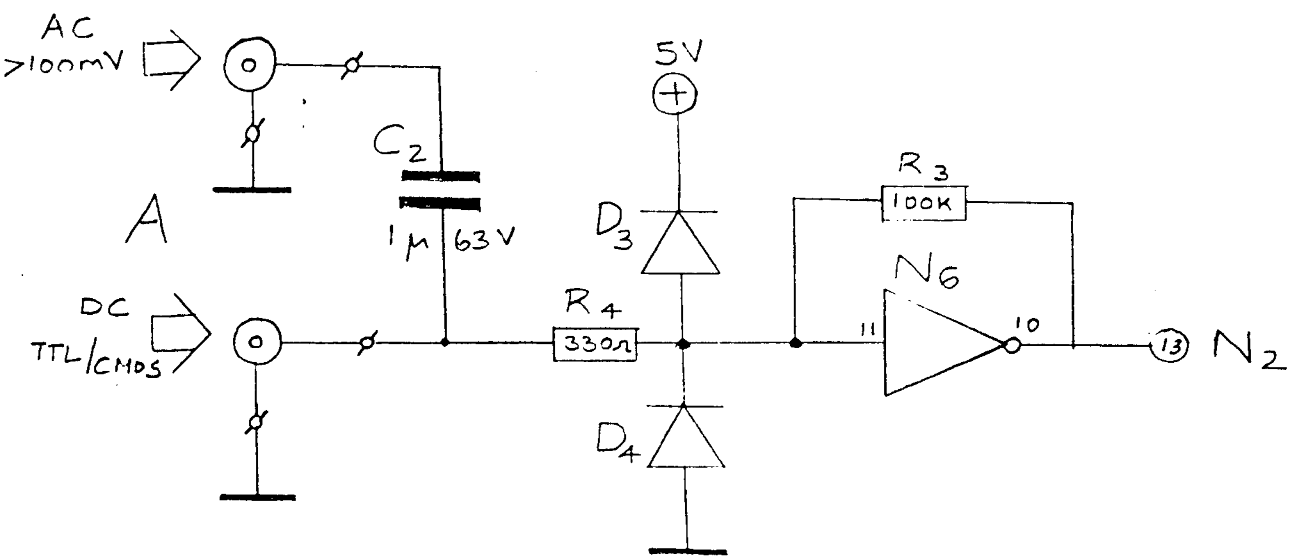


FIGURE.10 : INPUT A

These protective networks fitted at the inputs of the invertors N_5 and N_6 enable applying atternating voltages as well as CMOS or TTL (digital) pulses. For small alternating voltages applied via C_1 - C_2, diodes D_1-D_2 or D_3-D_4 do not have a limiting effect, so that the invertors N_5-N_6 operate as amplifiers. When the input amplitude is greater than about $2V_{pp}$, the inverters operate as buffers.

The limiting of the input signal takes place when the input signal at the digital inputs is lower than -0.6V or higher than +5.6V. This means that AC coupled input voltages are clipped to about 6 V_{pp}. The input sensitivity stated in the circuit diagram is an average and frequency dependent value.

The invertors N_5-N_6 are connections from IC_2. When the type 74HCT04 in position IC_2 is replaced with a 74HCU04 which is Hex invertor the input sensitivity increases by a factor 5 to 10. The value of the capacitors C_1 and C_2 used are 1μ farad ; 63V non electrolitic type capacitors. The diode type 1 N 4148 is used for the Diodes D_1, D_2, D_3 and D_4.

3.5. RANGE AND FUNCTION SWITCHES :

The RANGE and FUNCTION switches connected to the counter IC_3 is shown in the figure.11. The FUNCTION switch S_2 used is a 2-pole 6-way rotary switch. The RANGE switch S_4 used is a 2-pole 4 or 6-way rotary switch.

The counter modes and functions that can be selected with the RANGE switch S_4 a-b, and the FUNCTION switch S_2 a-b, are summarized in Table 3. The position 6 of S_2 is used for checking whether the internal oscillator works, but not for verifying the frequency of oscillation.

The range input selects whether the measurement is made for 1, 10, 100 or 1000 counts of the reference counter or if the EXTernal RANGE INput determines the measurement time. In all functional modes except unit counter, a change in the RANGE input will stop the measurement in progress, without updating the display and initiate a new measurement. This prevents an erroneous first reading after the RANGE input is changed.

There are six functions which can be selected. They are Frequency, Period, Time interval, Unit Counter, Frequency ratio and Oscillator frequency. These functions

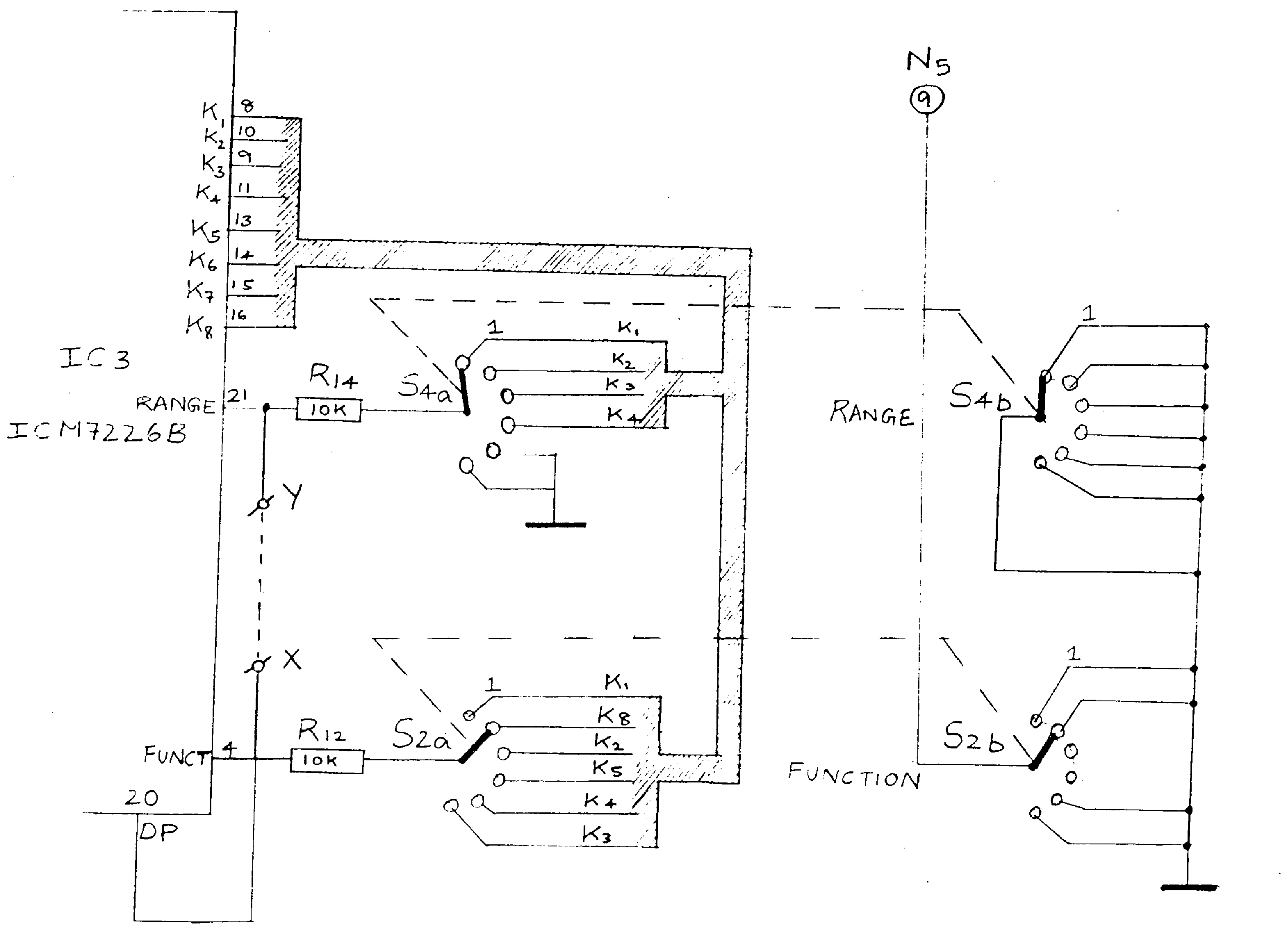


FIGURE. 11: RANGE AND FUNCTION SWITCHES

Table 3:

Switch S_2: FUNCTION

Position	Function
1 (K1)	frequency (f_A)
2 (K8)	period (T_A)
3 (K2)	frequency ratio (f_A/f_B; $f_A > f_B$)
4 (K5)	time interval ($t_A \rightarrow t_B$)
5 (K4)	unit counter
6 (K3)	oscillator test

Switch S_4: RANGE

Position	Accumulation time / cycle(s)
1 (K1)	0.01 s / 1 cycle
2 (K2)	0.1 s / 10 cycles
3 (K3)	1 s / 100 cycles
4 (K4)	10 s / 1,000 cycles

select which signal is counted into the main counter and which signal is counted by the reference counter. A change in the FUNCTION input will stop the measurement in progress without up dating the display and then initiate a new measurement. This prevents an erroneous first reading after the FUNCTION input is changed. If the main counter over-flows, an over flow indication is output on the Decimal Point Output during D_8.

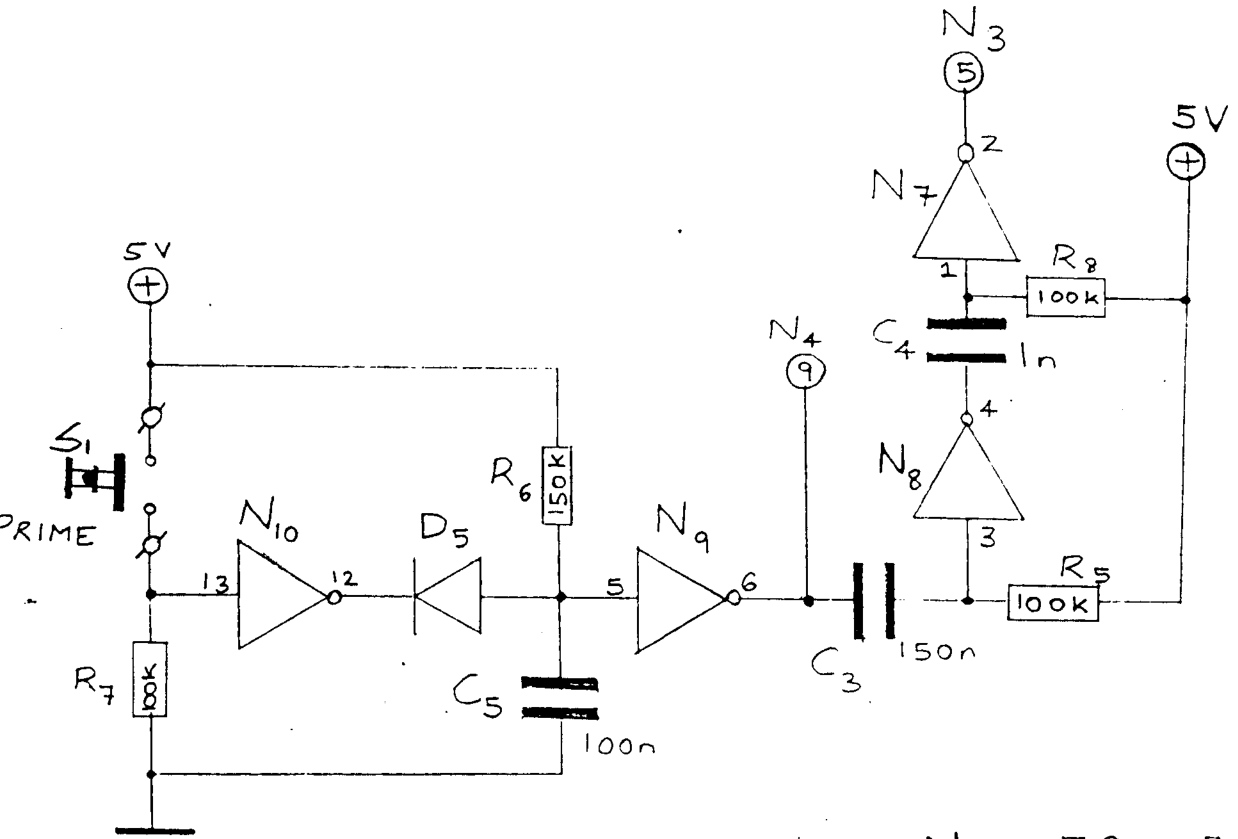
3.6. PRIMING CIRCUIT :

The figure.12 explains the PRIME function of the circuit. A push-button switch is used here. It consists of inverters N_7, N_8, N_9 and N_{10} and XOR gates N_3-N_4 which is shown in the figure.13. The IC 74HCU04 which is an Hex inverter is used for $N_7...N_{10}$. This type of IC has the input and output both buffered and the typical propagation delay of 6 nano seconds. The IC 74HCU04 also has a wide operating temperature range of - 40° c to + 85°C, balanced transition times and a high noise immunity.

The IC used for the XOR gates is 74HC(T)86. This IC is a Quad 2 - Input Exclusive - OR Gate. It has four independent Exclusive - OR gates and it also has buffered inputs and outputs.

The circuit around $N_7...N_0$ incl. and XOR gates N_3-N_4 is used for measuring time intervals, i.e., period that lapses between the positive edges of the signals applied to inputs A and B. A bistable internal to the ICM 7226B is set and reset by the pulse transitions at input A and B respectively.

When the bistable is set, the oscillator pulses are internally fed to the counter input. Evidently, the



$N_5 \ldots N_{10} = IC_2 = 74HCU04$

$D_5 = 1N4148$

FIGURE. 12: PRIMING CIRCUIT

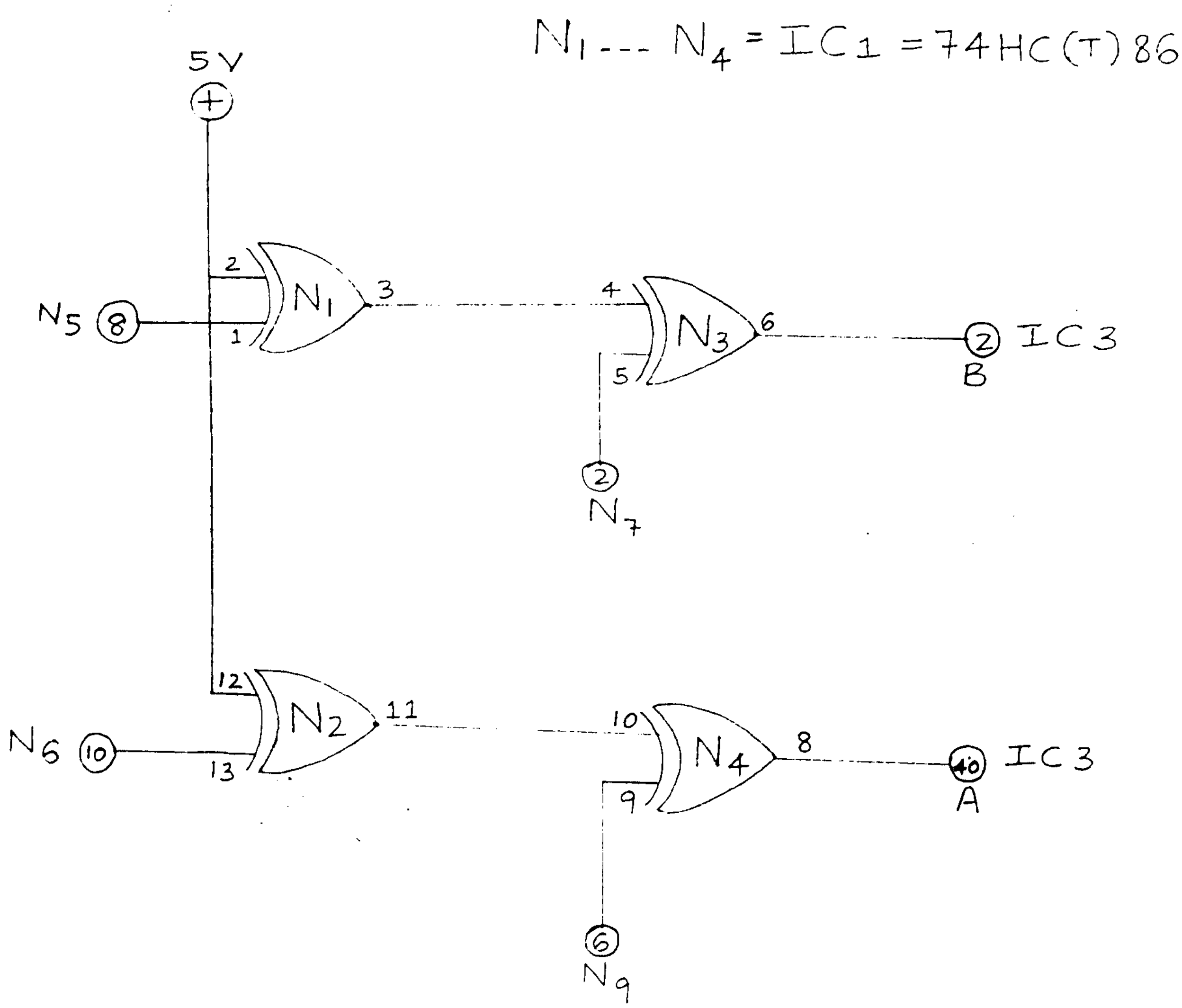


FIGURE. 13: EX-OR GATES CONNECTIONS

longer the bistable remains set, the more pulses are counted, and the higher the read-out on the display. Push-button PRIME is pressed before measuring the time interval for a single event. Inverters N_{10}-N_9 generate a brief pulse for chip in put A.

The inverters N_8-N_7 generate a slightly delayed pulse for input B. The internal logic in the ICM 7226 B is thus primed ready for measuring the interval for one event, delimited by the positive edges of the pulses applied to the instrument input A and input B. Pressing the push-button PRIME is not required when these inputs are driven with a repetitive signal, as the first alternating signal states cause automatic priming of the counter chip.

3.7. HOLD SWITCH AND 10 MHZ CRYSTAL CONNECTIONS :

The figure.14 represents the HOLD switch which is a push-button switch and the 10 MHz crystal connections of the circuit. The read-out can is retained or 'frozen' as long as the HOLD switch S_5 is presssed. Except in the unit counter mode, when the HOLD input is at V^+, any measurement in progress is stopped, the main counter is reset and the chip is held ready to intiate a new measurement as soon as HOLD goes low.

The latches which hold the main counter data are not up dated, so the last complete measurement is displayed. In the unit counter mode when HOLD Input is at V^+, the counter is not stopped or reset, but the display is forzen at that instantaneous value. When HOLD goes low, the count continues from the new value in the counter.

The signal at BUFF. OSC can be used for setting the oscillator frequency to 10.000 MHz precisely with the aid of trimmer capacitor C_9. The value of C_9 used is 40 pico farad.

With a 10 MHz time-base crystal, the time between the two events can be as long as 10 Seconds. Accurate resolution in time interval measurement is 100 nano secs.

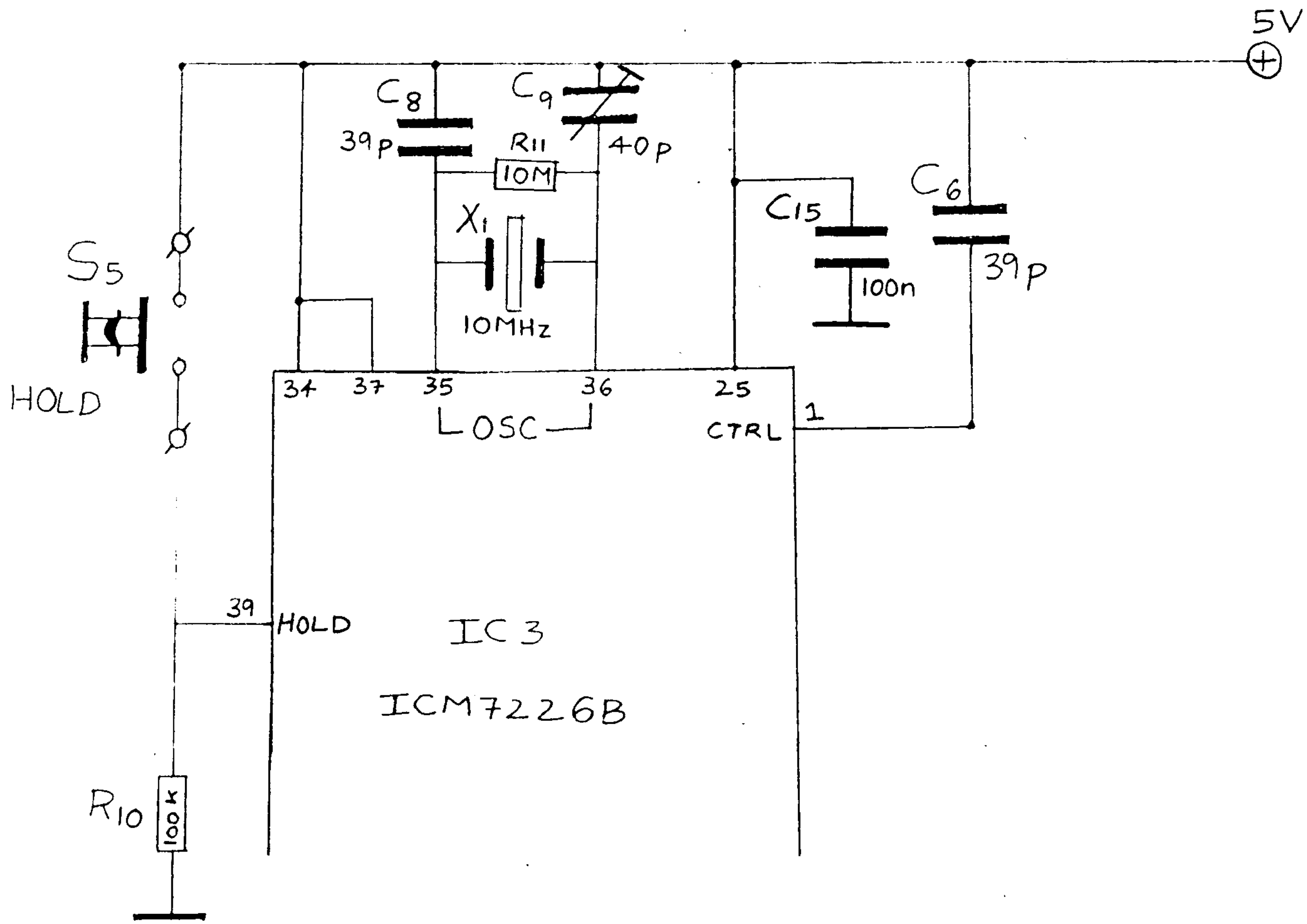


FIGURE. 14: HOLD SWITCH AND 10MHz CRYSTAL CONNECTIONS

3.8 POWER SUPPLY CONNECTIONS FOR THE CIRCUIT :

The circuit connections through which the power is supplied to the circuit is shown in the figure 15. The power supply used is a 5 V power supply and is of conventional design. A variable power supply can be used. The supply is given to pin number 14 of IC_1 and pin number 7 IC_2. The LED D_{14} used is a red LED which glows when the power is ON.

The IC_4 used is a voltage regulator IC 7805. It is a three terminal voltage regulator whose voltage range is 5 V. It will allow over 1.0 A load current if adequate heat sinking is provided. The To-220 type heat sink is used here. Current limiting is included in this IC to limit the peak output current to a safe value.

If the internal power dissipation becomes too high for the heat sinking provided, the thermal shut down circuit takes over preventing the IC from over heating. The capacitors C_{10} and C_{11} used are for filtering purpose.

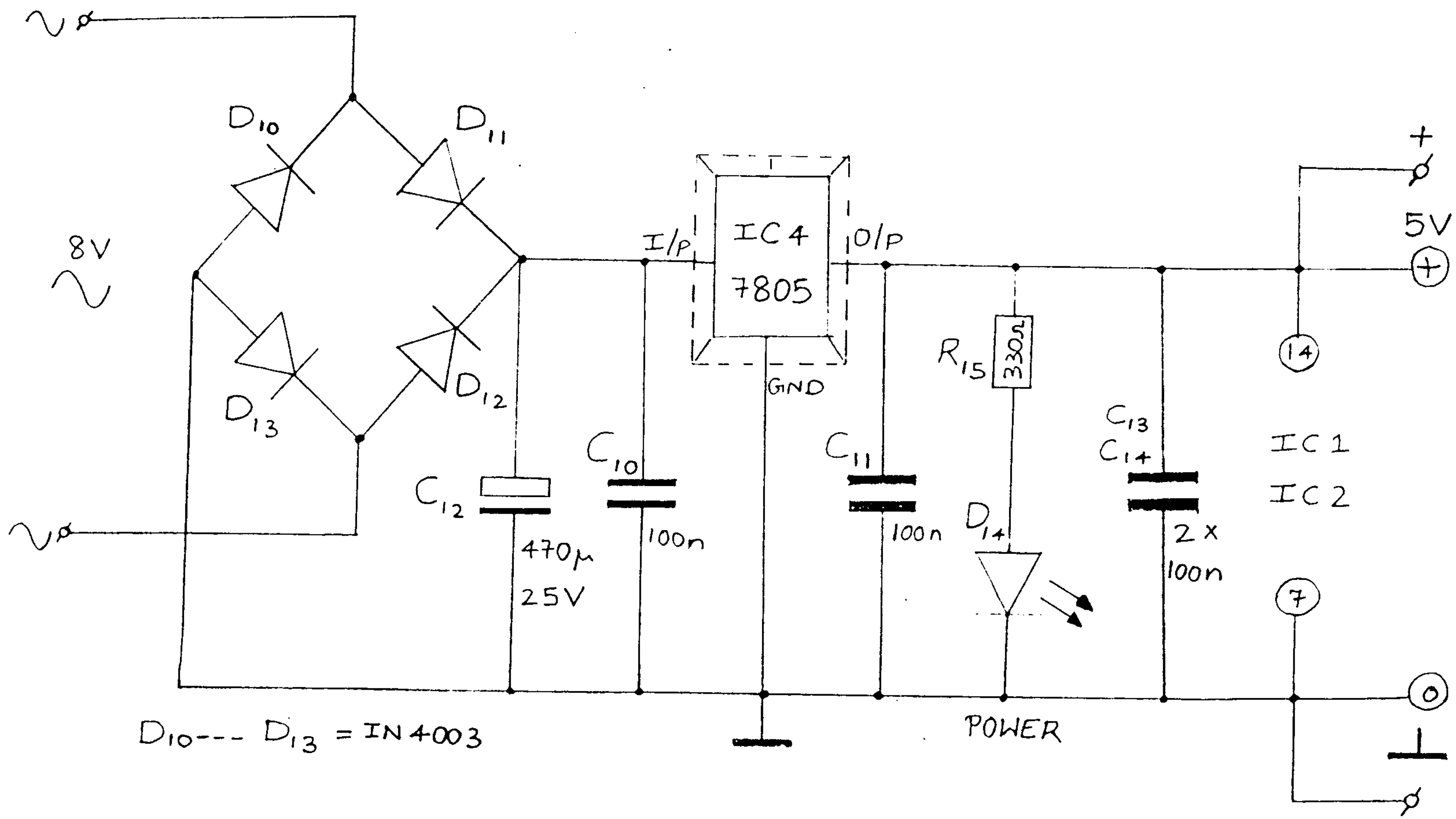


FIGURE. 15: POWER SUPPLY CONNECTIONS.

The brige circuit composed of diodes D_{10} - D_{13} is used for rectification purpose. The mains transformer used in the circuit is a 8 V ; 0.5 A transformer. The resistor R_{15} used in series with the LED is a pull-up resistor. The value of the pull-up resistor R_{15} is 330 Ω.

CHAPTER IV

DESIGN OF THE FRONT PANEL FOIL

The figure.16 shows the lay-out of the front panel foil for the frequency meter. The figure.17 shows the drilling diagram for the front panel. The switch S_2 used for selecting a particular FUNCTION is a 2 pole 6-way rotary switch. The different which can be selected are Frequency, Period, Time Interval, Unit Counter, Frequency Ratio and Oscillator Frequency.

The switch S_4 which is the RANGE selector switch can select for different ranges which are 0.01 Sec/ 1 cycle, .1 sec/10 cycles, 1 sec/100 cycles and 10 sec/1000 cycles. The switch S_4 used can be a 2-pole 4 or 6-way rotary switch. There are two red LEDs used one is a high brilliance red LED used to indicate over flow and the other red LED is used to indicate the power ON.

There are 3-push-button switches S_3, S_5 and S_1 used for RESET, HOLD and PRIME operations respectively. There are 4 BNC sockets used. Two are used for Channel A for AC and DC and the other two are used for channel B for AC and DC respectively.

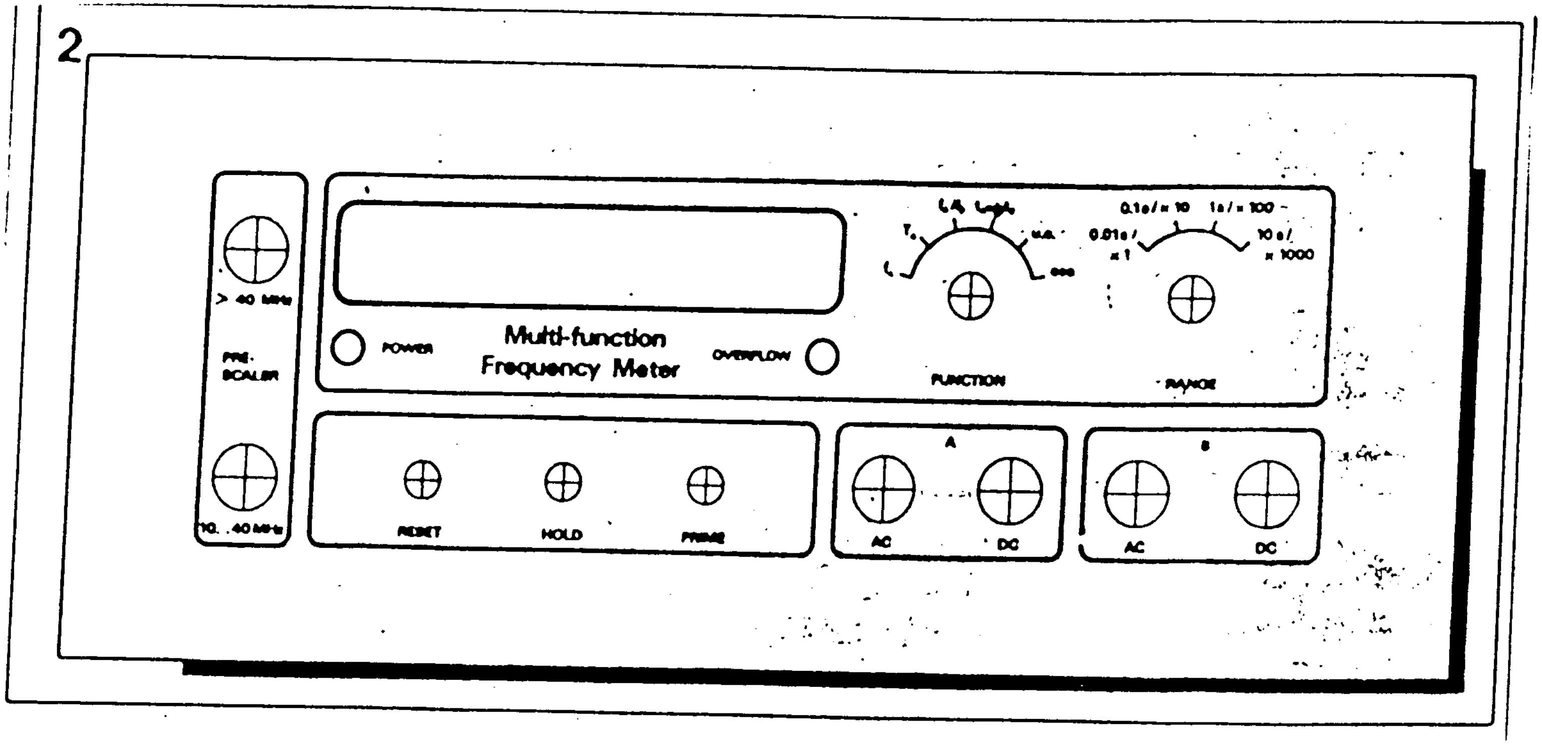


FIGURE 16: LAYOUT OF THE FRONT PANEL FOIL

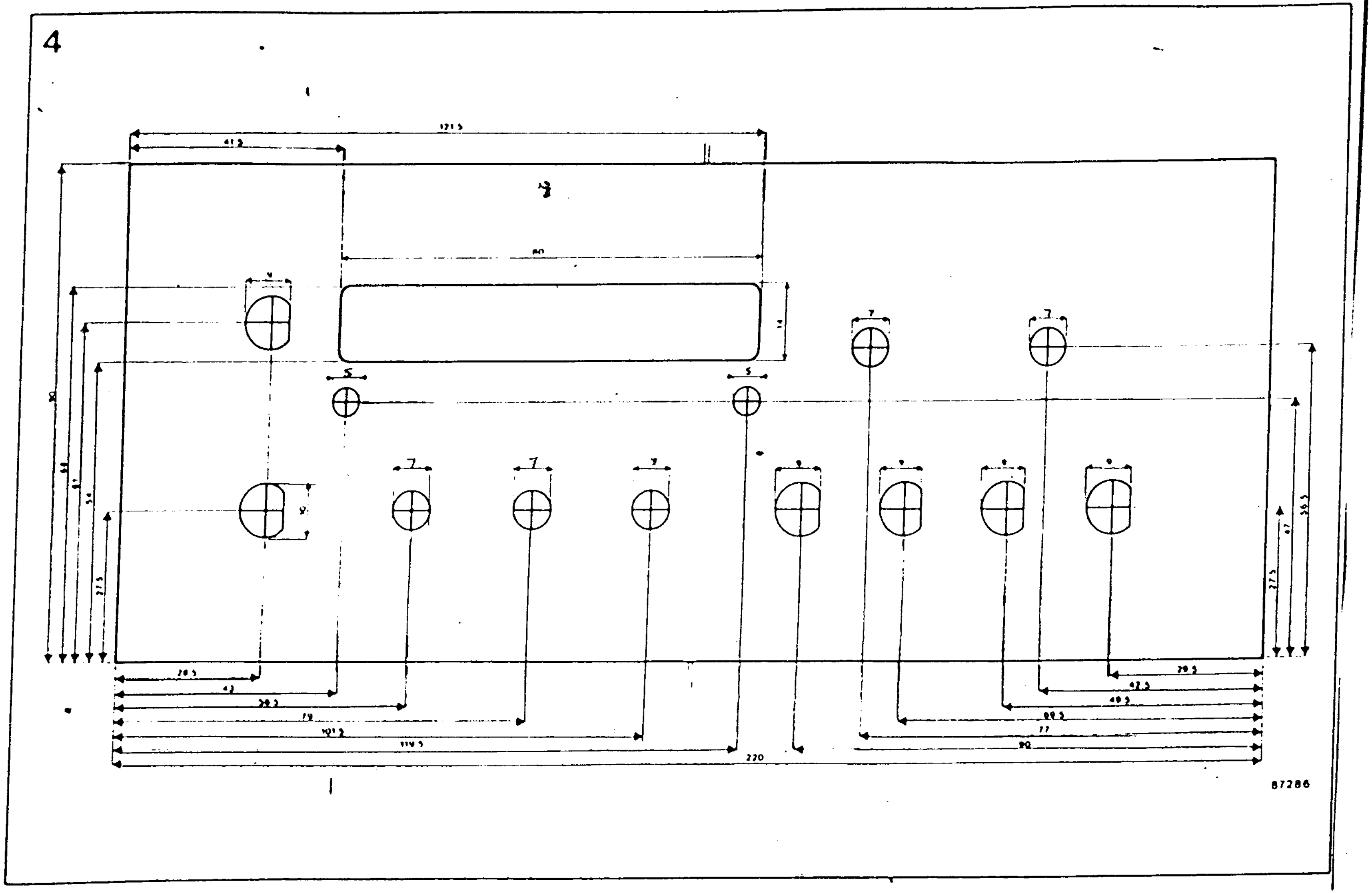


FIGURE. 17 : DRILLING DIAGRAM FOR THE FRONT PANEL

There are two more switches used which are for the operation of the Pre-scaler used. One switch is used when the frequency range is from 10 - 40 MHz and the other switch is used when the frequency goes beyond 40 MHz. There is an 8 cm wide Gap which is provided for the 8 digit display of the frequency meter. An ON/OFF switch is also used for switching the power.

CHAPTER - V

CONSTRUCTION OF THE CIRCUIT

Virtually all parts shown in the circuit diagram are fitted on a single printed circuit board. The figures 18 and 19 show the track lay out and the component mounting plan of the printed circuit board respectively.

PRINTED CIRCUIT BOARD DESIGN :

Printed circuit boards are generally used for laying out complex digital circuits.

The Common problems which we meet with if not properly designed are listed as follows :

1. Reflections (causing signal delays and also double pulsing i.e. conversion of one pulse into two or more pulses.

2. Cross talk (inter ference between neibhouring signal lines).

3. Ground and supply line noise.

4. Electro magnetic interference from pulse type EM fields (under high noise conditions).

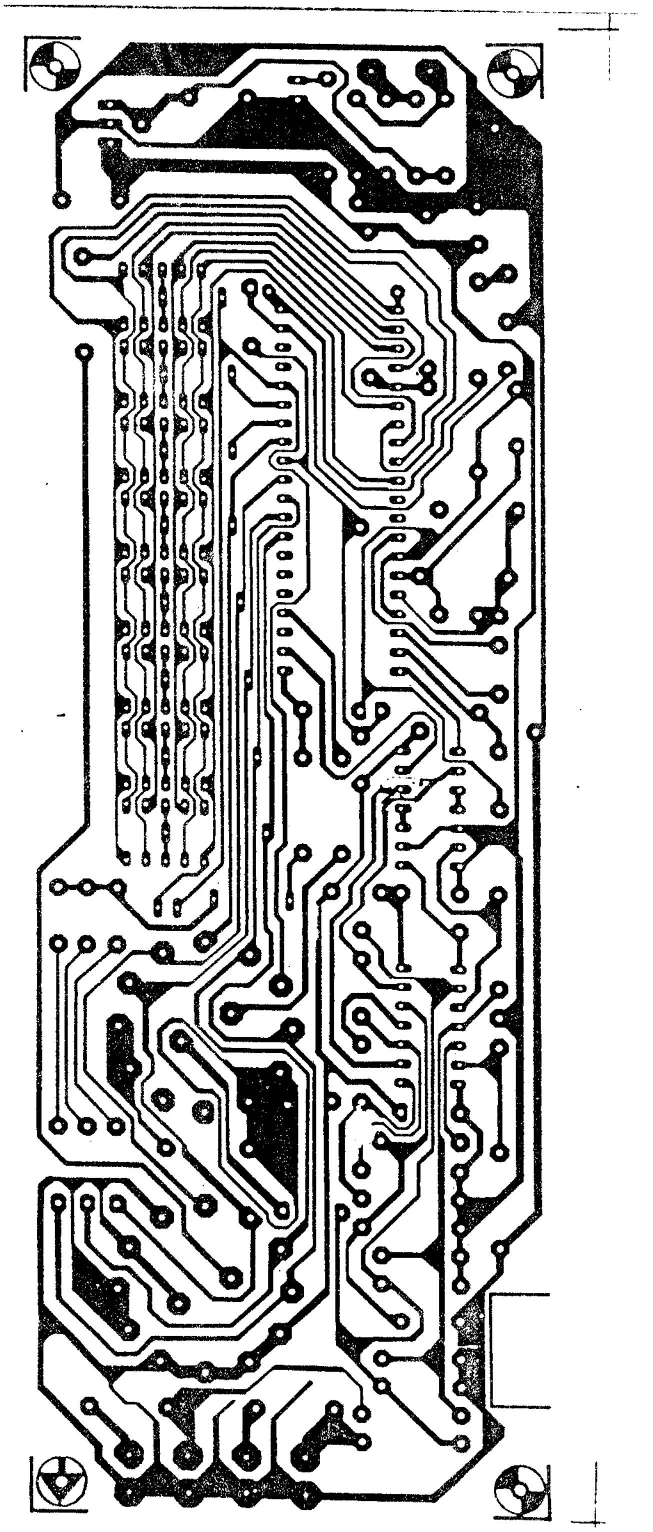


FIGURE. 18 : TRACK LAY-OUT OF THE PCB.

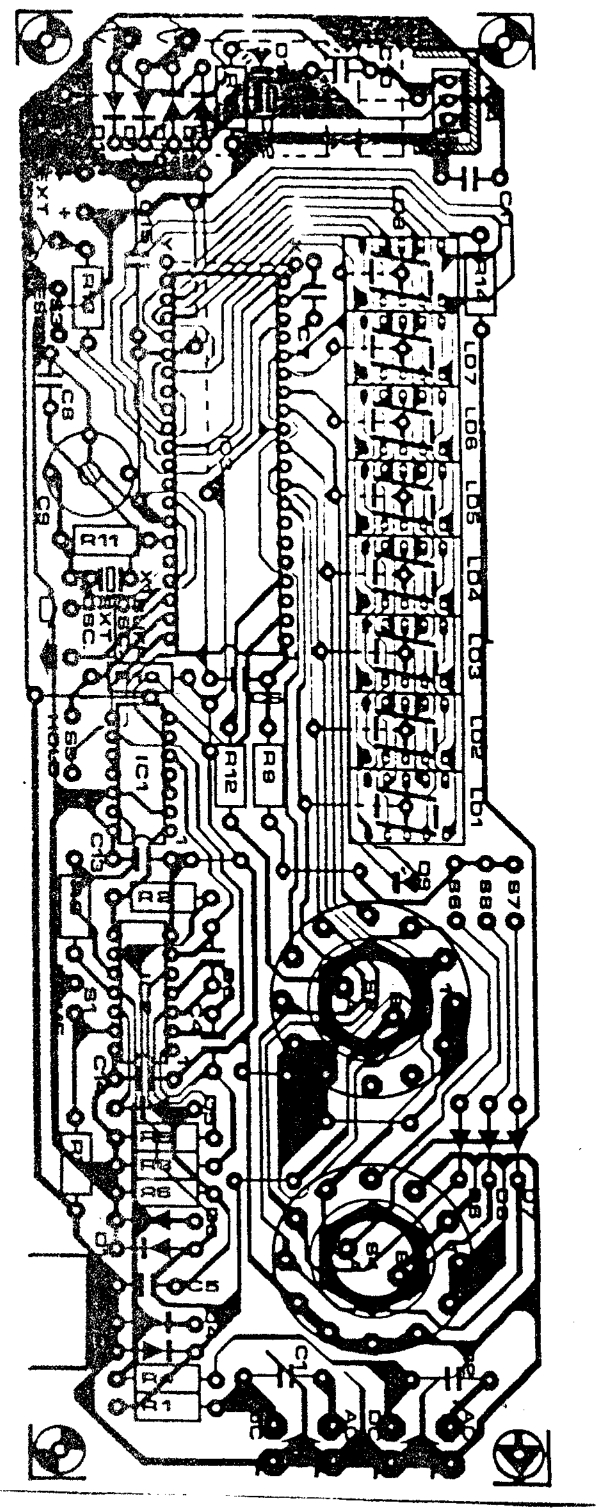


FIGURE. 19 : COMPONENT MOUNTING PLAN.

REFLECTIONS :

In families of fast t_r(rise time) of IC's the conductors must be looked as a piece of transmission lines rather than short circuits. The transmission lines are normally mismatched on both sides so that multiple reflections take place based on the particular value of wave impedance of the conductor.

While designing, the main points to be looked is that it must be having a proper value of wave impedance a value which has least reflections.

This wave impedance is chosen by selecting the width of the signal lines lower values of wave impedance such as needed in ECL IC's require broader signal conductors. Relatively larger value of wave impedance as needed by TTL, CMOS etc., require small width signal conductors. As in a digital circuit we are having a low operating frequency, double pulsing can't be tolerated. The double pulsing is the result of reflections.

For TTL logic, a wave impedance of 100 to 150 is desirable. The signal lines hence is 0.5 mm wide. The standard width of PCB dielectric is 1.6 mm. The signal lines can be even 1 mm wide only if the ground lines are farther away.

Current drawn or sunk back into the IC will be very large 20 mA and -55 mA for 50 line PCB for the rising and trailing edges respectively. These currents spikes have to be supplied by the V_{cc} line, (rising edge) or fed to the ground lines (trailing edge). Hence, in TTL PCB's wave impedance of 50 or less must be avoided.

Very high impedance such as 7200γ also cause problems making voltage as well as double pulsing very high. Hence, in TTL IC's loose wiring (high impedance) must be avoided and signal connections must run always near the ground line.

For CMOS circuits, broad PCB conductors for signal lines is avoided. The wave impedance must be high and the signal line width is 0.5 mm. If the wave impedance is 150 to 300 ohms, the transition will be considerably faster. The above value can be obtained if signal line width is low, the ground lines are not too broad and kept too near the signal lines. In the wiring between PCB's one should defintely avoide using 50 ohm cables and also the wave impedance must be high.

CROSS TALK :

The considerations that cross talk can be kept low are uncritical. If a ground line or a ground plate is nearby. A ground line that runs between two signal lines eliminates almost all cross talk and should be used when ever the situation becomes too critical. A special problematric situation occurs, when signal lines run next to each other with a logical flow(signal flow) on opposite directions. There it will be generally advisable to run a ground line between the two signal lines, specially for the more critical cases of TTL and ECL IC's.

GROUND AND SUPPLY LINE NOISE :

This is perhaps the most serious problem with TTL - IC's and is present in reduced from with ECL-IC's and in very much reduced form, with C-MOS IC's. This problem can definitely be solved with proper PCB lay out and with a few, very simple measures.

The two principal measures are :

a) To have a low inpedance Z_w between proper supply line and ground line. This is obtained by providing a large copper surface for ground either full ground broad as it is possible in the case of multilayer boards or at least a ground mesh of finally leaving the copper in all unused parts of PCB such as corners etc., and connecting it to the ground.

Current spikes are drawn from the Vcc line and fed into the ground line during the IC's transition. These current spikes are partly needed to charge or discharge the transistor within the IC while they switch and this current is referred as internal current spike which is required to charge or discharge the transmission lines(i.e., conductors) connected to the IC's output. Internal and external spike are super imposed and must be carried by the same Vcc and ground lines. If many synchronous gates or flip-flops are connected to the same point, the situation becomes even worse. Thus ground and supply line noise is reduced.

The construction is commenced with fitting all the wire links. Care should be taken tht the 8 short wire links underneath the displays are also fitted. The electrolytic capacitor C_{12} is fitted at the track side of the board. It is fitted securely and slightly off the board to prevent sharp solder points piercing the insulating material and causing short circuits with the grounded metal can. It is advantageous to use only good quality sockets for all integrated circuits.

The displays can either be connected directly to the printed circuit board or they can also be fitted in 10-way sockets, made from terminal strips or 14-way IC sockets. Short lengths of strong wire is used to ensure the correct height of the displays above the board. D_9 is a high brilliance type whose leads are lengthened and its top is made in level with the displays in the sockets.

The voltage regulator IC_4 is mounted with a To-220 type heat-sink. The RANGE and FUNCTION switches S_4 and S_2 are soldered direct on to the board, or with short length of component wire, to minimize stray inductance and capacitance. This effectively prevents the unwanted effects such as indeterminate illumination of digits ("ghosting").

As already stated, the function switches S_6, S_7 and S_8 are not required on the front panel of the instrument. The inputs A and B are made in flange-type or single hole BNC sockets. Two more of these are required when it is intended to extend the frequency meter with the prescaler.

The signal of BUFF,OSC can be used for setting the oscillation frequency to 10 MHz precisely with the aid of the trimmer cpacitor C_9. It is also possible to use the signal for driving other circuits, providedthe BUFF.OSC output is fitted with a 10K resistor to the +5V rail.

The supply voltage for the prescaler is available on 2 soldering pins next to the EXT.DP output.

The shafts of the rotary switches, S_2 and S_4, are cut to size to enable fitting suitable knobs. The LED displays are fitted in a rectangular clearance cut in the front panel. The visibility of the read-out is enchanced by the semi-transparent bezel in the front panel foil. The overflow indicator, D_9 if fitted immediately below the right had side of the display bezel.

It is intended to furnish the frequency meter with its own, internal mains supply, the mains socket and fuse (100 mA) should be fitted at safe locations. The mains transformer should be preferably an 8V, 0.5A type. The current consumption of the circuit is about 55mA with all displays blanked, and 175mA will all displays illuminated.

CHAPTER - VI

1.2 GHz PRESCALER

This 1.2 GHz prescaler is an add-on board that extends the usable frequency range of the instrument from 10 MHz to well over 1.2 GHz. The prescaler described here is intended as an optional extension of the multifunction frequency meter.

There are various ways of adding a prescaler to an existing frequency meter. The simplest of these is based on the assumption that the instrument is mainly intended for measuring relatively low frequencies, indicated on a kilohertz (KHz) scale. Fitting a prescaler with a divisor of 1,000 to the input of such a frequency meter effectively changes the KHz scale into a MHz scale, obviating the need for changing the position of the decimal point, The main disadvantage of the above method is the reduction by 1,000 of the meter's resolution.

A better approach entails increasing the gate time of the counter by a factor 1,000. This results in more count pulses fed to the counter circuits, and hence re-tains the formerly available resolution. The gate time of a frequency meter is determined primarily by the output frequency of the central clock oscillator, which is quartz-controlled in most cases.

The oscillator frequency is scaled down internally to obtain the required gate time. Inserting, for instance, a binary scaler between the clock output and the internal divider cascade results in a doubling of the gate time, so that the measured signal must be passed through a ÷ 2 divider also. These applications are often thought to be restricted to the use of decade scalers, while in practice any other division works equally well.

6.1 BLOCK DIAGRAM OF THE PRESCALER :

The present prescaler is designed for ready connection to the multi-function frequency meter without compromising its usability in other, similar instruments.

Figure.20 shows the block diagram of the prescaler circuit. With reference to the block diagram of fig.18, electronic switches ES_5, ES_6 and ES_7 select between 10MHz, 1.2 MHz and 78.125 KHz at point E. The switches are controlled by signal detectors on the input channels.

The existing 10 MHz input on the multi-function frequency meter is retained along with the 2 prescaler inputs, so that the complete instrument has 3 frequency, ranges in all.

A seperate 10...40 MHz input is used in view of the reduced sensitivity of the $\div$ 64 prescaler in this frequency range. The sensitivity of the $\div$ 64 prescaler is highest at around 250 MHz. The use of the 10...40 MHz input is also advantageous because it enables the use of relatively short gate periods.

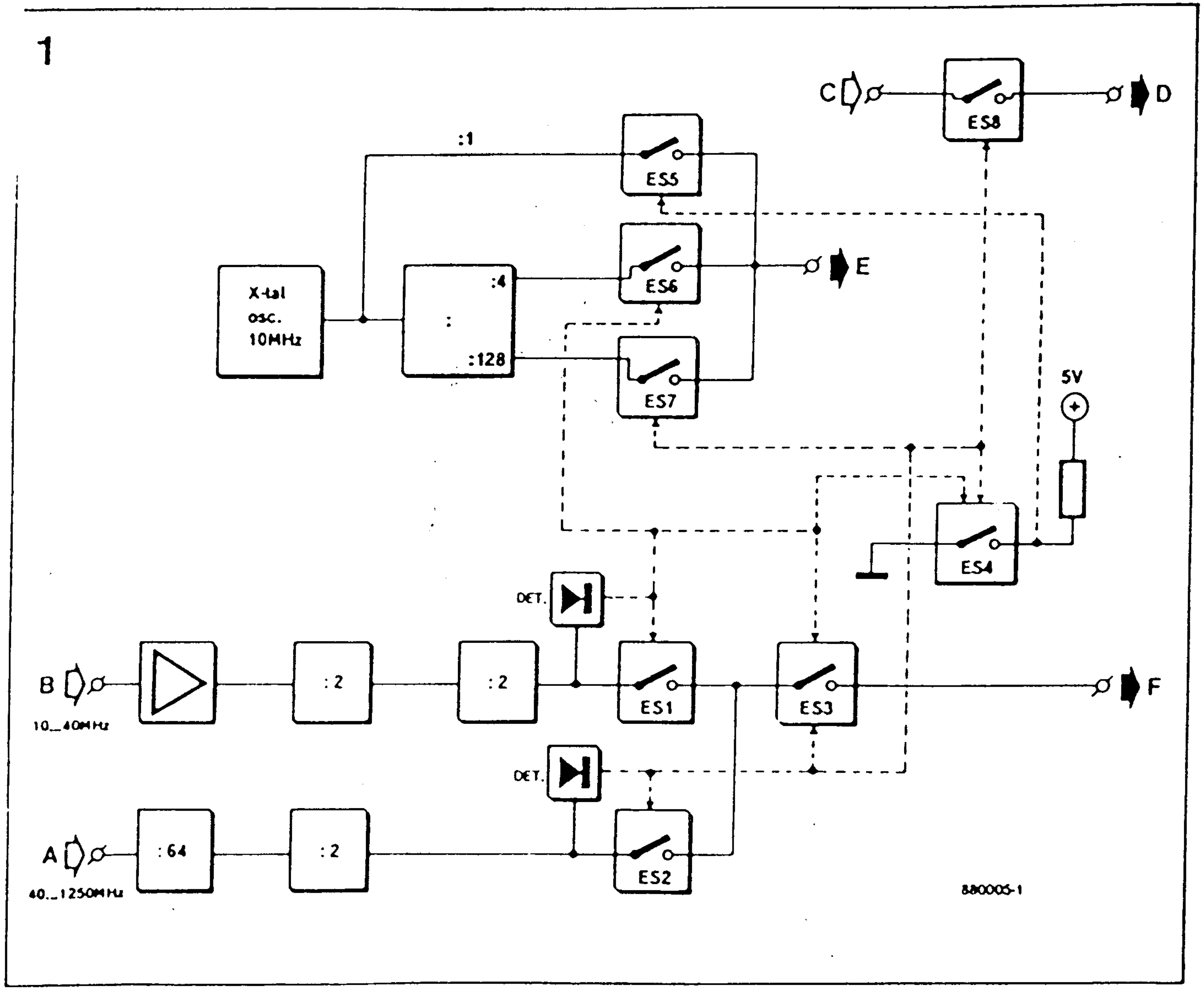


FIGURE.20: BLOCK DIAGRAM OF 1.2GHz PRESCALER

With the greatest divisor, 128, the available gate periods are in the range from 0.14 to 140 sec. Detector controlled switches ES_1 and ES_2 arrange the correct selection or disconnection of prescaler outputs on the 10 MHz input of the main frequency meter. ES_4 functions as an inverter, while ES_8 takes care of the "mode" settings, and the shifting of the decimal point.

The switch configurations for the 3 frequency ranges of the meter are as follows.

Switch (ES)	1	2	3	4	5	6	7	8
Range (MHz) 40-1250	X	.	.	.	X	X	.	.
40-40	.	X	.	.	X	.	X	X
< 10	X	X	X	X	.	X	X	X

X : Switch opened

. : Switch closed

6.2. PREPARING FOR THE EXTENSION :

A few simple modifications are required on the main frequency meter board before the prescaler extension can be used.

With reference to figure 1, the power for the prescaler is available from the terminals + and $\perp$ at the output of the regulated 5V supply on the frequency meter board. The AC coupled input of channel A on the frequency meter, point F, accepts the prescaler output signal. The divided or undivided clock signal from the prescaler board is connected to the EXT.OSC input of IC_3 (Point E). Points X and Y are connected by a wire link as shown.

The configuration switch S_7 is replaced by a wire link. Remove S_6 and S_8, since their functions are taken over by ES_8 on the prescaler board. Connect the anodes of D_6 and D_8 to create point D. Point C in the prescaler circuit is connected to junction R_9-A_{D7}. The 10 MHz crystal may be removed for re-use in the oscillator on the prescaler board. Figure 21 and figure 22 shows the locations of various points and connections on the frequency meter board.

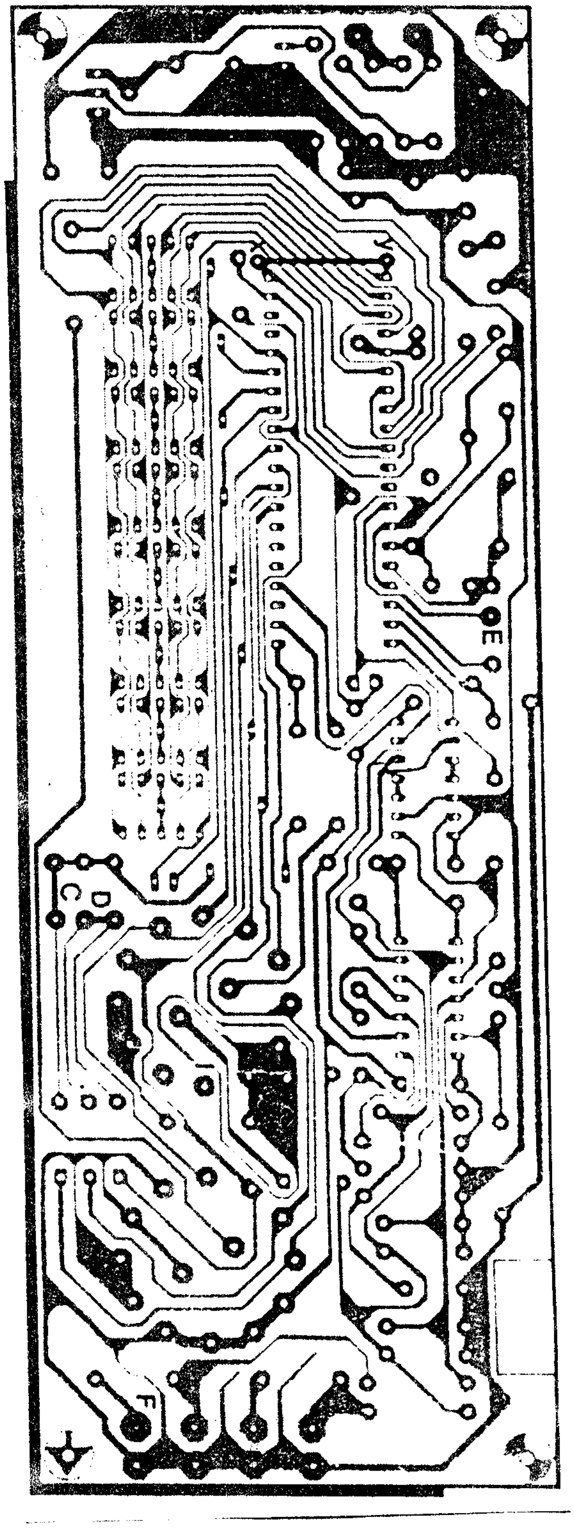


FIGURE .2.1 : TRACK LAY-OUT OF THE PCB

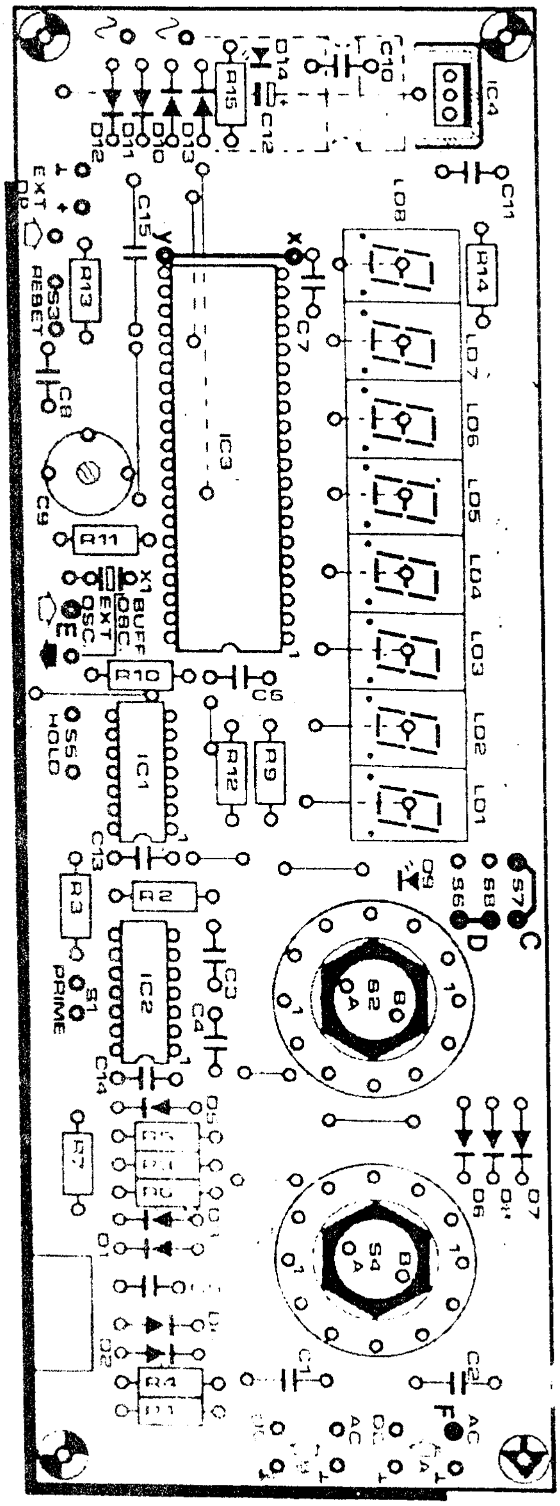


FIGURE. 22: COMPONENT MOUNTING PLAN.

CHAPTER VII

CIRCUIT DESCRIPTION OF THE PRESCALER :

The main functional blocks in the prescaler discussed under the block diagram are readily found back in the circuit diagram of figure 23. The crystal oscillator which is a 10 MHz crystal and the buffer T_1-T_2 where T_1 is a transistor BF 494 and T_2 is a dual-gate MOSFET BF982 which is used in the VHF, UHF range, ensures the required stability of the 10 MHz digital signal applied to counter IC_1 which is a 74HCT 4024 and the electronic switch ES_5.

The IC_1 which is a 74HCT 4024 IC, is a 7-stage Binary Ripple Counter. All counter stages are Master-slave flip-flops. The state of the stage advances one count on the negative transition of each input pulse; a high voltage level on the MR line resets all counters to their zero statge. All inputs and outputs are buffered. It has fully static operation and common reset. It has a wide operating temperature range of -40 to +85°C. It has balanced propagation delay and transition times and a high noise immunity.

The electronic switch ES_1...ES_4 are utilised from a single IC which is IC_6. The IC used is 74HCT 4066. The electronic switches ES_5....ES_8 also form IC_7 which is also a 74HCT 4066 IC. The 74HCT 4066 is a high-speed CMOS logic Quad Bilateral switch. It contains four independent digitally controlled analog switches that use silicon-gate CMOS technology to acheive high operating speeds and it has low power consumption. Each switch is turned ON by a high-level voltage on its control input. It has a wide analog-input-voltage range of 0-10 V. It has low "ON" resistance, fast switcing and propagation delay times and low "OFF" leakage current. It has a wide operating temperature range of -40 to +85°C and high noise immunity.

The binary ripple outputs Q_2 ($\div 2^2 = 4$) and Q_7 ($\div 2_7 = 128$) of IC_1 carry the 2.5 MHz and 78.125 KHz clock signal, respectively.

The signals applied to the 10...40 MHz input are amplified in fast op amp $IC_2$and divided by 4 in bistables FF_1 ($\div 2$) and FF_2($\div 2$).

The IC_2used is a differential video amplifier. It is a two stage, differential input, differtential output, wide band video amplifier. The use of internal series-shunt feedback gives wide band width with low phase distortion and high gain stability. Emitter follower output provide a high current drive, low impedance capability.

It's 120 MHz bandwidth and selectable gains of 10, 100 and 400, without need for frequency compensation, make it a very useful circuit for memory element drivers, pulse amplifiers and wide band linear gain stages. It has a 250 KΩ input resistance and a high common mode rejection ratio at high frequencies. The LM 733 is specified for operation over the -55°C to +125°C temperature range for military purpose and 0°C to +70°C for general purposes.

The FF_1 and FF_2 are available in a single IC chip. Similarly FF_3 and FF_4 are also available in an IC chip. The IC used is 74HCT74. It is a high-speed CMOS logic Dual D flip-flop with set and Reset and positive Edge Trigger. This flip-flop has independent DATA, $\overline{\text{SET}}$, $\overline{\text{RESET}}$ and CLOCK inputs and Q and $\overline{Q}$ Outputs. The logic level present at the data input is transferred to the output during the positive-going transition of the clock pulse.

$\overline{\text{SET}}$ and $\overline{\text{RESET}}$ are independent of the clock and are accomplished by a low level at the appropriate input. It has a wide operating temperature range of -40°C to +85°C, balanced propagation delay and transition times and high noise immunity. The main type features of this IC are hysterisis on clock inputs for improved noise immunity and increased input rise and fall times, Asynchronous set and reset, complementary outputs and buffered inputs.

The preset P_1 which is a 4K7 preset H enables accurate setting of the bistable's switching threshold to 2.5 V, The rectifier (signal detector) for controlling the electronic switches as discussed is formed by diodes D_3, D_4 and D_7, together with R-C combination R_9-C_{12}.

The signals in the frequency range of 40...1250 MHz are applied direct to $\div$64 prescaler IC_4 a type U664B from AEG- Telefunken . The bistable FF_3 divides by 2, so that the total divisor on this channel is 128. The function of the rectifier and the threshold preset is similar to that of the corresponding circuits in the 10 ... 40 MHz channel. The dashed lines in the circuit diagram denote metal screens fitted to prevent stray radiation and erroneous meter readings caused by digital interference.

CHAPTER - VIII

CONSTRUCTION OF THE PRESCALER

The first components which are fitted on the prescaler board are lead less ceramic capacitor C_{13} and C_{14}. Both disc and rectangular versions can be used in these positions. The values of C_{13} and C_{14} are 1n0.

Figure 24 shows the track lay-out and the component mounting plan for the prescaler circuit PCB. Required slots are cut in the PCB to push the capacitors, the pre-tinned sides to the relevent copper areas are carefully soldered. Soldering is done fast and accurately; leadless ceramic capacitors are relatively brittle components and hence it is advantageous to use them.

The next some what unusual part is prescaler IC_4. Precision pliers are used to carefully bend the 8 pins of this IC over 180° and the chip is mounted at the track side of the board by observing the orientation indicated on the component over-lay. If bending the pins is considered risky, it is also possible to mount the IC at the component side of the PCB, provided a suitable clearance is cut. What ever mounting method is adopted, the connections to the prescaler pins should be as short as possible.

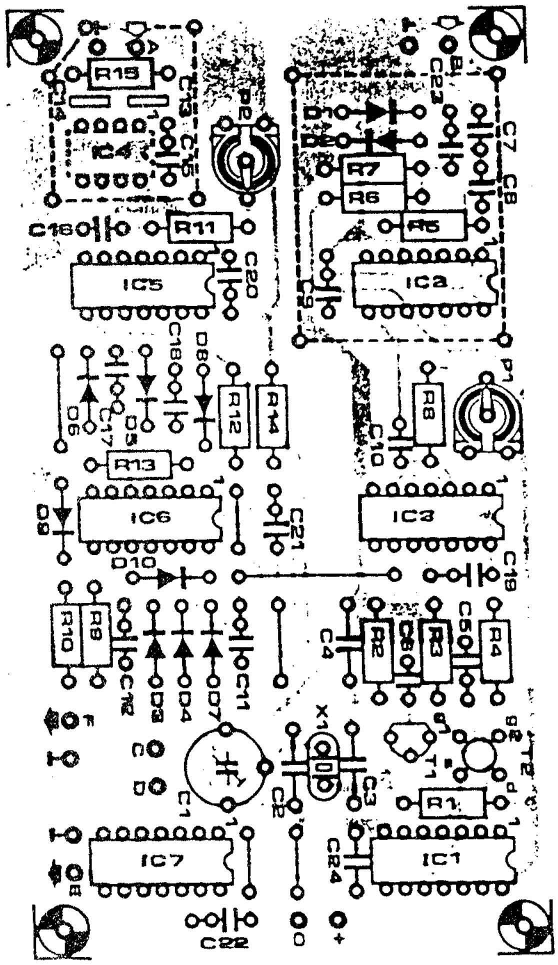


FIGURE. 24 : PRESCALER PCB.

The fitting of the remaining components on the prescaler board is straight forward. It is recommended to use sockets for the 6 IC's. The metal screens at the component side of the PCB are made of 15mm high brass or tin metal sheet, bent to shape and secured with the aid of soldering pins.

The screening of the VHF/UHF prescaler is "continued"at the track side of the PCB. The connections between the BNC sockets and the prescaler inputs are made in thin(Ø3mm) coaxial cable. The connection of the centre cores to the prescaler inputs are kept as short as possible. The shielding braid of the 40.....1250MHz input cable is soldered direct to the screening plate at the track side. Copper foil is used to shield the connections of the BNC sockets to the coaxial cables.

It is recommended to make the connections between the prescaler and the main frequency board in coaxial cable, with the exception of the supply wires. The completed prescaler board is fitted vertically behind the main frequrncy meter baord. Finally, it is made sure that the mains adoptor can handle the additional current drain of the prescaler board.

CHAPTER - IX

SETTING UP OF THE INSTRUMENT :

The setting up of the extended frequency meter is fairly simple if a signal source of 10.....40MHz and 40.....1250MHz is available. To begin with, the clock oscillation is set to 10,000 MHz precisely with the aid of a second, calibrated, frequency meter.

A test signal is applied at a frequency higher than 40MHz to the prescaler input A, and the generator output is reduced untill the read-out becomes unstable. P_2 is adjusted to restore the correct read-out, the input signal is reduced, and P_2 is re-adjusted and so on, untill the optimum threshold setting is achieved. The sensitivity of the prescaler's B input is set like wise.

A carefully aligned prototype of the frequency meter can achieve a sensitivity of about 400mVrms at 1190MHz.

CHAPTER - X

CONCLUSION

The ICM7226B has been designed as a stand alone universal counter, or used with prescalers and other circuitary in a variety of applications. Since A IN and B IN are digital inputs, additional circuitry is required in many applications for input buffering amplification, hysteresis and level shifting to obtain the required digital voltages. For many applications a FET sources follower can be used for input buffering and an ECL 10116 line receiver can be used for amplification and hysteresis to obtain high impedance input, sensitivity and band width.

However, cost and complexity of this circuitry can vary widely, depending upton the sensitivity and band width required. Prescalers can be designed even for frequency measurement well above 1.2 GHz say upto the micro wave ranges also. But the important problem faced is the availability of components which work at these frequencies. In case of the 1.2 GHz prescaler used in this project, an important IC-U664 B was not available and hence, some otehr arrangements were made. U664 B is a ÷ by 64 counter from AEG Telefunken distributors in UK. Instead, ÷ by16 counters were cascaded to obtain the result. But in this case the speed of the equipment became very low. Hence the improvement of this project ot higher frequency ranges will be very advantageous for micro wave applications, provided the components needed are available in the market.

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9. LINEAR - Data Book

FROM NATIONAL SEMICONDUCTORS CORPORATION.

INTERSIL

ICM7226A/B

10MHz Universal Counter System for LED Displays

FEATURES

- CMOS design for very low power
- Output drivers directly drive both digits and segments of large 8 digit LED displays. Both common anode and common cathode versions are available
- Measures frequencies from DC to 10MHz; periods from 0.5μs to 10s
- Stable high frequency oscillator uses either 1MHz or 10MHz crystal
- Control signals available for external systems operation
- Multiplexed BCD outputs

APPLICATIONS

- Frequency Counter
- Period Counter
- Unit Counter
- Frequency Ratio Counter
- Time Interval Counter

ORDERING INFORMATION

DISPLAY	DEVICE	PACKAGE	ORDER NUMBER
Common Anode	ICM7226A	CERDIP	ICM7226AIJL
		DICE	ICM7226A/D
Common Cathode	ICM7226B	Plastic	ICM7226BIPL
		DICE	ICM7226B/D

NOTE: An evaluation kit is available for these devices — order ICM7226AEV/KIT.

GENERAL DESCRIPTION

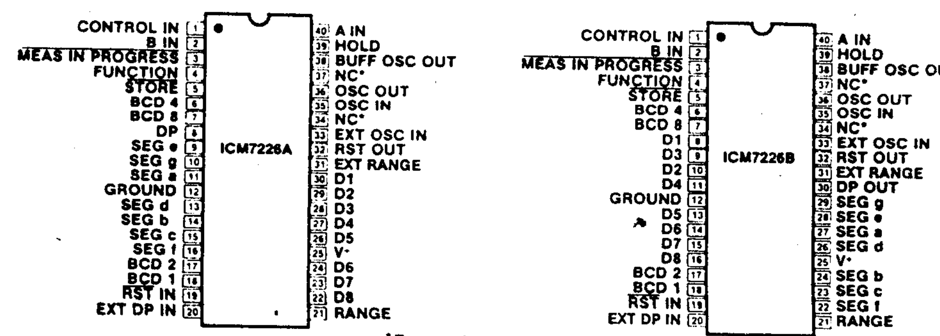
The ICM7226 is a fully integrated Universal Counter and LED display driver. It combines a high frequency oscillator, a decade timebase counter, an 8 decade data counter and latches, a 7 segment decoder, digit multiplexer, and segment and digit drivers which can directly drive large LED displays. The counter inputs accept a maximum frequency of 10MHz in **frequency** and **unit counter** modes and 2MHz in the other modes. Both inputs are digital inputs. In many applications amplification and level shifting will be required to obtain proper digital signals for these inputs.

The ICM7226 can function as a frequency counter, period counter, frequency ratio (f_A/f_B) counter, time interval counter or a totalizing counter. The devices require either a 10MHz or 1MHz crystal timebase, or if desired an external timebase can also be used. For **period** and **time interval**, the 10MHz timebase gives a 0.1μsec resolution. In **period average** and **time interval average**, the resolution can be in the nanosecond range. In the **frequency** mode, the user can select accumulation time of 10ms, 100ms, 1s and 10s. With a 10s accumulation time, the frequency can be displayed to a resolution of 0.1Hz. There is a 0.2s interval between measurements in all ranges. Control signals are provided to enable gating and storing of prescaler data.

Leading zero blanking has been incorporated with frequency display in kHz and time in μs. The display is multiplexed at a 500Hz rate with a 12.2% duty cycle for each digit. The ICM7226A is designed for common anode display with typical peak segment currents of 25mA, and the ICM7226B is designed for common cathode displays with typical segment currents of 12mA. In the **display off** mode, both digit drivers & segment drivers are turned off, allowing the display to be used for other functions.

6

PIN CONFIGURATION (outline dwgs JL, PL)



*For maximum frequency stability, connect to V+ or GROUND

ICM7226A/B

INTERSIL

ABSOLUTE MAXIMUM RATINGS

Maximum Supply Voltage 6.5V
Maximum Digit Output Current 400mA
Maximum Segment Output Current 60mA
*Voltage on any Input or
Output Terminal (Note 1) .... Not to exceed V$^+$ or GND by more than 0.3V
Maximum Power Dissipation at 70°C (Note 2)
ICM7226A 1.0W
ICM7226B 0.5W
Maximum Operating Temperature Range .... −20°C to +85°C
Maximum Storage Temperature Range .... −55°C to +125°C
Lead Temperature (soldering, 10 seconds) .... 300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

***Note 1:** Destructive latchup may occur if input signals are applied before the power supply is established or if inputs or outputs are forced to voltages exceeding V$^+$ or GROUND by 0.3V.

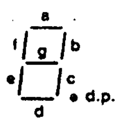
Note 2: Assumes all leads soldered or welded to PC board and free air flow.

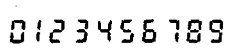
ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: V$^+$ = 5.0V, Test Circuit, T_A = 25°C, unless otherwise specified.

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Operating Supply Current	I_{OP}	Display Off Unused inputs to GROUND		2	5	mA
Supply Voltage Range	V_{SUPP}	-20°C < T_A < 85°C Input A, Input B Frequency at f_{MAX}	4.75		6.0	V
Maximum Guaranteed Frequency Input A, Pin 40	$f_{A(max)}$	-20°C < T_A < 85°C 4.75V < V$^+$ < 6.0V Figure 1 Function = Frequency, Ratio, Unit Counter Function = Period, Time Interval	10 2.5	14		MHz
Maximum Frequency Input B, Pin 2	$f_{B(max)}$	-20°C < T_A < 85°C 4.75V < V$^+$ < 6.0V Figure 2	2.5			MHz
Minimum Separation Input A to Input B Time Interval Function		-20°C < T_A < 85°C 4.75V < V$^+$ < 6.0V Figure 3	250			ns
Maximum osc. freq. and ext. osc. freq. (minimum ext. osc. freq.)	f_{osc}	-20°C < T_A < 85°C 4.75V < V$^+$ < 6.0V	(0.1)	10		MHz
Oscillator Transconductance	g_m	V$^+$ = 4.75V T_A = +85°C	2000			μs
Multiplex Frequency	f_{mux}	f_{osc} = 10 MHz		500		Hz
Time Between Measurements		f_{osc} = 10 MHz		200		ms
Minimum Input Rate of Charge	dV_{in}/dt	Inputs A, B		15		mV/μs

SEGMENT IDENTIFICATION AND DISPLAY FONT





LED overflow indicator connections:
Overflow will be indicated on the decimal point output of digit 8.

	CATHODE	ANODE
ICM7226A	d.p.	D_8
ICM7226B	D_8	d.p.

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ELECTRICAL CHARACTERISTICS (Continued)

TEST CONDITIONS: V⁺ = 5.0V, test circuit, T_A = 25°C, unless otherwise specified.

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
INPUT VOLTAGES PINS 2,19,33,39,40,35 input low voltage	V_{IL}	-20°C < T_A < +70°C	1.0			V
input high voltage	V_{IH}				3.5	V
PIN 2, 39, 40 INPUT LEAKAGE, A, B	I_{ILK}				20	μA
Input resistance to V⁺ PINS 19,33	R_{IN}	V_{IN} = V⁺ −1.0V.	100	400		kΩ
Input resistance to GROUND PIN .·	R_{IN}	V_{IN} = +1.0V	50	100		kΩ
Output Current PINS 3,5,6,7,17,18,32,38	I_{OL}	V_{OL} = +0.4V	400			μA
PINS 5,6,7,17,18,32	I_{OH}	V_{OH} = +2.4V	100			μA
PINS 3,38	I_{OH}	V_{OH} = V⁺ −0.8V	265			μA
ICM7226A PINS 22,23,24,26,27,28,29,30 DIGIT DRIVER high output current	I_{OH}	V_O = V⁺ −2.0V	150	180		mA
low output current	I_{OL}	V_O = +1.0V		−0.3		mA
SEGMENT DRIVER PINS 8,9,10,11,13,14,15,16 low output current	I_{OL}	V_O = +1.5V	25	35		mA
high output current	I_{OH}	V_O = V⁺ −1.0V		100		μA
MULTIPLEX INPUTS PINS 1,4,20,21 input low voltage	V_{IL}				0.8	V
input high voltage	V_{IH}		2.0			V
input resistance to GROUND	R_{IN}	V_{IN} = +1.0V	50	100		kΩ
ICM7226B DIGIT DRIVER PINS 8,9,10,11,13,14,15,16 low output current	I_{OL}	V_O = +1.0V	50	75		mA
high output current	I_{OH}	V_O = V⁺ −2.5V		100		μA
SEGMENT DRIVER PINS 22,23,24,26,27,28,29,30 high output current	I_{OH}	V_O = V⁺ −2.0V	10	15		mA
leakage current	I_L	V_O = GROUND			10	μA
MULTIPLEX INPUTS PINS 1,4,20,21 input low voltage	V_{IL}				V⁺ −2.0	V
input high voltage	V_{IH}		V⁺−0.8			V
input resistance to V⁺	R_{IN}	V_{IN} = V⁺ −1.0V	200	360		kΩ

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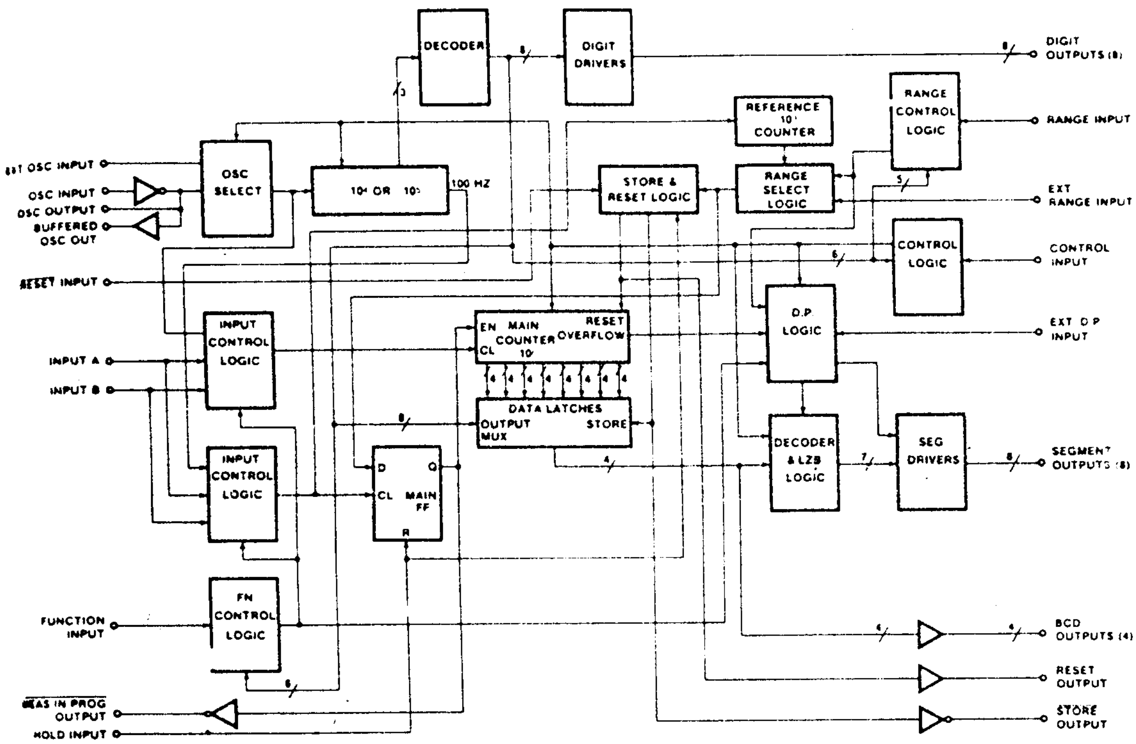
EVALUATION KIT

An evaluation kit is available for the ICM7226. It includes all the components necessary to assemble and evaluate a universal frequency/period counter based on the ICM7226. With the help of this kit, an engineer or technician can have the ICM7226 "up-and-running" in less than an hour. Specifically, the kit contains an ICM7226AIJL, a 10MHz quartz crystal, eight each 7-segment 0.3" LEDs, PC board, resistors, capacitors, diodes, switches and IC socket. Order Number ICM7226AEV/Kit.

ICM7226A/B

INTERSIL

BLOCK DIAGRAM



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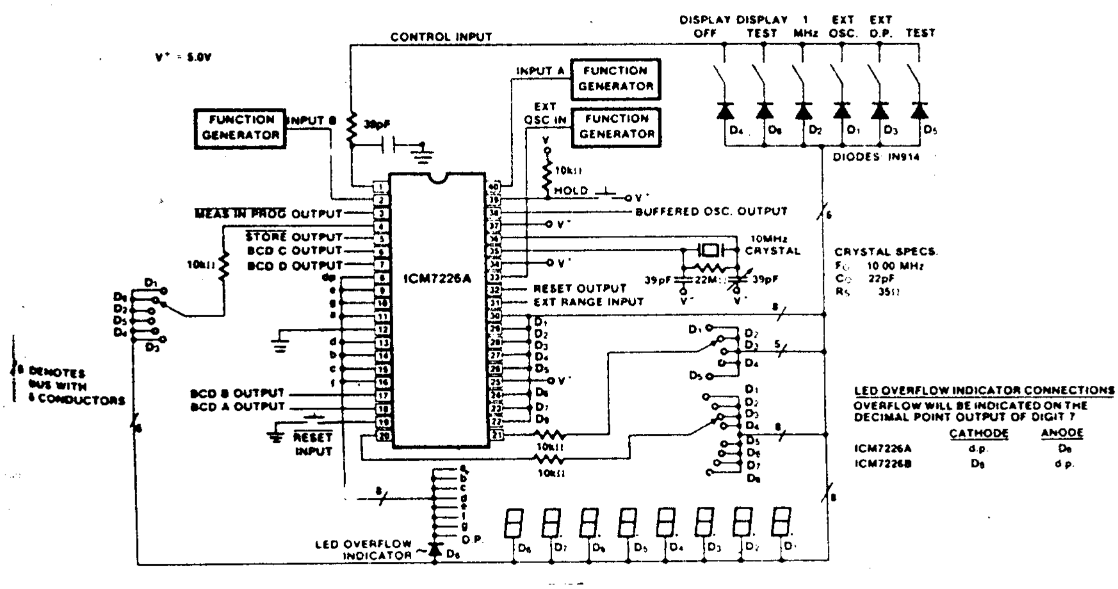
TEST CIRCUIT



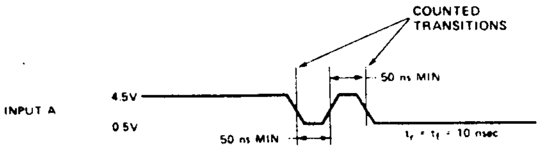


FIGURE 1. Waveform for Guaranteed Minimum $f_{A(max)}$ Function = Frequency, Frequency Ratio, Unit Counter.

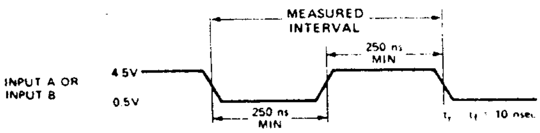


FIGURE 2. Waveform for Guaranteed Minimum $f_{B(max)}$ and $f_{A(max)}$ for Function = Period and Time Interval.

TIME INTERVAL MEASUREMENT

The ICM7226A/B can be used to accurately measure the time interval between two events. With a 10 MHz time-base crystal, the time between the two events can be as long as ten seconds. Accurate resolution in time interval measurement is 100ns.

The feature operates with Channel A going low at the start of the event to be measured, followed by Channel B going low at the end of the event.

When in the time interval mode and measuring a single event, the ICM7226A/B must first be "primed" prior to measuring the event of interest. This is done by first generating a negative going edge on Channel A followed by a negative going edge on Channel B to start the "measurement interval." The inputs are then primed ready for the measurement. Positive going edges on A and B, before or after the priming, will be needed to restore the original condition.

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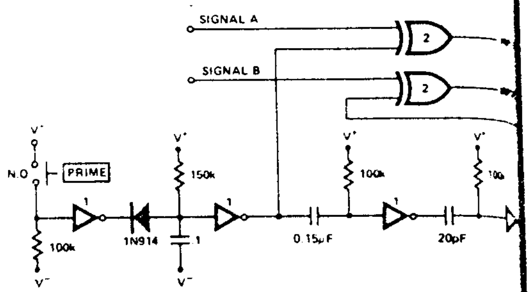
This can be easily accomplished with the follow[ing] circuit: (Figure 3b).



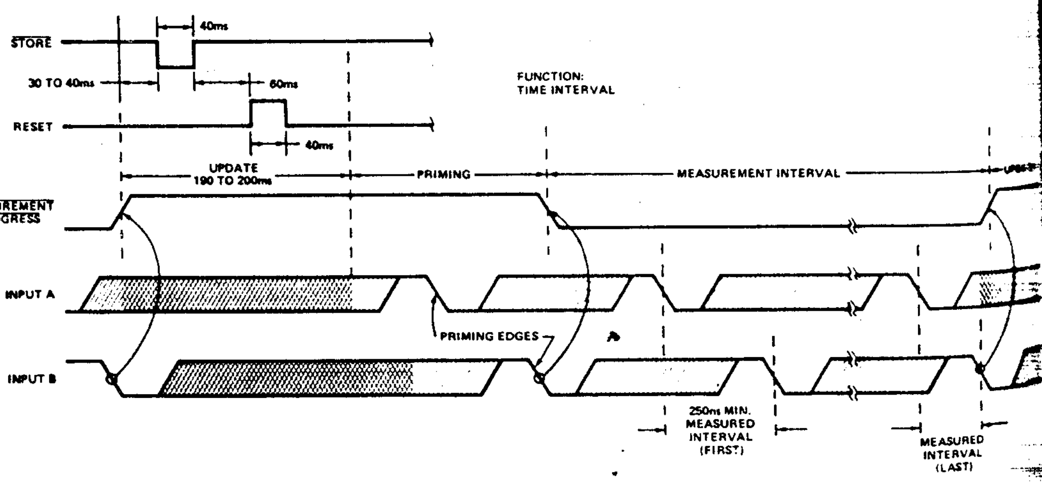
Device	Type
1	CD4049B Inverting Buffer
2	CD4070B Exclusive-OR

FIGURE 3b. Priming Circuit, Signal A&B High or Low.

Following the priming procedure (when in single e[vent] or 1 cycle range input) the device is ready to meas[ure] one (only) event.

When timing repetitive signals, it is not necessar[y to] "prime" the ICM7226A/B as the first alternating sig[nal] states automatically prime the device. See Figure 3a.

During any time interval measurement cycle, the ICM7226A/B requires 200ms following B going low to update all internal logic. A new measurement cy[cle] will not take place until completion of this inter[nal] update time.



NOTE: IF RANGE IS SET TO 1 EVENT, FIRST AND LAST MEASURED INTERVAL WILL COINCIDE.

FIGURE 3a. Waveforms for Time Interval Measurement (Others are similar, without priming phase)

APPLICATION NOTES

GENERAL

INPUTS A & B

The signal to be measured is applied to INPUT A in **frequency period, unit counter, frequency ratio** and **time interval** modes. The other input signal to be measured is applied to INPUT B in **frequency ratio** and **time interval**. f_A should be higher than f_B during **frequency ratio**.

Both inputs are digital inputs with a typical switching threshold of 2.0V at V^+ = 5V and input impedance of 250kΩ. For optimum performance, the peak to peak input signal should be at least 50% of the supply voltage and centered about the switching voltage. When these inputs are being driven from TTL logic, it is desirable to use a pullup resistor. The circuit counts high to low transitions at both inputs.

Note: The amplitude of the input should not exceed the supply by more than 0.3V otherwise, the circuit may be damaged.

MULTIPLEXED INPUTS

The FUNCTION, RANGE, CONTROL and EXTERNAL DECIMAL POINT inputs are time multiplexed to select the input function desired. This is achieved by connecting the appropriate digit driver output to the inputs. The input function, range and control inputs must be stable during the last half of each digit output, (typically 125µsec). The multiplex inputs are active high for the common anode ICM7226A, and active low for the common cathode ICM7226B.

Noise on the multiplex inputs can cause improper operation. This is particularly true when the **unit counter** mode of operation is selected, since changes in voltage on the digit drivers can be capacitively coupled through the LED diodes to the multiplex inputs. For maximum noise immunity, a 10kΩ resistor should be placed in series with the multiplex inputs as shown in the application notes.

Table 1 shows the functions selected by each digit for these inputs.

TABLE 1. Multiplexed Input Control

	FUNCTION	DIGIT
FUNCTION INPUT PIN 4	Frequency	D_1
	Period	D_8
	Frequency Ratio	D_2
	Time Interval	D_5
	Unit Counter	D_4
	Oscillator Frequency	D_3
RANGE INPUT PIN 21	0.01 Sec/1 Cycle	D_1
	0.1 Sec/10 Cycles	D_2
	1 Sec/100 Cycles	D_3
	10 Sec/1k Cycles	D_4
PIN 31	Enable External Range Input	D_5
CONTROL INPUT PIN 1	Blank Display	D_4&Hold
	Display Test	D_8
	1MHz Select	D_2
	External Oscillator Enable	D_1
	External Decimal Point Enable	D_3
	Test	D_5
EXTERNAL DECIMAL POINT INPUT, PIN 20	Decimal Point is Output for Same Digit That is Connected to This Input	

CONTROL INPUTS

Display Test - All segments are enabled continuously, giving a display of all 8's with decimal points. The display will be blanked if display off is selected at the same time.

Display Off - To enable the **display off** mode it is necessary to tie D_4 to the CONTROL input and have the HOLD input at V^+. The chip will remain in this mode until HOLD is switched low. While in the **display off** mode, the segment and digit driver outputs are open and the oscillator continues to run (with a typical supply current of 1.5mA with a 10MHz crystal) but no measurements are made. In addition, signals applied to the multiplexed inputs have no effect. A new measurement is initiated after the HOLD input goes low. (This mode does not operate when functioning as a unit counter.)

1MHz Select - The **1MHz select** mode allows use of a 1MHz crystal with the same digit multiplex rate and time between measurements as a 10MHz crystal. The internal decimal point is also shifted one digit to the right in **period** and **time interval**, since the least significant digit will be in 1µs increments rather than 0.1µs.

External Oscillator Enable - In this mode, the EXTernal OSCillator INput is used, rather than the on-chip oscillator, for the Timebase and Main Counter inputs in **period** and **time interval** modes. The on-chip oscillator will continue to function when the external oscillator is selected, but have no effect on circuit operation. The external oscillator input frequency must be greater than 100kHz or the chip will reset itself and enable the on-chip oscillator. Connect external oscillator to **both** OSC IN (pin 35) and EXT OSC IN (pin 33), or provide crystal for "default" oscillation, to avoid hang-up problems.

External Decimal Point Enable - When **external decimal point** is enabled, a decimal point will be displayed whenever the digit driver connected to the EXTERNAL DECIMAL POINT pin is active. Leading Zero Blanking will be disabled for all digits following the decimal point.

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Test Mode - This is a special mode used only in high speed production testing, and serves no other purpose.

RANGE INPUT

The range input selects whether the measurement is made for 1, 10, 100 or 1000 counts of the reference counter, or if the EXTernal RANGE INput determines the measurement time. In all functional modes except **unit counter**, a change in the RANGE input will stop the measurement in progress, without updating the display, and initiate a new measurement. This prevents an erroneous first reading after the RANGE input is changed.

FUNCTION INPUT

Six functions can be selected. They are: **Frequency, Period, Time Interval, Unit Counter, Frequency Ratio and Oscillator Frequency.**

These functions select which signal is counted into the main counter and which signal is counted by the reference counter, as shown in Table 2. In **time interval**, a flip flop is set first by a 1−0 transition at INPUT A and then reset by a 1−0 transition at INPUT B. The oscillator is gated into the Main Counter during the time the flip flop is set. A change in the FUNCTION input will stop the measurement in progress without updating the display and then initiate a new measurement. This prevents an erroneous first reading after the FUNCTION input is changed. If the main counter overflows, an overflow indication is output on the Decimal Point Output during D_8.

TABLE 2. Input Routing

DESCRIPTION	MAIN COUNTER	REFERENCE COUNTER
Frequency (f_A)	Input A	100Hz (Oscillator ÷ 10^5 or 10^4)
Period (t_A)	Oscillator	Input A
Ratio (f_A/f_B)	Input A	Input B
Time Interval (A–B)	Osc ON Gate	Osc OFF Gate
Unit Counter (Count A)	Input A	Not Applicable
Osc. Freq. (f_{OSC})	Oscillator	100Hz (Osc ÷ 10^5 or 10^4)

EXTERNAL DECIMAL POINT INPUT

When the **external decimal point** is selected, this input is active. Any of the digits, except D_8, can be connected to this point. D_8 should not be used since it will override the overflow output and leading zeros will remain unblanked after the decimal point.

HOLD Input - Except in the **unit counter** mode, when the HOLD Input is at V$^+$, any measurement in progress (before STORE goes low) is stopped, the main counter is reset and the chip is held ready to initiate a new measurement as soon as HOLD goes low. The latches which hold the main counter data are not updated, so the last complete measurement is displayed. In **unit counter** mode when HOLD Input is at V$^+$, the counter is not stopped or reset, but the display is frozen at that instantaneous value. When HOLD goes low the count continues from the new value in the counter.

RESET Input - The RESET Input resets the main counter, stops any measurement in progress, and enables the main counter latches, resulting in an all zero output. A capacitor to ground will prevent any hang-ups on power-up.

EXTernal RANGE Input - The EXTernal RANGE Input is used to select other ranges than those provided on the chip. Figure 4 shows the relationship between MEASurement IN PROGRESS and EXTernal RANGE Input.

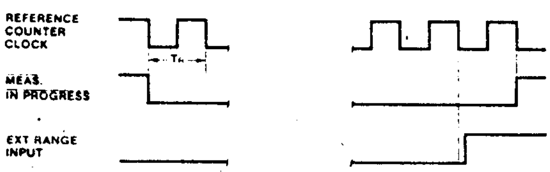

Figure 4: External Range Input to End of Measurement in Progress.

MEASUREMENT IN PROGRESS, STORE AND RESET Outputs - These Outputs are provided to facilitate external interfacing. Figure 5 shows the relationship between these signals during the time between measurements. All three outputs can drive a low power Schottky TTL load. The MEASUREMENT IN PROGRESS output can directly drive one ECL load, if the ECL device is powered from the same power supply as the ICM7226.

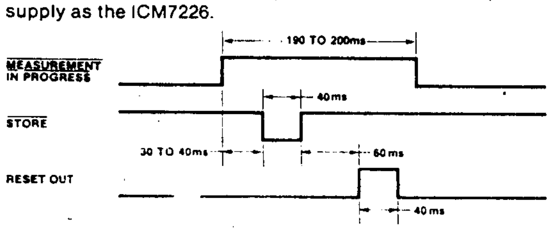

Figure 5: RESET OUT, STORE, and MEASUREMENT IN PROGRESS Outputs Between Measurements.

BCD Outputs - The BCD representation of each digit output is available at the BCD outputs; see Table 3 for Truth Table. The positive going (ICM7226A - Common Anode) or negative going (ICM7226B - Common Cathode) digit drivers lag the BCD data by 2 to 6 microseconds; the leading edge of the digit drive signal should be used to externally latch the BCD data. Each BCD output will drive one low power Schottky TTL load and when interfacing low power Schottky TTL latches, it is necessary to use 1kΩ pull down resistors on the TTL inputs for optimum results. T' . display is multiplexed from MSD to LSD. Leading zero blanking has no effect on the BCD outputs.

TABLE 3 Truth Table BCD Outputs

NUMBER	BCD 8 PIN 7	BCD 4 PIN 6	BCD 2 PIN 17	BCD 1 PIN 18
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

BUFFered OSCillator OUTput - The BUFFered OSCillator OUTput has been provided to enable use of the on chip oscillator signal without loading the oscillator itself. This output will drive one low power Schottky TTL load. Care should be taken to minimize capacitive loading on this pin.

DISPLAY CONSIDERATIONS

The display is multiplexed at a 500Hz rate with a digit time of 244μs, and an interdigit blanking time of 6μs to prevent ghosting between digits. The decimal point and leading zero blanking have been implemented for right hand decimal point displays; zeros following the decimal point will not be blanked. Leading zero blanking will also be disabled if the Main Counter overflows. The internal decimal point control displays frequency in kHz and time in μs.

The ICM7226A is designed to drive common anode LED displays at a peak cu... t of 25mA/segment, using displays with V_F = 1.8V at 25mA. The average DC current will be greater than 3mA under these conditions. The ICM7226B is designed to drive common cathode displays at a peak current of 15mA/segment, using displays with V_F = 1.8V at 15mA. Resistors can be added in series with the segment drivers to limit the display current, if required. Figures 6, 7, 8 and 9 show the digit and segment currents as a function of output voltage for common anode and common cathode drivers.

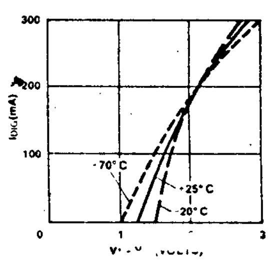

Figure 6: ICM7226A Typical IG vs. V+-Vo 4.5 ≤ V+ ≤ 6.0V

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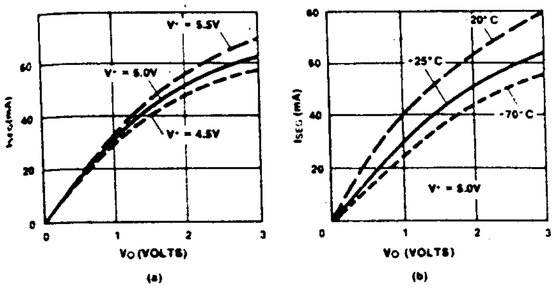


Figure 7: ICM7226A Typical I_{SEG} vs. Vo

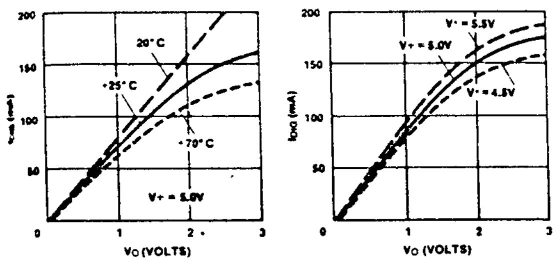


Figure 8: ICM7226B Typical I_{DIG} vs. Vo

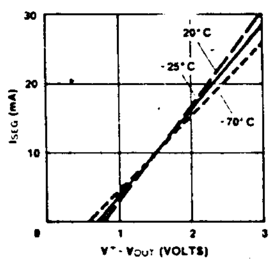


Figure 9: ICM7226B Typical I_{SEG} vs. $(V^+ - V_O)$ $4.5V \le V^+ \le 6.0V$

To increase the light output from the displays, V+ may be increased to 6.0V, however care should be taken to see that maximum power and current ratings are not exceeded.

The SEGment and Digit outputs in both the 7226A and B are not directly compatible with either TTL or CMOS logic. Therefore, level shifting with discrete transistors may be required to use these outputs as logic signals. External latching should be done on the leading edge of the digit signal.

ACCURACY

In a Universal Counter, crystal drift and quantization errors cause errors. In **frequency, period** and **time interval** modes, a signal derived from the oscillator is used either in the Reference Counter or Main Counter, and in these modes, an error in the oscillator frequency will cause an identical error in the measurement. For instance, an oscillator temperature coefficient of 20ppm/°C will cause a measurement error of 20ppm/°C.

In addition, there is a quantization error inherent in any digital measurement of ±1 count. Clearly this error is reduced by displaying more digits. In the **frequency** mode, maximum accuracy is obtained with high frequency inputs, and in **period** mode maximum accuracy is obtained with low frequency inputs. As can be seen in Figure 10, the least accuracy will be obtained at 10kHz. In **time interval** measurements there is a maximum error of 1 count per interval. As a result there is the same inherent accuracy in all ranges, as shown in Figure 11. In **frequency ratio** measurement more accuracy can be obtained by averaging over more cycles of INPUT B as shown in Figure 12.

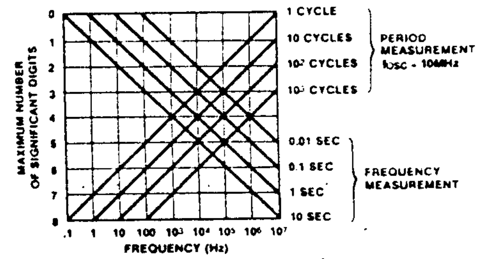


Figure 10: Maximum Accuracy of Frequency and Period Measurements Due to Limitations of Quantization Errors.

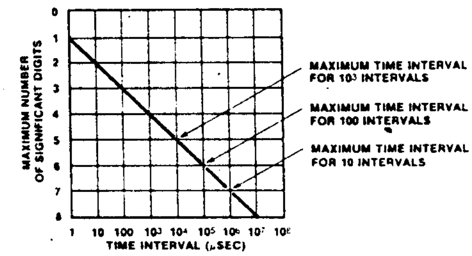


Figure 11: Maximum Accuracy of Time Interval Measurement Due to Limitations of Quantization Errors.

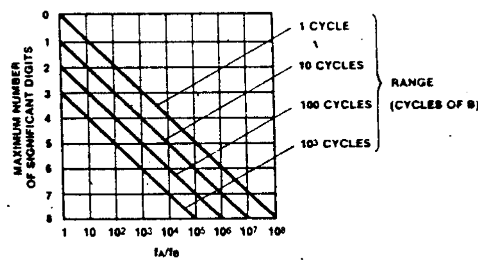


Figure 12: Maximum Accuracy for Frequency Ratio Measurement Due to Limitations of Quantization Errors.

CIRCUIT APPLICATIONS

The ICM7226 has been designed as a complete stand alone Universal Counter, or used with prescalers and other circuitry in a variety of applications. Since A IN and B IN are digital inputs, additional circuitry will be required in many applications, for input buffering, amplification, hysteresis, and level shifting to obtain the required digital voltages. For many applications an FET source follower can be used for input buffering, and an ECL 10116 line receiver can be used for amplification and

ICM7226A/B

hysteresis to obtain high impedance input, sensitivity and bandwidth. However, cost and complexity of this circuitry can vary widely, depending upon the sensitivity and bandwidth required. When TTL prescalers or input buffers are used, pull up resistors to V+ should be used to obtain optimal voltage swing at A IN and B IN.

If prescalers aren't required, the ICM7226 can be used to implement a minimum component Universal counter as shown in figure 13.

For input frequencies up to 40MHz, the circuit shown in figure 14 can be used to implement a **frequency and period counter**. To obtain the correct value when measuring frequency and period, it is necessary to divide the 10MHz oscillator frequency down to 2.5MHz. In doing this the time between measurements is lengthened to 800ms and the display multiplex rate is decreased to 125Hz.

If the input frequency is prescaled by ten, the oscillator frequency can remain at either 10MHz or 1MHz, but the decimal point must be moved. Figure 15 shows use of a ÷10 prescaler in **frequency counter** mode. Additional logic has been added to enable the 7226 to count the input directly in **period** mode for maximum accuracy. Note that A IN comes from Q_C rather than Q_D, to obtain an input duty cycle of 40%. If an output with a duty cycle not near 50% must be used then it may be necessary to use a 74121 monostable multivibrator or similar circuit to stretch the input pulse to guarantee a 50ns minimum pulse width.

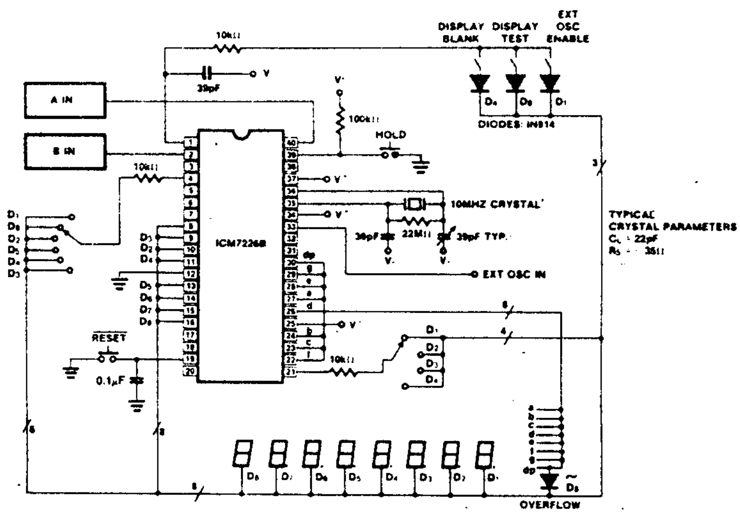
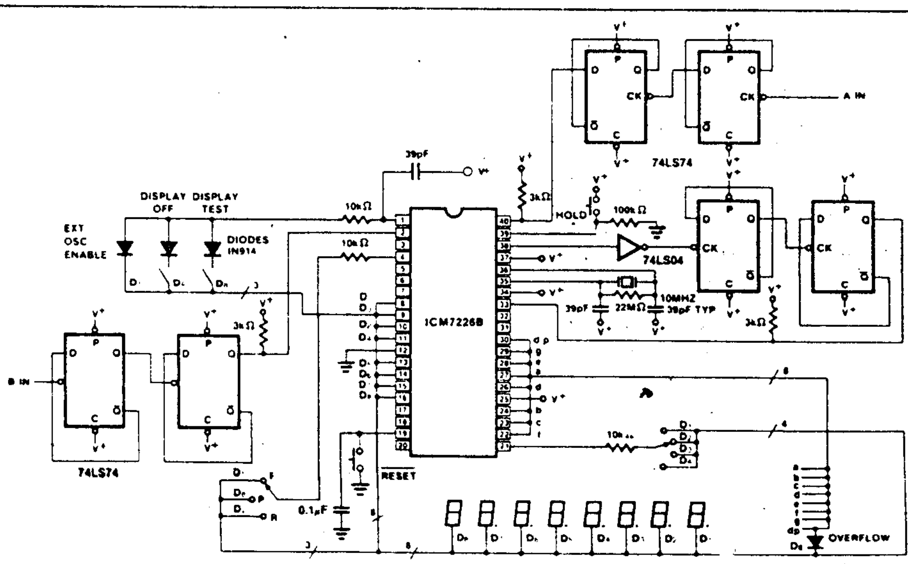


Figure 13: 10MHz Universal Counter



Notes: If a 2.5MHz crystal is used, diode D1 and I.C.'s 1 and 2 can be eliminated.

Figure 14: 40MHz Frequency, Period Counter

Figure 16 shows the use of a CD4C analog multiplexer to multiplex the digital outputs back ne FUNCTION Input. Since the CD4016 is a digitally controlled analog transmission gate, no level shifting of the digit output is required. CD4051's or CD4052's could also be used to select the proper inputs for the multiplexed input on the ICM7226 from 2 or 3 bit digital inputs. These analog multiplexers may also be used in systems in which the mode of operation is controlled by a microprocessor rather than directly from front panel switches. TTL multiplexers such as the 74153 or 74251 may also be used, but some additional circuitry will be required to convert the digit output to TTL compatible logic levels.

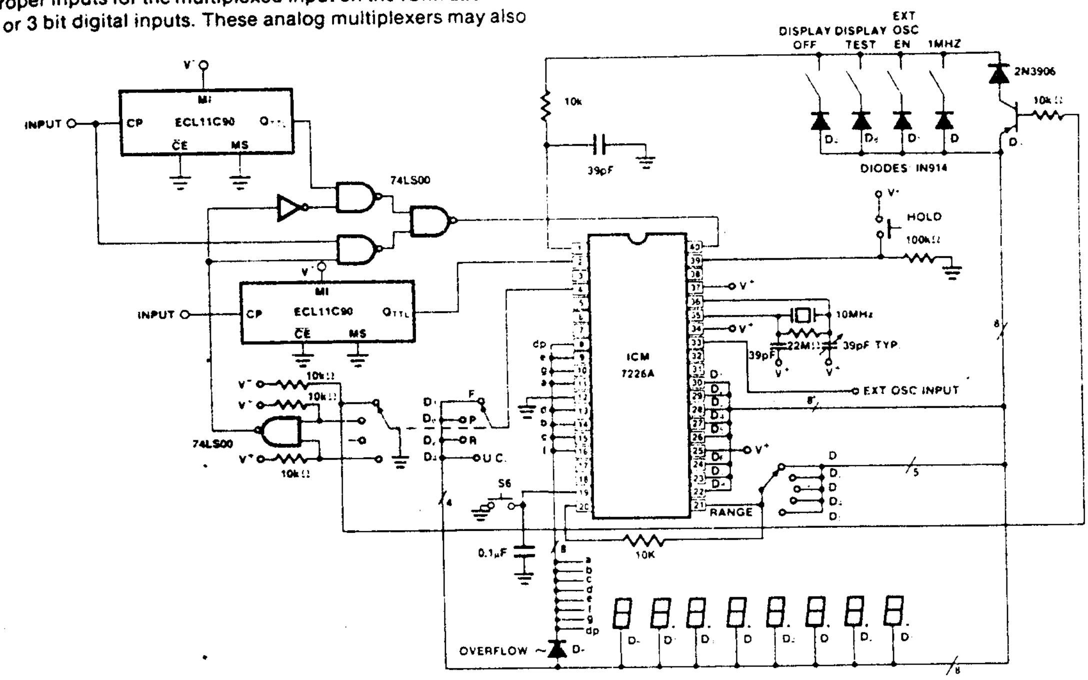


Figure 15: 100MHz Multi Function Counter

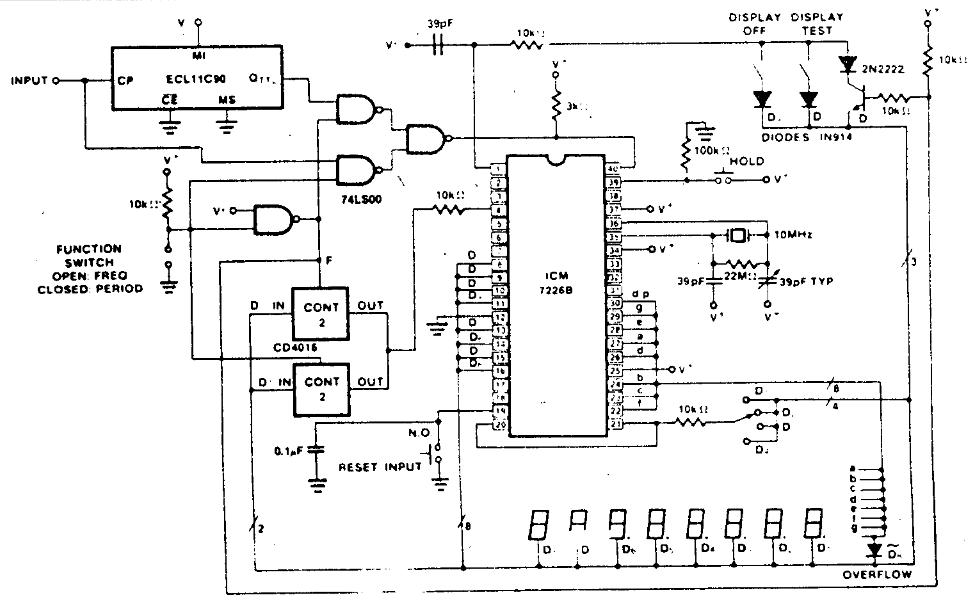


Figure 16: 0MHz Frequency Period Counter

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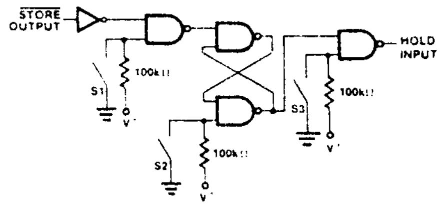
The circuit shown in figure 17 can be used in any of the circuit applications shown to implement a single measurement mode of operation. This circuit uses the $\overline{STORE}$ output to put the ICM7226 into a hold mode. The HOLD input can also be used to reduce the time between measurements. The circuit shown in figure 18 puts a short pulse into the HOLD input a short time after STORE goes low. A new measurement will be initiated at the end of the pulse on the HOLD Input. This circuit reduces the time between measurements to less than 40ms from 200ms; use of the circuit shown in Figure 18 on the circuit shown in Figure 14 will reduce the time between measurements from 1600ms to 800ms.



SWITCH	FUNCTION
S1	OPEN SINGLE MEAS MODE ENABLED
S2	CLOSED INITIATE NEW MEASUREMENT
S3	CLOSED HOLD INPUT

Figure 17: Single Measurement Circuit for Use With ICM7226

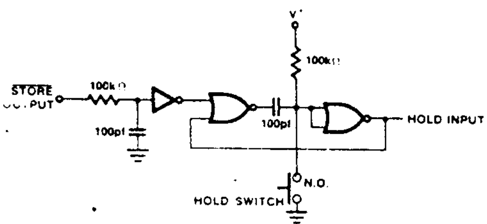


Figure 18: Circuit for Reducing Time Between Measurements

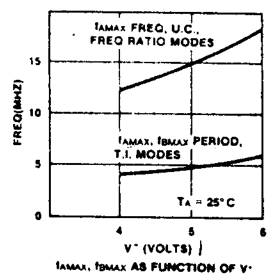


Figure 19: Typical Operating Characteristics

Figure 20 shows the ICM7226 being interfaced to LCD displays, by using its BCD outputs and 8 digit lines to drive 2 ICM7211 display drivers. The ICM7226 EV/Kit may easily be interfaced to 2 ICM7211 EV/Kits in this way. A similar arrangement can be used for driving vacuum fluorescent displays with the ICM7235.

OSCILLATOR CONSIDERATIONS

The oscillator is a high gain complementary FET inverter. An external resistor of 10MΩ or 22MΩ should be connected between the oscillator input and output to provide biasing. The oscillator is designed to work with a parallel resonant 10MHz quartz crystal with a load capacitance of 22pF and a series resistance of less than 35Ω. Among suitable crystals is the 10MHz CTS KNIGHTS ISI-002.

For [specific] crystal and load capacitance, the required g_m can [be c]alculated as follows:

$$g_m = \omega^2 C_{IN} C_{OUT} R_S \left(1 + \frac{C_O}{C_L}\right)^2$$

$$\text{where } C_L = \left(\frac{C_{IN} C_{OUT}}{C_{IN} + C_{OUT}}\right)$$

C_O = Crystal static capacitance
R_S = Crystal Series Resistance
Cin = Input Capacitance
Cout = Output Capacitance
$\omega = 2\pi f$

The required g_m should not exceed 50% of the g_m specified for the ICM7226 to insure reliable startup. The oscillator input and output pins each contribute about 4pF to C_{IN} and C_{OUT}. For maximum frequency stability, C_{IN} and C_{OUT} should be approximately twice the specified crystal load capacitance.

In cases where nondecade prescalers are used, it may be desirable to use a crystal which is neither 10MHz nor 1MHz. In this case both the multiplex rate and the time between measurements will be different. The multiplex rate is $f_{mux} = \frac{f_{osc}}{2 \times 10^4}$ for 10MHz mode and $f_{mux} = \frac{f_{osc}}{2 \times 10^3}$ for the 1MHz mode. The time between measurements is $\frac{2 \times 10^6}{f_{osc}}$ in the 10MHz mode and $\frac{2 \times 10^5}{f_{osc}}$ in the 1MHz mode. The buffered oscillator output should be used as an oscillator test point or to drive additional logic; this output will drive one low power Schottky TTL load. When the buffered oscillator output is used to drive CMOS or the external oscillator input, a 10kΩ resistor should be added from the buffered oscillator output to V+.

The crystal and oscillator components should be located as close to the chip as practical to minimize pickup from other signals. In particular, coupling from the BUFfered OSCillator OUTput and EXTernal OSCillator INput to the OSCillator OUTput or OSCillator INput can cause undesirable shifts in oscillator frequency. To minimize this coupling, pins 34 and 37 should be connected to V+ or GROUND and these two signals should be kept away from the oscillator circuit.

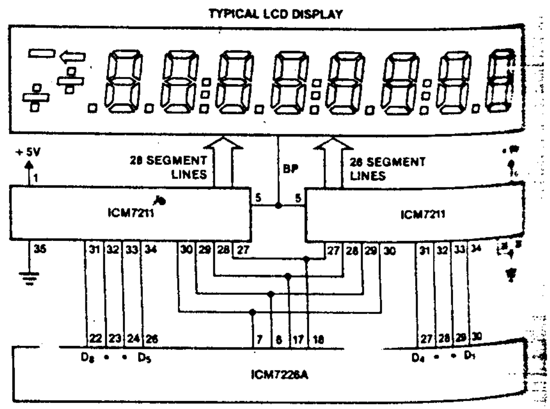


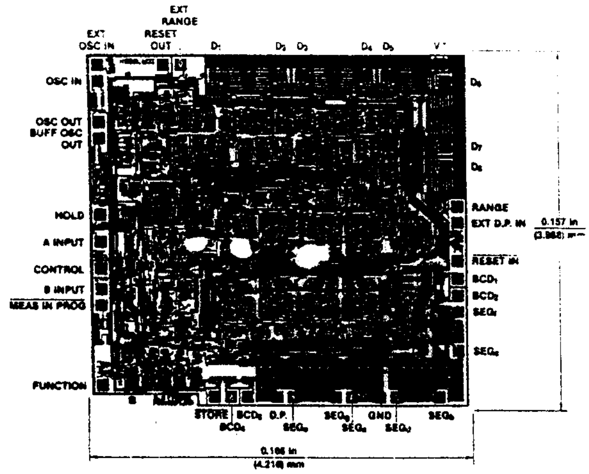
Figure 20: 10MHz Universal Counter System with LCD Display

6

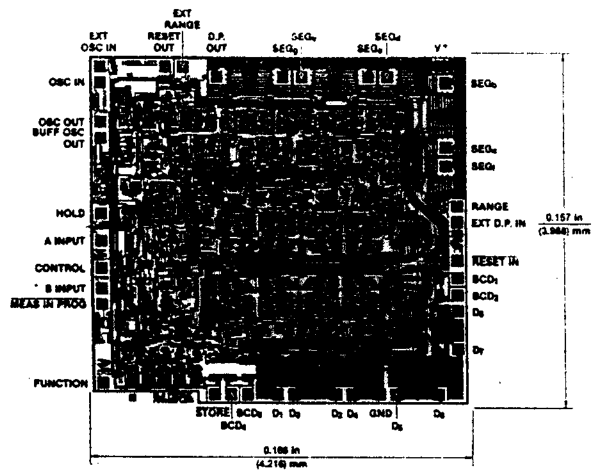
ICM7226 / B

INTERSIL

CHIP TOPOG PHIES



ICM7226A



ICM7226B

National Semiconductor

Industrial Blocks

LM733/LM733C Differential Video Amp

General Description

The LM733/LM733C is a two-stage, differential input, differential output, wide-band video amplifier. The use of internal series-shunt feedback gives wide bandwidth with low phase distortion and high gain stability. Emitter-follower outputs provide a high current drive, low impedance capability. It's 120 MHz bandwidth and selectable gains of 10, 100, and 400, without need for frequency compensation, make it a very useful circuit for memory element drivers, pulse amplifiers, and wide band linear gain stages.

The LM733 is specified for operation over the −55°C to +125°C military temperature range. The LM733C is specified for operation over the 0°C to +70°C temperature range.

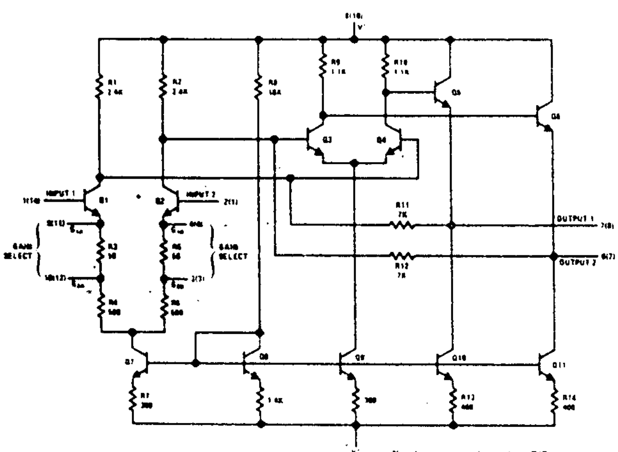
Features

- 120 MHz bandwidth
- 250 kΩ input resistance
- Selectable gains of 10, 100, 400
- No frequency compensation
- High common mode rejection ratio at high frequencies.

Applications

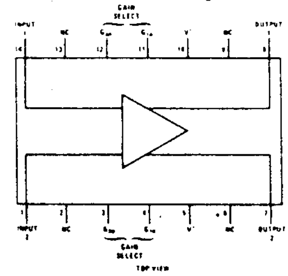
- Magnetic tape systems
- Disk file memories
- Thin and thick film memories
- Woven and plated wire memories
- Wide band video amplifiers.

Schematic and Connection Diagrams



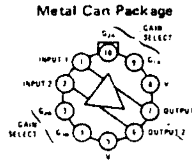
Numbers in parentheses show DIP connections.

Dual-In-Line Package



Order Number LM733CN
See NS Package N14A

Metal Can Package

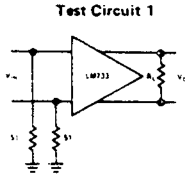


Note: Pin 5 connected to case.
TOP VIEW

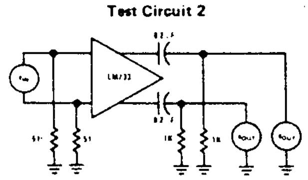
Order Number LM733H or LM733CH
See NS Package H10D

Test Circuits

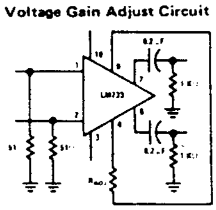
Test Circuit 1



Test Circuit 2



Voltage Gain Adjust Circuit



$V_S = 6V$, $T_A = 25°C$
(Pin numbers apply to TO 5 package)

Absolute Maximum Ratings

Differential Input Voltage	±5V
Common Mode Input Voltage	±6V
V_{CC}	±8V
Output Current	10 mA
Power Dissipation (Note 1)	500 mW
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range LM733	-55°C to +125°C
LM733C	0°C to +70°C
Lead Temperature (Soldering, 10 sec)	300°C

Electrical Characteristics (T_A = 25°C, unless otherwise specified, see test circuits, V_S = ±6.0V)

CHARACTERISTICS	TEST CIRCUIT	TEST CONDITIONS	LM733 MIN	LM733 TYP	LM733 MAX	LM733C MIN	LM733C TYP	LM733C MAX	UNITS
Differential Voltage Gain	1	R_L = 2 kΩ V_{OUT} = 3 V_{pp}							
Gain 1 (Note 2)			300	400	500	250	400	600	
Gain 2 (Note 3)			90	100	110	80	100	120	
Gain 3 (Note 4)			9.0	10	11	8.0	10	12	
Bandwidth	2								
Gain 1				40			40		MHz
Gain 2				90			90		MHz
Gain 3				120			120		MHz
Rise Time	2	V_{OUT} = 1 V_{pp}							
Gain 1				10.5			10.5		ns
Gain 2				4.5	10		4.5	12	ns
Gain 3				2.5			2.5		ns
Propagation Delay	2	V_{OUT} = 1 V_{pp}							
Gain 1				7.5			7.5		ns
Gain 2				6.0	10		6.0	10	ns
Gain 3				3.6			3.6		ns
Input Resistance									
Gain 1				4.0			4.0		kΩ
Gain 2			20	30		10	30		kΩ
Gain 3				250			250		kΩ
Input Capacitance		Gain 2		2.0			2.0		pF
Input Offset Current				0.4	3.0		0.4	5.0	μA
Input Bias Current				9.0	20		9.0	30	μA
Input Noise Voltage		BW = 1 kHz to 10 MHz		12			12		μVrms
Input Voltage Range	1		±1.0			±1.0			V
Common Mode Rejection Ratio	1								
Gain 2		V_{CM} = ±1V f ≤ 100 kHz	60	86		60	86		dB
Gain 2		V_{CM} = ±1V f = 5 MHz		60			60		dB
Supply Voltage Rejection Ratio Gain 2	1	ΔV_S = ±0.5V	50	70		50	70		dB
Output Offset Voltage	1	R_L = ∞							
Gain 1				0.6	1.5		0.6	1.5	V
Gain 2 and 3				0.35	1.0		0.35	1.5	V
Output Common Mode Voltage	1	R_L = ∞	2.4	2.9	3.4	2.4	2.9	3.4	V
Output Voltage Swing	1	R_L = 2k	3.0	4.0		3.0	4.0		
Output Sink Current			2.5	3.6		2.5	3.6		mA
Output Resistance				20			20		Ω
Power Supply Current	1	R_L = ∞		18	24		18	24	mA

Electrical Characteristics (Continued)

(The following specifications apply for $-55^{\circ}C < T_A < 125^{\circ}C$ for the LM733 and $0^{\circ}C < T_A < 70^{\circ}C$ for the LM733C, $V_S = \pm 6.0V$)

CHARACTERISTICS	TEST CIRCUIT	TEST CONDITIONS	LM733 MIN	LM733 TYP	LM733 MAX	LM733C MIN	LM733C TYP	LM733C MAX	UNITS
Differential Voltage Gain									
Gain 1			200		600	250		600	
Gain 2	1	$R_L = 2\ k\Omega$, $V_{OUT} = 3\ V_{PP}$	80		120	80		120	
Gain 3			8.0		12.0	8.0		12.0	
Input Resistance Gain 2			8			8			kΩ
Input Offset Current					5			6	μA
Input Bias Current					40			40	μA
Input Voltage Range	1		±1			±1			V
Common Mode Rejection Ratio									
Gain 2	1	$V_{CM} = \pm 1V$, $f \leq 100\ kHz$	50			50			dB
Supply Voltage Rejection Ratio									
Gain 2	1	$\Delta V_S = \pm 0.5V$	50			50			dB
Output Offset Voltage									
Gain 1	1	$R_L = \infty$			1.5			1.5	V
Gain 2 and 3					1.2			1.5	V
Output Voltage Swing	1	$R_L = 2k$	2.5			2.8			V_{PP}
Output Sink Current			2.2			2.5			mA
Power Supply Current	1	$R_L = \infty$			27			27	mA

Note 1: The maximum junction temperature of the LM733 is 150°C, while that of the LM733C is 100°C. For operation at elevated temperatures devices in the TO-100 package must be derated based on a thermal resistance of 150°C/W junction to ambient or 45°C/W junction to case. Thermal resistance of the dual-in-line package is 100°C/W.

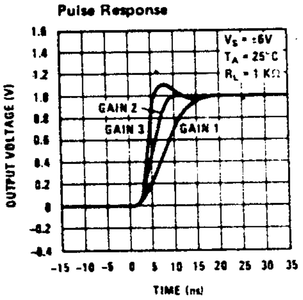
Note 2: Pins G1A and G1B connected together.

Note 3: Pins G2A and G2B connected together.

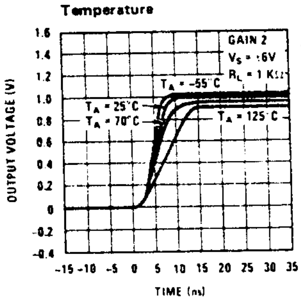
Note 4: Gain select pins open.

Typical Performance Characteristics

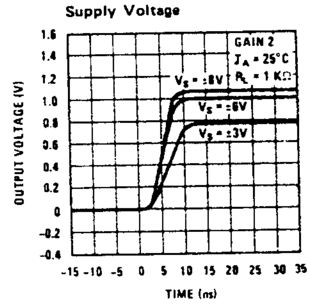
Pulse Response



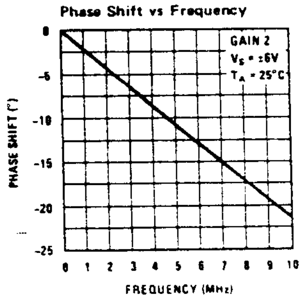
Pulse Response vs Temperature



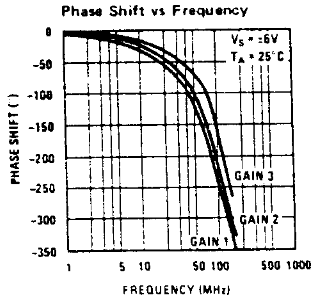
Pulse Response vs Supply Voltage



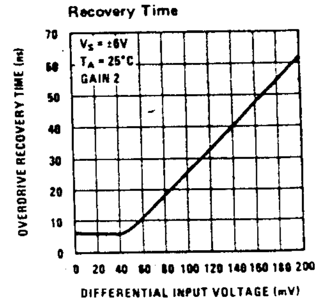
Phase Shift vs Frequency



Phase Shift vs Frequency

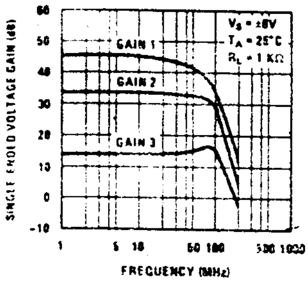


Differential Overdrive Recovery Time

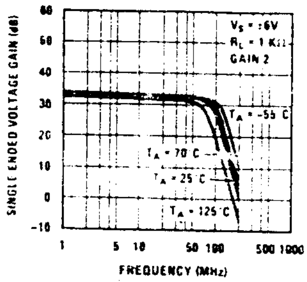


Typical Performance Characteristics (Continued)

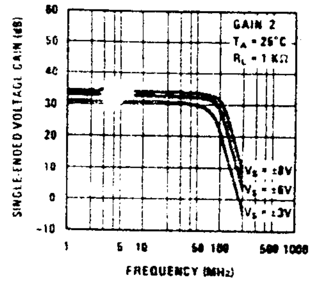
Voltage Gain vs Frequency



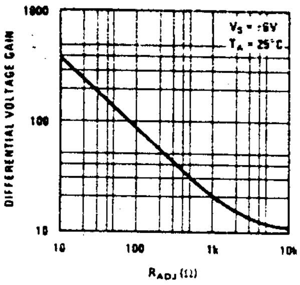
Gain vs Frequency Temperature



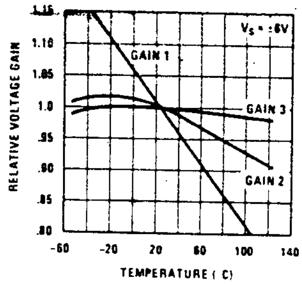
Gain vs Frequency vs Supply Voltage



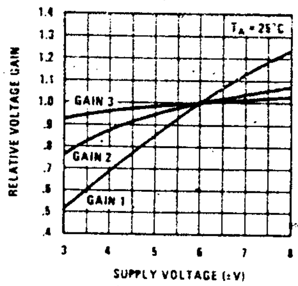
Voltage Gain vs R_{ADJ}



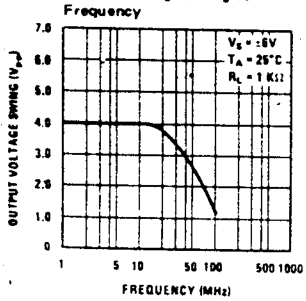
Voltage Gain vs Temperature



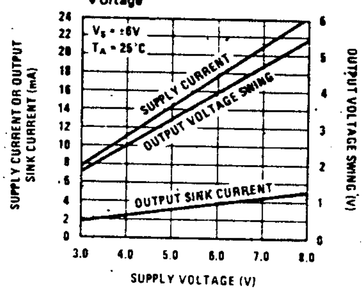
Voltage Gain vs Supply Voltage



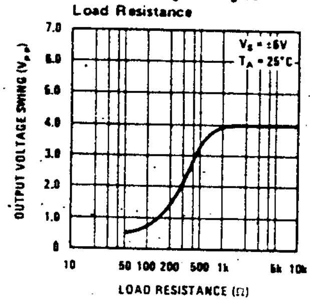
Output Voltage Swing vs Frequency



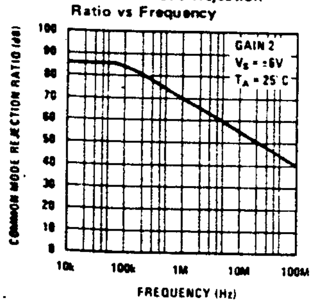
Supply Current, Output Voltage and Current Swing vs Supply Voltage



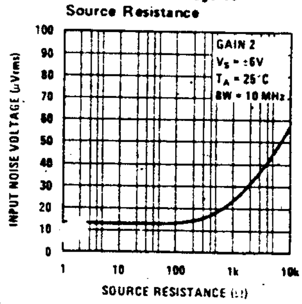
Output Voltage Swing vs Load Resistance



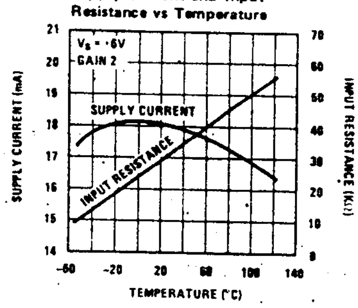
Common Mode Rejection Ratio vs Frequency



Input Noise Voltage vs Source Resistance



Supply Current and Input Resistance vs Temperature



National Semiconductor

Voltage Regulators

LM78XX Series Voltage Regulators

General Description

The LM78XX series of three terminal regulators is available with several fixed output voltages making them useful in a wide range of apr'ications. One of these is ,ocal on card regulation, eliminating the distribution problems associated with single point regulation. The voltages available allow these regulators to be used in logic systems, instrumentation, HiFi, and other solid state electronic equipment. Although designed primarily as fixed voltage regulators these devices can be used with external components to obtain adjustable voltages and currents.

The LM78XX series is available in an aluminum TO-3 package which will allow over 1.0A load current if adequate heat sinking is provided. Current limiting is included to limit the peak output current to a safe value. Safe area protection for the output transistor is provided to limit internal power dissipation. If internal power dissipation becomes too high for the heat sinking provided, the thermal shutdown circuit takes over preventing the IC from overheating.

Considerable effort was expended to make the LM78XX series of regulators easy to use and minimize the number of external components. It is not necessary to bypass the output, although this does improve transient response. Input bypassing is needed only if the regulator is located far from the filter capacitor of the power supply.

For output voltage other than 5V, 12V and 15V the LM117 series provides an output voltage range from 1.2V to 57V.

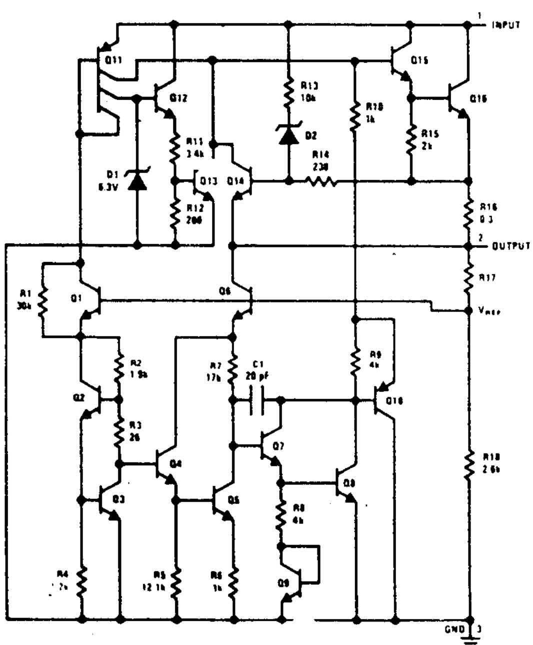
Features

- Output current in excess of 1A
- Internal thermal overload protection
- No external components required
- Output transistor safe area protection
- Internal short circuit current limit
- Available in the aluminum TO-3 package

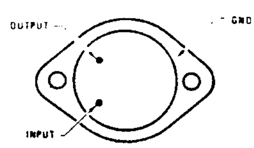
Voltage Range

LM7805C	5V
LM7812C	12V
LM7815C	15V

Schematic and Connection Diagrams



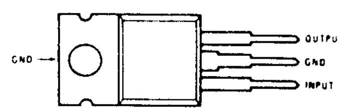
Metal Can Package
TO-3 (K)
Aluminum



BOTTOM VIEW

Order Numbers
LM7805CK
LM7812CK
LM7815CK
See Package KC02A

Plastic Package
TO-220 (T)



TOP VIEW

Order Numbers:
LM7805CT
LM7812CT
LM7815CT
See Package T03B

Absolute Maximum Ratings

Input Voltage (V_O = 5V, 12V and 15V)	35V
Internal Power Dissipation (Note 1)	Internally Limited
Operating Temperature Range (T_A)	0°C to +70°C
Maximum Junction Temperature	
(K Package)	150°C
(T Package)	125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	
TO-3 Package K	300°C
TO-220 Package T	230°C

Electrical Characteristics LM78XXC (Note 2) 0°C ≤ Tj ≤ 125°C unless otherwise noted.

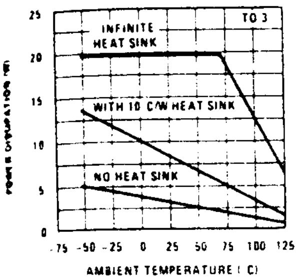
OUTPUT VOLTAGE				5V			12V			15V			
INPUT VOLTAGE (unless otherwise noted)				10V			19V			23V			UNITS
PARAMETER		CONDITIONS		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_O	Output Voltage	T_j = 25°C, 5 mA ≤ I_O ≤ 1A		4.8	5	5.2	11.5	12	12.5	14.4	15	15.6	
		P_D ≤ 15W, 5 mA ≤ I_O ≤ 1A V_{MIN} ≤ V_{IN} ≤ V_{MAX}		4.75 (7 ≤ V_{IN} ≤ 20)		5.25	11.4 (14.5 ≤ V_{IN} ≤ 27)		12.6	14.25 (17.5 ≤ V_{IN} ≤ 30)		15.75	
ΔV_O	Line Regulation	I_O = 500 mA	T_j = 25°C ΔV_{IN}		3 (7 ≤ V_{IN} ≤ 25)	50		4 (14.5 ≤ V_{IN} ≤ 30)	120		4 (17.5 ≤ V_{IN} ≤ 30)	150	
			0°C ≤ T_j ≤ +125°C ΔV_{IN}		(8 ≤ V_{IN} ≤ 20)	50		(15 ≤ V_{IN} ≤ 27)	120		(18.5 ≤ V_{IN} ≤ 30)	150	
		I_O ≤ 1A	T_j = 25°C ΔV_{IN}		(7.3 ≤ V_{IN} ≤ 20)	50		(14.6 ≤ V_{IN} ≤ 27)	120		(17.7 ≤ V_{IN} ≤ 30)	150	
			0° ≤ T_j ≤ +125°C ΔV_{IN}		(8 ≤ IN ≤ 12)	25		(16 ≤ V_{IN} ≤ 22)	60		(20 ≤ V_{IN} ≤ 26)	75	
ΔV_O	Load Regulation	T_j = 25°C	5 mA ≤ I_O ≤ 1.5A		10	50		12	120		12	150	
			250 mA ≤ I_O ≤ 750 mA			25			60			75	
		5 mA ≤ I_O ≤ 1A, 0°C ≤ T_j ≤ +125°C				50			120			150	
I_Q	Quiescent Current	I_O ≤ 1A	T_j = 25°C			8			8			8	
			0°C ≤ T_j ≤ +125°C			8.5			8.5			8.5	
ΔI_Q	Quiescent Current Change	5 mA ≤ I_O ≤ 1A				0.5			0.5			0.5	
		T_j = 25°C, I_O ≤ 1A V_{MIN} ≤ V_{IN} ≤ V_{MAX}			(7.5 ≤ V_{IN} ≤ 20)	1.0		(14.8 ≤ V_{IN} ≤ 27)	1.0		(17.9 ≤ V_{IN} ≤ 30)	1.0	
		I_O ≤ 500 mA, 0°C ≤ T_j ≤ +125°C V_{MIN} ≤ V_{IN} ≤ V_{MAX}			(7 ≤ V_{IN} ≤ 25)	1.0		(14.5 ≤ V_{IN} ≤ 30)	1.0		(17.5 ≤ V_{IN} ≤ 30)	1.0	
V_N	Output Noise Voltage	T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			40			75			90		
$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	Ripple Rejection	f = 120 Hz	I_O ≤ 1A, T_j = 25°C or	62	80		55	72		54	70		dB
			I_O ≤ 500 mA 0°C ≤ T_j ≤ +125°C	62			55			54			dB
		V_{MIN} ≤ V_{IN} ≤ V_{MAX}			(8 ≤ V_{IN} ≤ 18)			(15 ≤ V_{IN} ≤ 25)			(18.5 ≤ V_{IN} ≤ 28.5)		
R_O	Dropout Voltage	T_j = 25°C, I_{OUT} = 1A			2.0			2.0			2.0		
	Output Resistance	f = 1 kHz			8			18			19		
	Short-Circuit Current	T_j = 25°C			2.1			1.5			1.2		A
	Peak Output Current	T_j = 25°C			2.4			2.4			2.4		A
	Average TC of V_{OUT}	0°C ≤ T_j ≤ +125°C, I_O = 5 mA			0.6			1.5			1.8		mV/°C
V_{IN}	Input Voltage Required to Maintain Line Regulation	T_j = 25°C, I_O ≤ 1A		7.3			14.6			17.7			V

NOTE 1: Thermal resistance of the TO-3 package (K, KC) is typically 4°C/W junction to case and 35°C/W case to ambient. Thermal resistance of the TO-220 package (T) is typically 4°C/W junction to case and 50°C/W case to ambient.

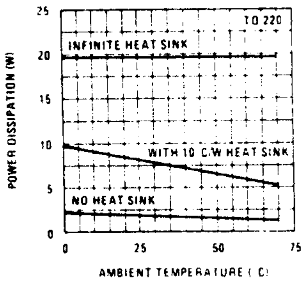
NOTE 2: All characteristics are measured with capacitor across the inut of 0.22 μF, and a capacitor across the output of 0.1 μF. All characteristics except noise voltage and ripple rejection ratio are measured using pulse techniques (t_W ≤ 10 ms, duty cycle ≤ 5%). Output voltage changes due to changes in internal temperature must be taken into account separately.

Typical Performance Characteristics

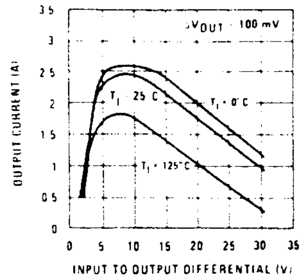
Maximum Average Power Dissipation



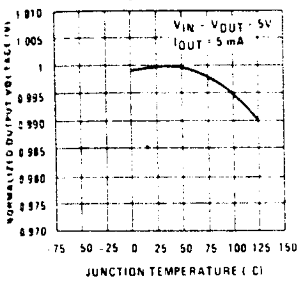
Maximum Average Power Dissipation



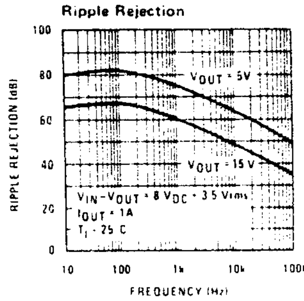
Peak Output Current



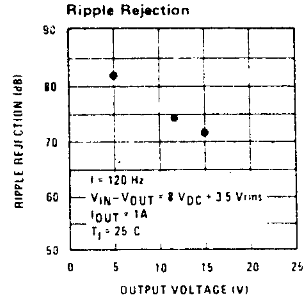
Output Voltage (Normalized to 1V at T_j = 25°C)



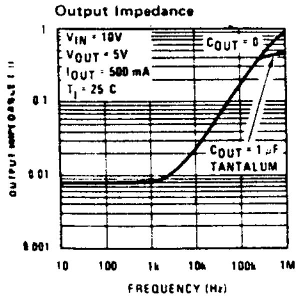
Ripple Rejection



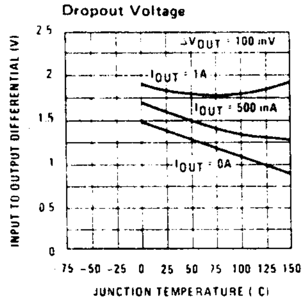
Ripple Rejection



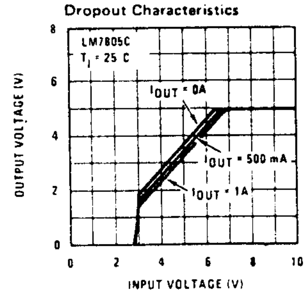
Output Impedance



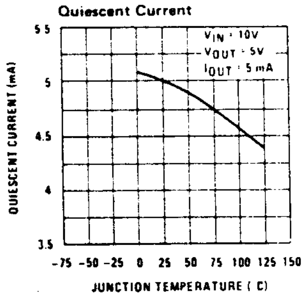
Dropout Voltage



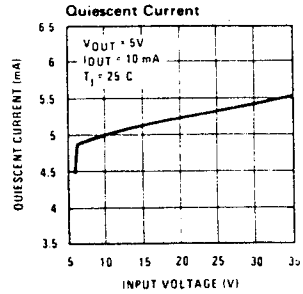
Dropout Characteristics



Quiescent Current



Quiescent Current

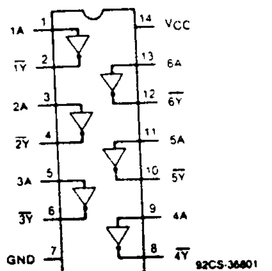


Technical Data

File Number **1471**

CD54/74HC04
CD54/74HCT04

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM AND TERMINAL ASSIGNMENT

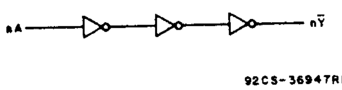
Hex Inverter

Type Features:

- *Input and Output are both buffered*
- *Typical propagation delay = 6 ns @ V_{CC} = 5V, C_L = 15 pF, T_A = 25° C*

The RCA-CD54/74HC04 and CD54/74HCT04 hex inverter utilize silicon-gate CMOS technology to achieve operating speeds similar to LSTTL gates with the low power consumption of standard CMOS integrated circuits. All devices have the ability to drive 10 LSTTL loads. The 54HCT/74HCT logic family is functionally as well as pin compatible with the standard 54LS/74LS logic family.

The CD54HC04 and CD54HCT04 are supplied in 14-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC04 and CD74HCT04 are supplied in 14-lead dual-in-line plastic packages (E suffix) and in 14-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).



LOGIC DIAGRAM

Family Features:

- *Fanout (Over Temperature Range):*
  - *Standard Outputs - 10 LSTTL Loads*
  - *Bus Driver Outputs - 15 LSTTL Loads*
- *Wide Operating Temperature Range:*
  - *CD74HC/HCT: -40 to +85° C*
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  - *2 to 6 V Operation*
  - *High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC}; @ V_{CC} = 5 V*
- *CD54HCT/CD74HCT Types:*
  - *4.5 to 5.5 V Operation*
  - *Direct LSTTL Input Logic Compatibility*
    - *V_{IL} = 0.8 V Max., V_{IH} = 2 V Min.*
  - *CMOS Input Compatibility*
    - *$I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}*

TRUTH TABLE

INPUTS	OUTPUTS
nA	nY
L	H
H	L

CD54/74HC04
CD54/74HCT04

MAXIMUM RATINGS, *Absolute-Maximum Values*:

DC SUPPLY-VOLTAGE, (V_{CC}) ... -0.5 to +7 V
(Voltages referenced to ground)
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} + 0.5$V) ... ±20mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC} + 0.5$V) ... ±20mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR $-0.5 V < V_O < V_{CC} + 0.5$V) ... ±25mA
DC V_{CC} OR GROUND CURRENT (I_{CC}) ... ±50mA
POWER DISSIPATION PER PACKAGE (P_D)
For T_A = -40 to +60°C (PACKAGE TYPE E) ... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) ... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H) ... 500 mW
For T_A +100 to +125°C (PACKAGE TYPE F, H) ... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M) ... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H ... -55 to +125°C
PACKAGE TYPE E, M ... -40 to +85°C
STORAGE TEMPERATURE (T_{stg}) ... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max ... +265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only ... +300°C

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS MIN.	LIMITS MAX.	UNITS
Supply Voltage Range (For TA = Full Package Range) VCC:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage VIN, VOUT	0	VCC	V
Operating Temperature TA:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times, tr, tf			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

*Unless otherwise specified, all voltages are referenced to Ground.

Technical Data

CD54/74HC04
CD54/74HCT04

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC04/CD54HC04 TEST CONDITIONS V_I V	I_O mA	V_{CC} V	74HC/54HC TYPES +25°C Min	Typ	Max	74HC TYPES -40/+85°C Min	Max	54HC TYPES -55/+125°C Min	Max	CD74HCT04/CD54HCT04 TEST CONDITIONS V_I V	V_{CC} V	74HCT/54HCT TYPES +25°C Min	Typ	Max	74HCT TYPES -40/+85°C Min	Max	54HCT TYPES -55/+125°C Min	Max	UNITS
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—		4.5								
			4.5	3.15	—	—	3.15	—	3.15	—	—	to	2	—	—	2	—	2	—	V
			6	4.2	—	—	4.2	—	4.2	—		5.5								
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5		4.5								
			4.5	—	—	1.35	—	1.35	—	1.35	—	to	—	—	0.8	—	0.8	—	0.8	V
			6	—	—	1.8	—	1.8	—	1.8		5.5								
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL}		2	1.9	—	—	1.9	—	1.9	—	V_{IL}									
	or	-0.02	4.5	4.4	—	—	4.4	—	4.4	—	or	4.5	4.4	—	—	4.4	—	4.4	—	V
	V_{IH}		6	5.9	—	—	5.9	—	5.9	—	V_{IH}									
TTL Loads	V_{IL}										V_{IL}									
	or	-4	4.5	3.98	—	—	3.84	—	3.7	—	or	4.5	3.98	—	—	3.84	—	3.7	—	V
	V_{IH}	-5.2	6	5.48	—	—	5.34	—	5.2	—	V_{IH}									
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL}		2	—	—	0.1	—	0.1	—	0.1	V_{IL}									
	or	0.02	4.5	—	—	0.1	—	0.1	—	0.1	or	4.5	—	—	0.1	—	0.1	—	0.1	V
	V_{IH}		6	—	—	0.1	—	0.1	—	0.1	V_{IH}									
TTL Loads	V_{IL}										V_{IL}									
	or	4	4.5	—	—	0.26	—	0.33	—	0.4	or	4.5	—	—	0.26	—	0.33	—	0.4	V
	V_{IH}	5.2	6	—	—	0.26	—	0.33	—	0.4	V_{IH}									
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	2	—	20	—	40	V_{CC} or Gnd	5.5	—	—	2	—	20	—	40	μA
Additional Quiescent Device Current per input pin. 1 unit load ΔI_{CC}*											V_{CC}-2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
ALL	1.2

*Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g. 360 μA max. @ 25°C.

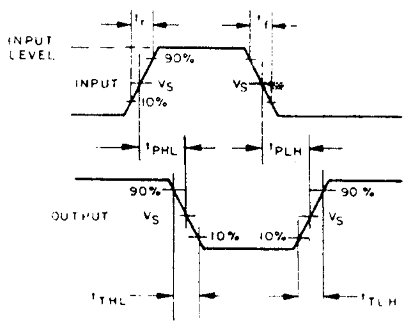
SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A 25°C, Input t_r, t_f 6 ns)

CHARACTERISTIC		Typical HC	Typical HCT	Units
Propagation Delay, Data Input to Output Y (Fig. 1) (C_L = 15 pF)	t_{PLH} t_{PHL}	6	7	ns
Power Dissipation Capacitance*	C_{PD}	21	24	pF

*CPD is used to determine the dynamic power consumption, per inverter where:
$P_D = V_{CC}^2 f (C_{PD} + C_L)$ where f = input frequency
C_L = output load capacitance
V_{CC} = supply voltage

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC		TEST CONDITION V_{CC} V	LIMITS 25°C HC		HCT		-40°C to +85°C 74HC		74HCT		-55°C to +125°C 54HC		54HCT		UNITS
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay	t_{PLH}	2	—	85	—	—	—	105	—	—	—	130	—	—	
Input to Output	t_{PHL}	4.5	—	17	—	19	—	21	—	24	—	26	—	29	ns
(Fig. 1)		6	—	14	—	—	—	18	—	—	—	22	—	—	
Transition Times	t_{TLH}	2	—	75	—	—	—	95	—	—	—	110	—	—	
(Fig. 1)	t_{THL}	4.5	—	15	—	15	—	19	—	19	—	22	—	22	ns
		6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C_I		—	10	—	10	—	10	—	10	—	10	—	10	pF



	54/74HC	54/74HCT
INPUT LEVEL	VCC	3V
VS	50% VCC	1.3V

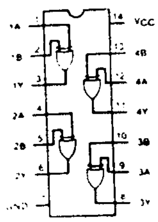
92CS-36948R1

Fig. 1 - Transition times and propagation delay times.

File Number **1644**

CD54/74HC86
CD54/74HCT86

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM AND TERMINAL ASSIGNMENT

Quad 2 - Input EXCLUSIVE - OR Gate

Type Features:

- *Four independent EXCLUSIVE - OR gates*
- *Buffered inputs and outputs*

Applications:

- *Logical comparators*
- *Parity generators and checkers*
- *Adders/Subtracters*

The RCA CD54/74HC86 and CD54/74HCT86 contain four independent EXCLUSIVE-OR gates in one package. They provide the system designer with a means for implementation of the EXCLUSIVE-OR function.

The CD54HC/HCT86 are supplied in 14-lead cermetic dual-in-line packages (F suffix). The CD74HC/HCT86 are supplied in 14-lead plastic dual-in-line packages (E suffix) and in 14-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

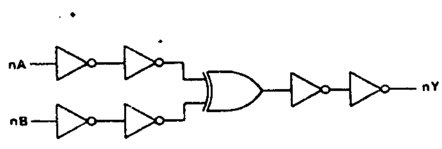


Fig. 1 - Logic diagram each gate.

Family Features:

- *Fanout (Over Temperature Range):*
  Standard Outputs - 10 LSTTL Loads
  Bus Driver Outputs - 15 LSTTL Loads
- *Wide Operating Temperature Range:*
  CD74HC/HCT: -40 to +85° C
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  2 to 6 V Operation
  High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} @ V_{CC} = 5 V
- *CD54HCT/CD74HCT Types:*
  4.5 to 5.5 V Operation
  Direct LSTTL Input Logic Compatibility
  V_{IL} = 0.8 V Max., V_{IH} = 2 V Min.
  CMOS Input Compatibility
  $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}

TRUTH TABLE

INPUTS		OUTPUT
nA	nB	nY
L	L	L
L	H	H
H	L	H
H	H	L

H = HIGH voltage level.
L = LOW voltage level.

Technical Data

CD54/74HC86
CD54/74HCT86

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}): ..... -0.5 to +7 V
(Voltages referenced to ground)
DC INPUT DIODE CURRENT, I_{IK} (FOR V_I < -0.5 V OR V_I > V_{CC} +0.5 V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR V_O < -0.5 V OR V_O > V_{CC} +0.5 V) ..... ±20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR -0.5 V < V_O < V_{CC} +0.5 V) ..... ±25 mA
DC V_{CC} OR GROUND CURRENT (I_{CC}): ..... ±50 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H ..... -55 to +125°C
PACKAGE TYPE E, M ..... -40 to +85°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only ..... +300°C

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS MIN.	LIMITS MAX.	UNITS
Supply-Voltage Range (For T_A = Full Package-Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times, t_r, t_f			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

*Unless otherwise specified, all voltages are referenced to Ground.

CD54/74HC86
CD54/74HCT86

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	CD74HC86/CD54HC86 TEST CONDITIONS			74HC/54HC TYPE			74HC TYPE		54HC TYPE		CD74HCT86/CD54HCT86 TEST CONDITIONS		74HCT/54HCT TYPE			74HCT TYPE		54HCT TYPE		UNITS
				+25°C			-40/ +85°C		-55/ +125°C				+25°C			-40/ +85°C		-55/ +125°C		
	V_I V	I_O mA	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max	V_I V	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or V_{IH}	-4	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} and Gnd	5.5	—	—	±0.1	—	±1	—	±1	µA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	2	—	20	—	40	V_{CC} or Gnd	5.5	—	—	2	—	20	—	40	µA
Additional Quiescent Device Current per Input Pin 1 Unit Load ΔI_{CC}*											V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	µA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT INPUT LOADING TABLE

INPUT	UNIT LOADS *
All Inputs	1

* Unit load · ΔI_{CC} limit specified in Static Characteristic Chart, e ., 360 µA max. @ 25°C.

CD54/74HC86
CD54/74HCT86

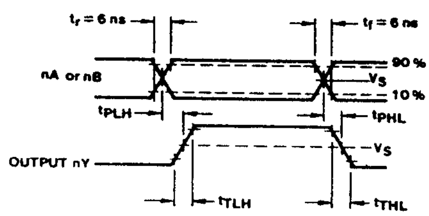
SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input t_r, t_f = 6 ns)

CHARACTERISTIC	C_L pF	SYMBOL	TYPICAL VALUES		UNITS
			54/74HC	54/74HCT	
Propagation Delay, Any Input	15	t_{PLH} t_{PHL}	9	13	ns
Power Dissipation Capacitance*	—	C_{PD}	22	27	pF

* C_{PD} is used to determine the dynamic power consumption, per gate.
$P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where:
f_i = nput frequency.
C_L = output load capacitance.
V_{CC} = supply voltage.

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC	SYMBOL	V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
			HC		HCT		74HC		74HCT		54HC		54HCT		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay, nA, nB to nY	t_{PLH} t_{PHL}	2		120		—		150		—		180		—	
		4.5		24		32		30		40		36		48	ns
		6		20		—		26		—		31		—	
Output Transition Time	t_{TLH} t_{THL}	2		75		—		95		—		110		—	
		4.5		15		15		19		19		22		22	ns
		6		13		—		16		—		19		—	
Input Capacitance	C_I		—	10	—	10	—	10	—	10	—	10	—	10	pF



92CS-38430R2

	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
Switching Voltage, V_S	50% V_{CC}	1.3 V

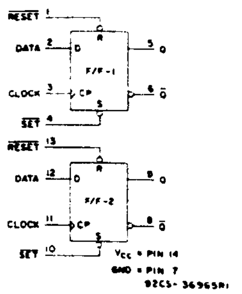
Fig. 2 - Transition times and propagation delay times.

Technical Data

File Number **1476**

CD54/74HC74
CD54/74HCT74

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

Dual D Flip-Flop with Set and Reset
Positive-Edge Trigger

Type Features:

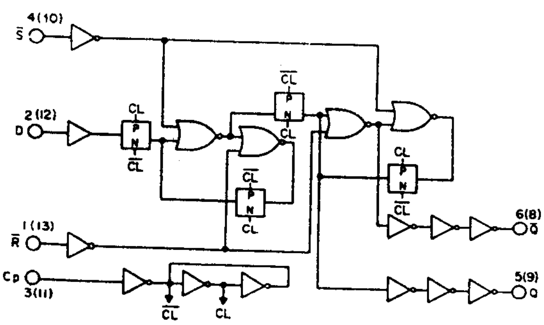
- *Hysteresis on clock inputs for improved noise immunity and increased input Rise and Fall times.*
- *Asynchronous Set and Reset*
- *Complementary Outputs*
- *Buffered Inputs*
- *Typical f_{max} = 50 MHz @ V_{CC} = 5V, C_L = 15 pF, T_A = 25°C*

The RCA-CD54/74HC74 and CD54/74HCT74 utilize silicon-gate CMOS technology to achieve operating speeds equivalent to LSTTL parts. They exhibit the low power consumption of standard CMOS integrated circuits, together with the ability to drive 10 LSTTL Loads.

This flip-flop has independent DATA, $\overline{SET}$, $\overline{RESET}$ and CLOCK inputs and Q and $\overline{Q}$ outputs. The logic level present at the data input is transferred to the output during the positive-going transition of the clock pulse. $\overline{SET}$ and $\overline{RESET}$ are independent of the clock and are accomplished by a low level at the appropriate input.

The 54HCT/74HCT logic family is functionally as well as pin compatible with the standard 54LS/74LS logic family.

The CD54HC74 and CD54HCT74 are supplied in 14-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC74 and CD74HCT74 are supplied in 14-lead dual-in-line plastic packages (E suffix) and in 14-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).



92CS-36966

Fig. 1 — Logic Diagram

Family Features:

- *Fanout (Over Temperature Range):*
  Standard Outputs - 10 LSTTL Loads
  Bus Driver Outputs - 15 LSTTL Loads
- *Wide Operating Temperature Range:*
  CD74HC/HCT: -40 to + 85° C
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  2 to 6 V Operation
  High Noise Immunity:
  N_{IL} = 30%, N_{IH} = 30% of V_{CC}; @ V_{CC} = 5 V
- *CD54HCT/CD74HCT Types:*
  4.5 to 5.5 V Operation
  Direct LSTTL Input Logic Compatibility
  V_{IL} = 0.8 V Max., V_{IH} = 2 V Min.
  CMOS Input Compatibility
  $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}

TRUTH TABLE

INPUTS				OUTPUTS	
$\overline{SET}$	$\overline{RESET}$	CP	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↗	H	H	L
H	H	↗	L	L	H
H	H	L	X	Q0	$\overline{Q0}$

H = High Level (Steady State)
L = Low Level (Steady State)
X = Don't Care
↗ = Transition from Low to High level

NOTES: Q0 = the level of Q before the indicated input conditions were established.
*This configuration is nonstable, that is, it will not persist when set and reset inputs return to their inactive (high) level.

Technical Data

CD54/74HC74
CD54/74HCT74

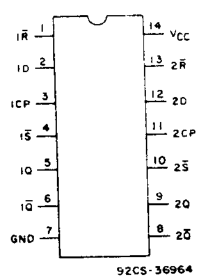
MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC})
(Voltages referenced to ground) .... -0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC}$ +0.5V) .... ±20mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC}$ +0.5V) .... ±20mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR -0.5 V < V_O < V_{CC} + 0.5V) .... ±25mA
DC V_{CC} OR GROUND CURRENT (I_{CC}) .... ±50mA
POWER DISSIPATION PER PACKAGE (P_D)
For T_A = -40 to +60°C (PACKAGE TYPE E) .... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) .... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H) .... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H) .... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M) .... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) .... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H .... -55 to +125°C
PACKAGE TYPE E, M .... -40 to +85°C
STORAGE TEMPERATURE (T_{stg}) .... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. .... +265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only .... +300°C

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_{in}, V_{out}	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times t_r, t_f•			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

*Unless otherwise specified, all voltages are referenced to Ground.
•Applicable for all inputs except clock.



TERMINAL ASSIGNMENT

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC74/CD54HC74 TEST CONDITIONS V_I V	I_O mA	V_{CC} V	74HC/54HC TYPES +25°C Min	Typ	Max	74HC TYPES -40/+85°C Min	Max	54HC TYPES -55/+125°C Min	Max	CD74HCT74/CD54HCT74 TEST CONDITIONS V_I V	V_{CC} V	74HCT/54HCT TYPES +25°C Min	Typ	Max	74HCT TYPES -40/+85°C Min	Max	54HCT TYPES -55/+125°C Min	Max	UNITS
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—		4.5								
			4.5	3.15	—	—	3.15	—	3.15	—	—	to	2	—	—	2	—	2	—	V
			6	4.2	—	—	4.2	—	4.2	—		5.5								
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5		4.5								
			4.5	—	—	1.35	—	1.35	—	1.35	—	to	—	—	0.8	—	0.8	—	0.8	[illegible]
			6	—	—	1.8	—	1.8	—	1.8		5.5								
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL}		2	1.9	—	—	1.9	—	1.9	—	V_{IL}									
	or	-0.02	4.5	4.4	—	—	4.4	—	4.4	—	or	4.5	4.4	—	—	4.4	—	4.4	—	V
	V_{IH}		6	5.9	—	—	5.9	—	5.9	—	V_{IH}									
* TTL Loads	V_{IL}										V_{IL}									
	or	-4	4.5	3.98	—	—	3.84	—	3.7	—	or	4.5	3.98	—	—	3.84	—	3.7	—	V
	V_{IH}	-5.2	6	5.48	—	—	5.34	—	5.2	—	V_{IH}									
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL}		2	—	—	0.1	—	0.1	—	0.1	V_{IL}									
	or	0.02	4.5	—	—	0.1	—	0.1	—	0.1	or	4.5	—	—	0.1	—	0.1	—	0.1	V
	V_{IH}		6	—	—	0.1	—	0.1	—	0.1	V_{IH}									
TTL Loads	V_{IL}										V_{IL}									
	or	4	4.5	—	—	0.26	—	0.33	—	0.4	or	4.5	—	—	0.26	—	0.33	—	0.4	V
	V_{IH}	5.2	6	—	—	0.26	—	0.33	—	0.4	V_{IH}									
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	4	—	40	—	80	V_{CC} or Gnd	5.5	—	—	4	—	40	—	80	μA
Additional Quiescent Device Current per input pin 1 unit load ΔI_{CC}*											V_{CC}-2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
D	0.5
$\overline{R}$	0.5
CP	0.7
$\overline{S}$	0.75

*Unit Load = ΔIcc limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.

CD54/74HC74
CD54/74HCT74

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25° C, Input t_r, t_f = 6 ns)

CHARACTERISTIC	SYMBOL	C_L (pF)	TYPICAL HC	TYPICAL HCT	UNITS
Propagation Delay	t_{PLH} t_{PHL}				
CP to Q, $\overline{Q}$ (Fig. 2)		15	14	14	ns
$\overline{R}$ to Q, $\overline{Q}$ (Fig. 3)		15	17	17	ns
$\overline{S}$ to Q, $\overline{Q}$ (Fig. 3)		15	17	17	ns
CP Frequency	f_{MAX}	15	50	50	MHz
Power Dissipation Capacitance*	C_{PD}	—	25	30	pF

*C_{PD} is used to determine the dynamic power consumption, per flip-flop.
$PD = C_{PD} V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o)$ where: f_i = input frequency
f_o = output frequency
C_L = output load capacitance
V_{CC} = supply voltage

PRE-REQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC		TEST CONDITIONS V_{CC} (V)	LIMITS 25° C HC Min.	HC Max.	HCT Min.	HCT Max.	-40° C to +85° C 74HC Min.	74HC Max.	74HCT Min.	74HCT Max.	-55° C to +125° C 54HC Min.	54HC Max.	54HCT Min.	54HCT Max.	UNITS
Data to CP	t_{SU}	2	60	—	—	—	75	—	—	—	90	—	—	—	ns
Set-up Time		4.5	12	—	12	—	15	—	15	—	18	—	18	—	
(Fig. 4)		6	10	—	—	—	13	—	—	—	15	—	—	—	
Hold Time	t_H	2	3	—	—	—	3	—	—	—	3	—	—	—	
		4.5	3	—	3	—	3	—	3	—	3	—	3	—	
(Fig. 4)		6	3	—	—	—	3	—	—	—	3	—	—	—	
Removal Time	t_{REM}	2	30	—	—	—	40	—	—	—	45	—	—	—	
$\overline{R}$, $\overline{S}$ to CP		4.5	6	—	6	—	8	—	8	—	9	—	9	—	
(Fig. 3)		6	5	—	—	—	7	—	—	—	8	—	—	—	
Pulse Width	t_W	2	80	—	—	—	100	—	—	—	120	—	—	—	
$\overline{R}$, $\overline{S}$		4.5	16	—	16	—	20	—	20	—	24	—	24	—	
(Figs. 2, 3)		6	14	—	—	—	17	—	—	—	20	—	—	—	
Pulse Width	t_W	2	80	—	—	—	100	—	—	—	120	—	—	—	
CP		4.5	16	—	18	—	20	—	23	—	24	—	27	—	
(Figs. 2, 3)		6	14	—	—	—	17	—	—	—	20	—	—	—	
CP Frequency	f_{MAX}	2	6	—	—	—	5	—	—	—	4	—	—	—	MHz
		4.5	30	—	25	—	25	—	20	—	20	—	16	—	
		6	35	—	—	—	29	—	—	—	23	—	—	—	

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC		VCC (V)	LIMITS 25° C HC Min.	HC Max.	HCT Min.	HCT Max.	-40° C to +85° C 74HC Min.	74HC Max.	74HCT Min.	74HCT Max.	-55° C to +125° C 54HC Min.	54HC Max.	54HCT Min.	54HCT Max.	UNITS
Propagation Delay,	t_{PLH}	2	—	175	—	—	—	220	—	—	—	265	—	—	ns
CP to Q, $\overline{Q}$	t_{PHL}	4.5	—	35	—	35	—	44	—	44	—	53	—	53	
(Fig. 2)		6	—	30	—	—	—	37	—	—	—	45	—	—	
$\overline{R}$, $\overline{S}$ to Q, $\overline{Q}$	t_{PHL}	2	—	200	—	—	—	250	—	—	—	300	—	—	
	t_{PLH}	4.5	—	40	—	40	—	50	—	50	—	60	—	60	
(Fig. 3)		6	—	34	—	—	—	43	—	—	—	51	—	—	
Transition Times	t_{TLH}	2	—	75	—	—	—	95	—	—	—	110	—	—	
	t_{THL}	4.5	—	15	—	15	—	19	—	19	—	22	—	22	
(Fig. 5)		6		13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C_I		—	10	—	10	—	10	—	10	-	10	—	10	pF

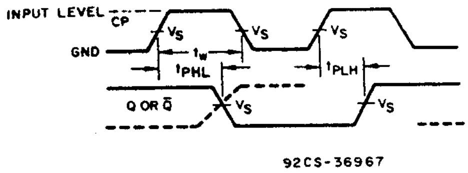


Fig. 2 — Clock pre-requisite and propagation delays.

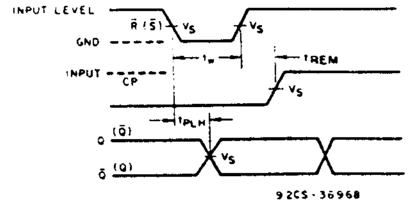


Fig. 3 — $\overline{Reset}$ or $\overline{Set}$ pre-requisite and propagation delays

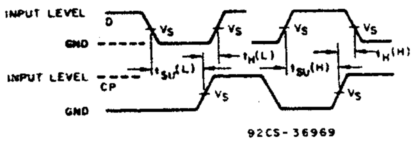


Fig. 4 — Data pre-requisite times.

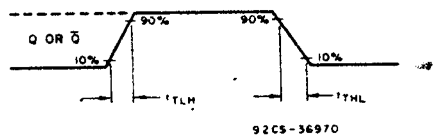


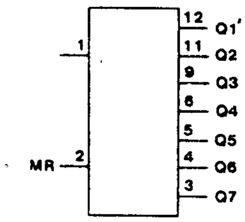
Fig. 5 — Output transition times.

	54/74HC	54/74HCT
INPUT LEVEL	V_{CC}	3V
V_S	50% V_{CC}	1.3V

File Number 1683

CD54/74HC4024
CD54/74HCT4024

High-Speed CMOS Logic



92CS-38450R1

CD54/74HC4024, HCT4024 FUNCTIONAL DIAGRAM

7-Stage Binary Ripple Counter

Type Features:

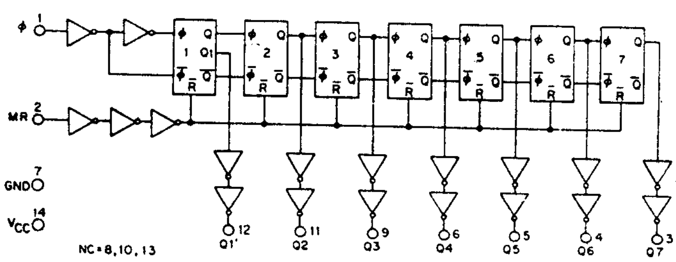
- *Fully static operation:*
- *Buffered inputs:*
- *Common reset*
- *Typical f_{MAX} = 50 MHz @ V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C*

The RCA-CD54/74HC4024 and CD54/75HCT4024 are 7-stage ripple-carry binary counters. All counter stages are master-slave flip-flops. The state of the stage advances one count on the negative transition of each input pulse; a high voltage level on the MR line resets all counters to their zero state. All inputs and outputs are buffered.

The CD54HC4024 and CD54HCT4024 are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC4024 and CD74HCT4024 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- *Fanout (over temperature range):*
  Standard outputs - 10 LSTTL loads
  Bus driver outputs - 15 LSTTL loads
- *Wide operating temperature range:*
  CD74HC/HCT: -40 to +85°C
- *Balanced propagation delay and transition times*
- *Significant power reduction compared to LSTTL logic ICs*
- *Alternate source is Philips/Signetics*
- *CD54HC/CD74HC types:*
  2 to 6 V operation
  High noise immunity: N_{IL}= 30%, N_{IH}=30% of V_{CC} @ V_{CC} =5 V
- *CD54HCT/CD74HCT types:*
  4.5 to 5.5 V operation
  Direct LSTTL input logic compatibility
  V_{IL}=0.8 V max., V_{IH}=2 V min.
  CMOS input compatibility
  $I_I \leq 1\ \mu A$ @V_{OL}, V_{OH}



92CM-38451R3

Fig. 1 - Logic diagram for the CD54/74HC/HCT4024.

TRUTH TABLE

φ	MR	OUTPUT STATE
↑ (rising edge)	L	No Change
↓ (falling edge)	L	Advance to Next State
X	H	All Outputs are Low

H = high level (steady state)
L = low level (steady state)
X = don't care

CD54/74HC4024
CD54/74HCT4024

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) .... -0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR V_I < -0.5 V OR V_I > V_{CC} +0.5 V) .... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR V_o < -0.5 V OR V_o > V_{CC} +0.5 V) .... ±20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR -0.5 V < V_o < V_{CC} +0.5 V) .... ±25 mA
DC V_{CC} OR GROUND CURRENT, (I_{CC}) .... ±50 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) .... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) .... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H) .... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H) .... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M) .... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) .... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H .... -55 to +125°C
PACKAGE TYPE E, M .... -40 to +85°C
STORAGE TEMPERATURE (T_{stg}) .... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. .... +265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only .... +300°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A=Full Package Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage, V_I, V_O	0	V_{CC}	V
Operating Temperature, T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times, t_r,t_f:			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

*Unless otherwise specified, all voltages are referenced to Ground.

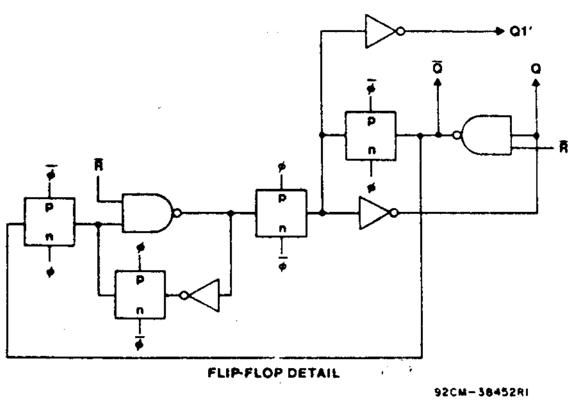


Fig. 2 - Flip-flop No. 1 detail.

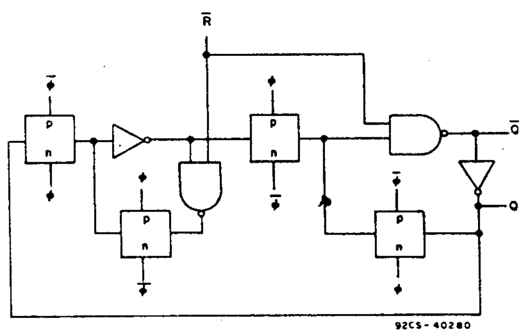


Fig. 3 - Detail for flip-flops 2 through 7.

CD54/74HC4024
CD54/74HCT4024

STATIC ELECTRICAL CHARACTERISTICS

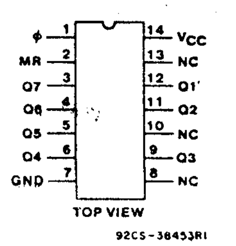
CHARACTERISTICS	CD74HC4024/CD54HC4024										CD74HCT4024/CD54HCT4024									UNITS
	TEST CONDITIONS			74HC/54HC TYPE			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPE			74HCT TYPE		54HCT TYPE		
				+25°C			-40/ +85°C		-55/ +125°C				+25°C			-40/ +85°C		-55/ +125°C		
	V_I V	I_O mA	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max	V_I V	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or V_{IH}										V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-4	4.5	3.98	—	—	3.84	—	3.7	—										
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			[illegible]	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}										V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		4	4.5	—	—	0.26	—	0.33	—	0.4										
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} and Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA
Additional Quiescent Device Current per Input Pin: 1 Unit Load ΔI_{CC}*											V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA

*For dual-supply system theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
ϕ, MR	0.5

*Unit Load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 360 μA max.@25°C.



TERMINAL ASSIGNMENT

CD54/74HC4024
CD54/74HCT4024

SWITCHING CHARACTERISTICS (V_{CC}=5 V, T_A=25°C, Input t_r,t_f=6 ns)

CHARACTERISTIC	SYMBOL	C_L (pF)	TYPICAL VALUES HC	TYPICAL VALUES HCT	UNITS
Propagation Delay ϕ to Q1'	t_{PHL}, t_{PLH}	15	11	17	ns
Qn to Qn+1	t_{PHL}, t_{PLH}	15	6	6	ns
MR to Q_n	t_{PHL}, t_{PLH}	15	14	17	ns
Power Dissipation Capacitance*	C_{PD}	—	30	30	pF

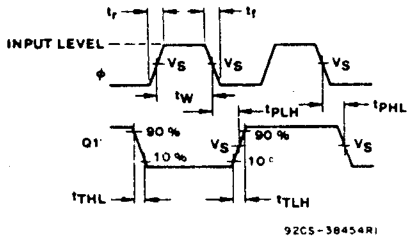
*C_{PD} is used to determine the dynamic power consumption, per package.
$P_D = C_{PD} V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_i/M)$ where:
$M=2^1,2^2,2^3,2^4,2^5,2^6,2^7$
C_L=output load capacitance
fi=input frequency

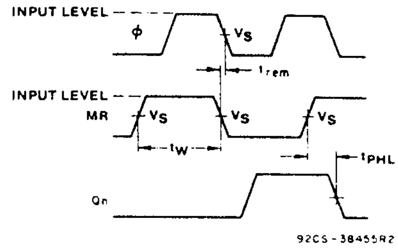
Prerequisite for Switching Function

CHARACTERISTIC	SYMBOL	VCC	25°C HC Min.	25°C HC Max.	25°C HCT Min.	25°C HCT Max.	-40°C to +85°C 74HC Min.	74HC Max.	74HCT Min.	74HCT Max.	-55°C to +125°C 54HC Min.	54HC Max.	54HCT Min.	54HCT Max.	UNITS
Maximum Input Pulse Frequency	f_{MAX}	2	6	—	—	—	5	—	—	—	4	—	—	—	MHz
		4.5	30	—	25	—	24	—	20	—	20	—	16	—	
		6	35	—	—	—	29	—	—	—	24	—	—	—	
Input Pulse Width	t_W	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
		4.5	16	—	20	—	20	—	25	—	24	—	30	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	
Reset Removal Time	t_{REM}	2	50	—	—	—	65	—	—	—	75	—	—	—	
		4.5	10	—	10	—	13	—	13	—	15	—	15	—	
		6	9	—	—	—	11	—	—	—	13	—	—	—	
Reset Pulse Width	t_W	2	80	—	—	—	100	—	—	—	120	—	—	—	
		4.5	16	—	20	—	20	—	25	—	24	—	30	—	
		6	14	—	—	—	17	—	—	—	20	—	—	—	

SWITCHING CHARACTERISTICS (C_L=50 pF, Input t_r,t_f=6 ns)

CHARACTERISTIC	SYMBOL	VCC	25°C HC Min.	25°C HC Max.	25°C HCT Min.	25°C HCT Max.	-40°C to +85°C 74HC Min.	74HC Max.	74HCT Min.	74HCT Max.	-55°C to +125°C 54HC Min.	54HC Max.	54HCT Min.	54HCT Max.	UNITS
Propagation Delay, ϕ to Q1' Output	t_{PLH}, t_{PHL}	2	—	140	—	—	—	175	—	—	—	210	—	—	ns
		4.5	—	28	—	40	—	35	—	50	—	42	—	60	
		6	—	24	—	—	—	30	—	—	—	36	—	—	
Propagation Delay Qn to Qn+1	t_{PLH}, t_{PHL}	2	—	75	—	—	—	95	—	—	—	110	—	—	ns
		4.5	—	15	—	15	—	19	—	19	—	22	—	22	
		6	—	13	—	—	—	13	—	—	—	19	—	—	
Propagation Delay MR to Q_n	t_{PHL}	2	—	170	—	—	—	215	—	—	—	255	—	—	ns
		4.5	—	34	—	40	—	43	—	50	—	51	—	60	
		6	—	29	—	—	—	27	—	—	—	43	—	—	
Output Transition Time	t_{TLH}, t_{THL}	2	—	75	—	—	—	95	—	—	—	110	—	—	ns
		4.5	—	15	—	15	—	19	—	19	—	22	—	22	
		6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C_I	—	—	10	—	10	—	10	—	10	—	10	—	10	pF





	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
Switching Voltage, V_S	50% V_{CC}	1.3 V

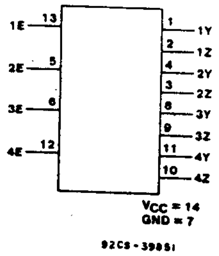
Fig. 4 - Input Pulse pre-requisite times, propagation delays and output transition times.

Fig. 5 - Master Reset pre-requisite and propagation delays.

CD54/74HC4066
CD54/74HCT4066

File No. 1777

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

Quad Bilateral Switch

Type Features:

- *Wide analog-input-voltage range: 0-10 V*
- *Low "ON" resistance: 25 Ω @ V_{CC} = 4.5 V*
  15 Ω @ V_{CC} = 9 V
- *Fast switching and propagation delay times*
- *Low "OFF" leakage current*

The RCA CD54/74 HC/HCT4066 contains four independent digitally controlled analog switches that use silicon-gate CMOS technology to achieve operating speeds similar to LSTTL with the low power consumption of standard CMOS integrated circuits.

These switches feature the characteristic linear "ON"-resistance of the metal-gate CD4066B. Each switch is turned on by a high-level voltage on its control input.

The CD54HC4066 and CD54HCT4066 are supplied in 14-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC4066 and CD74HCT4066 are supplied in 14-lead dual-in-line plastic packages (E suffix) and in 14-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- *Alternate Source: Philips/Signetics*
- *Wide operating temperature range:*
  CD74HC/HCT: -40 to +85° C
- *CD54HC/CD74HC types:*
  2 V to 10 V operation
  High noise immunity:
  N_{IL} = 30%, N_{IH} = 30% of V_{CC}; @ V_{CC} = 5 V & 10 V
- *CD54HCT/CD74HCT types:*
  Direct LSTTL input logic compatibility
  V_{IL} = 0.8 V Max., V_{IH} = 2 V Min.
  CMOS input compatiblity
  $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}

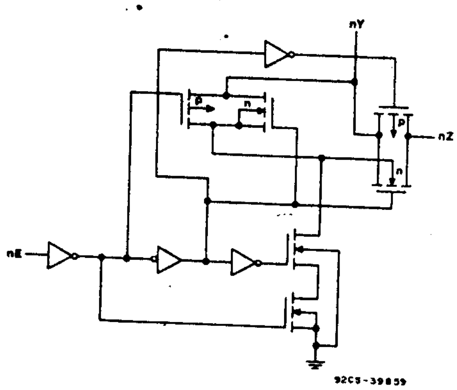


Fig. 1 - Logic diagram (one switch).

TRUTH TABLE

INPUT nE	SWITCH
L	off
H	on

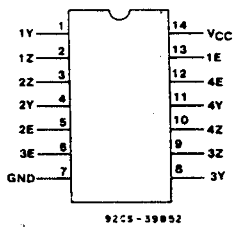
H = HIGH Level
L = LOW Level

CD54/74HC4066
CD54/74HCT4066

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):	
(Voltages referenced to ground)	
HCT Types	-0.5 to +7 V
HC Types	-0.5 to +10.5 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} + 0.5$ V)	±20 mA
DC SWITCH DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC} + 0.5$ V)	±20 mA
• DC SWITCH CURRENT, I_O, (FOR $V_I > -0.5$ V OR $V_I < V_{CC} + 0.5$ V)	±25 mA
DC V_{CC} OR GROUND CURRENT (I_{CC})	±50 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H)	Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M)	400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M)	Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPE F, H	-55 to +125°C
PACKAGE TYPE E, M	-40 to +85°C
STORAGE TEMPERATURE (T_{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only	+300°C

• In certain applications, the external load-resistor current may include both V_{CC} and signal-line components. To avoid drawing V_{CC} current when switch current flows into the transmission gate inputs, (terminals 1, 4, 8 and 11) the voltage drop across the bidirectional switch must not exceed 0.6 volt (calculated from R_{on} values shown in the Electrical Characteristics Chart). No V_{CC} current will flow through R_L if the switch current flows into terminals 2, 3, 9 and 10.



TERMINAL ASSIGNMENT

CD54/74HC4066
CD54/74HCT4066

RECOMMENDED OPERATING CONDITIONS: For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS MIN.	LIMITS MAX.	UNITS
Supply-Voltage Range (For T_A = Full Package-Temperature Range) V_{CC}:*			
CD54/74HC Types	2	10	V
CD54/74HCT Types	4.5	5.5	V
DC Input Voltage, V_C, and Analog Switch Voltage, V_{IO}	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times t_r, t_f (Control Inputs)			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 9 V	0	250	ns

*Unless otherwise specified, all voltages are referenced to Ground.

STATIC ELECTRICAL CHARACTERISTICS

CD74HC4066/CD54HC4066

CHARACTERISTIC	Test Conditions: CONTROL V_I V	Test Conditions: SWITCH V_{IS} V	V_{CC} V	74HC/54HC Types +25°C Min	+25°C Typ	+25°C Max	74HC Types -40/+85°C Min	-40/+85°C Max	54HC Types -55/+125°C Min	-55/+125°C Max
High-Level Input Voltage V_{IH}	—	—	2	1.5	—	—	1.5	—	1.5	—
			4.5	3.15	—	—	3.15	—	3.15	—
			9	6.3	—	—	6.3	—	6.3	—
Low-Level Input Voltage V_{IL}	—	—	2	—	—	0.5	—	0.5	—	0.5
			4.5	—	—	1.35	—	1.35	—	1.35
			9	—	—	2.7	—	2.7	—	2.7
Input Leakage Current (Any Control) I_{IL}	V_{CC} or Gnd	—	10	—	—	±0.1	—	±1	—	±1
Off-Switch Leakage Current I_Z	V_{IL}	V_{CC} or Gnd	10	—	—	±0.1	—	±1	—	±1
"On" Resistance I_O = 1 mA (Fig. 2) R_{on}	V_{CC}	V_{CC} or Gnd	4.5	—	25	80	—	106	—	128
			6	—	20	75	—	94	—	113
			9	—	15	60	—	78	—	95
	V_{CC}	V_{CC} to Gnd	4.5	—	35	95	—	118	—	142
			6	—	24	84	—	105	—	126
			9	—	16	70	—	88	—	105
"On" Resistance Between Any Two Switches ΔR_{on}	V_{CC}	—	4.5	—	1	—	—	—	—	—
			6	—	0.75	—	—	—	—	—
			9	—	0.5					
Quiescent Device Current I_{CC}	V_{CC} or Gnd	—	6	—	—	2	—	20	—	40
			10	—	—	16	—	160	—	320
Additional Quiescent Device Current per Input Pin: 1 Unit Load ΔI_{CC}*	—	—	—	—	—	—	—	—	—	—

CD74HCT4066/CD74HCT4066

CHARACTERISTIC	Test Conditions: CONTROL V_I V	Test Conditions: SWITCH V_{IS} V	V_{CC} V	74HCT/54HCT Types +25°C Min	+25°C Typ	+25°C Max	74HCT Types -40/+85°C Min	-40/+85°C Max	54HCT Types -55/+125°C Min	-55/+125°C Max	UNITS
High-Level Input Voltage V_{IH}	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
Low-Level Input Voltage V_{IL}	—	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
Input Leakage Current (Any Control) I_{IL}	Any Voltage Between V_{CC} & Gnd	—	5.5	—	—	±0.1	—	±1	—	±1	µA
Off-Switch Leakage Current I_Z	V_{IL}	V_{CC} or Gnd	5.5	—	—	±0.1	—	±1	—	±1	µA
"On" Resistance I_O = 1 mA (Fig. 2) R_{on}	V_{CC}	V_{CC} or Gnd	4.5	—	25	80	—	106	—	128	Ω
			—	—	—	—	—	—	—	—	
			—	—	—	—	—	—	—	—	
	V_{CC}	V_{CC} to Gnd	4.5	—	35	95	—	118	—	142	Ω
			—	—	—	—	—	—	—	—	
			—	—	—	—	—	—	—	—	
"On" Resistance Between Any Two Switches ΔR_{on}	V_{CC}	—	4.5	—	1	—	—	—	—	—	Ω
			—	—	—	—	—	—	—	—	
			—	—	—	—	—	—	—	—	
Quiescent Device Current I_{CC}	V_{CC} or Gnd	—	5.5	—	—	2	—	20	—	40	µA
Additional Quiescent Device Current per Input Pin: 1 Unit Load ΔI_{CC}*	V_{CC}-2.1	—	4.5 to 5.5	—	100	360	—	450	—	490	µA

* For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads *
All	1

* Unit load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 3[illegible] μA max. @ 25°C.

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input t_r, t_f = 6 ns)

CHARACTERISTIC		C_L pF	TYPICAL HC	TYPICAL HCT	UNITS
Propagation Delay Time: Switch In to Out	t_{PHL} t_{PLH}	15	4	4	ns
Switch Turn Off	t_{PHZ}, t_{PLZ}	15	12	14	ns
Switch Turn On	t_{PZH}, t_{PZL}	15	8	9	ns
Power Dissipation Capacitance*	C_{PD}	—	25	38	pF

* C_{PD} is used to determine the dynamic power consumption, per package.
$P_D = C_{PD} V_{CC}^2 f_i + \Sigma (C_L + C_S) V_{CC}^2 f_o$ where: f_i = input frequency, C_L = load capacitance, V_{CC} = supply voltage, f_o = output frequency, C_S = switch capacitance

SWITCHING CHAARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC		V_{CC}	25°C HC Min.	25°C HC Max.	25°C HCT Min.	25°C HCT Max.	-40°C to +85°C 74HC Min.	-40°C to +85°C 74HC Max.	-40°C to +85°C 74HCT Min.	-40°C to +85°C 74HCT Max.	-55°C to +125°C 54HC Min.	-55°C to +125°C 54HC Max.	-55°C to +125°C 54HCT Min.	-55°C to +125°C 54HCT Max.	UNITS
Propagation Delay Time Switch In to Out	t_{PLH} t_{PHL}	2	—	60	—	—	—	75	—	—	—	90	—	—	ns
		4.5	—	12	—	12	—	15	—	15	—	18	—	18	
		9	—	8	—	—	—	11	—	—	—	13	—	—	
Switch Turn On Delay	t_{PZH} t_{PZL}	2	—	100	—	—	—	125	—	—	—	150	—	—	
		4.5	—	20	—	24	—	25	—	30	—	30	—	36	
		9	—	12	—	—	—	15	—	—	—	18	—	—	
Switch Turn Off Delay	t_{PHZ}, t_{PLZ}	2	—	150	—	—	—	190	—	—	—	225	—	—	
		4.5	—	30	—	35	—	38	—	44	—	45	—	53	
		9	—	24	—	—	—	30	—	—	—	36	—	—	
Input (Control) Capacitance	C_I	—	—	10	—	10	—	10	—	10	—	10	—	10	pF

CD54/74HC4066
CD54/74HCT4066

ANALOG CHANNEL CHARACTERISTICS - Typical Values at T_C = 25°C

CHARACTERISTIC	TEST CONDITIONS		V_{CC} V	HC	HCT	UNITS
Switch Frequency Response Bandwidth at -3 dB (Fig. 12)	Fig. 3 Notes 1 & 2		4.5	200	200	MHz
Cross Talk Between Any Two Switches (Fig. 13)	Fig. 4 Notes 2 & 3		4.5	-72	-72	dB
Total Harmonic Distortion	1 KHz,	V_{IS} = 4 Vpp	4.5	0.022	0.023	%
	Fig. 5	V_{IS} = 8 Vpp	9	0.008	N/A	
Control to Switch Feedthrough Noise	Fig. 6		4.5	TBE	TBE	mV
			9	TBE	TBE	
Switch "OFF" Signal Feedthrough (Fig. 13)	Fig. 7 Notes 2 & 3		4.5	-72	-72	dB
Switch Input Capacitance C_S	—		—	5	5	pF

Notes: 1. Adjust input level for 0 dBm at output, f = 1 MHz.
2. V_{IS} is centered at $V_{CC}/2$.
3. Adjust input for 0 dBm at V_{IS}.

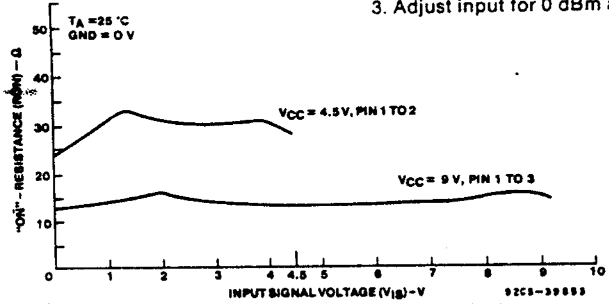


Fig. 2 - Typical "ON" resistance vs. input signal voltage.

ANALOG TEST CIRCUITS

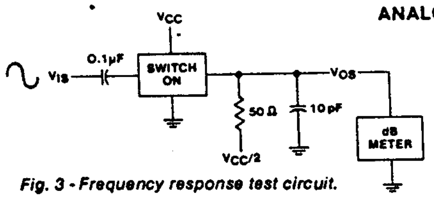


Fig. 3 - Frequency response test circuit.

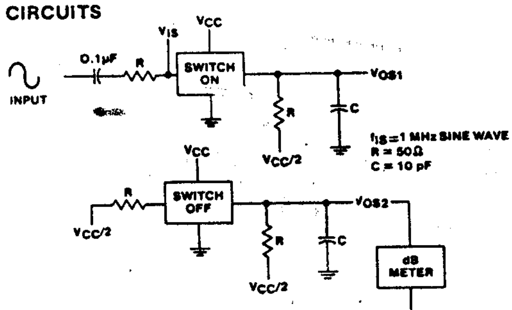


Fig. 4 - Crosstalk between two switches test circuit.

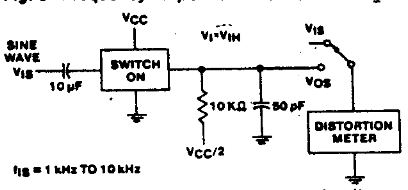


Fig. 5 - Total harmonic distortion test circuit.

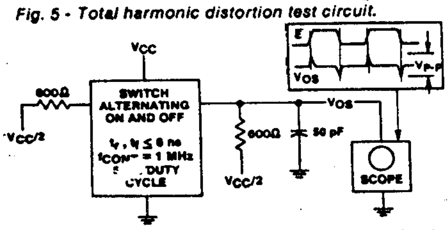


Fig. 6 - Control-to-switch feedthrough noise test circuit.

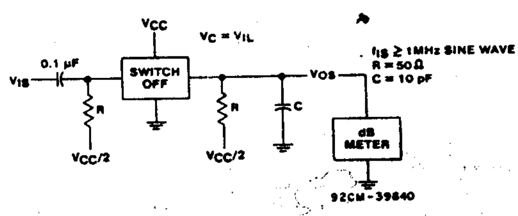


Fig. 7 - Switch off signal feedthrough.

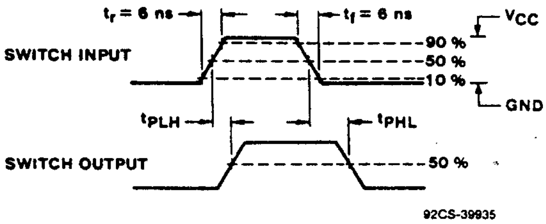


Fig. 8 - Switch propagation - delay times waveforms.

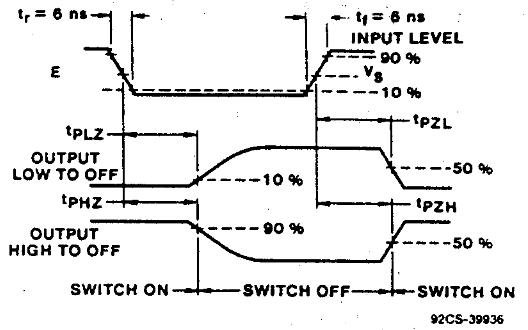


Fig. 9 - Switch turn-on and turn-off propagation delay times waveforms.

	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
Switching Voltage, V_s	50% V_{CC}	1.3 V

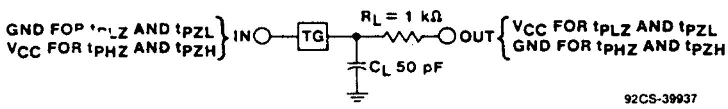


Fig. 10 - Switch on/off propagation delay time test circuit.

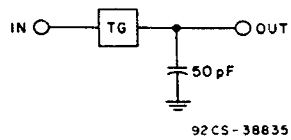


Fig. 11 - Switch-in to switch-out propagation delay time test circuit.

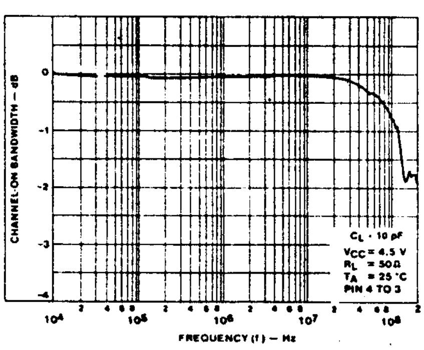


Fig. 12 - Switch frequency response, V_{CC} = 4.5 V.

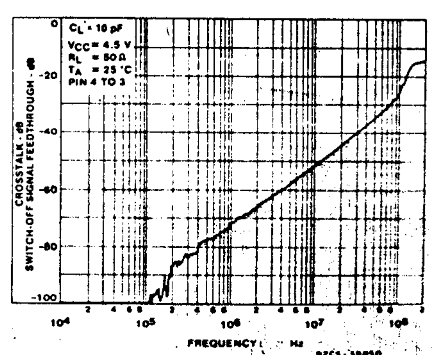
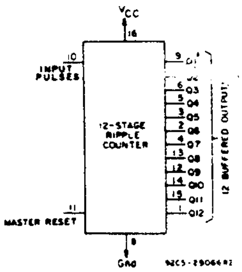


Fig. 13 - Switch-off signal feedthrough and crosstalk vs. frequency, V_{CC} = 4.5 V.

CD54/74HC4040
CD54/74HCT4040

File Number **1483**

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

12-Stage Binary Counter

Type Features:

- *Fully static operation*
- *Buffered inputs*
- *Common reset*
- *Negative edge pulsing*
- *Typical f_{MAX} = 50 MHz @ V_{CC} = 5 V, C_L = 15 pF, T_A = 25° C*

The RCA-CD54/74HC4040 and CD54/74HCT4040 are 12-stage ripple-carry binary counters. All counter stages are master-slave flip-flops. The state of the stage advances one count on the negative transition of each input pulse; a high voltage level on the MR line resets all stages to their zero state. All inputs and outputs are buffered.

The CD54HC4040 and CD54HCT4040 are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC4040 and CD74HCT4040 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface mount plastic package (M suffix). Both types are also available in chip form (H suffix).

TRUTH TABLE

φ	MR	Output State
⎍ (rising)	L	No Change
⎍ (falling)	L	Advance to next state
X	H	All Outputs are low

H = high level (steady state)
L = low level (steady state)
X = don't care

Family Features:

- *Fanout (Over Temperature Range):*
  - *Standard Outputs - 10 LSTTL Loads*
  - *Bus Driver Outputs - 15 LSTTL Loads*
- *Wide Operating Temperature Range:*
  - *CD74HC/HCT: -40 to +85° C*
- ***Balanced Propagation Delay and Transition Times***
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  - *2 to 6 V Operation*
  - *High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC} @ V_{CC} = 5 V*
- *CD54HCT/CD74HCT Types:*
  - *4.5 to 5.5 V Operation*
  - *Direct LSTTL Input Logic Compatibility V_{IL} = 0.8 V Max., V_{IH} = 2 V Min.*
  - *CMOS Input Compatibility $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}*

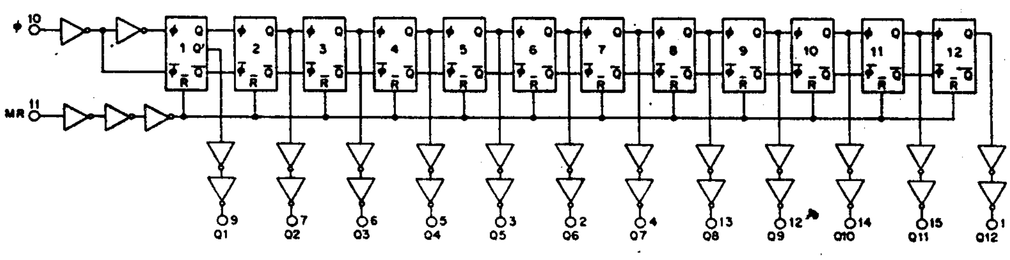


Fig. 1 - Logic block diagram.

92CL-37015R3