"WIPAC"

INTELLIGENT WINDING PACKAGE CONTROLLER

PROJECT WORK 1992 - 93

SUBMITTED BY

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UNDER THE GUIDANCE OF

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In partial fulfilment of the requirements for the award of degree of

BACHELOR OF ENGINEERING IN ELECTRONICS & COMMUNICATION ENGINEERING

of Bharathiar University,

COIMBATORE

APRIL - 1993

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CERTIFICATE

This is to Certify that the report entitled

"W I P A C"

INTELLIGENT WINDING PACKAGE CONTROLLER

has been submitted by

Mr____________________________

in partial fulfilment for the award of Bachelor of Engineering in the ELECTRONIC AND COMMUNICATION ENGINEERING branch of the Bharathiar University, Coimbatore during the academic year 1992 - 1993

Guide　　　　　　　　　　Head of the Department

Certified that the Candidate was examined by us in the Project Work Viva - Voce Examination held on .... and the University register number was________________

Internal Examiner　　　　　　　　　　External Examiner

ACKNOWLEDGEMENT

We are grateful and indebted to our Principal **MAJOR.T. S.RAMAMURTHY, B.E., M.I.S.T.E** and the MANAGEMENT for the ample facilities made available to us for carrying out our project.

We would like to thank our prolific Professor and Head of Electronics and Communication Engineering Rtn. Prof. **K.PALANISWAMI, M.E., M.I.E.E.E., M.I.E., M.I.S.T.E., M.C.S.I., F.I.E.T.E.,** without whom this project would never have seen the light of this day.

We are thankful to **MR.G.R.JAGANATHAN** PROPRIETOR of **MICRO ELECTRIC CONTROLS** for providing all facilities in his company for fulfilment of this project and to **Mr.N.PARTHASARTHI** Development Engineer **MICRO ELECTRIC CONTROLS** for his help during the implementation of this project in the company.

We wish to record our deep gratitude to **MR.R.SIVAKUMAR,M.E., M.I.E** Partner of **INTEGRATED ELECTRONICS COMPANY** Bangalore.

We are thankful to **MR.K.RAMPRAKASH M.E.,** for his guidance in the process of project development. We would also like to note our appreciation and gratitude to our guiding light **Mrs. G.KALA,B.E.,** Department of Electronics and Communication Engineering for her valuable suggestions at all stages of this project.

We are thankful to **Mr.RAMASWAMY M.E.,** Assistant Professor and **Mr.SHANMUGA SHANKER B.E.,** of Computer Science Engineering Department for their guidance in the process of our project.

We would be failing in our duty if we don't thank the other staff members and the laboratory technicians of our Department for help they have rendered to us.

- AUTHORS.

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SYNOPSIS

The "**WINDING PACKAGE CONTROLLER " (WIPAC)** is an advanced, versatile instrument capable of accurate measurement of yarn length and shift efficiency. In addition to these it can also locate the head which has mechanical error. This involves

1. Sensing and Fabrication of an electronic circuit to find out the presence of yarn.
2. Design of hardware to show the yarn length wound.
3. Software for
   a. Counting the length of the yarn.
   b. Displaying the count.
   c. Shift Efficiency.
   d. Locating the mechanical error.
4. Interfacing with microprocessor system

This system finds wide application in textile industry.

PRESENT SYSTEM

In present existing textile mills there are number of units such as cotton purifier, cotton to yarn, yarn into the knitting yarn. This knitting yarn is wound on the cone. There will be number of cones which are being wound by a single spindle drum, which is surface driven. This arrangement is shown in figure 1. The spindle drum as shown in figure 1 is made of bakelite on which helical grooves are present to direct yarn to the cone. These helical grooves helps in uniform yarn winding.

The motor follows a principle called stop-run method to avoid loose winding of yarn on the cone. This occurs in the rate of 76 STOPS/MIN. The speed of the spindle is approximately **2050 r.p.m. There are different types of yarn which are to be wound depending on their thickness.** eg. 38's type -40's type.

For 40's type the weight of 1 metre is **0.069 gm.** The cone -yarn arrangement in the machine is called as **HEAD.**

ARRANGEMENT OF YARN WINDING SYSTEM.

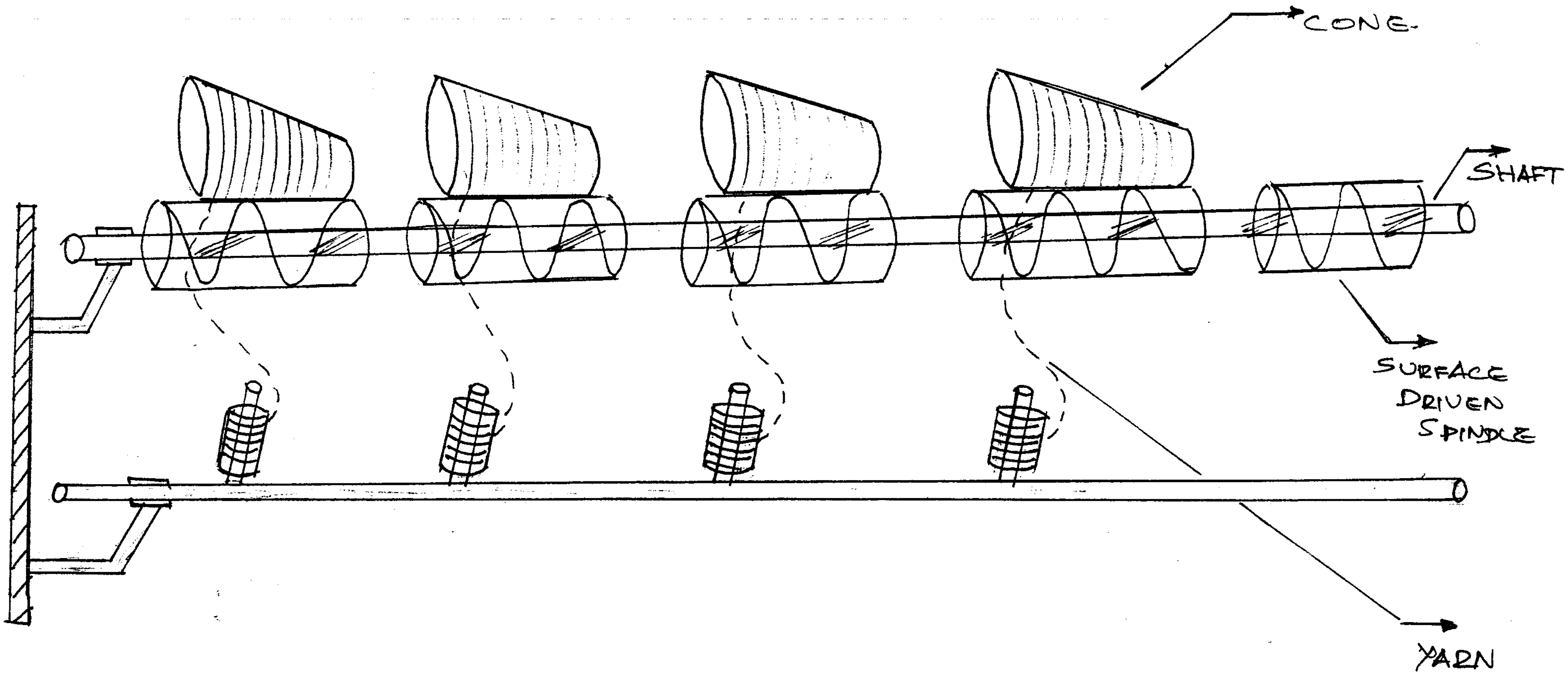


FIGURE (1)

EFFICIENCY:

Efficiency of the shift is defined as

$$EFF = \frac{\text{Total time of shift} - \text{Total time of cones stopped}}{\text{Total time of shift}}$$

Total time of shift is nothing but the total time for which the machine runs in a shift. Total time of cones stopped is nothing but the time for which cone 1 stopped + cone 2 stopped +------ cone n stopped.

MECHANICAL ERROR

If a yarn of particular head is broken many times the problem might not be due to the yarn, It is the problem associated with the cone rotation which is mechanical part. Usually if a yarn of particular head has broken more than 5 times in an hour, then it is said to have mechanical error.

As in this system all cones are weighed manually one by one which is not an efficient method as it decreases the productivity.

INTRODUCTION

There is a tremedous change in science and technology which implemented in all fields. In the textile field, new technologies such as CNC are implemented which is costly and it is not used by small scale industry. So the operations such as knotting, weighing of the cone removal of flux etc. are performed manually.

In our project, the burden of operator, in weighing the cone repeatedly to standarise is eliminated. Automatic weighing of each cone in a unit is not easy and economic as there are many cones to be wound in a unit. The length and weight of the cone are having definite proportion, so istead of weighing the cone we go for length.

Our project WIPAC determines the exact length of the yarn to be wound on the cone to have a standard weight. For this we use phototransistor, photo LED, programmable peripheral interface (8255), times (IC 555). Microprocessor, serial shift registers(4094) and seven segment displays.

The system WIPAC consists of following units

1. Sensing unit
2. Serial shift register and Display unit
3. Timer unit
4. Interface unit
5. Microprocessor unit

Along with this WIPAC also includes the determination of efficiency of the shift and locating the cone which is mechanically erroneous.

BLOCK DIAGRAM AND DESCRIPTION

We use PRECITRON MICROPROCESSOR (8085) TRAINER KIT. We make use of some subroutines inbuilt such as RDKBD to sense the keyboaard, output to display the digits on display of PRECITRON KIT, HILO to subtract 16 bit numbers and CLEAR to clear the display. We use RST 6.5 and RST 5.5 interrupts to interrupt the MPU main program operation. RST 6.5 is connected to the proximity switch output and the RST 5.5 is connected to the timer (Astable multi) output.

Two 8255'S present in the kit is used for external hardware interface.8255-I port A is connected to the input of the display unit. 8255 -II port B is connected to the output of the photodetectors. 8255 -I port C is connected to the input of the cutters. 8255-II port A is connected to the mechanical indicators. 8255-II portB and port C can be used for future expansion.

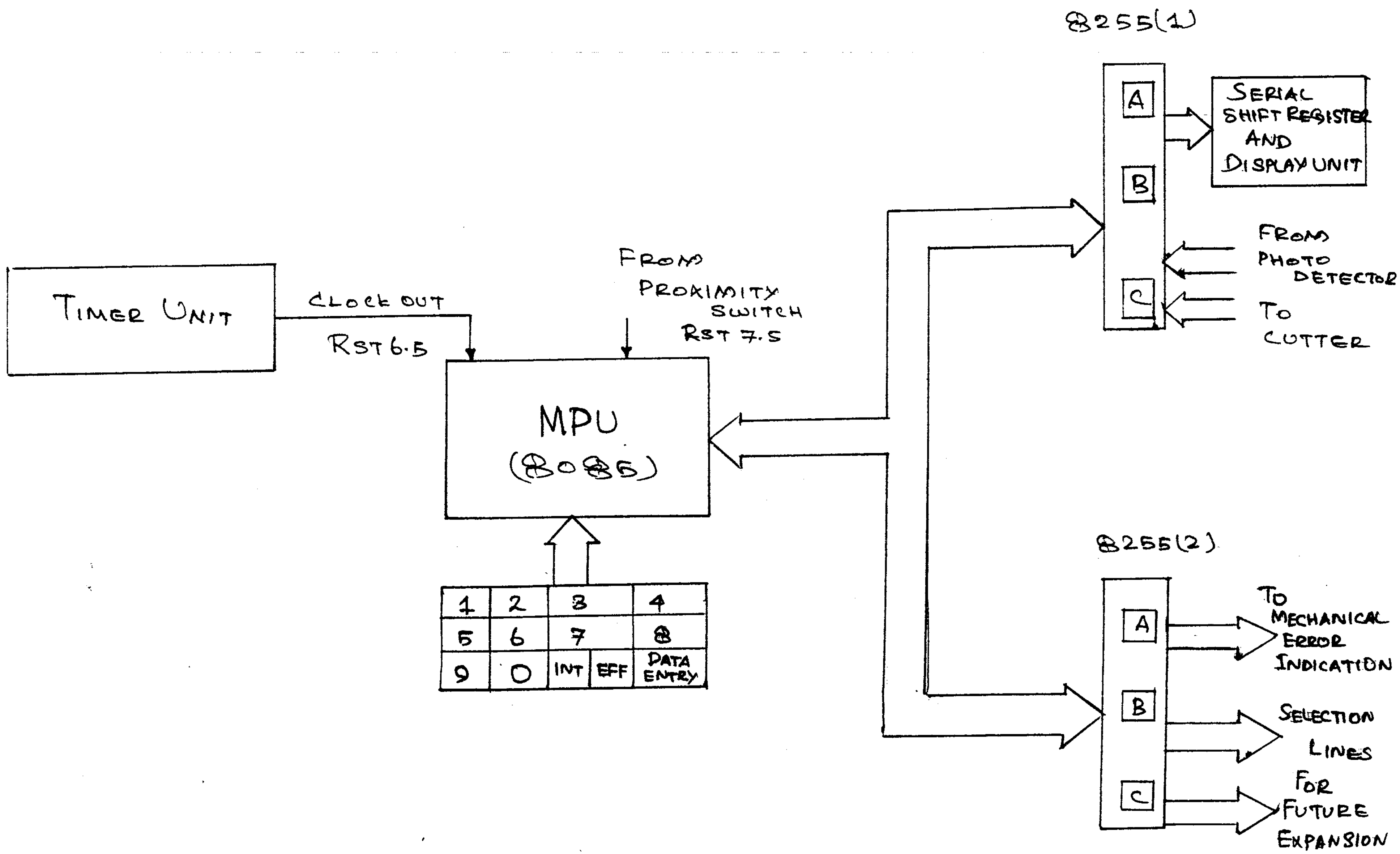
In the keyboard some keys are renamed as follows.

COMP KEY- INITIALISATION

DEL KEY- DATA ENTRY

NEXT KEY- EFFICIENCY

BLOCKDIAGRAM OF WIPAC SYSTEM.



The MPU is the heart of this sytem. The MPU will be continuously monitoring the keyboard. If the INITALISATION key is pressed the MPU calls INIT -WI subroutine to initialise (i.e make zero) the length count of all heads and time counts. If DATA ENTRY key is pressed the MPU calls DATENT-WI subroutine to get the count which is going to be entered by the operator via keyboard and to display it. If EFFICIENCY KEY is pressed MPU calls EFF-WI subroutine to calculate and display the efficiency of the shift.

With these if 6.5 has interrupted the MPU enters into the subroutine COUNT-UPDT-WI to check the presence of yarn, increment the count , Display the count, Check the count with the count entered by the operator and to send the signal to cutter. And if 5.5 has interrupted the MPU enters into the TIMINC -WI subroutine to increment the total time of shift, check the presence of yarn and the total time of shift, check the presence of yarn and to increment the total time of run, locate the mechanically erroneous head and to indicate it.

This processes are shown in flow chart(1)

CIRCUIT DESCRIPTION

MPU (8085) can communicate with the 8255 (I) and 8255 -(II) through data lines. 8255-I port A, A0(data), A1(clock), A2(strobe), lines are connected to the buffer (4050) at the pins 3,5 and 7 respectively. The buffer outputs at pins 2,4 and 6 of 4050 is connected as follows.

4094 IC is a serial shift register with storage and it has 3 inputs as data, clock and strobe. It also has 10 outputs, 8 for latched outputs and 2 for data outputs for fast and slow operation. Pin 2 of 4050 is Data and this is connected to the data input pin 2 of 4094. Data output of 4094 IC pin 9 is connected to the Data input of next 4094 IC(pin 2).

All clock lines of 4094's are tied together and connected to the Pin 4 of 4050. All strobe lines (pin 1) of 4094's are tied together and connected to the pin 6 of 4050.

The 8255-I port B is used to read the photodetectors. A photo LED is used to glow always and a phototransistor is used to sense the presence of yarn. The output of the photodetector is connected to the Port B lines. 8255-I port c is connected to the octal buffer 74241 and outputs of buffer is connected to activate the monostable multivibrator using IC 555 which is designed for 1 sec to operate the relay. The design for 1 sec is shown below

$t = 1.1\ Ra \times C$

Assuming $Ra = 10$ M ohm $\quad t = 1$ sec

$C = 1/1.1 \times 10$ M ohm

$= 0.09$ micro farad

$\simeq 0.1$ micro farad.

8255- II port A is connected to the LED's to indicate the mechanical error.

DESCRIPTION OF EACH UNIT

SENSING UNIT:

There are two type of sensors used, they are

1. Yarn sensors.
2. Shaft rotation sensors.

1. YARN SENSORS

The presence of yarn should be detected inorder to know whether yarn being wound on the cone for the incrementing of the count(length) of that particular head. Using of mechanical sensors such as variable capacitors and springs are not advisable as they will affect the tension of the yarn as the yarn might be broken. So we use optical sensors. This comprises of photodetectors(phototransistor and Photo diode etc.) and photo LED. Photo transistors are preferred as they provide amplication.

Photo tranistors senses the yarn presence which is traversing between photo LED and phototransistor. The operator is indicated if the yarn is broken by glowing a LED. We use infra-red LED so that their won't be any interference from other light sources present in the industry. As shown in figure 2 when the yarn is being wound, the photodetector is

PHOTODETECTOR CIRCUIT.

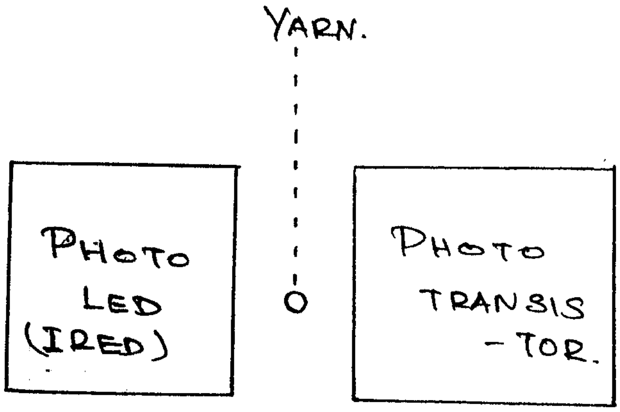


FIG [1]

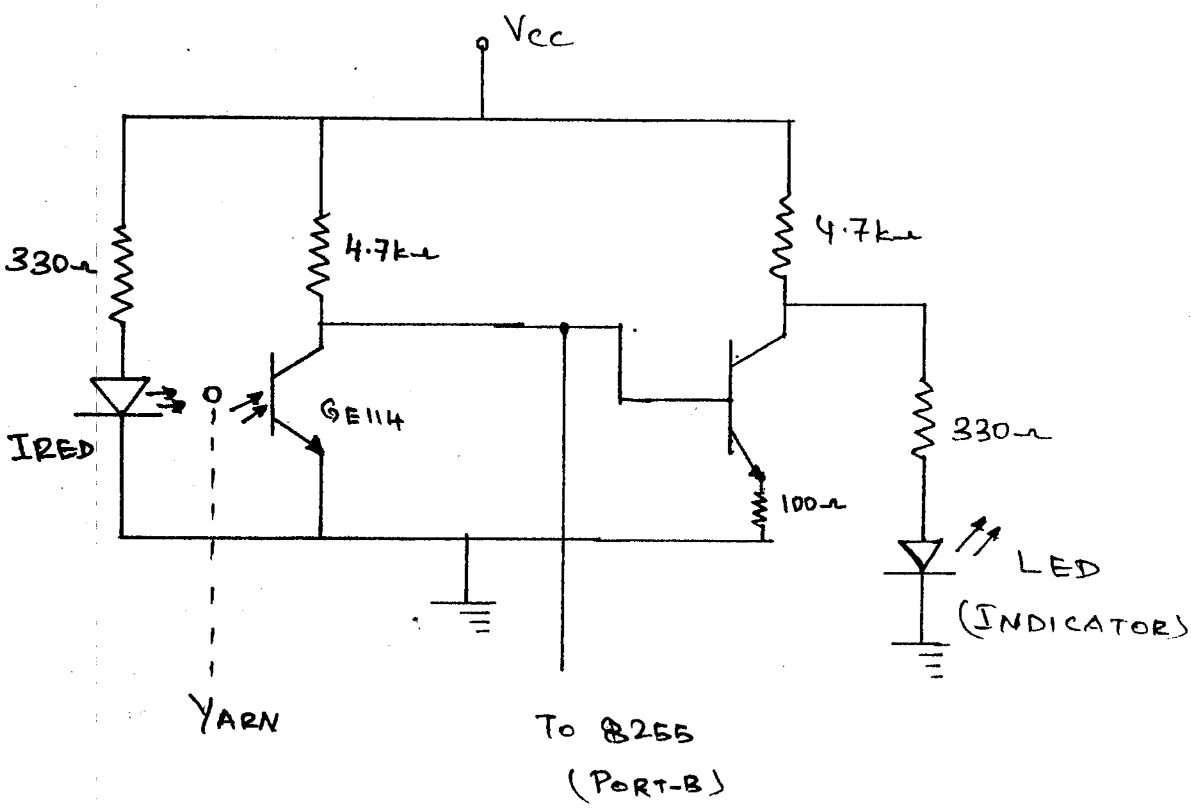


FIG [2]

is blocked by yarn to get the IR light and so it is in cut-off state. So output is Vcc =5v, when the yarn is cut the IR light falls on the phototransistor and it is driven into the active region and output is 0v. So photo-detector output is 1 when the yarn is present and zero when the yarn is found cut. Instead of sensing a yarn we sense yarn break detector. Photodetector is connected to MPU through 8255-I port B. MPU checks the photodetector output for each rotation of the shaft and the increments the count if the photodetector output is set. MPU also uses the photodetector output for the finding out the mechanical error and efficiency. The photodetector output is inverted by the inverter 7404 IC and it drives a LED for indication to the operator. We use 55GE 522 LED and GE114G photo transistor.

2. SHAFT ROTATION SENSORS.

In this we use proximity switch which converts the rotation into the pulses. We use this sensor to convert the rotation of the shaft into the pulses. These pulses are used to the interrupt the MPU to update the length wound on the cone. Block diagram of proximity switch is shown in the figure 3. RF oscillator is used to create magnetic field. This magnetic field is disturbed when a metal comes near the field. The output of the RF oscillator is given to the schmitt trigger and it is output decreases. So when the metal is in the field, the output is low, else the output is high.

SHAFT ROTATION SENSOR.
[PROXIMITY SWITCH.]

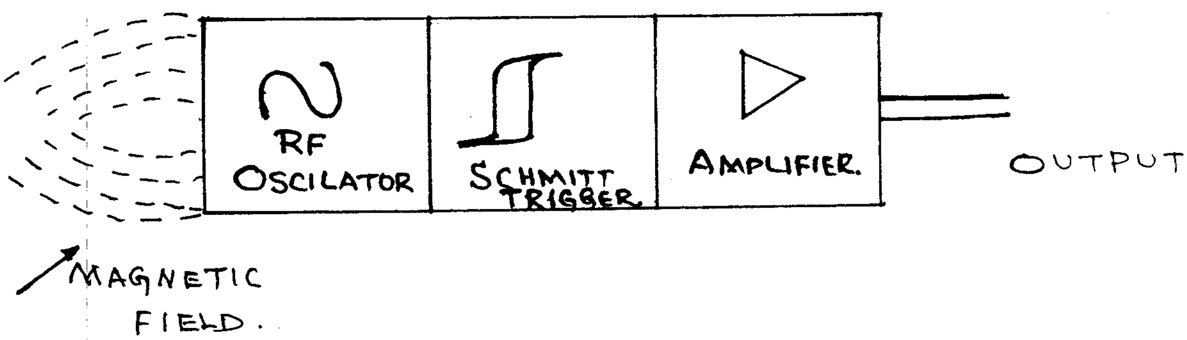


FIGURE. 3

SERIAL SHIFT REGISTER AND DISPLAY UNIT

This unit is used to display the current length of the yarn that is wound on the cone of every head. To display the count of each head(5 digits per head) the display datas are transferred to the display serially using a special IC 4094, which is serial shift register with storage as shown in the figure 4.

So if a digit has to be displayed in a seven segment display the details of a,b,c,d,e,f,g and dot has to be given to the display. For this, having a single line which is connected to the data input of the IC 4094 through which 8 bits a,b,c,d,e,f,g and dot are transferred one by one using clock. The data regarding the digit to be displayed is transferred to the serial shift register. And now if strobe is enabled, the contents of serial shift register is latched and the digits are displayed on the display.

So, to transfer the count in memory to the display the same procedure is adapted. As the data output of first 4094 IC is connected to the data input of the next IC 4094 all digits of the count of the head can

Serial Shift Register With Display

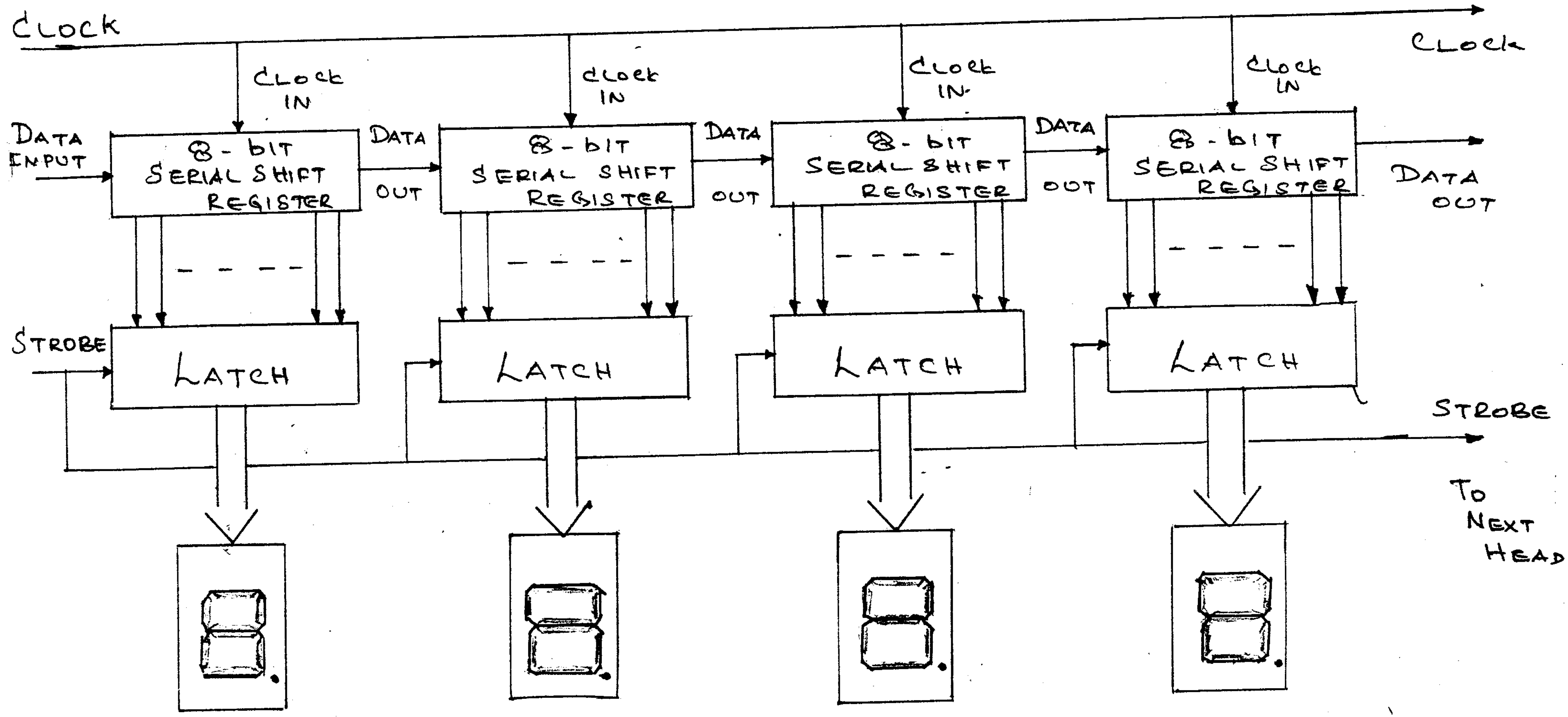
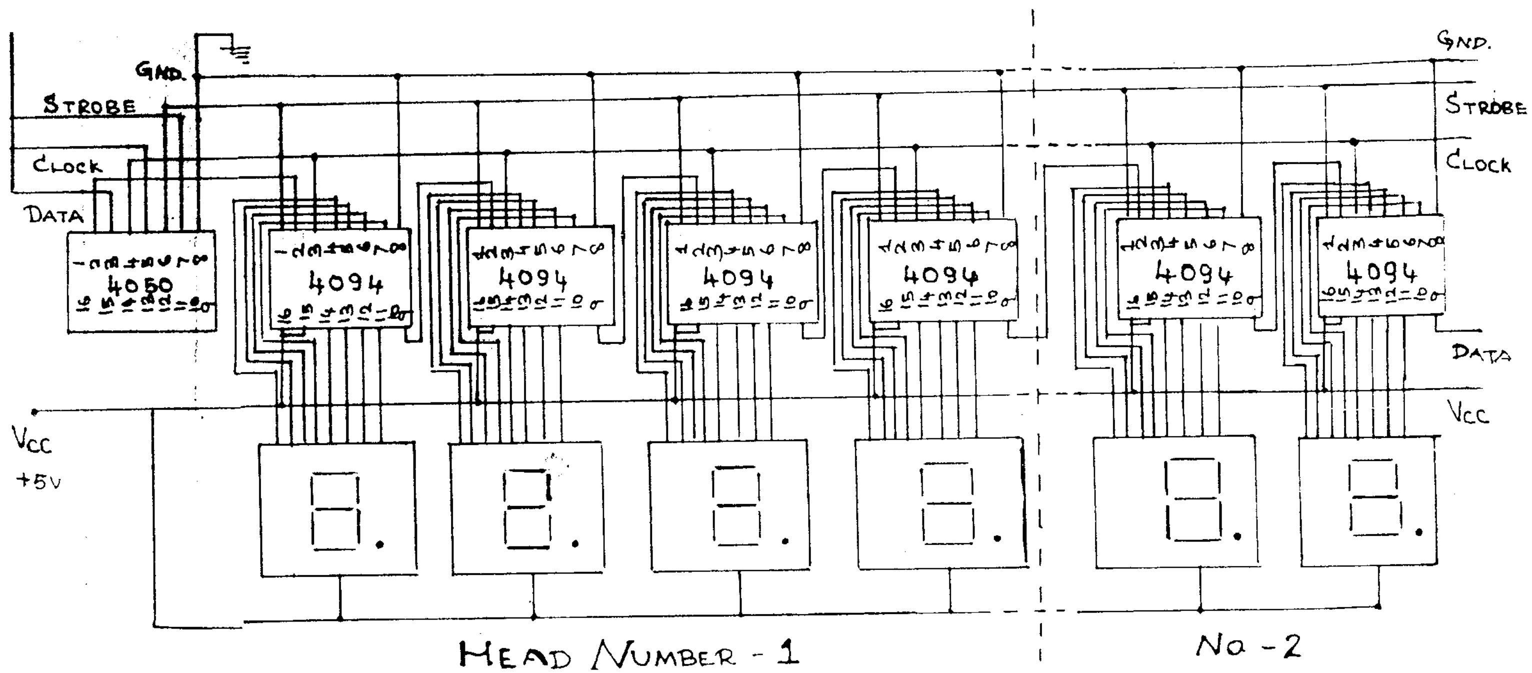
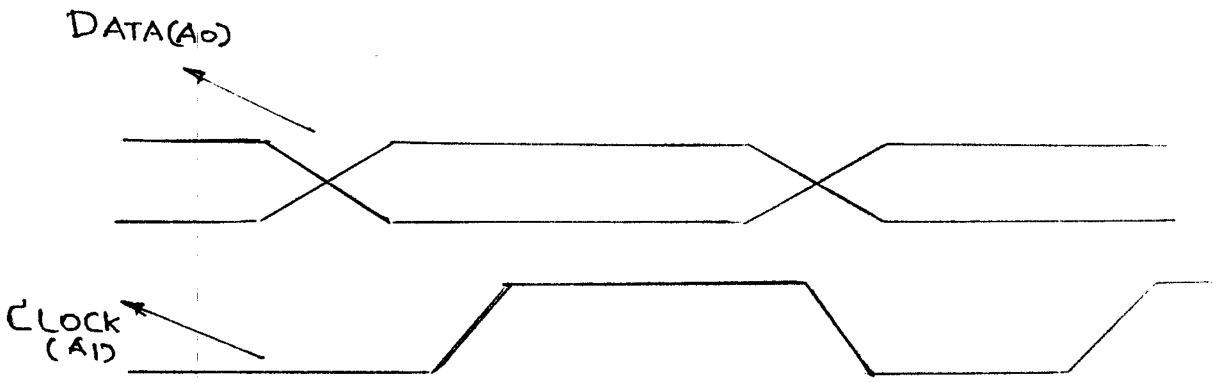


FIGURE 4.


GND.
STROBE
CLOCK
DATA
4050
4094
4094
4094
4094
4094
4094
VCC
+5V
GND.
STROBE
CLOCK
DATA
VCC
HEAD NUMBER - 1
No - 2

SERIAL REGISTER TIMING DIAGRAM.



FIGURE·4

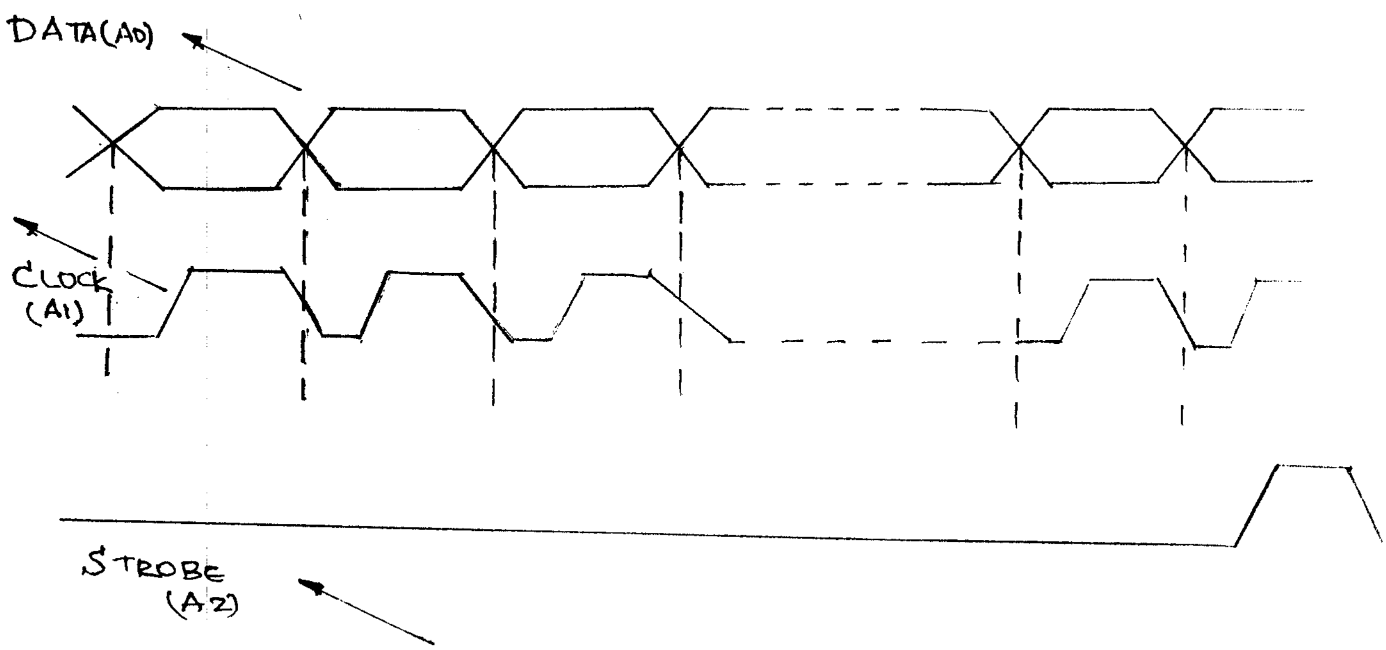


FIGURE.5

be transferred serially. As the updating of the display is done after each interrupt from the proximity switch (ie. for every revolution) and as the spindle rotates at low speed such as 1000-1200 rpm the microprocessor has enough time to transfer the count in the memory serially.

Data output from the IC 4094 (LSB) of first head is connected to the data input of first IC 4094(MSB) and so on. So, by using **ONLY 3 LINES**, MPU can update the display The 3 lines are 1.Data lines 2. Clock lines 3. Strobe lines. Clock line is connected to clock inputs of all IC 4094 and strobe line is connected to the strobe of all IC 4094. The data lines A0,A1, and A2 of port A of 8255-I are utilized for these three lines. The MPU first places the serial data in the data line (A0) and without affecting it, the clock is transferred through the clock line (A1)

After all transfer of data bits for all digits of all heads, the strobe is transferred through strobe line(A2) and the bytes in the serial register is latched and display is updated. The timing diagram is shown in figure 4a and 4b. The procedure is shown in flow chart 2.

TIMER UNIT

Timer unit is used to give a pulse in each second . The pulse in each second is used to interrupt the MPU. On interrupt, MPU will enter into the time increment subroutine. Timer unit is designed by using an IC 555. The circuit diagram shown in figure 5.

An astable multivibrator is designed for a pulse width of 1ms and the time width of 1sec. If the circuit is connected as shown in figure 5 (pin 2 and pin 6 connected) it will trigger itself and free run as a multivibrator. The external capacitor changes through (Ra+Rb) and discharges through Rb. Thus the duty cycle may be precisely set by the ratio of these two resistors. In this mode of operation the capacitor charges and discharges between 1/3 Vcc and 2/3 Vcc. As in the triggered mode, the charge and discharge time and therefore the frequency are independent of the supply voltage. The charge time(output high)t1 is given by

$t2 = 1$ ms $T = 1$ sec

$t1 = 0.693(Ra + Rb)\ C$ Assuming $C = 1$micro farad

$t2 = 0.693\ (Rb)\ C$

$Rb = 1$ kilo ohm

$Ra = 2$ Mega ohm

ASTABLE Multivibrator.

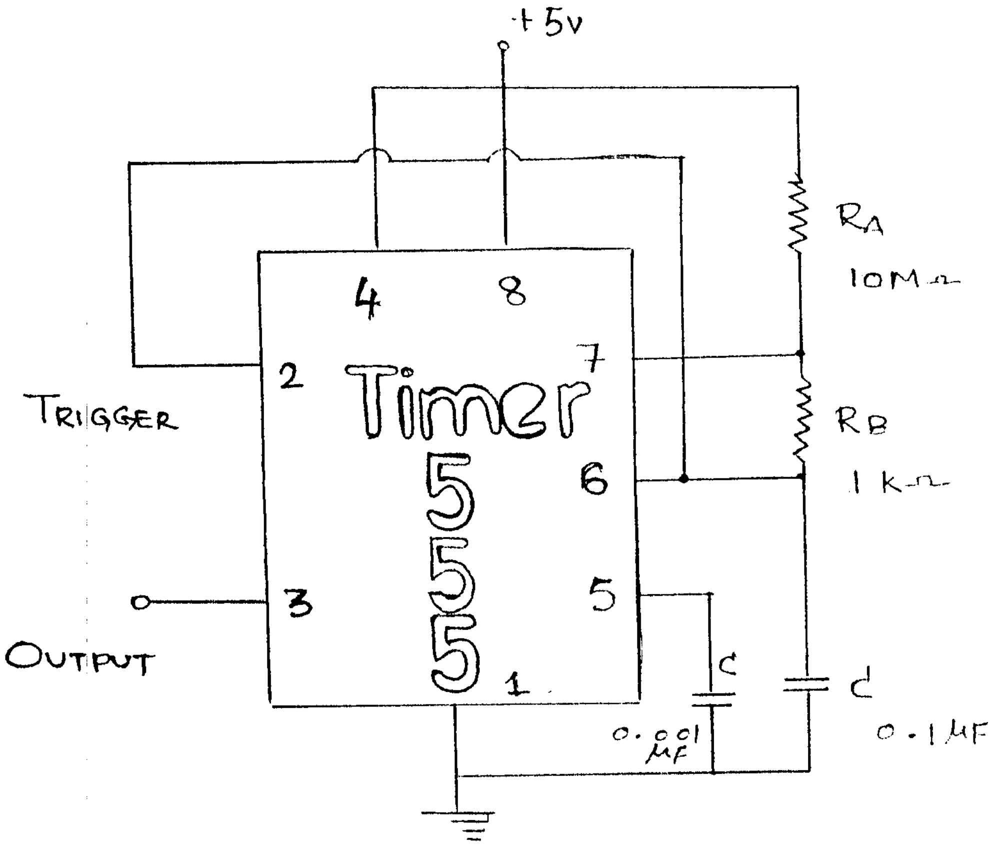


FIGURE. 5

INTERFACE UNIT

In our WIPAC system the interfacing is done using two 8255's. One 8255 -I is utilised for updating the display, reading photodetectors, and activating cutters. For these three operations port A , port B and port C of the 8255 is utilised respectively.

a. Port A output lines ie. Data line, Clock line and Strobe line are connected to a buffer(4050) as these lines namely clock line and strobe line have to be connected to many IC's. This interface is shown in figure 6.

b. Port B is used to receive the photodetector output and it is used in input mode. Phototransistor collector output is connected to port B as shown in figure 7.

c. Port C is used to activate the cutter if the required length is reached. As cutter requires high current in the order of 500mA and voltage of 12v, the port C outputs cannot drive the solenoids used in the cutter. Port C output is connected to open collector transistor which is designed to satisfy the requirement of the cutter

INTERFACE UNIT

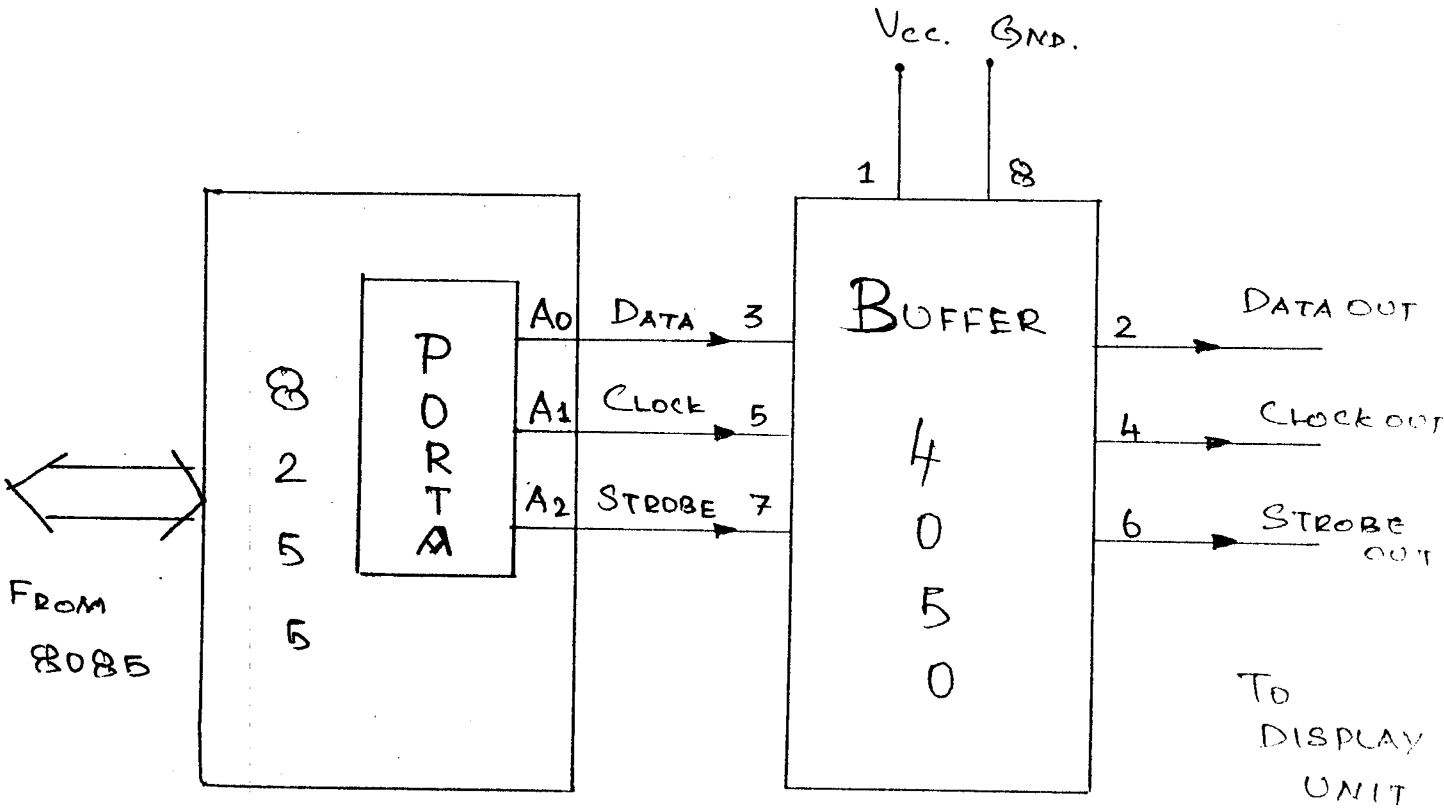


FIGURE. 6

INTERFACE TO PHOTODETECTOR.

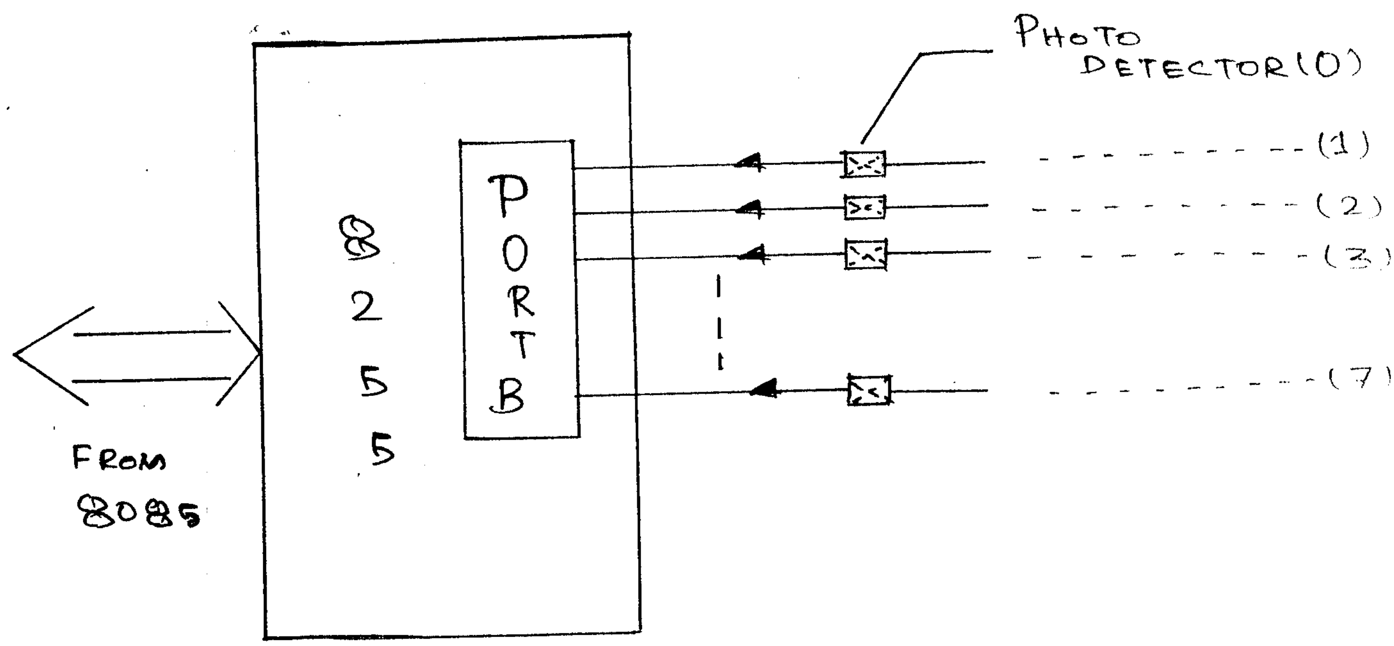


FIG. 7(a)

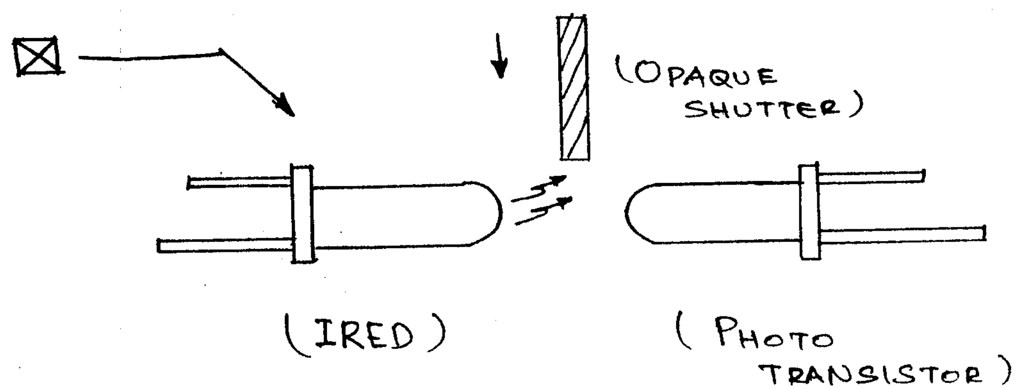


FIG. 7.(b)

The output from the port C of 8255 I is connected to the trigger input of the monostable multivibrator using IC 555 timer shown in figure 8b. The output from the mono stable multivibrator is connected to the solenoid which activates the cutter to cut the yarn shown in figure 8a. Monostable multivibrator is nothing but the shot timer. The external capacitor is initially held discharged buy a transistor inside the timer. Upon application of a negative trigger pulse of less than 1/3Vcc to pin 2, the flipflop is set which is both releases the short circuit across the capacitor and drives the output high. The voltage across the capacitor then increases exponentially for a period of t = 1.1 Ra C at the end of this time the voltage equals 2/3Vcc. The comparator then resets the flipflop which is inturn discharges the capacitor and drives the output to its lowstate. During the timing cycle when the output is high, the further application of a trigger pulse will not effect the circuit. However the circuit can be reset during this time by the apllication of a negative pulse to the reset terminal. The output will then remains in the low state until a trigger pulse is again applied.

YARN CUTTER CIRCUIT.

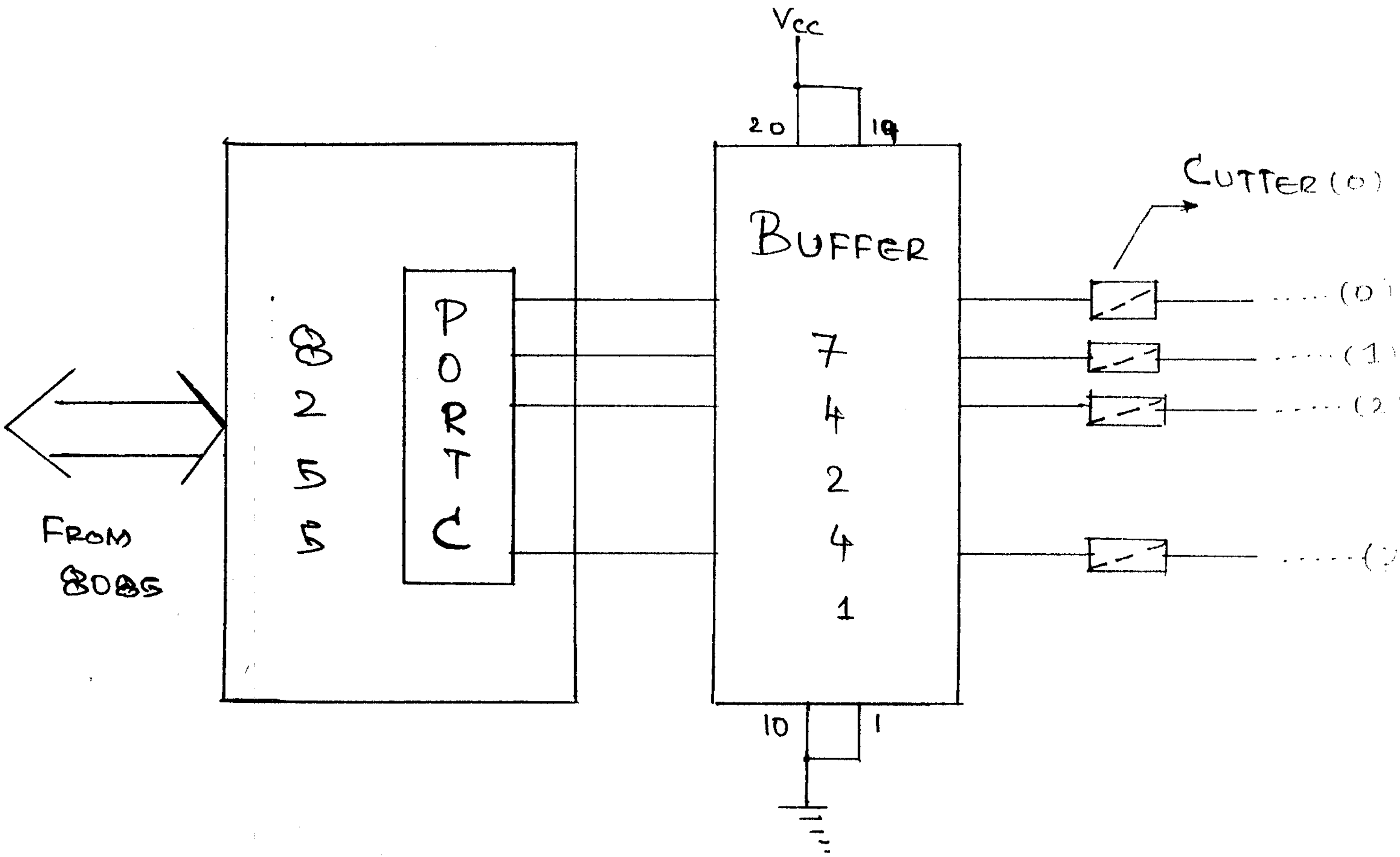
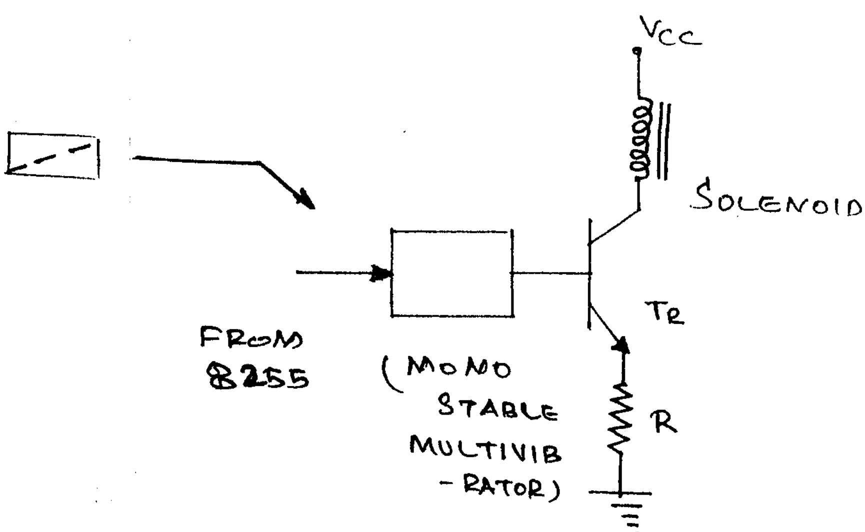


FIGURE. 8(a)



MONOSTABLE MULTI.

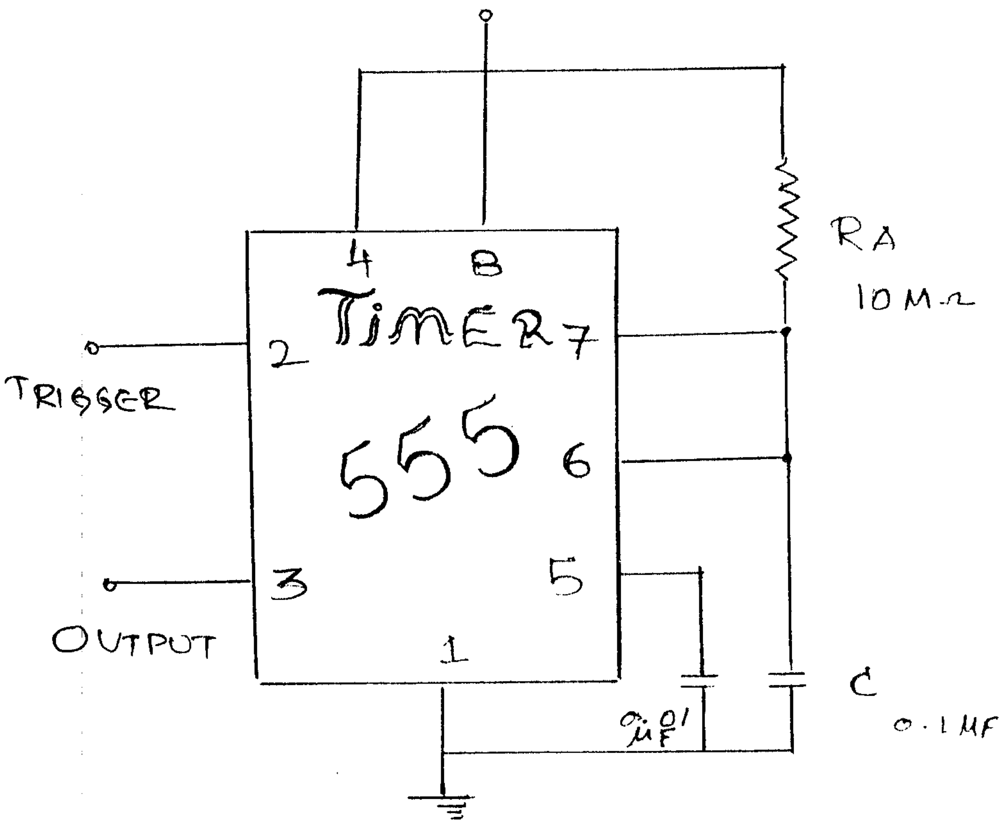


FIGURE. 8b

MECHANICAL ERROR INDICATOR CIRCUIT

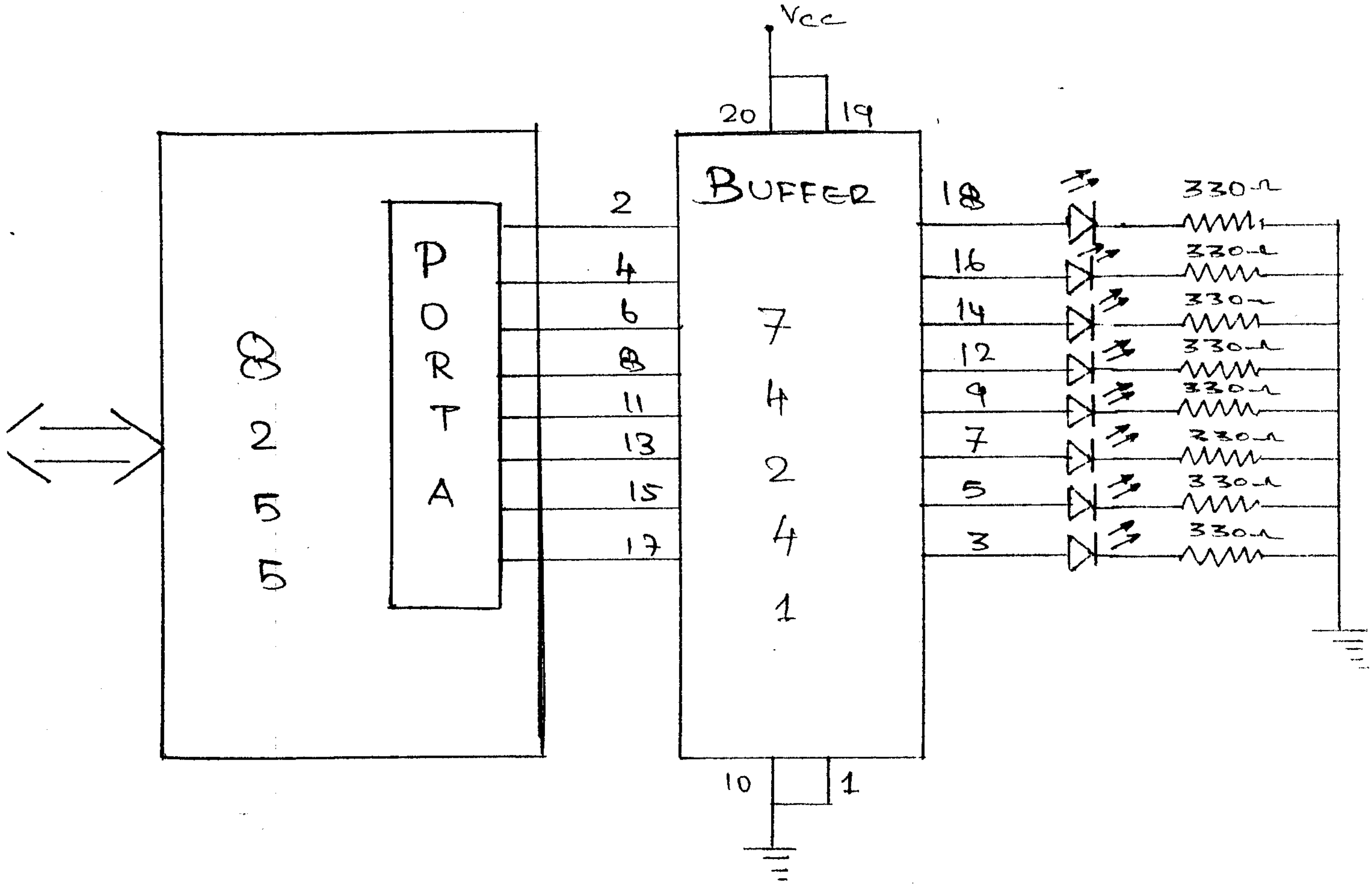


FIGURE 9

Inorder to avoid false triggering (when reset function is not use) reset function must be connected to Vcc.

Time for 1sec

t =1.1. Ra C

Assume Ra=10 Mega ohm

C=0.1 micro farad.

The second 8255 is used to send the indication about the mechanically erroneous heads and selection. Port A of this 8255 is connected to LED's to indicate the mechanically erroneous heads. For this the buffered output of the port A is connected to the LED's . This is shown in figure 9.

MICROPROCESSOR UNIT

Microprocessor unit which is the heart of the WIPAC system has the following operation

a. Intialisation

b. Data entry

c. Counting the length and sending signal to cutter.

d. Displaying the count.

e. Counting the time of shift.

f. Efficiency

g. Locating the mechanically erroneous head.

MPU has five interrupt inputs. One is called INTR which is identical with the INT input in 8080 A. The other four are automatically vectored to specific location without any external hardware.

INTERRUPTS	Call location
1. RST 7.5	FE12H
2. RST 6.5	FE0CH
3. RST 5.5	FE06H

All the details of the call locations are present in the precitron kit. The 'TRAP' has highest priority followed by RST 7.5, 6.5,5.5 and INTR in that order. Except 7.5 others are level trigger.

RST 7.5 ,6.5 AND 5.5

These maskable interrupts are enabled under program control with two instruction EI and SIM . The SIM operation can be done as shown in figure 10. In our project we are using interrupts 5.5,6.5.

When the shift is started, the operator should press a key in the keyboard to intialise the count of all heads. When he wants to enter or alter the required length count he should press another key in the keyboard and now MPU will be waiting for the operator to enter the count and the entered data is stored in memory. To know efficiency of the shift there is an another key named efficiency which has to be pressed and when pressed ,MPU will calculate the efficiency and display in the monitor. For reading the keyboard , the subroutine RDKBD which is available in precitron kit. This is explained in the flow chart 3.

SIM OPERATION.

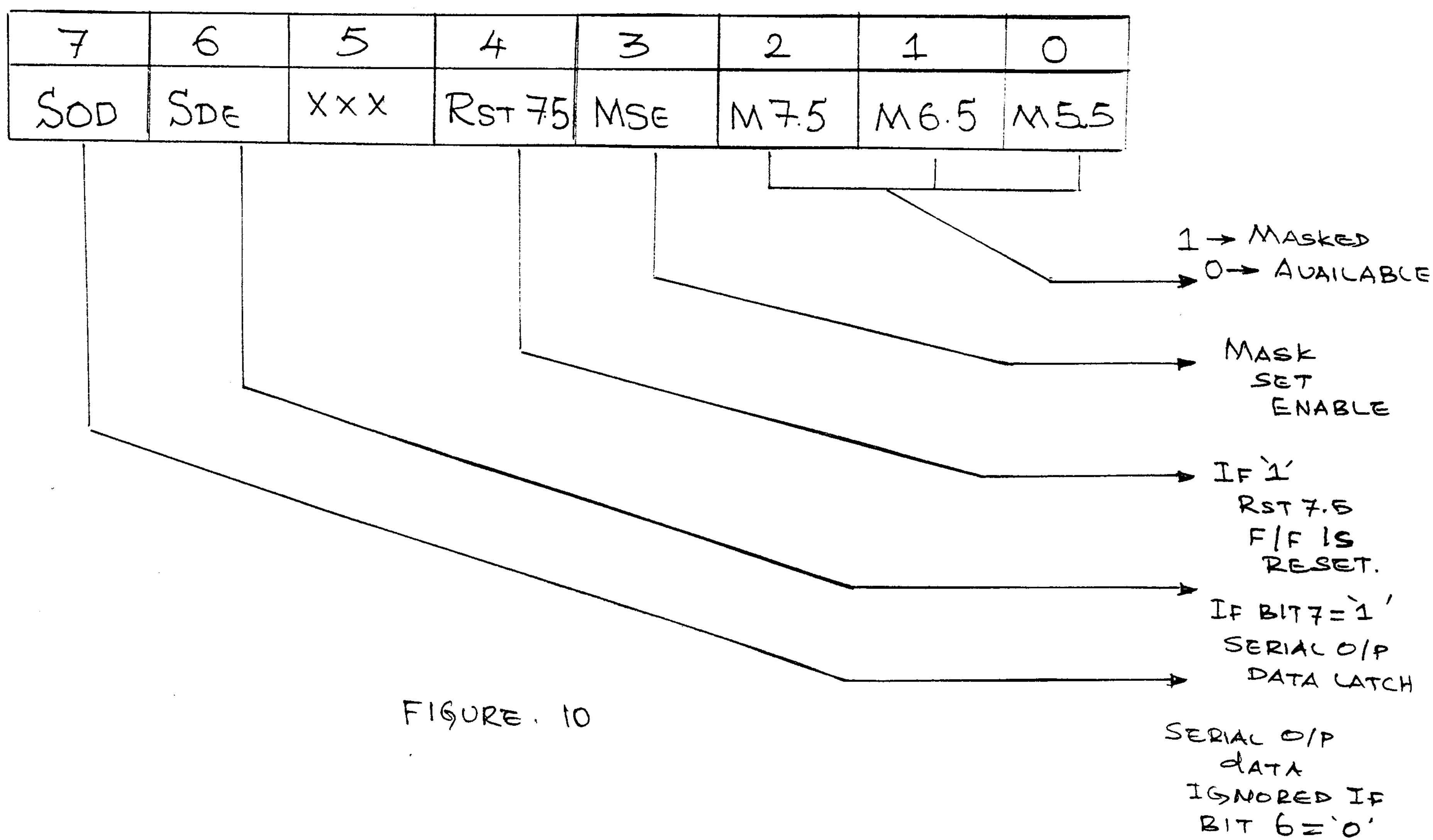


FIGURE. 10

INITIALISATION

When the shift starts or if the operator wants to initialise the count of all heads at any time he should press the key named INITIALISATION and when this key is sensed by the MPU, it enters into the initialisation sub-routine. Now the MPU memory address is set to the starting address of the length count stored in the memory and starts to make the count to zero one by one incrementing the memory address. Like wise the count of all heads are made zero. After this, both the time counts are made zero. The display subroutine is called to display . This explained in the flowchart 4.

b. DATA ENTRY

The subroutine is used store the new entered count or altered count in the memory. For this a key in the keyboard named DATA ENTRY is used. When this key is pressed the MPU will show the count which is previously present in the memory. So if the operator wants to enter new count or alter he has to enter the count using the keys numbered 0 to 9 . When he is entering the numbers altered are displayed for visual feedback. After entering it, the count will be displayed for a time and blanked. In the middle of the entry of count if the operator wants to end the count entry he has to again press the same DATA ENTRY key. This operation is shown in the flow chart 5.

COUNTING THE LENGTH AND SENDING SIGNAL TO CUTTER

On each rotation of the spindle, the proximity switch will interrupt the MPU. On interrupt, the MPU first checks the photodetector output to check the presence of yarn. If the yarn is present, the length count is incremented one's else MPU go to the next head. After incrementing, the MPU checks whether the count has reached the required length count and if so sends the signal to the cutter else it goes to the next head. And this same procedure is carried out for the remaining heads.

After the incrementing and checking procedure is over, the display updating subroutine is called to show the count. After sending the signal to the cutter the count is reset by making the count to zero. In incrementing the length count the following procedure is followed. The length wound on cone on each rotation of the spindle is only 0.235 metre. And so, there are two countsA and B are used. After 424 rotation (count A) the length wound is 100 metre. So when count A reaches 424 it is cleared and count B is incremented once. Only count B is displayed on the display. This is shown in flow chart 6.

d. DISPLAYING THE COUNT

The count of each head is displayed using a 4 digit display. For this as illustrated in the previous chapter, shiftregister with storage IC4050 is used. The data out of one head display is connected to Data in of the next head. For this MPU sends the data and clock and strobe serially one by one. This is explained in the flow chart 7.

When the interrupt from the proximity switch (for each rotation) occurs after incrementing the length count the DISPLAY subroutine is called. After initialisation also the DISPLAY subroutine is called. In the DISPLAY subroutine, the head number is intialised as 1 and the address of the starting address is obtained. Then the first digit is retrieved and then the seven segment detail which is stored in the memory is retrieved and it is transferred bit by bit. After the valid data is set in the data line the clock line is raised from low to high and as IC 4094 is **POSITIVE EDGE** triggered the data is serially transferred. Then the next bit of seven segment detail is transferred following the clock bit.

Then the next digit data also transferred in the same manner until all count digits of a head are transferred. This procedure is repeated for all heads. After all heads count data is transferred to the serial register the strobe signal is given. Before the strobe signal is sent, the seven segment details are present in all shift register and when strobe becomes high the data in all registers are transferred to the latch. As the latch output are connected to the seven segment display the new count is displayed.

e. COUNTING THE SHIFT OF SHIFT

To find the efficiency of the shift two time

g. LOCATING THE MECHANICALLY ERRONEOUS HEAD

As this locating of the mechanical error subroutine is called in each second, after incrementing the time counts. In this subroutine a one hour counter is used. This is incremented in each second. After this MPU checks each head whether the yarn is present previously and now it is cut. If so, the count of that particular head is incremented. Then this count is checked for 5. If it has reached 5 within one hour the mechanical error indicator is glown for indication. These procedure is repeated for all heads. When one hour is completed these counts are cleared for fresh incrementation. This procedure is illustrated in flow chart 10.

ASSEMBLY OF PHOTODETECTOR AND CUTTER

The photodetector is explained in the sensor unit. The sensor unit has a LED, Photodetector, these are kept facing each other which are placed perpendicular to the travel of yarn. The cutter which is operated by a solenoid has a knife edge which is moved perpendicular to the yarn, so that yarn is cut when solenoid is activated. This is shown in figure 10. The cutter and photodetectors are kept in a U shaped yarn guide as shown in figure 11.

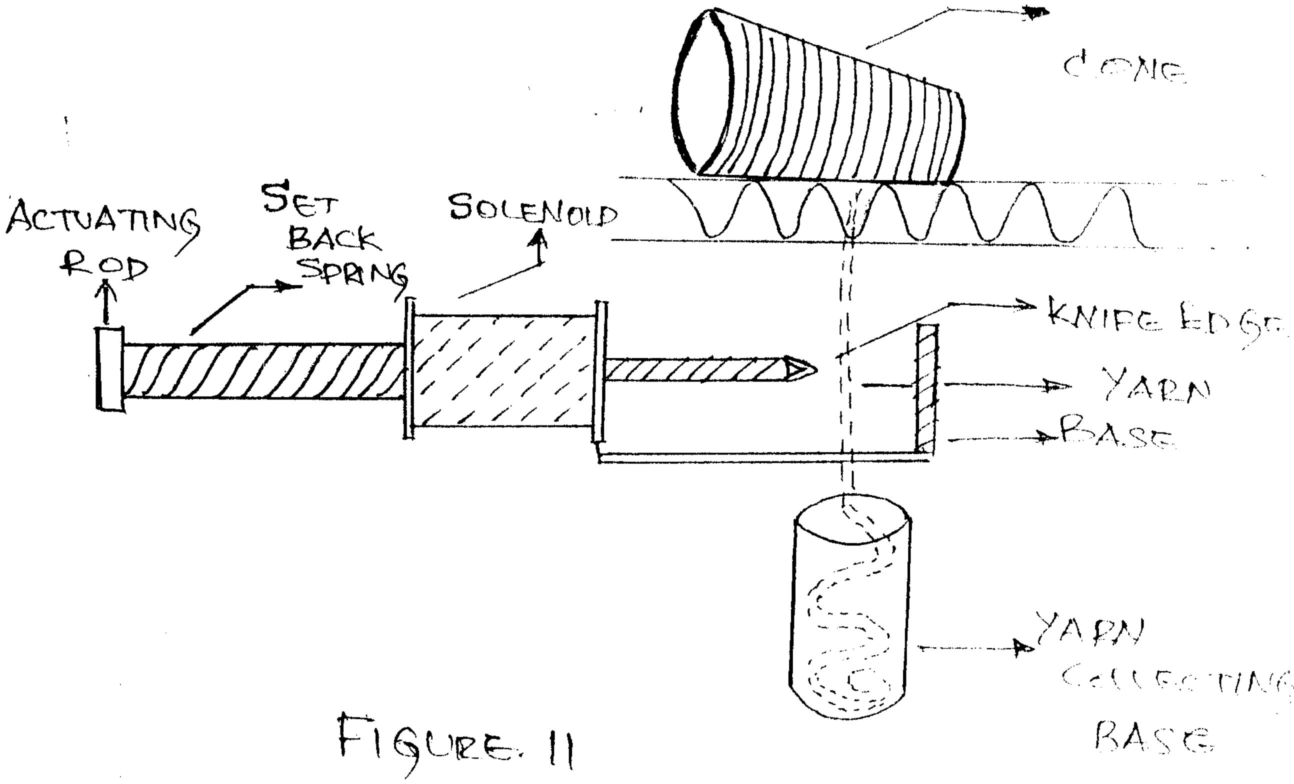


FIGURE. 11

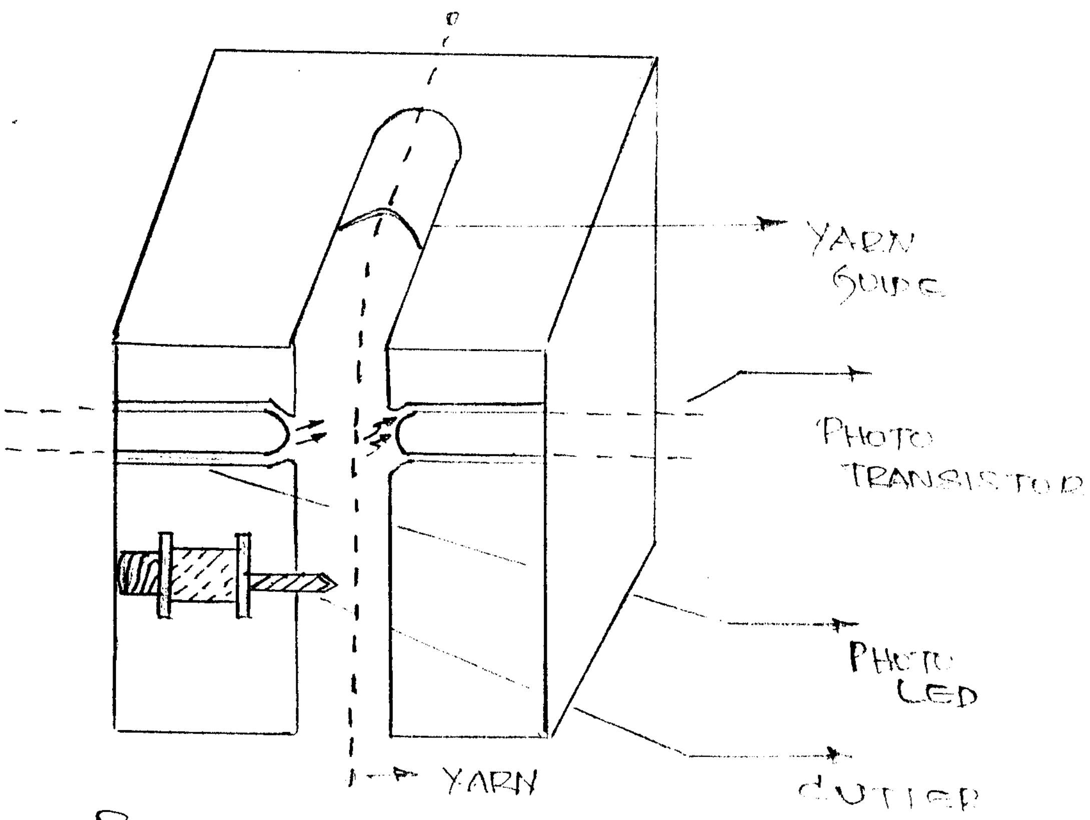


FIGURE. 12

COMPONENTS USED

a. SENSING UNIT

1. Photo LED 55BGE 522
2. Photo transistor GE 114G
3. Resistors 330 ohm,4.7kohm
4. Proximity switch

b. MICROPROCESSOR UNIT

1. INTEL 8085

c. INTERFACING UNIT

1. IC 8255
2. Buffer 74241

d. SHIFT REGISTER AND DISPLAY UNIT

1. IC 4050 Buffer
2. IC 4094 Serial shift register with storage

e. DISPLAY UNIT

1. Common anode 7 segment display FND507

f. CUTTER UNIT

1. Solenoid with knife
2. IC 555 timer

g. TIMER UNIT

1. IC 555 timer

CONCLUSION

By use of our project, manpower requirement is reduced, by which production is increased. Efficiency is calculated and displayed using our project and the operator can thus know how effectively the machine is utilized in that shift. If there is any mechanically erroneous head in that machine, the WIPAC can identify and indicate it, and the operator can repair it. Circuitry is simple and the cost of manufacturing is less.

FUTURE DEVELOPMENT

Using the concept of multiplexing the project can be extended to number of heads.

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07 LINEAR DATA BOOK

08 INFRA RED OPTO ELECTRONICS DEVICES AND APLLICATIONS

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J.SCOTT BECHTER

09 OPTO ELECTRONICS

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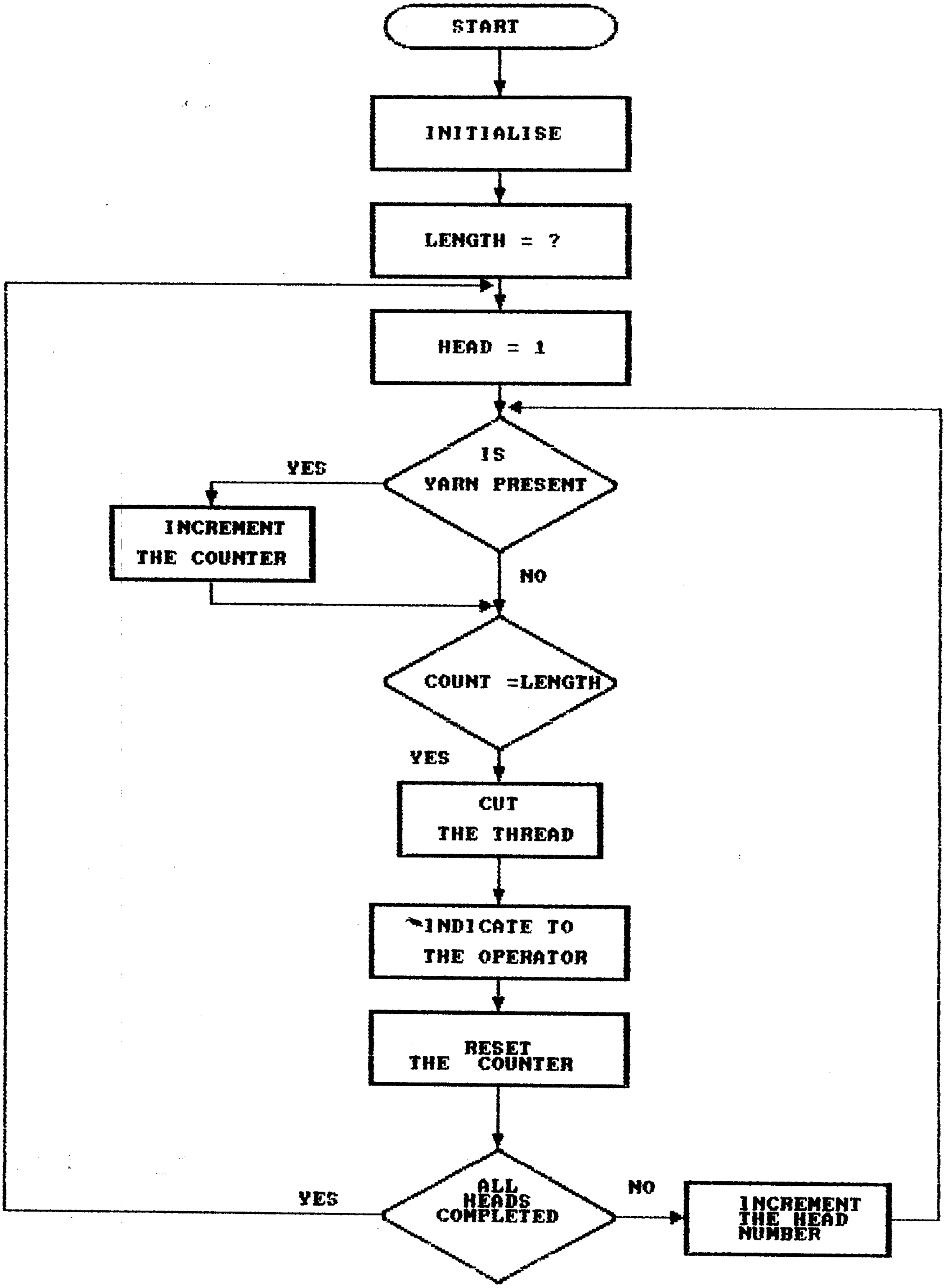
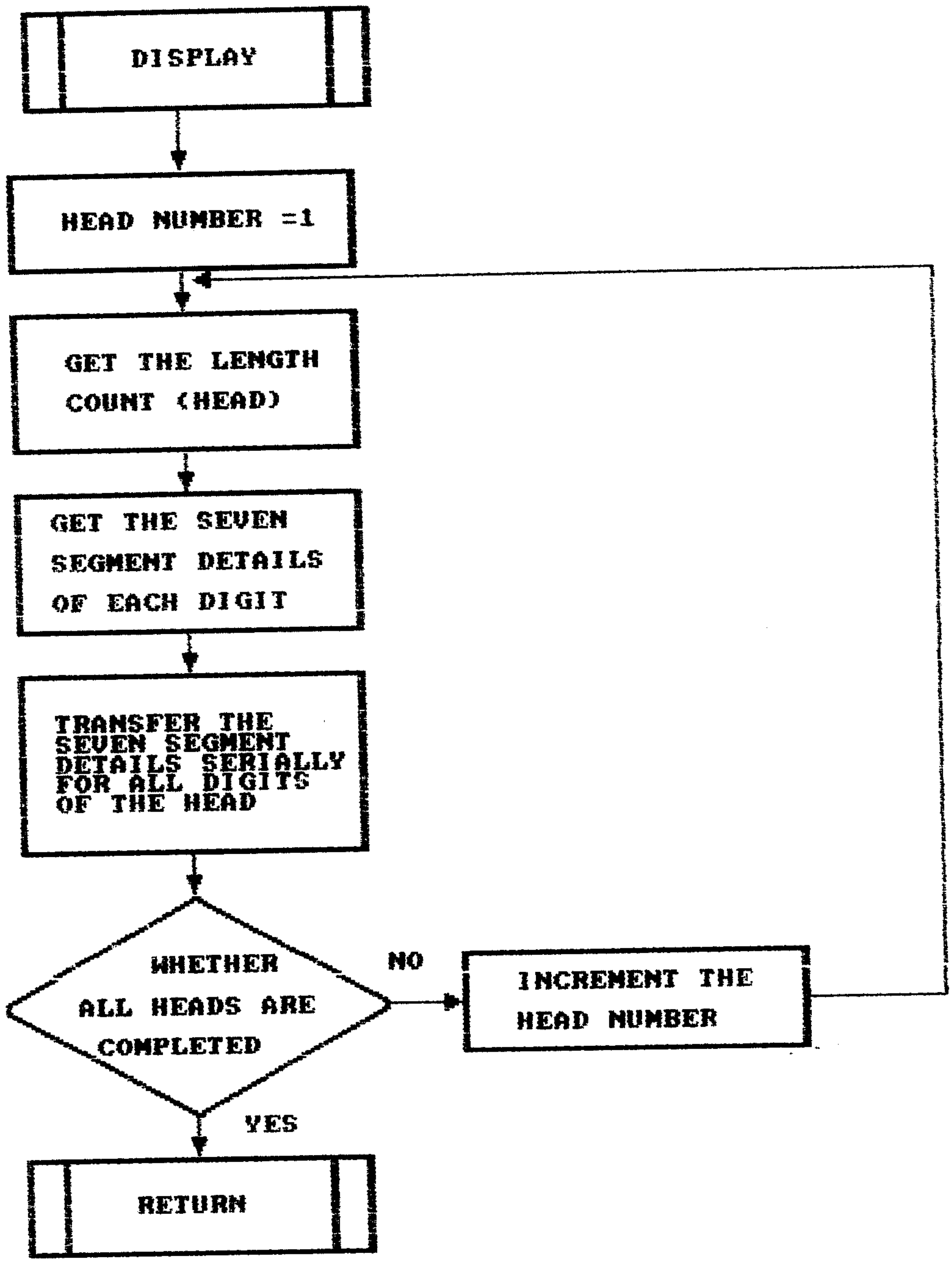
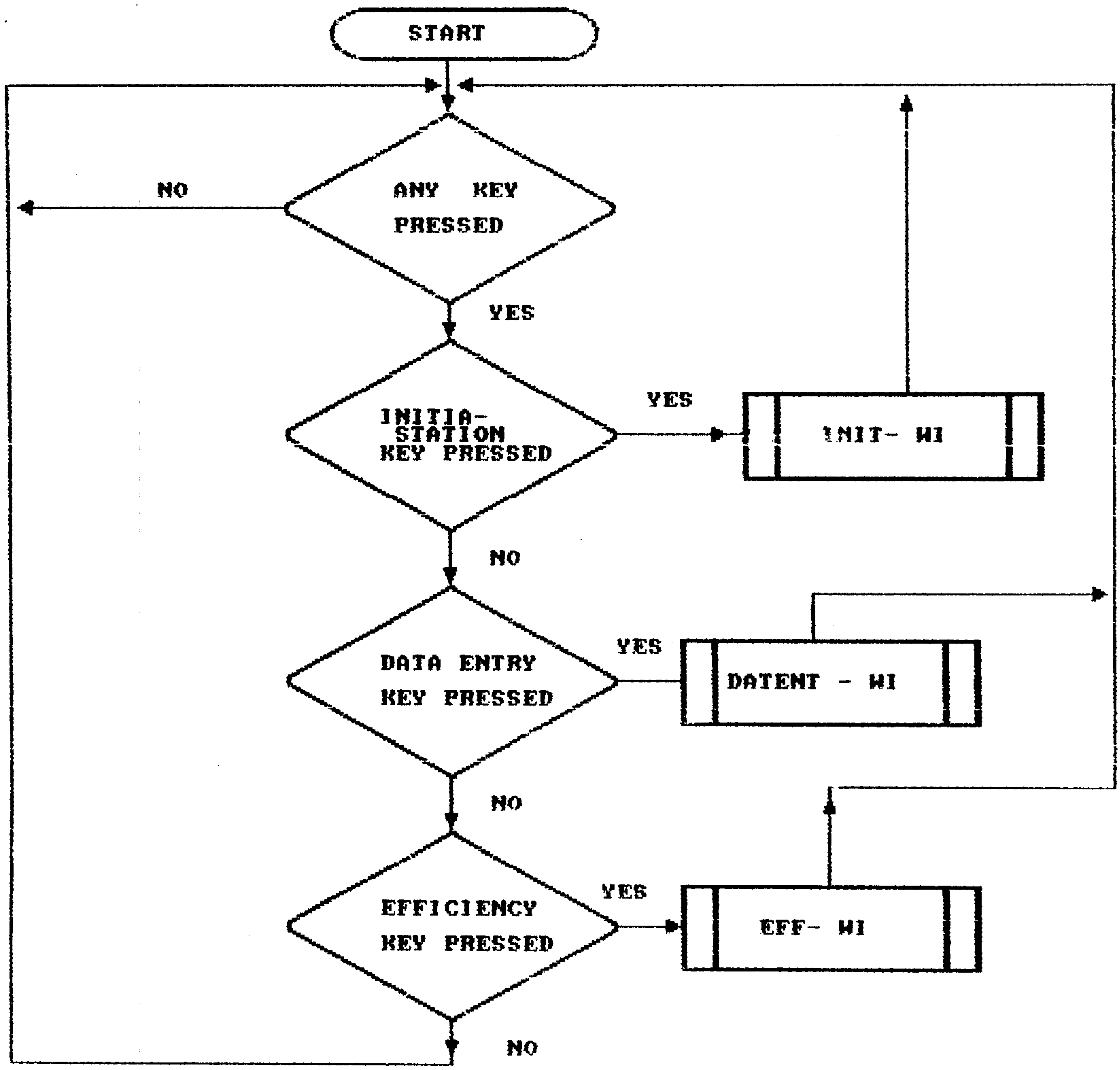

START
INITIALISE
LENGTH = ?
HEAD = 1
IS YARN PRESENT
YES
INCREMENT THE COUNTER
NO
COUNT =LENGTH
YES
CUT THE THREAD
INDICATE TO THE OPERATOR
RESET THE COUNTER
ALL HEADS COMPLETED
YES
NO
INCREMENT THE HEAD NUMBER

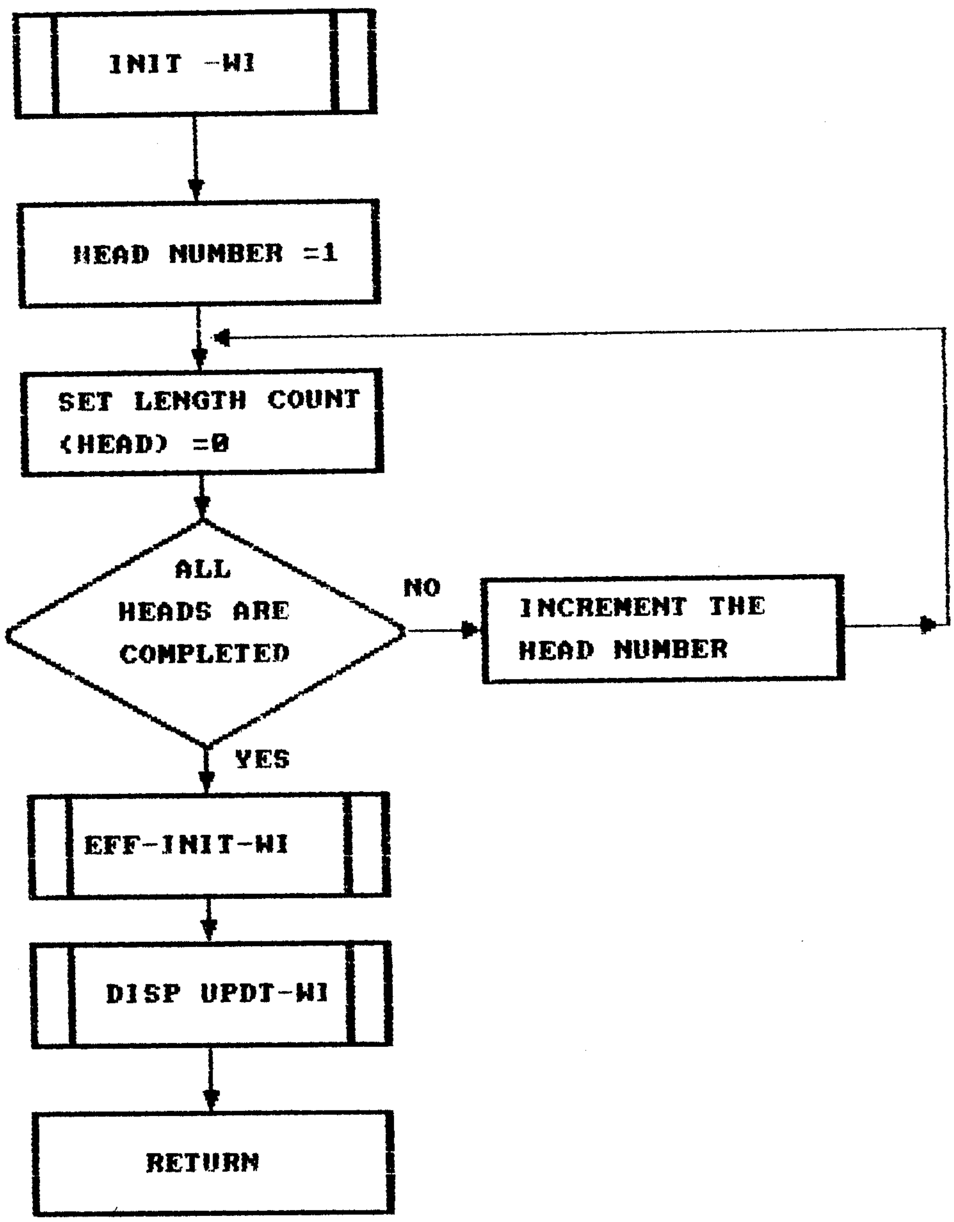
FLOW CHART 1.


DISPLAY
HEAD NUMBER =1
GET THE LENGTH COUNT (HEAD)
GET THE SEVEN SEGMENT DETAILS OF EACH DIGIT
TRANSFER THE SEVEN SEGMENT DETAILS SERIALLY FOR ALL DIGITS OF THE HEAD
WHETHER ALL HEADS ARE COMPLETED
NO
INCREMENT THE HEAD NUMBER
YES
RETURN

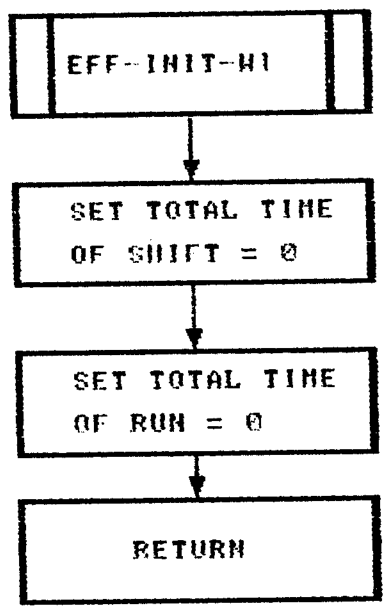
FLOW CHART (2)

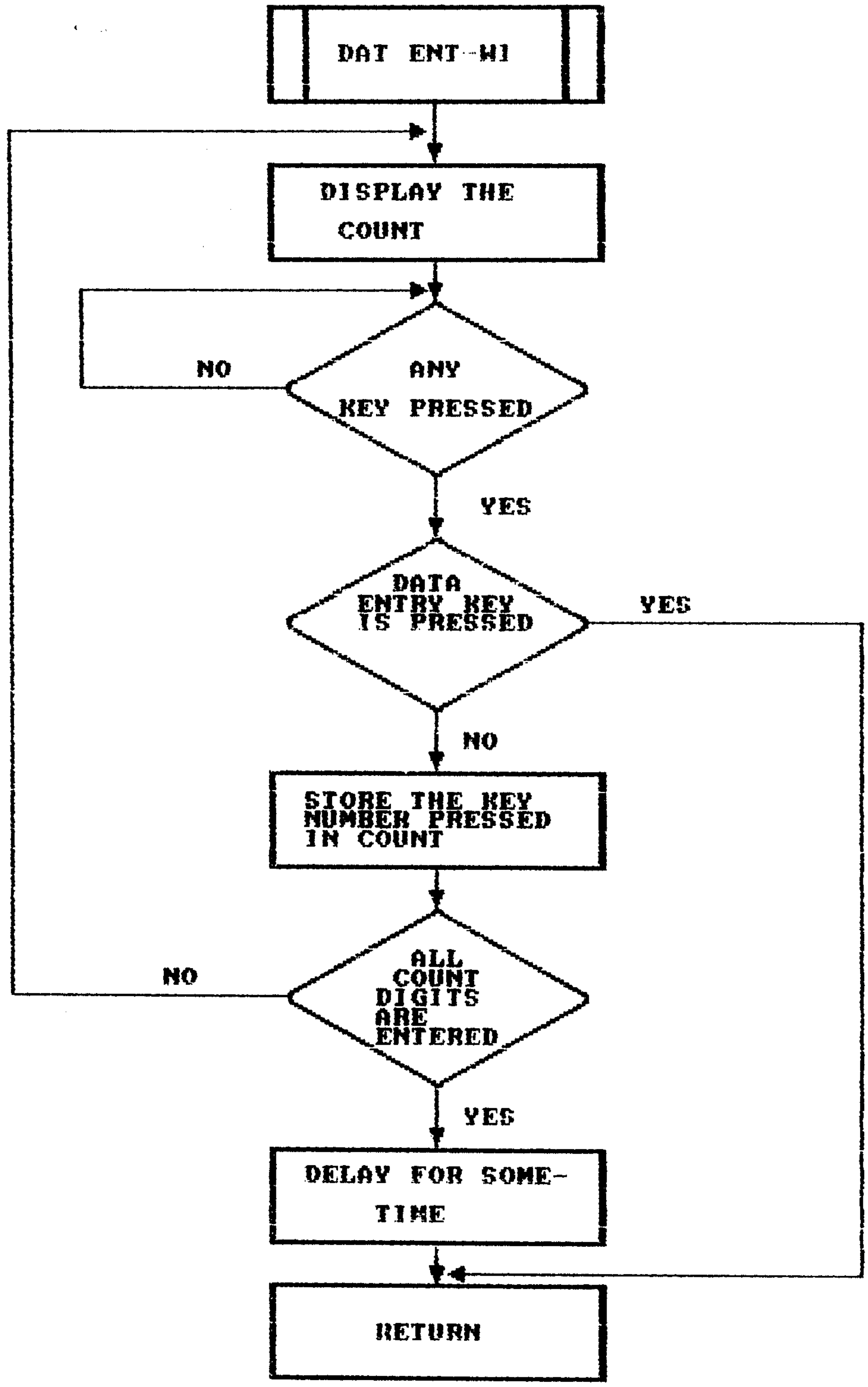

START
NO
ANY KEY PRESSED
YES
INITIA-STATION KEY PRESSED
YES
INIT- WI
NO
DATA ENTRY KEY PRESSED
YES
DATENT - WI
NO
EFFICIENCY KEY PRESSED
YES
EFF- WI
NO

FLOW CHART (3)

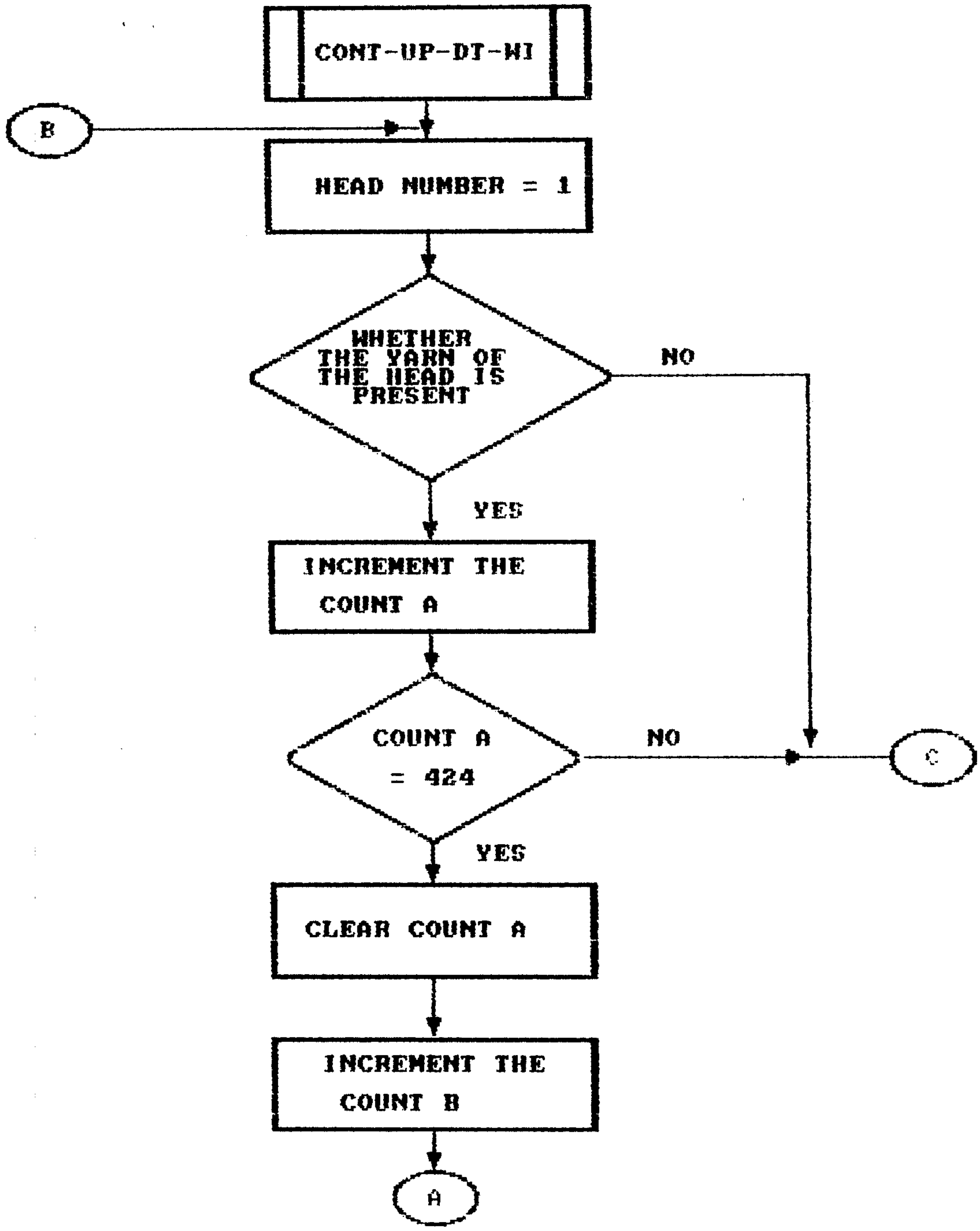

INIT -WI
HEAD NUMBER =1
SET LENGTH COUNT
(HEAD) =0
ALL
HEADS ARE
COMPLETED
NO
INCREMENT THE
HEAD NUMBER
YES
EFF-INIT-WI
DISP UPDT-WI
RETURN

FLOW CHART. 4.


EFF-INIT-H1
SET TOTAL TIME
OF SHIFT = 0
SET TOTAL TIME
OF RUN = 0
RETURN

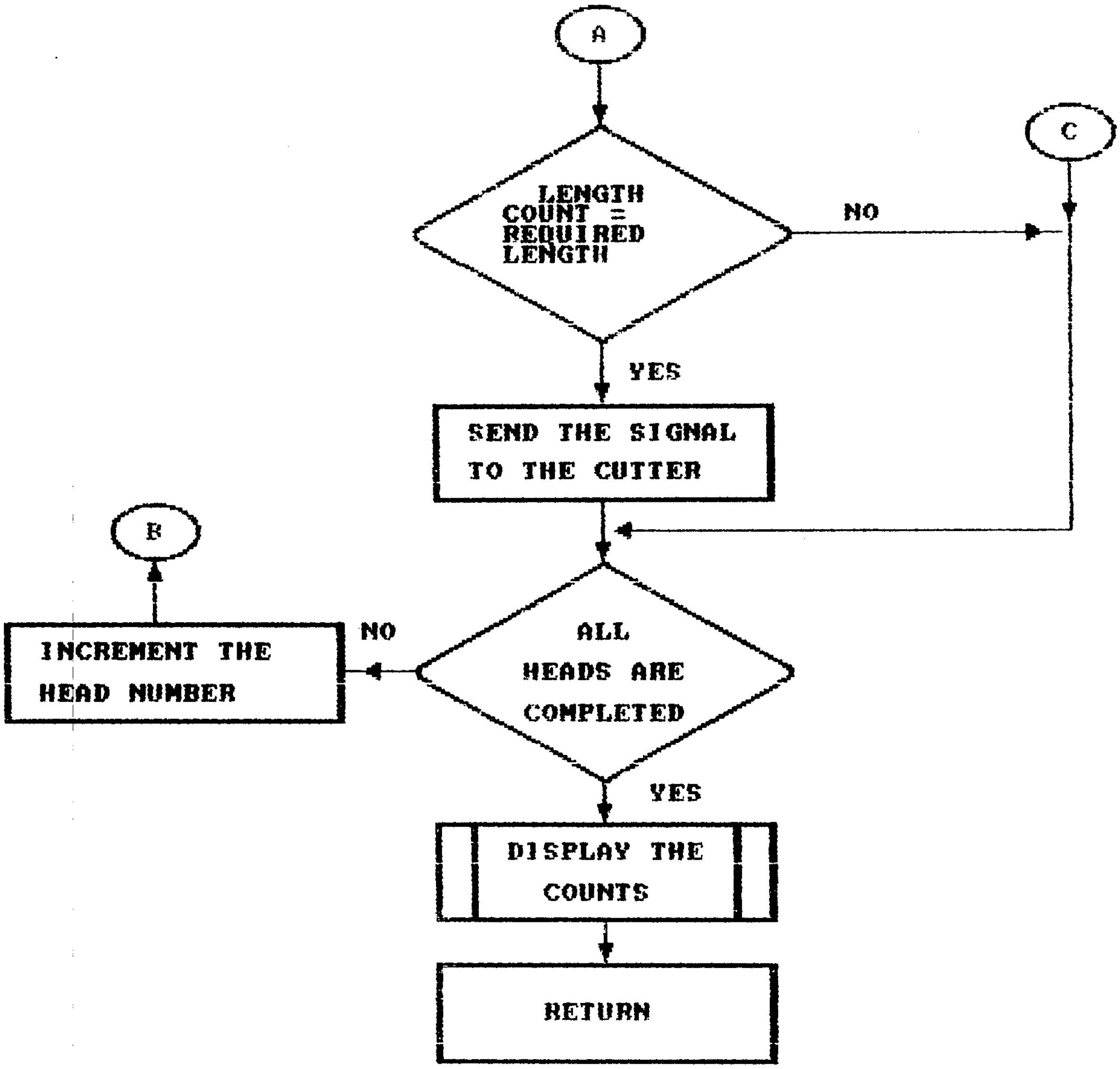

DAT ENT-W1
DISPLAY THE COUNT
ANY KEY PRESSED
NO
YES
DATA ENTRY KEY IS PRESSED
YES
NO
STORE THE KEY NUMBER PRESSED IN COUNT
ALL COUNT DIGITS ARE ENTERED
NO
YES
DELAY FOR SOME-TIME
RETURN

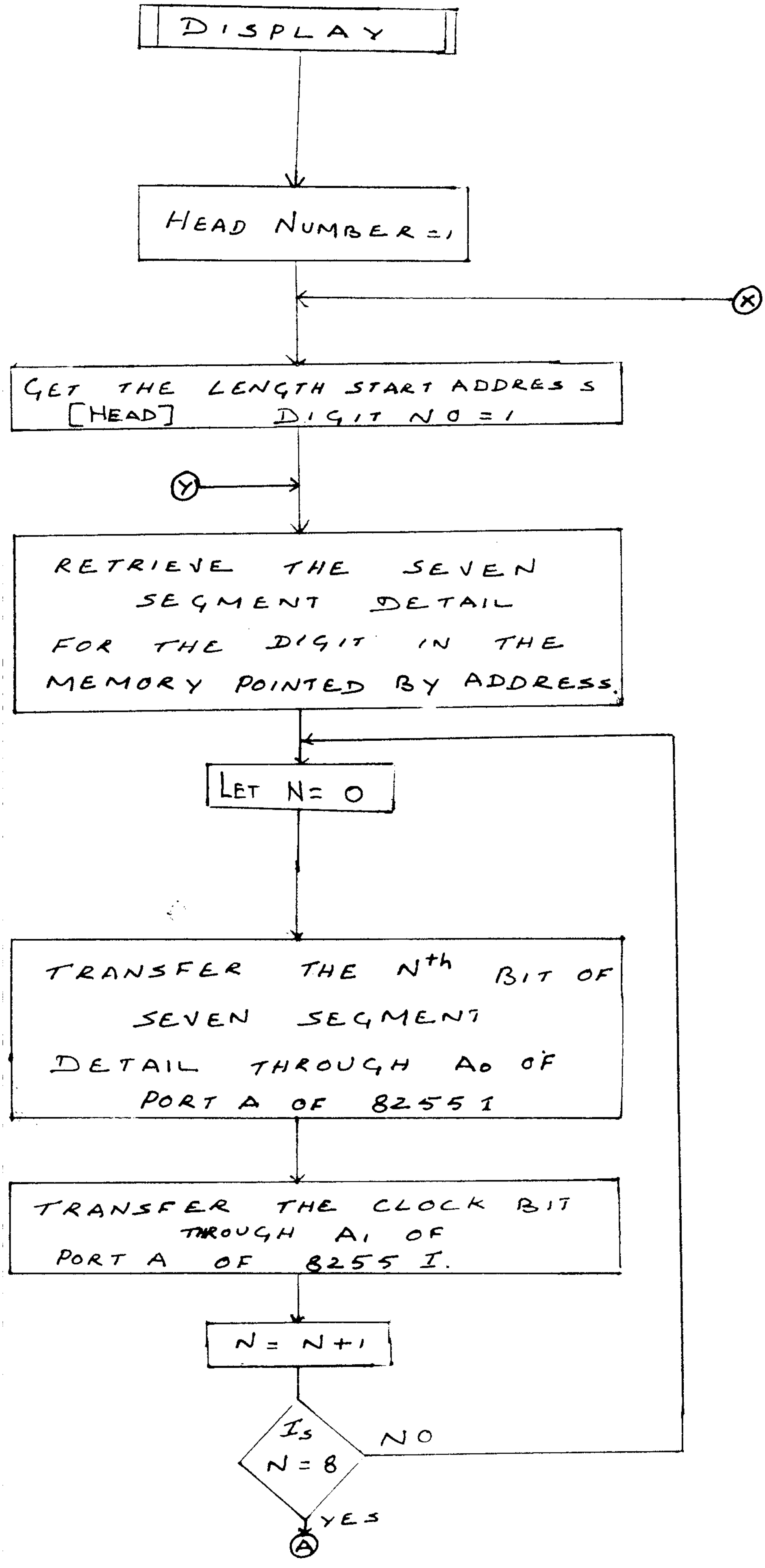
FLOW CHART. 5

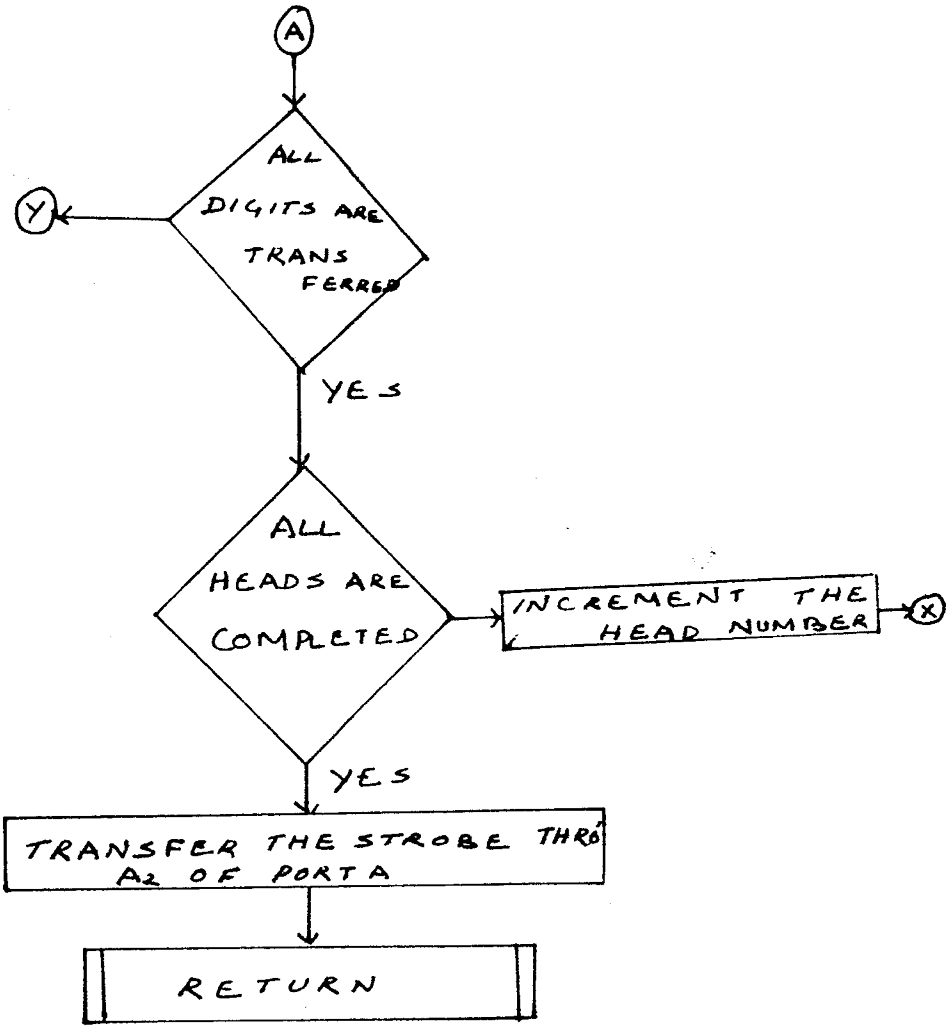


CONT-UP-DT-WI
B
HEAD NUMBER = 1
WHETHER THE YARN OF THE HEAD IS PRESENT
NO
YES
INCREMENT THE COUNT A
COUNT A = 424
NO
C
YES
CLEAR COUNT A
INCREMENT THE COUNT B
A

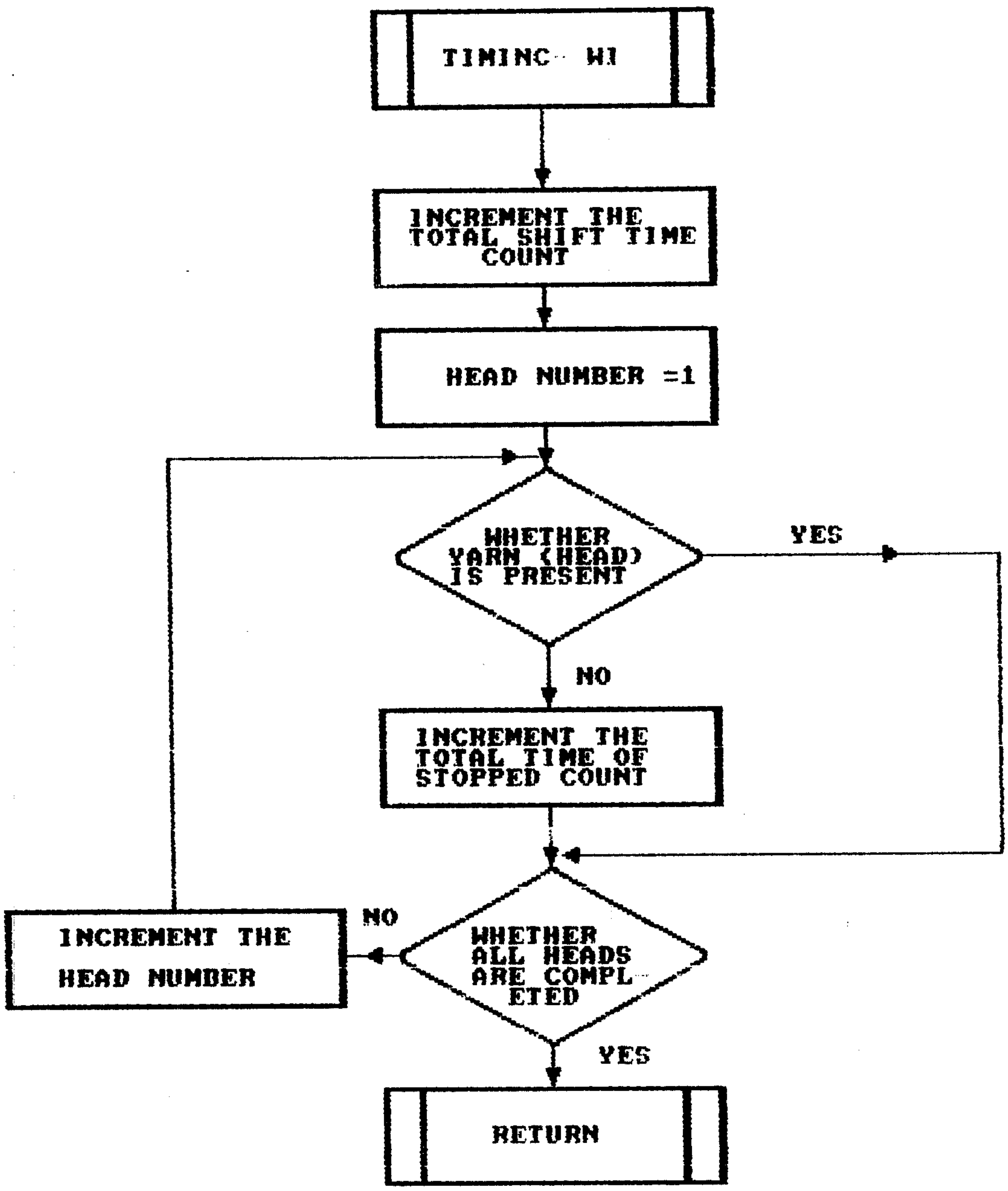
FLOW CHART. 6


A
C
LENGTH COUNT = REQUIRED LENGTH
NO
YES
SEND THE SIGNAL TO THE CUTTER
B
INCREMENT THE HEAD NUMBER
NO
ALL HEADS ARE COMPLETED
YES
DISPLAY THE COUNTS
RETURN

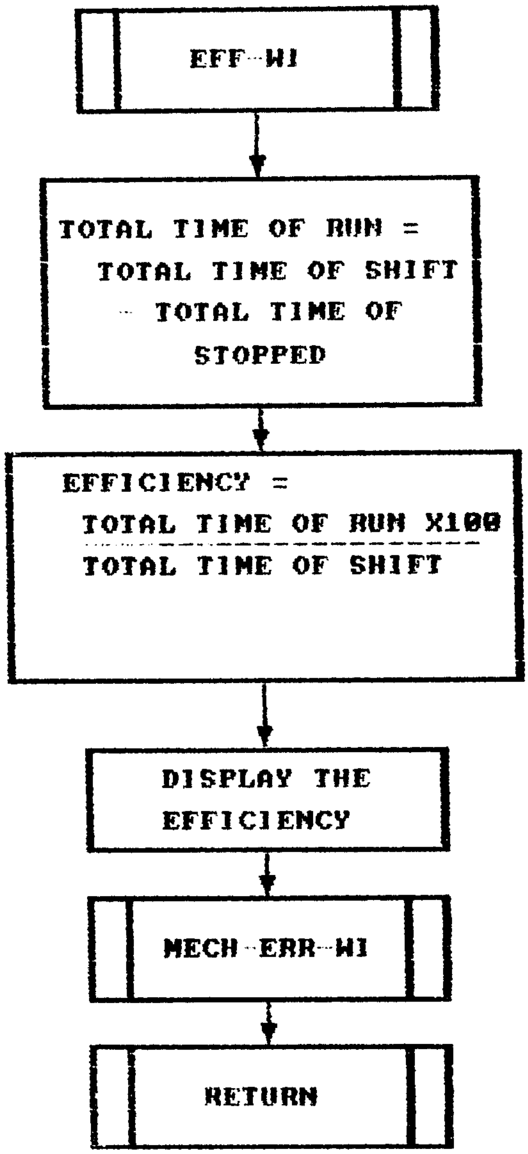

DISPLAY
HEAD NUMBER =1
GET THE LENGTH START ADDRESS [HEAD] DIGIT NO =1
X
Y
RETRIEVE THE SEVEN SEGMENT DETAIL FOR THE DIGIT IN THE MEMORY POINTED BY ADDRESS.
LET N= O
TRANSFER THE Nth BIT OF SEVEN SEGMENT DETAIL THROUGH A0 OF PORT A OF 8255 I
TRANSFER THE CLOCK BIT THROUGH A1 OF PORT A OF 8255 I.
N = N+1
Is N = 8
NO
YES
A


A
ALL DIGITS ARE TRANSFERRED
Y
YES
ALL HEADS ARE COMPLETED
INCREMENT THE HEAD NUMBER
X
YES
TRANSFER THE STROBE THRO' A2 OF PORT A
RETURN

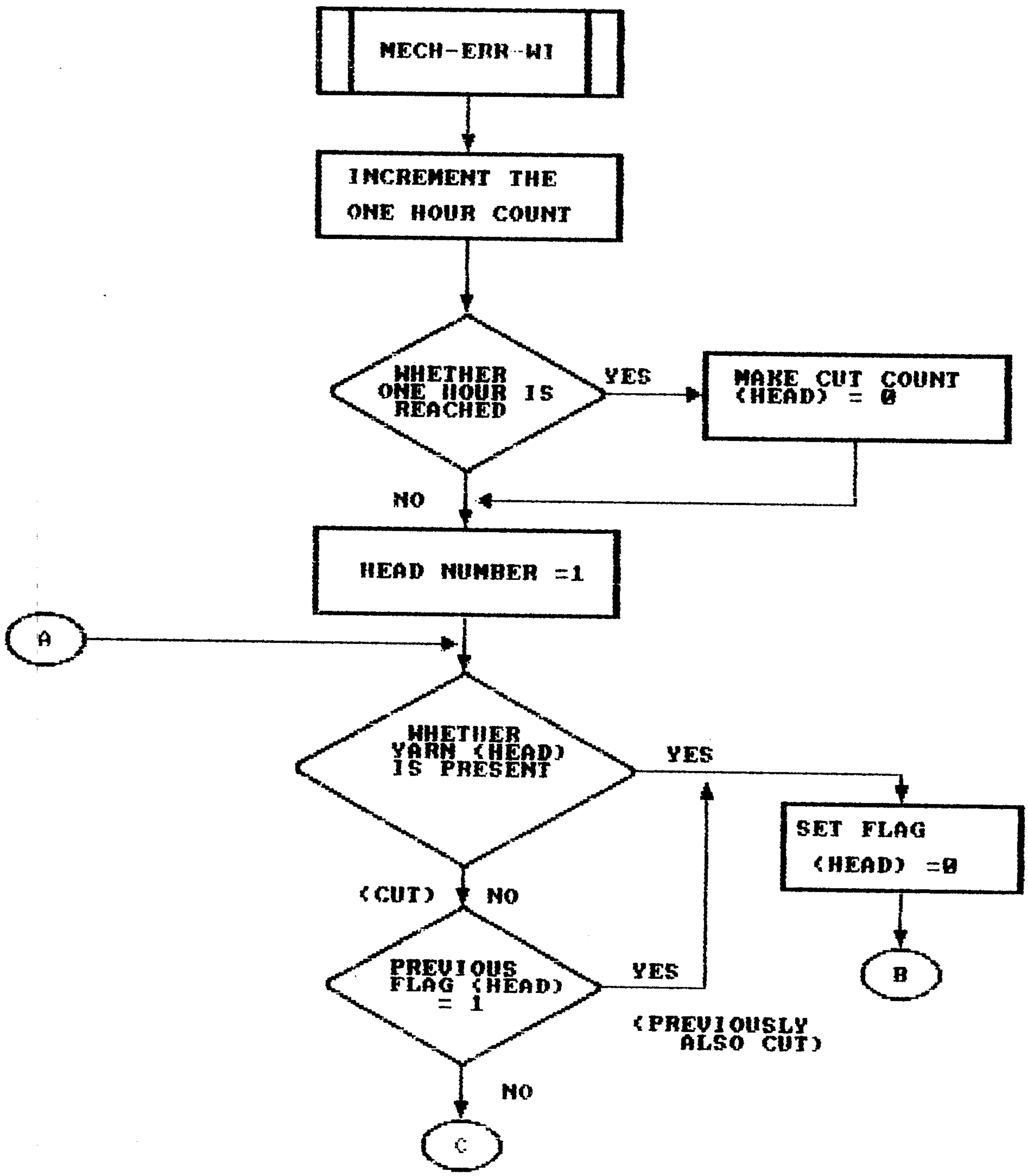
FLOW CHART. 7.


TIMINC WI
INCREMENT THE TOTAL SHIFT TIME COUNT
HEAD NUMBER =1
WHETHER YARN (HEAD) IS PRESENT
YES
NO
INCREMENT THE TOTAL TIME OF STOPPED COUNT
WHETHER ALL HEADS ARE COMPL ETED
NO
INCREMENT THE HEAD NUMBER
YES
RETURN

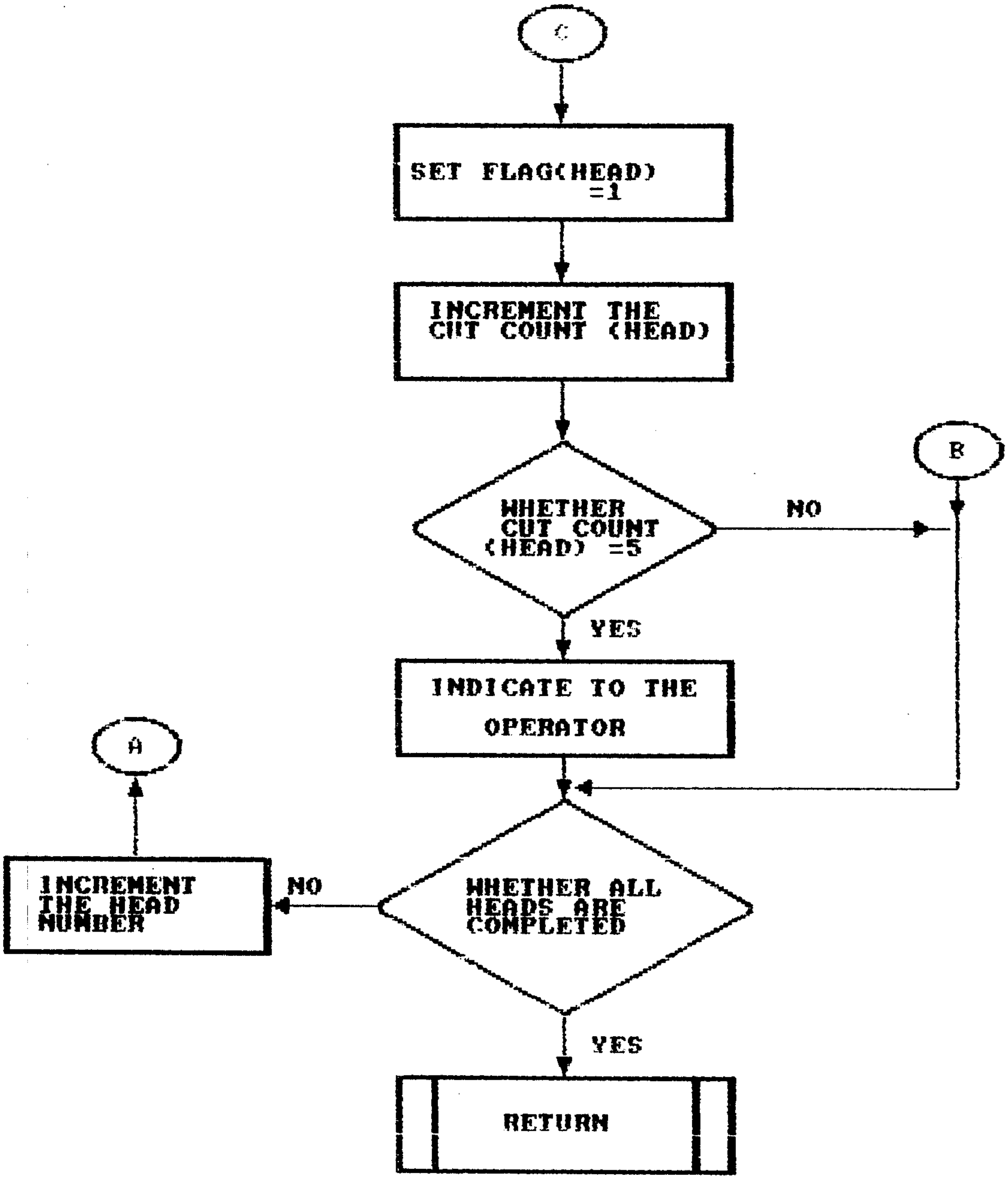
FLOW CHART. 8


EFF-WI
TOTAL TIME OF RUN = TOTAL TIME OF SHIFT - TOTAL TIME OF STOPPED
EFFICIENCY = TOTAL TIME OF RUN X100 / TOTAL TIME OF SHIFT
DISPLAY THE EFFICIENCY
MECH-ERR-WI
RETURN

FLOW CHART. 9



FLOW CHART. 10


C
SET FLAG(HEAD) =1
INCREMENT THE CUT COUNT (HEAD)
WHETHER CUT COUNT (HEAD) =5
NO
B
YES
INDICATE TO THE OPERATOR
A
INCREMENT THE HEAD NUMBER
NO
WHETHER ALL HEADS ARE COMPLETED
YES
RETURN

SOFTWARE ROUTINE

LABEL	MNEMONIC
	MAIN PROGRAM
	EI
	MVI A OC
	SIM
	MVI A, 82
	OUT 03
	MVI A,80
	OUT 43
LOOP 1	CALL RDKBD
	CPI 12(COMP KEY)
	CZ INITWI
	CPI 15(DELETE KEY)
	CZ DATENTWI
	CPI 16(OUT BYTE KEY)
	CZ EFFWI
	CPI 17
	JMP LOOP1

INITIALISATION

(CLEARING THE LENGTH COUNTS OF ALL HEADS)

LABEL	MNEMONIC
	PUSH H
	PUSH D
	PUSH B
	PUSH PSW
	MVI D,00
	LXI H,9FFE(LENGTH COUNT START ADDRESS)
	MVI B,00
LOOP 2	MVI M,00
	INX H
	INR B
	MOV A,B
	CPI 06
	JNZ LOOP2
	INR D
	INX H

LABEL	MNEMONIC
	MVI M,00
	INR A
	CPI 04
R	RZ
	INX H
	JMP LOOP 2

DATA ENTRY

	CALL DISP WI
	LXI H, A300(required length store start address
LOOP	PUSH H
	PUSH D
	CALL RDKBD
	POP D
	POP H
	CPI 15
	JZ LOOP X
	PUSH H
	CALL DISPWI
	POP H
	INX H
	JMP LOOP
LOOP X	CALL CLEAR
	RET

LABEL	MNEMONIC
	DISP WI
	MVI A,00
	MVI B,00
	LXI H,A300
	CALL OUTPUT
	RET
	DIS UPDT WI
	MVI B,00
	MVI H,A0
LOOP 5	MOV L,B
	MOV A,M
	PUSH H
	MOV L,A
	MVI H,A4
	MVI C,01
LOOP 4	MVI A,00
	OUT PORT A
	MOV A,M
	ANA C
	CMP C
	JZ LOOP 7
	MVI A,00
	JMP LOOP 8

LABEL	MNEMONIC
LOOP 7	MVI A 01
LOOP 8	OUT PORT A
	ADI 02
	OUT PORT A
	MOV A,C
	RAL
	MOV C,A
	JNC LOOP 4
	POP H
	INR B
	MOV A,B
	ANI 07
CPI 04	
	JNZ LOOP 5
	MOV A,B
	ANI F8
	ADI 08
	CPI 10
	JZ LOOP 6
	MOV B,A
	JMP LOOP 5
LOOP 6	MVI A, 04

LABEL	MNEMONIC
	OUT PORT A
	MVI A,00
	OUT PORT A
	RET

COUNT UPDT WI(6.5 INTERRUPT)

	PUSH H
	PUSH D
	PUSH B
	PUSH PSW
	MVI A,0E
	SIM
	EI
	LXI H, A350(cutter data address)
	MVI M,00
	MVI B,00
	MVI C, 01
LOOP X	MVI H ,A0
	IN PORT B
	ANA C
	CMP C
	JNZ LOOP 5
	MOV L,B

LABEL	MNEMONIC
	DCX H
	DCX H
	INR M
	MOV A,M
	CPI 6C
	JNZ LOOP 5
	MVI M,00
	INX H
	INR M
	MOV A,M
	CPI 04
	JNZ LOOP 3
	MVI M,00
	INX H
	INR M
LOOP 4	MOV A,M
	CPI 0A
	JNZ LOOP 3
	MVI M,00
	INX H
	INR M
	JMP LOOP 4

LABEL	MNEMONIC
	LXI D,A303
	MOV L,B
LOOP 6	MOV A,M
	XCHG
	CMP M
	XCHG
	JNZ LOOP 5
	INX H
	DCX D
	MOV A,L
	ANI 07
	CPI 04
	JNZ LOOP 6
	JMP LOOP 10
LOOP 5	MOV A,B
	ADI 08
	MOV B,A
	MOV A,C
	RLC
	MOV C,A
	CPI 04

LABEL	MNEMONIC
	JNZ LOOP X
	JMP LOOP 9
LOOP 10	MVI A, 00
LOOP 11	DCX H
	MVI M, 00
	INR A
	CPI 06
	JNZ LOOP 11
	PUSH H
	LXI H, A350
	MOV A,C
	ORA M
	MOV M,A
	POP H
	JMP LOOP 5
LOOP 9	LDA A350
	OUT PORT C
	POP PSW
	POP B
	POP D
	POP H
	MVI A, OC
	SIM
	RET

TIMINC - W1

LABEL	MNEMONIC
	PUSH H
	PUSH D
	PUSH B
	PUSH PSW
	LX1 H, A200 (Total time of shift Address)
	MOV A,M
	ADI 01
	MOV M,A
	JNC Loop2
	CMC
	MV1 M, 00
	INX H
	INR M
LOOP2	LX1 H AZ OZ (Total time of run Address)
	MV1 C, 01
LOOP1	IN port B1
	ANA C
	CMP C
	JNZ loop4
	MOV A, M

```
        ADI 01
        MOV M, A
        JNC loop4

LABEL   MNEMONIC
        CMC
        MVI M, 00
        INX H
        INR M
LOOP4   MOV A,C
        R L C
        MOV C, A
        CPl 04
        JNZ loop
        CALL MECH - ERR - w l
        POP PSW
        POP B
        POP D
        POP H
        EI
        RET
```

MECH - ERR - W 1

LABEL	MNEMONIC
	MVI C, 01
	LXI H A 355 (Address of one have cormt)
	INR M
	MOV A, M
	CPI 90
	JNZ loop1 A
	MVI M, 00
	INX H
	INR M
	MOV A, M
	CPI 19
	JZ loop2
loop,A	LX1 H, A 500 (Mech error flag & count start address)
loop1	MOV A,C
	IN Port B1
	ANA C
	CMP C
	JZ LOOP4
	MVI A, 00

LABEL MNEMONIC

```
ADD M
JNZ loop4
MVI MFf
INX H
INR M
MOV A, M

CPI 05
JNZ loop5
MVI M, 00
MOV A,C
PUSH H
LXI H A450
ORA M
MOV M, A
POP H
INX H
MOV A,C
RLC
MOV C, A
CPI 04
JNZ loopl
LXI H A50 (mechanical error
           bit address)
```

LABEL MNEMONIC

```
MOV A, M
OUT Port AII
POP PSW
POP B
POP D
POP H
RET.
```

LABLE	MNEMONIC
LOOP 4	MVI M,OO
	INX H
	JMP LOOP 5
	MVI M,OO
	MVI B 02
	LXI H A501
LOOP 2B	MVI M,OO
	INX H
	INX H
	DCR B
	JNZ LOOP 2B
	LXI H, A450
	MVI M,OO
	JMP LOOP 1A

LABLE	MNEMONIC
	MVI A,03
	LXI H, A600
LOOP 1	MVI M,00
	INX H
	DCR A
	JNZ LOOP 1
	MVI M,OE
	LHLD A202
	XCHG
	LXI H,0000
	MVI B,00
	MVI C,332
LOOP 2	MOV A,C
	ADD E
	MOV L,A
	MOV A,H
	ADC D
	MOV H,A
	JNC LOOP 3
	INR B
	CMC
LOOP 3	DCR C
	JNZ LOOP 2
	XCHG
	MVI C,00

LABLE	MNEMKONIC
LOOP 3A	LHLD A200 (TOTAL TIME OF SHIFT ADD)
	JC LOOP 6A
	CALL INC RI _ WI
	JMP LOOP 3A
LOOP 6A	MVI A,00
	ADD B
	JZ LOOP 4
	CALL INCRI- WI
	JMP DECI- AD- WI
INCRI- WI	
	PUSH H
	LXI H, A603
	inr m
	MOV A,M
	CPI OA
	JNZ LOOP 5
	MVI M, 00
	DCX H
	INR M
	MOV A, M
	CPI OA
	JNZ LOOP 5
	MVI M,00
	DCX H

LABLE	MNEMONIC
DECI- AD- WI	
	MOV A,O
	CMA
	MOV D,A
	MOV A,E
	CMA
	MOV E,A
	DCR B
	XCHG
	LXI D,FFFF
	CALL HILO
	MVI M,OO
	ADD B
	JNZ LOOP3A
	LHLD A200
	PUSH D
	CALL HILO
	JC LOOP $ 4a
	MOV A, D
LOOP 4	MVI M,OO
	INX H
	JMP LOOP5
	MVI M 00
	MVI B 02
	LXI H A501
loop 2B	MVI M,00
	INX H

LABEL	MNEMONIC
	ADD E
	JC LOOP X
	JZ LOOP 4B
LOOP X	POP D
	JMP LOOP 3A
LOOP 4A	POP H
LOOP 4	LXI H A200
	MVI A00
	MVI B00
	CALL OUTPUT
	RET

LENGTH COUNT START ADDRESS -9FFFH

A000

A001

A002

A003) FIRST HEAD

TOTAL TIME OF SHIFT START ADDRESS	A200
TOTAL TIME OF RUN START ADDRESS	A202
CHECK COUNT START ADDRESS	A300
CUTTER DATA ADDRESS	A350
SEVEN SEGMENT DATA START ADDRESS	-A400
MECHANICAL ERROR BIT ADDRESS	A450
TOTAL TIME OF SHIFT ADDRESS	A360
TOTAL TIME OF RUN	A362
ONE HOUR ADDRESS	A355
MECHANICAL ERROR AND COUNT START ADDRESS	A500
EFFICIENCY START ADDRESS	A600

DESCRIPTION OF CHIPS:

8085:

It is an 8 bit general purpose microprocessor. It has 16 line address bus and is capable of addressing 64 K of memory. Its operating frequency is 3 MHz (single phase clock). It has 40 pins and requires a power supply of +5V. It is an enhanced version of 8080 A. Its instruction set is upward compatible with that of 8080 A.

ADDRESS AND DATA BUS:

The address bus consists of A_0 - A_{15} out of which A_{15} - A_8 is unidirectional. A_0 - A_7 is bidirectional as it is multiplexed for data and it is also the lower order bus.

CONTROL AND STATUS SIGNAL:

This signals are usd to identify the nature of operation. They are

S1 AND S0:

These status signals, similar to IO/$\overline{M}$ can identify various operations, but they are rarely used in small systems.

8085 MACHINE CYCLE STATUS AND CONTROL SIGNALS

Machine Cycle	IO/$\overline{M}$	Status		Control Signals
		S1	S0	
Opcode Fetch	0	1	1	$\overline{RD}$ = 0
Memory Read	0	1	0	$\overline{RD}$ = 0
Memory write	0	0	1	$\overline{WR}$ = 0
I/O Read	1	1	0	$\overline{RD}$ = 0
I/O Write	1	0	1	$\overline{WR}$ = 0
INTR Acknowledge	1	1	1	$\overline{INTA}$ = 0
Halt	Z	0	0	$\overline{RD}$, $\overline{WR}$ = Z $\overline{INTA}$ = 1
Hold	Z	X	X	
Reset	Z	X	X	

CLOCK FREQUENCY:

X1, X2 : Crystal is connected at these two pins. The frequency is internally divided by two ; therefore, to operate a system at 3 MHz, the crystal should have a frequency of 6 MHz.

This is a positive going pulse generated every time the 8085 begins an operation. It indicates that the bits on $AD_7 - AD_0$ are address bits. This signal is used primarily to latch the low order address from the multiplexed bus and generate a separate set of eight address line $A_7 - A_0$.

READ ($\overline{RD}$):

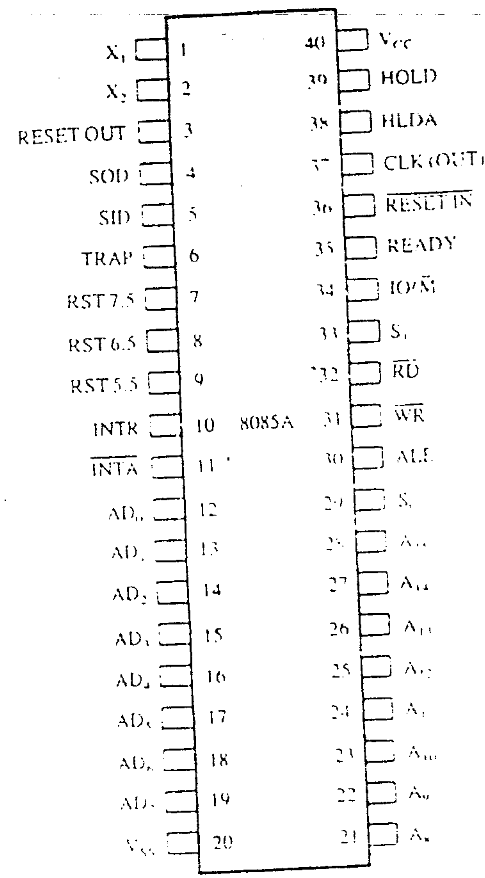
This is a read control signal (active low). This signal indicates that the selected I/O or memory device is to be read and data are available on the data bus.

WRITE ($\overline{WR}$):

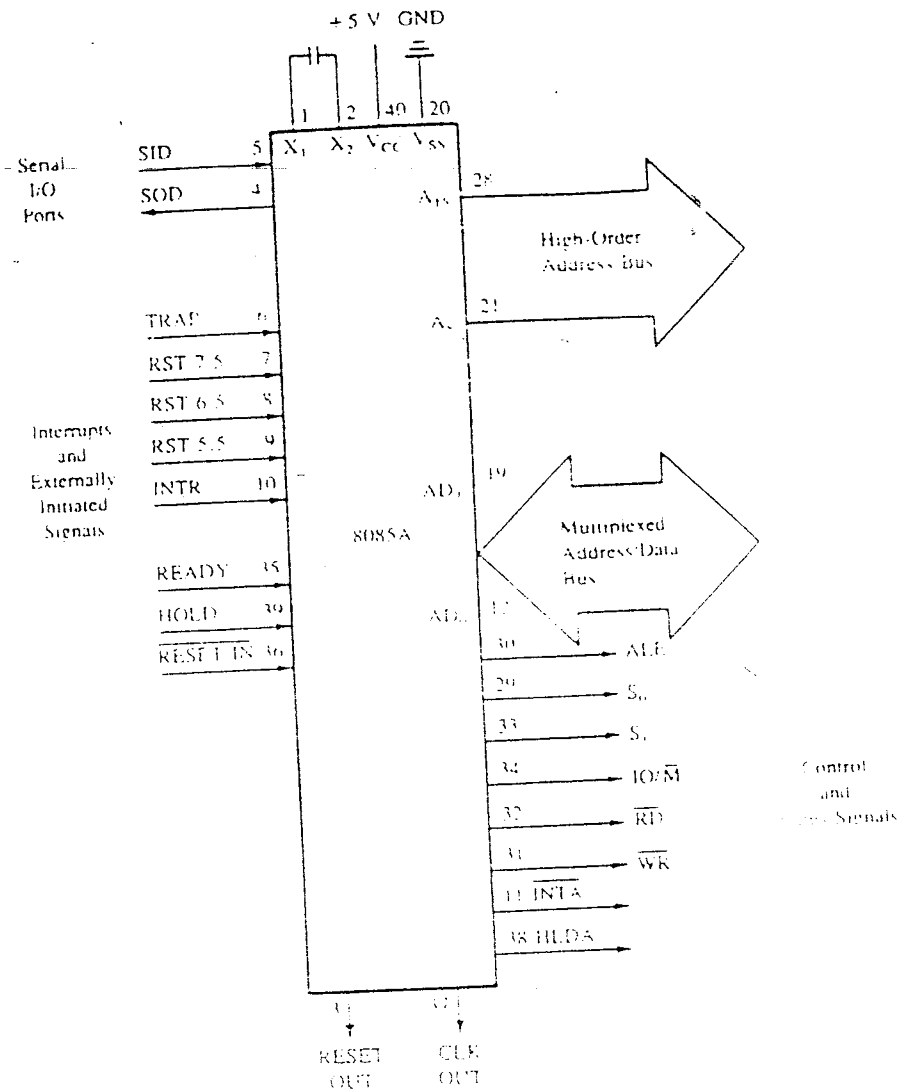
This is a write control signal (active low). This signal indicates that the data on the data bus are to be written into a selected memory or I/O location.

IO/$\overline{M}$:

This is a status signal used to differentiate between I/O and memory operations. When it is high, it indicates an I/O operation, when it is low, it indicates a memory operation. This signal is combined with RD and WR to generate I/O and memory control signals.



8085 Pinout



8085 Microprocessor Pinout and Signals

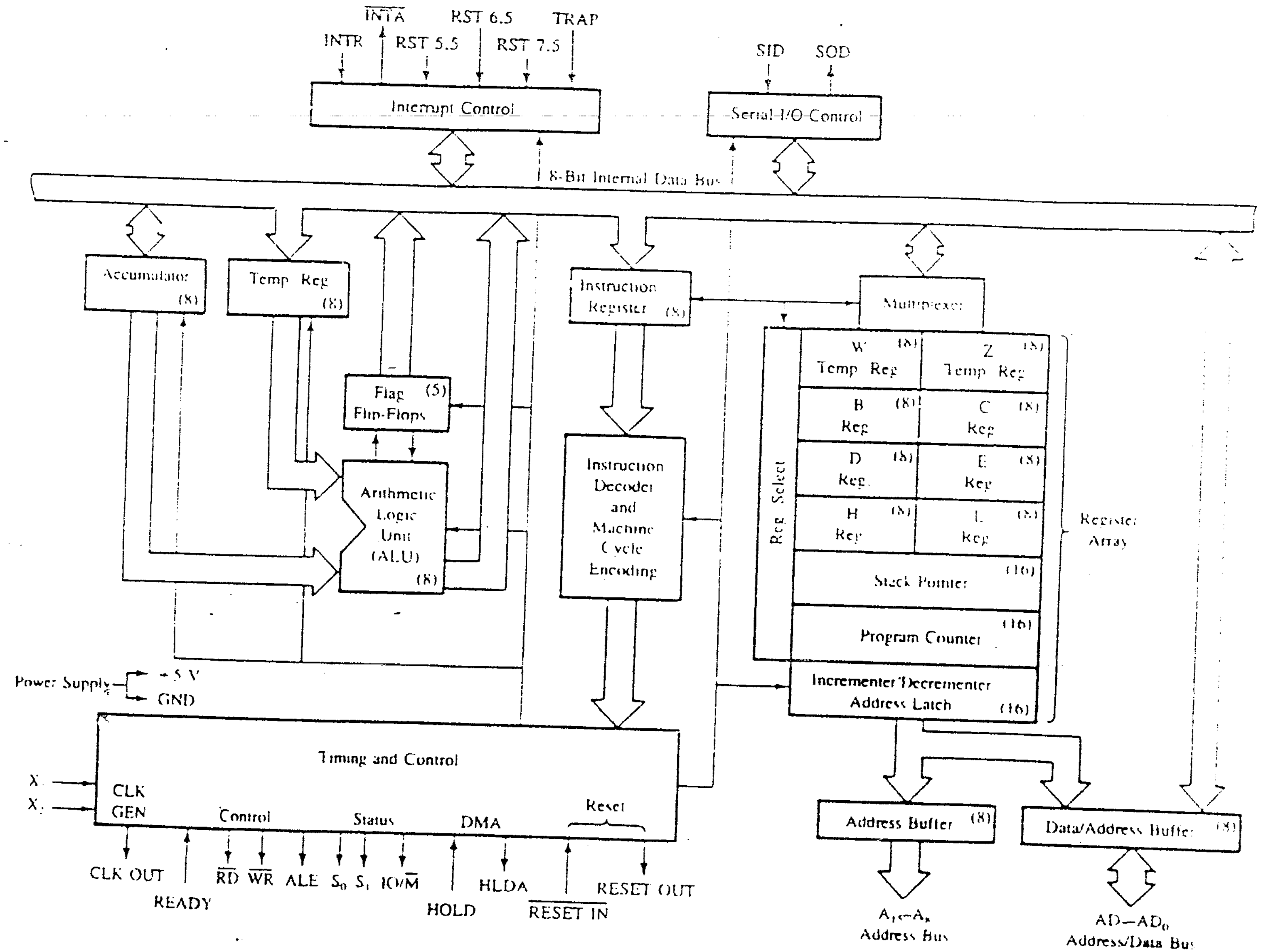


FIG. 1.2 The 8085A Microprocessor: Functional Block Diagram

FIG 4-1-A Schematic to Generate Read/Write Control Signals for Memory and I/O

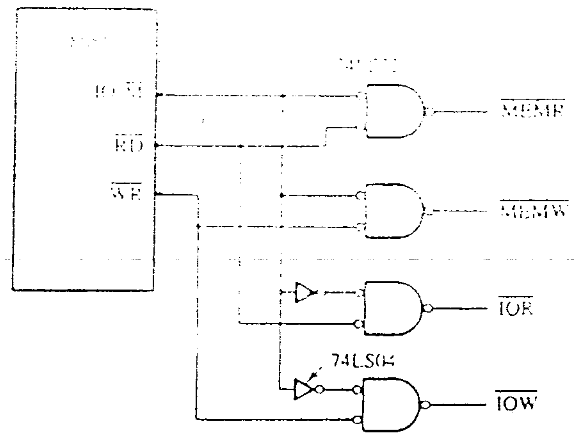
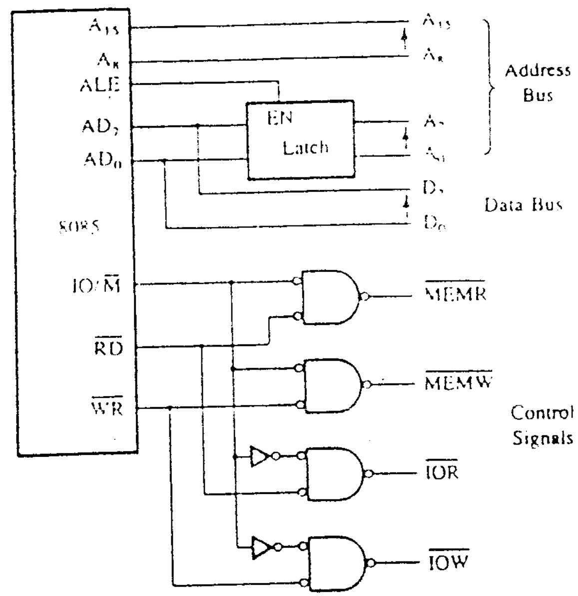


FIG 4-1-B 8085 Demultiplexed Address and Data Bus with Control Signals



INTERRUPTS AND EXTERNALLY INITIATED OPERATIONS:

The 8085 has got five interrupt signals that can be used to interrupt a program execution.

INTR	Inter Request This is used as a general purpose interrupt
RST 7.5 RST 6.5 RST 5.5	Restart Interrupt

These are vectored interrupts and transfer the program control to specific memory location. Among these three the priority order is 7.5, 6.5 and 5.5.

TRAP	This is a non-maskable interrupt and has got the highest priority.
HOLD	This signal indicates that a peripheral such as a DMA controller is requesting the use of address and data buses.
$\overline{INTA}$	This is an output signal and is used to acknowledge the interrupt.
HLDA	Hold acknowledge. This signal acknowledges the Hold request.
READY	This is also an output signal. This signal is used to delay the microprocessor Read or Write.

* Decimal, binary and double precision arithmetic.
* Direct addressing capability to 64 k bytes of memory.

The 8085 A is complete 8 bit parallel central processing unit (CPU). Its instruction set is 100% software compatible with the 8080 A microprocessor, and it is designed to improve the present 8080 A's performance by higher system speed. Its high level of system integration allows a minimum system of three IC's [8085 A (CPU), 8156 (RAM/IO) and 8355/8755 A (ROM/PROM/IO) while maintaining total system expandability.

The 8085 A incorporates all of the features that the 8224 (clock generator) and 8228 (system controller) provided for the 8080 A, thereby offering a high level of system integration.

The 8085 A uses a multiplexed data bus. The address is split between the 8 bit address bus and the 8 bit data bus. The on - chip address latches of 8155/8156/8355/8755 A memory products allow a direct interface with the 8085 A.

is 1, the number will be viewed as a negative number. If it is 0, the number will be considered as positive. In arithmetic operations with signed numbers, bit D7 is reserved for indicating the sign, and the remaining seven bits are used to represent the magnitude of a number.

ZERO FLAG (Z):

The Zero flag is set if the ALU operation results in 0, and the flag is reset if the result is not 0. This flag is modified by the results in the accumulator as well as in the other registers.

AUXILLARY CARRY FLAG (AC):

In an arithmetic operation, when a carry is generated by digit D3 and passed on to digit D4, the AC flag is set. The flag is used only internally for BCD operations, and is not available for the programmer to change the sequence of a program with a jump instruction.

PARITY FLAG (P):

After an arithmetic or logic operation, if the result has an even number of 1s, the flag is set. If it has an odd number of 1s, the flag is reset.

CARRY FLAG (CY):

If an arithmetic operation results in a carry the carry flag is set, otherwise it is reset.

EXECUTION:

The MPU places the memory address of the instruction of the address bus and it indicates the operation status on the status lines. MPU sends sthe MEMR signal to enable the memory, fetches the instruction byte and places it in the instruction decoder and also the MPU executes the instruction.

SINGLE CHIP 8-BIT N-CHANNEL MICROPROCESSOR [8085 A]:

* Single + 5V power supply.
* 100% software compatible with 8080 A.
* 1.3 micro seconds instruction cycle.
* On chip system controller, advanced cycle status information available for large system control.
* On chip clock generator (with external crystal, LC or RC Network.
* Four Vectored interrupt inputs (one is non-maskable) plus an 8080 A compatible interrupt.
* Serial In / Serial Out port.

8255A/8255A-5
PROGRAMMABLE PERIPHERAL INTERFACE

- MCS-85™ Compatible 8255A-5
- 24 Programmable I/O Pins
- Completely TTL Compatible
- Fully Compatible with Intel® Microprocessor Families
- Improved Timing Characteristics
- Direct Bit Set/Reset Capability Easing Control Application Interface
- Reduces System Package Count
- Improved DC Driving Capability
- Available in EXPRESS
  - —Standard Temperature Range
  - —Extended Temperature Range

The Intel® 8255A is a general purpose programmable I/O device designed for use with Intel® microprocessors. It has 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation. In the first mode (MODE 0), each group of 12 I/O pins may be programmed in sets of 4 to be input or output. In MODE 1, the second mode, each group may be programmed to have 8 lines of input or output. Of the remaining 4 pins, 3 are used for handshaking and interrupt control signals. The third mode of operation (MODE 2) is a bidirectional bus mode which uses 8 lines for a bidirectional bus, and 5 lines, borrowing one from the other group, for handshaking.

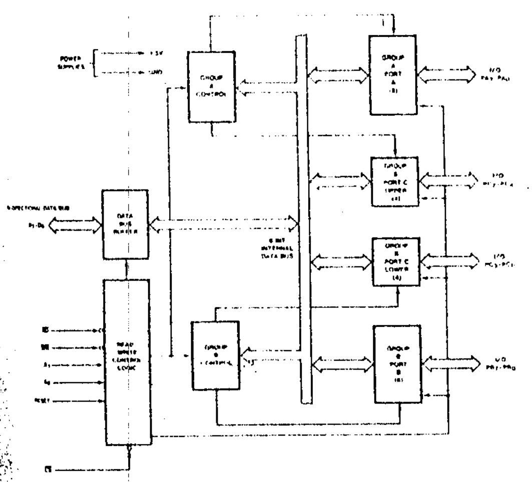


Figure 1. 8255A Block Diagram

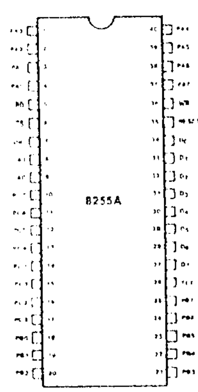


Figure 2. Pin Configuration

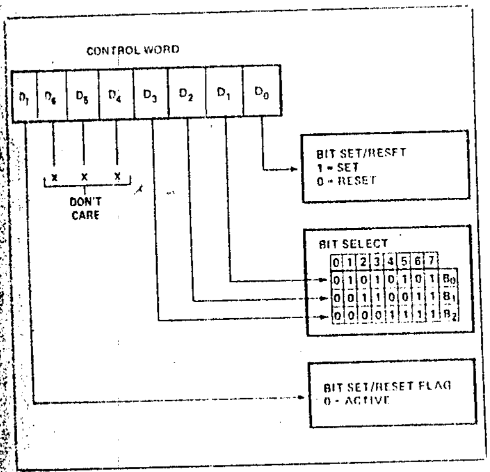


Figure 7. Bit Set/Reset Format

When Port C is being used as status/control for Port A or B, these bits can be set or reset by using the Bit Set/Reset operation just as if they were data output ports.

Interrupt Control Functions

When the 8255A is programmed to operate in mode 1 or mode 2, control signals are provided that can be used as interrupt request inputs to the CPU. The interrupt request signals, generated from port C, can be inhibited or enabled by setting or resetting the associated INTE flip-flop, using the bit set/reset function of port C.

This function allows the Programmer to disallow or allow a specific I/O device to interrupt the CPU without affecting any other device in the interrupt structure.

INTE flip-flop definition:

(BIT-SET) -- INTE is SET -- Interrupt enable
(BIT-RESET) -- INTE is RESET -- Interrupt disable

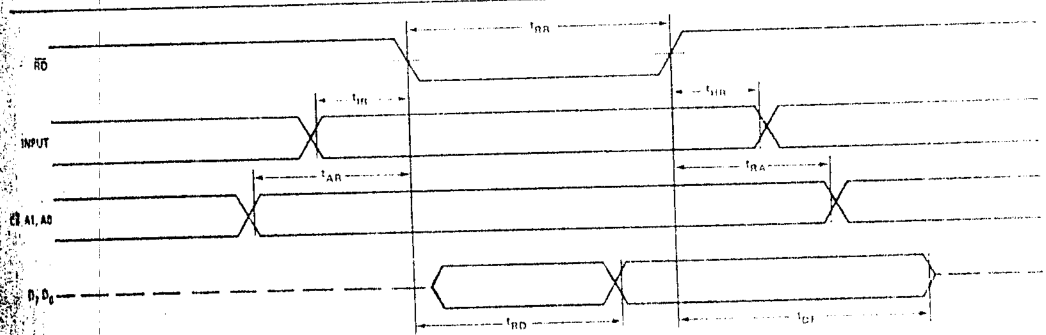
Note: All Mask flip-flops are automatically reset during mode selection and device Reset.

Operating Modes

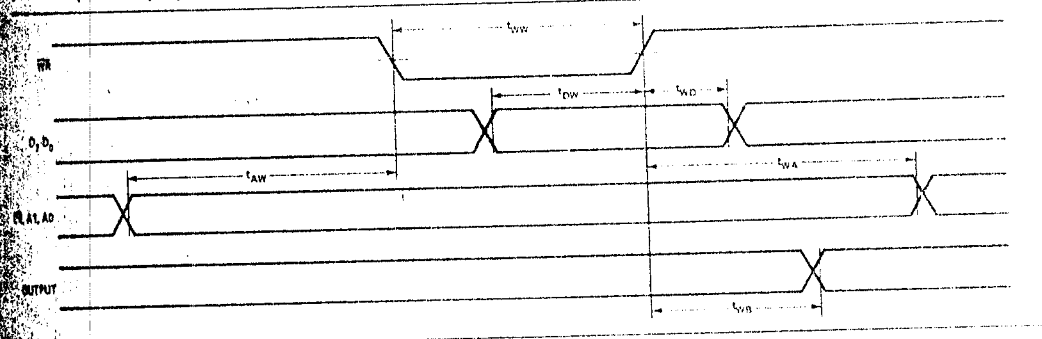
MODE 0 (Basic Input/Output). This functional configuration provides simple input and output operations for each of the three ports. No "handshaking" is required, data is simply written to or read from a specified port.

Mode 0 Basic Functional Definitions:

- Two 8-bit ports and two 4-bit ports.
- Any port can be input or output.
- Outputs are latched.
- Inputs are not latched.
- 16 different Input/Output configurations are possible in this Mode.



MODE 0 (Basic Input)



MODE 0 (Basic Output)

Input Control Signal Definition

$\overline{STB}$ (Strobe Input). A "low" on this input loads data into the input latch.

IBF (Input Buffer Full F/F)

A "high" on this output indicates that the data has been loaded into the input latch; in essence, an acknowledgement. IBF is set by STB input being low and is reset by the rising edge of the RD input.

INTR (Interrupt Request)

A "high" on this output can be used to interrupt the CPU when an input device is requesting service. INTR is set by the $\overline{STB}$ is a "one", IBF is a "one" and INTE is a "one". It is reset by the falling edge of $\overline{RD}$. This procedure allows an input device to request service from the CPU by simply strobing its data into the port.

INTE A

Controlled by bit set/reset of PC_4.

INTE B

Controlled by bit set/reset of PC_2.

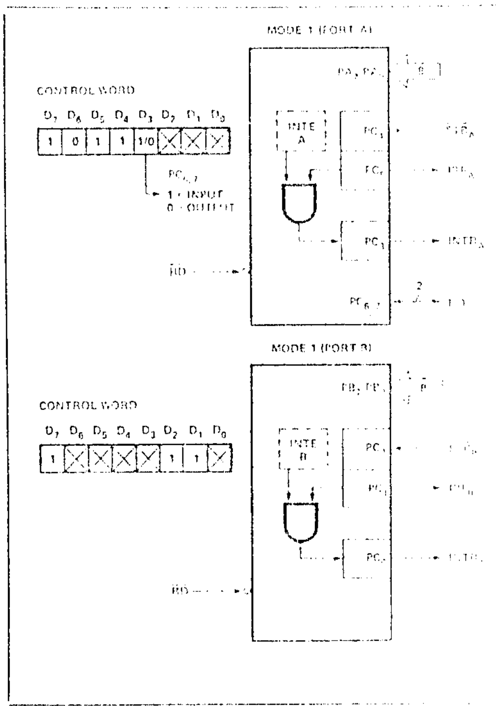


Figure 8. MODE 1 Input

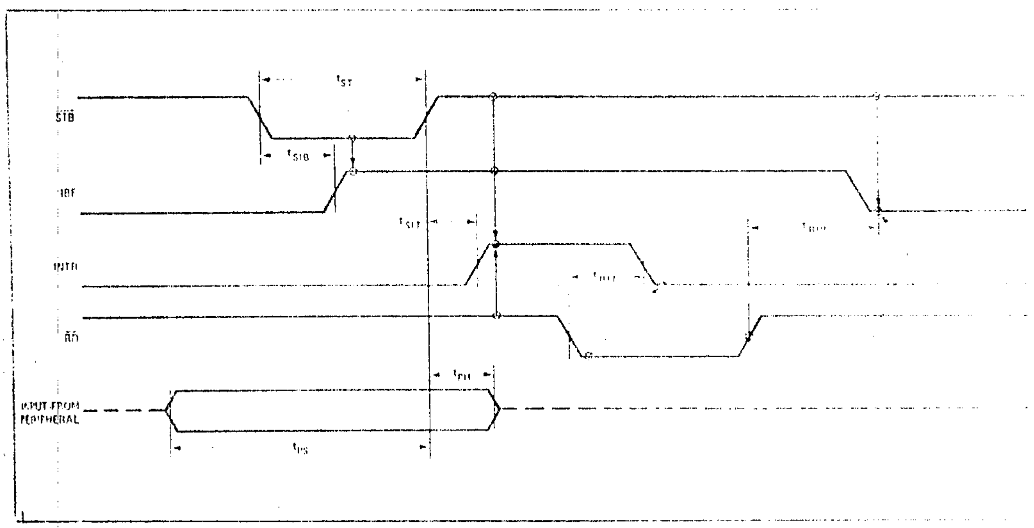


Figure 9. MODE 1 (Strobed Input)

Output Control Signal Definition

$\overline{OBF}$ (Output Buffer Full F/F). The $\overline{OBF}$ output will go "low" to indicate that the CPU has written data out to the specified port. The $\overline{OBF}$ F/F will be set by the rising edge of the $\overline{WR}$ input and reset by $\overline{ACK}$ input being low.

$\overline{ACK}$ (Acknowledge Input). A "low" on this input informs the 8255A that the data from port A or port B has been accepted. In essence, a response from the peripheral device indicating that it has recieved the data output by the CPU.

INTR (Interrupt Request). A "high" on this output can be used to interrupt the CPU when an output device has accepted data transmitted by the CPU. INTR is set when $\overline{ACK}$ is a "one", $\overline{OBF}$ is a "one", and INTE is a "one". It is reset by the falling edge of $\overline{WR}$.

INTR (Interrupt Request). A "high" on this output can be used to interrupt the CPU when an output device has accepted data transmitted by the CPU. INTR is set when $\overline{ACK}$ is a "one", $\overline{OBF}$ is a "one", and INTE is a "one". It is reset by the falling edge of WR.

INTE A

Controlled by bit set/reset of PC_6.

INTE B

Controlled by bit set/reset of PC_2.

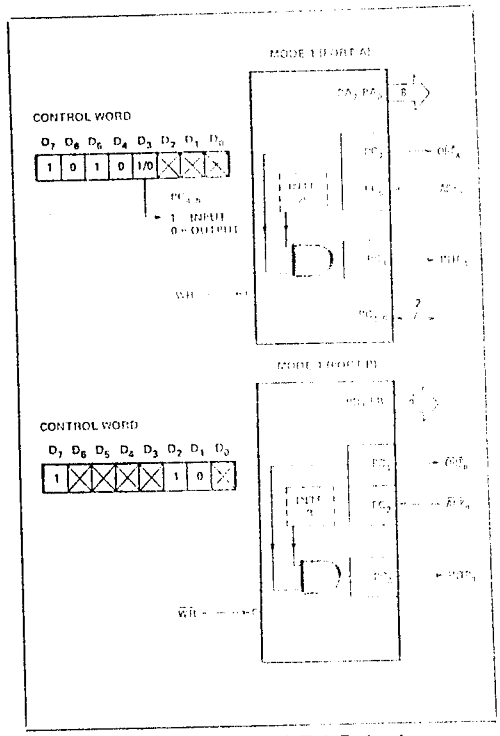


Figure 10. MODE 1 Output

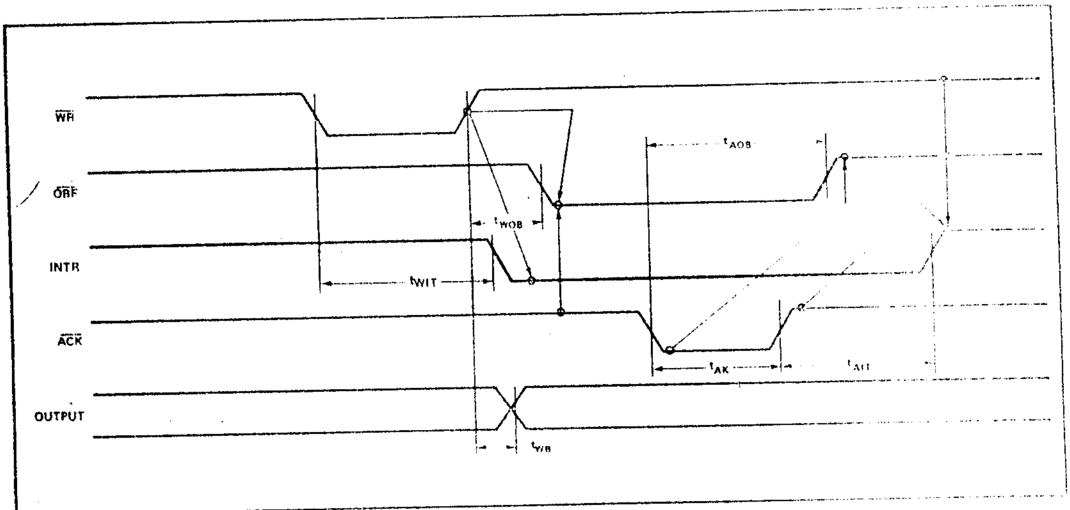


Figure 11. Mode 1 (Strobed Output)

Combinations of MODE 1

Port A and Port B can be individually defined as input or output in Mode 1 to support a wide variety of strobed I/O applications.

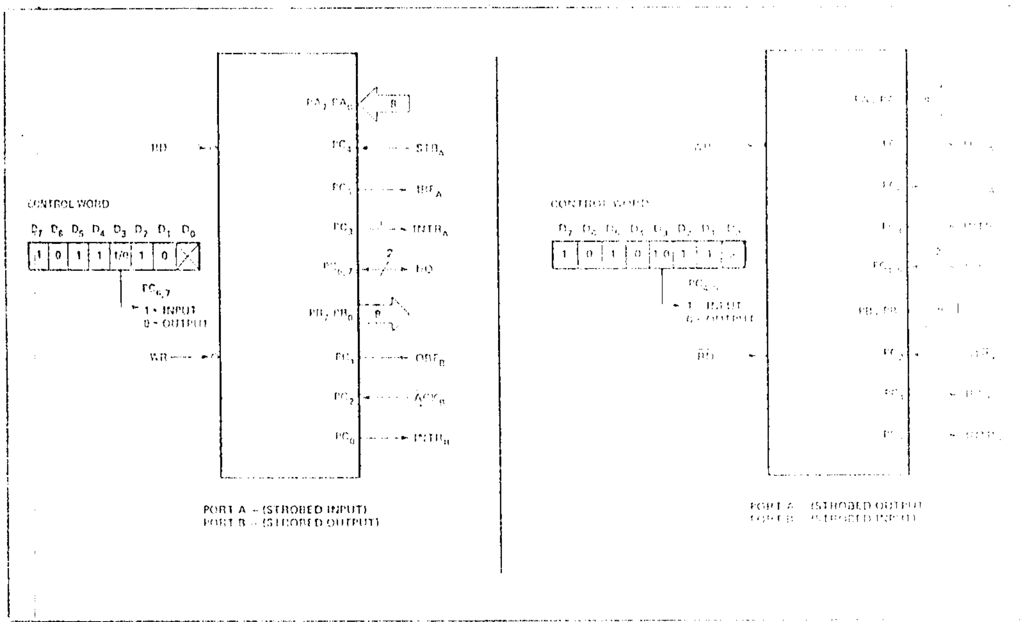


Figure 12. Combinations of MODE 1

Operating Modes

MODE 2 (Strobed Bidirectional Bus I/O). This functional configuration provides a means for communicating with a peripheral device or structure on a single 8-bit bus for both transmitting and receiving data (bidirectional bus I/O). "Handshaking" signals are provided to maintain proper bus flow discipline in a similar manner to MODE 1. Interrupt generation and enable/disable functions are also available.

MODE 2 Basic Functional Definitions:

- Used in Group A only.
- One 8-bit, bi-directional bus Port (Port A) and a 5-bit control Port (Port C).
- Both inputs and outputs are latched.
- The 5-bit control port (Port C) is used for control and status for the 8-bit, bi-directional bus port (Port A).

Bidirectional Bus I/O Control Signal Definition

INTR (Interrupt Request). A high on this output can be used to interrupt the CPU for both input or output operations.

Output Operations

$\overline{OBF}$ (Output Buffer Full). The $\overline{OBF}$ output will go "low" to indicate that the CPU has written data out to port A.

$\overline{ACK}$ (Acknowledge). A "low" on this input enables the tri-state output buffer of port A to send out the data. Otherwise, the output buffer will be in the high impedance state.

INTE 1 (The INTE Flip-Flop Associated with OBF). Controlled by bit set/reset of PC_6.

Input Operations

$\overline{STB}$ (Strobe Input). A "low" on this input loads data into the input latch.

IBF (Input Buffer Full F/F). A "high" on this output indicates that data has been loaded into the input latch.

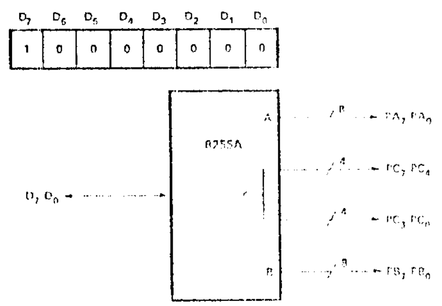
INTE 2 (The INTE Flip-Flop Associated with IBF). Controlled by bit set/reset of PC_4.

MODE 0 Port Definition

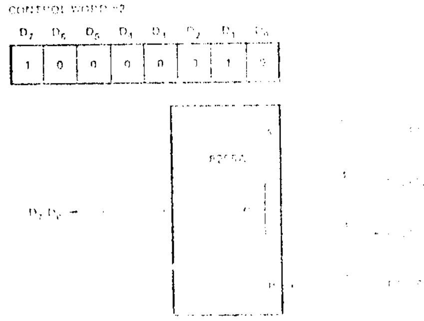
A		B		GROUP A			GROUP B	
D4	D3	D1	D0	PORT A	PORT C (UPPER)	#	PORT B	PORT C (LOWER)
0	0	0	0	OUTPUT	OUTPUT	0	OUTPUT	OUTPUT
0	0	0	1	OUTPUT	OUTPUT	1	OUTPUT	INPUT
0	0	1	0	OUTPUT	OUTPUT	2	INPUT	OUTPUT
0	0	1	1	OUTPUT	OUTPUT	3	INPUT	INPUT
0	1	0	0	OUTPUT	INPUT	4	OUTPUT	OUTPUT
0	1	0	1	OUTPUT	INPUT	5	OUTPUT	INPUT
0	1	1	0	OUTPUT	INPUT	6	INPUT	OUTPUT
0	1	1	1	OUTPUT	INPUT	7	INPUT	INPUT
1	0	0	0	INPUT	OUTPUT	8	OUTPUT	OUTPUT
1	0	0	1	INPUT	OUTPUT	9	OUTPUT	INPUT
1	0	1	0	INPUT	OUTPUT	10	INPUT	OUTPUT
1	0	1	1	INPUT	OUTPUT	11	INPUT	INPUT
1	1	0	0	INPUT	INPUT	12	OUTPUT	OUTPUT
1	1	0	1	INPUT	INPUT	13	OUTPUT	INPUT
1	1	1	0	INPUT	INPUT	14	INPUT	OUTPUT
1	1	1	1	INPUT	INPUT	15	INPUT	INPUT

MODE 0 Configurations

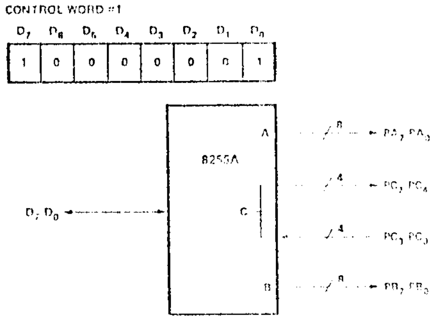
CONTROL WORD #0



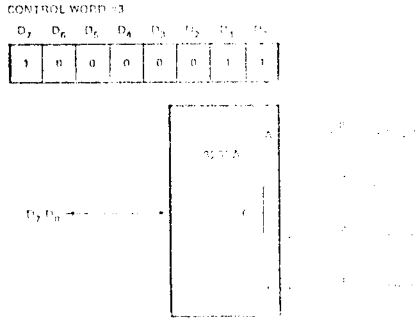
CONTROL WORD #2



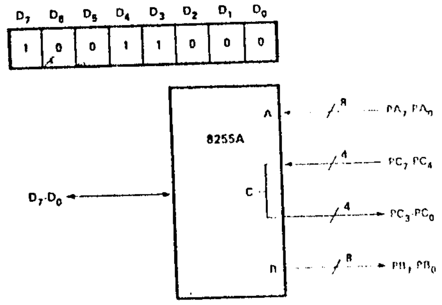
CONTROL WORD #1



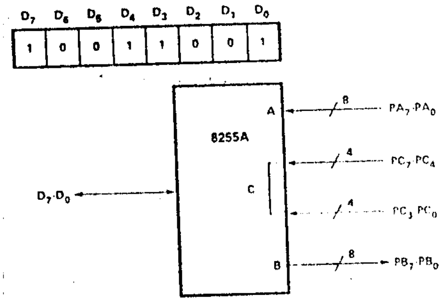
CONTROL WORD #3



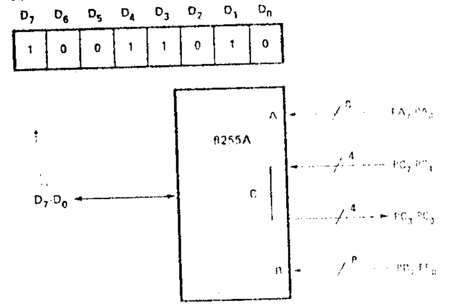
CONTROL WORD #12



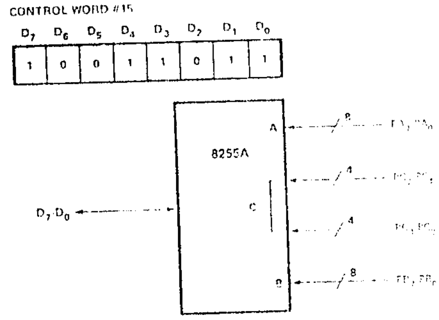
CONTROL WORD #13



CONTROL WORD #14



CONTROL WORD #15



Operating Modes

MODE 1 (Strobed Input/Output). This functional configuration provides a means for transferring I/O data to or from a specified port in conjunction with strobes or "handshaking" signals. In mode 1, port A and port B use the lines on port C to generate or accept these "hand-shaking" signals.

Mode 1 Basic Functional Definitions:

- Two Groups (Group A and Group B)
- Each group contains one 8-bit data port and one 4-bit control/data port.
- The 8-bit data port can be either input or output. Both inputs and outputs are latched.
- The 4-bit port is used for control and status of the 8-bit data port.

CD4094B Types

CMOS 8-Stage Shift-and-Store Bus Register

High-Voltage Types (20-Volt Rating)

The RCA-CD4094B is an 8-stage serial shift register having a storage latch associated with each stage for strobing data from the serial input to parallel buffered 3-state outputs. The parallel outputs may be connected directly to common bus lines. Data is shifted on positive clock transitions. The data in each shift register stage is transferred to the storage register when the STROBE input is high. Data in the storage register appears at the outputs whenever the OUTPUT-ENABLE signal is high.

Two serial outputs are available for cascading a number of CD4094B devices. Data is available at the Q_S serial output terminal on positive clock edges to allow for high-speed operation in cascaded systems in which the clock rise time is fast. The same serial information, available at the Q'_S terminal on the next negative clock edge, provides a means for cascading CD4094B devices when the clock rise time is slow.

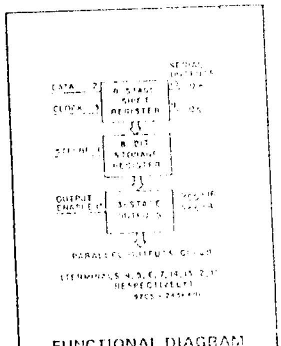
The CD4094B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).

Features:

- 3-state parallel outputs for connection to common bus
- Separate serial outputs synchronous to both positive and negative clock edges for cascading
- Medium speed operation – 5 MHz at 10 V (typ.)
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (full package temperature range):
  1 V at V_{DD} = 5 V 2 V at V_{DD} = 10 V
  2.5 V at V_{DD} = 15 V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Serial-to-parallel data conversion
- Remote control holding register
- Dual-rank shift, hold, and bus applications



FUNCTIONAL DIAGRAM

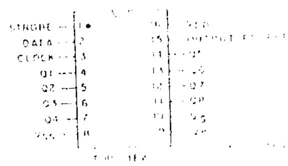


Fig. 1 – Terminal assignment

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)	-0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = -55 to +100°C (PACKAGE TYPES D, F, K)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR: For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A)	
PACKAGE TYPES D, F, K, H	-55 to +125°C
PACKAGE TYPE E	-40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING): At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

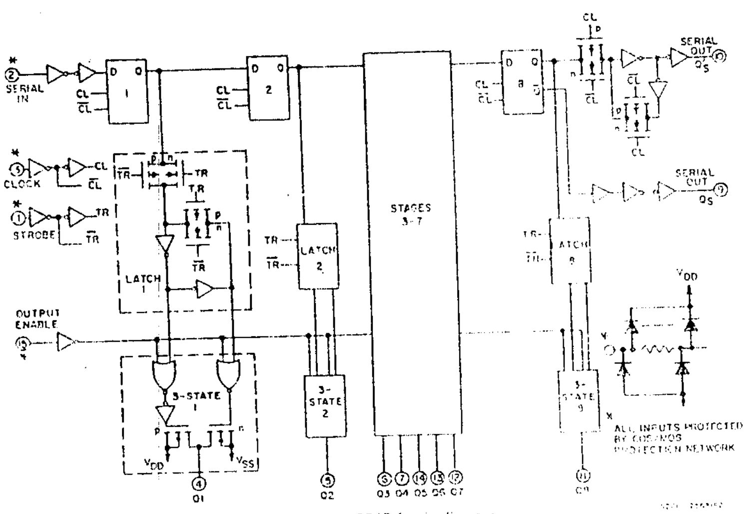


Fig. 2 – CD4094B Logic diagram.

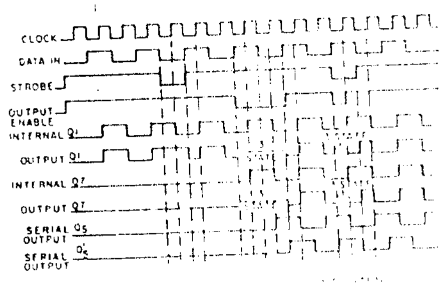


Fig. 3 – Timing diagram.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A=25°C; Input t_r,t_f=20 ns, C_L=50 pF, R_L=200 kΩ

CHARACTERISTIC	CONDITIONS V_{IN}	CONDITIONS V_{CC}	LIMITS ALL PKGS. Typ.	LIMITS ALL PKGS. Max.	UNITS
Propagation Delay Time: Low-to-High, t_{PLH} CD4049UB	5	5	60	120	ns
	10	10	32	65	
	10	5	45	90	
	15	15	25	50	
	15	5	45	90	
CD4050B	5	5	70	140	
	10	10	40	80	
	10	5	45	90	
	15	15	30	60	
	15	5	40	80	
High-to-Low, t_{PHL} CD4049UB	5	5	32	65	ns
	10	10	20	40	
	10	5	15	30	
	15	15	15	30	
	15	5	10	20	
CD4050B	5	5	55	110	
	10	10	22	55	
	10	5	50	100	
	15	15	15	30	
	15	5	50	100	
Transition Time: Low-to-High, t_{TLH}	5	5	80	160	ns
	10	10	40	80	
	15	15	30	60	
High-to-Low, t_{THL}	5	5	30	60	
	10	10	20	40	
	15	15	15	30	
Input Capacitance, C_{IN} CD4049UB	–		15	22.5	pF
CD4050B	–	–	5	7.5	

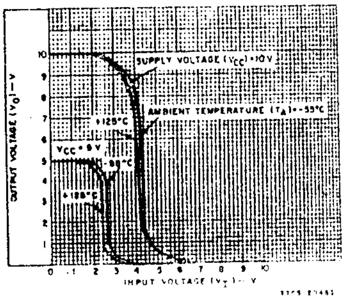


Fig. 8 – Typical voltage transfer characteristics as a function of temperature for CD4049UB.

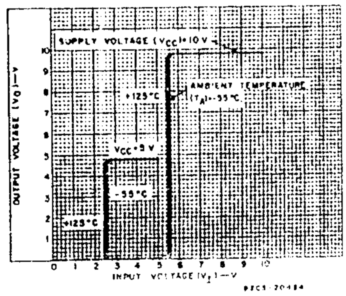


Fig. 9 – Typical voltage transfer characteristics as a function of temperature for CD4050B.

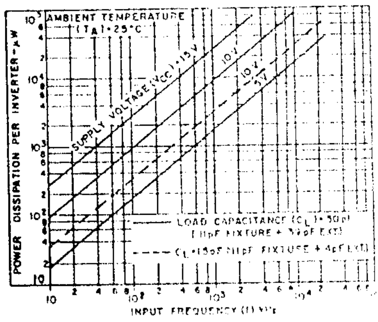


Fig. 10 – Typical power dissipation vs. frequency characteristics.

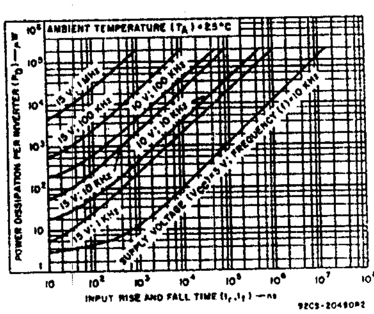


Fig. 11 – Typical power dissipation vs. input rise and fall times per inverter for CD4049UB.

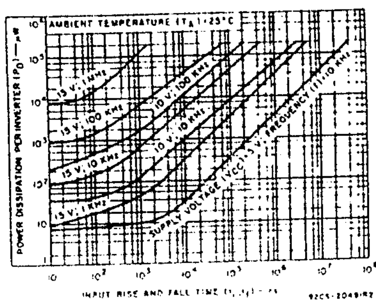


Fig. 12 – Typical power dissipation vs. input rise and fall times per inverter for CD4050B.

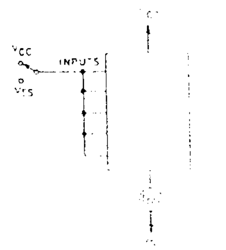


Fig. 13 – Quiescent device current test circuit.

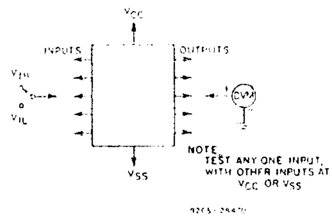


Fig. 14 – Input voltage test circuit.

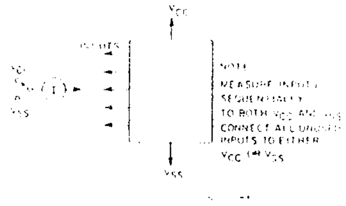


Fig. 15 – Input current test circuit.

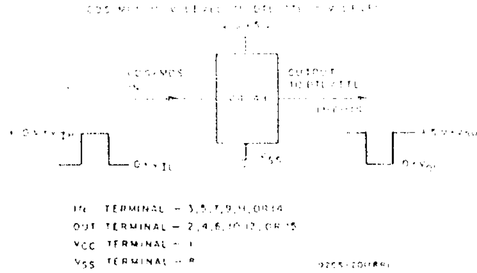
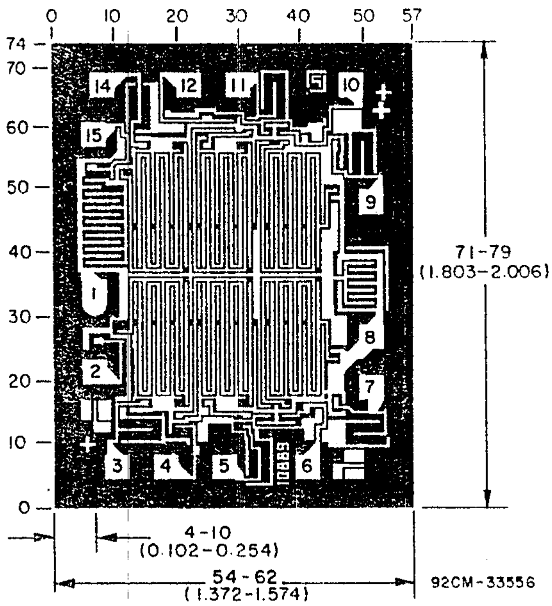
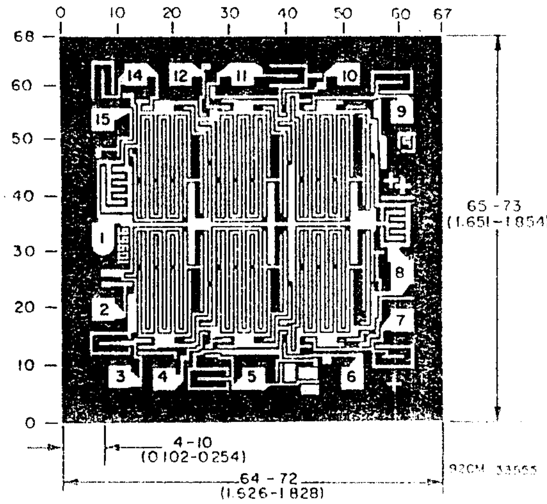


Fig. 16 – Logic-level conversion application.

CHIP PHOTOGRAPHS DIMENSIONS AND PAD LAYOUTS



CD4049UBH

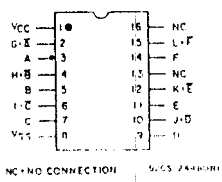


CD4050BH

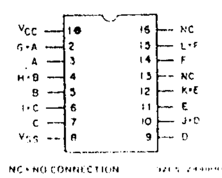
Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is separated into individual chips, the angle of cleavage may vary with respect to the chip face for different chips. The actual dimensions of the isolated chip, therefore, may differ slightly from the nominal dimensions shown. The user should consider a tolerance of −3 mils to +16 mils applicable to the nominal dimensions shown.

TERMINAL ASSIGNMENTS



CD4049UB



CD4050B

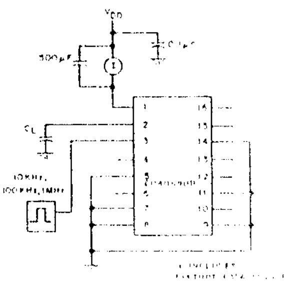


Fig. 17 – Dynamic power dissipation test circuit.

[S]TATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS V_O (V)	V_{IN} (V)	V_{CC} (V)	Limits At Indicated Temperatures (°C) *Values at -55, +25, +125 Apply to D, F, K, H Pkgs. Values at -40, +25, +85 Apply to E Package* −55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	UNITS
Quiescent Device Current, I_{DD} Max.	–	0,5	5	1	1	30	30	–	0.02	1	µA
	–	0,10	10	2	2	60	60	–	0.02	2	
	–	0,15	15	4	4	120	120	–	0.02	4	
	–	0,20	20	20	20	600	600	–	0.04	20	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	4.5	3.3	3.1	2.1	1.8	2.6	5.2	–	mA
	0.4	0,5	5	4	3.8	2.9	2.4	3.2	6.4	–	
	0.5	0,10	10	10	9.6	6.6	5.6	8	16	–	
	1.5	0,15	15	26	25	20	18	24	48	–	
Output High (Source) Current I_{OH} Min.	4.6	0,5	5	−0.81	−0.73	−0.58	−0.48	−0.65	−1.2	–	
	2.5	0,5	5	−2.6	−2.4	−1.9	−1.55	−2.1	−3.9	–	
	9.5	0,10	10	−2.0	−1.8	−1.35	−1.18	−1.65	−3.0	–	
	13.5	0,15	15	−5.2	−4.8	−3.5	−3.1	−4.3	−8.0		
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05					0	0.05	
	–	0,15	15	0.05					0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10		
	–	0,15	15	14.95				14.95	15		
Input Low Voltage: V_{IL} Max. CD4049UB	4.5	–	5	1				–	–	1	V
	9	–	10	2				–	–	2	
	13.5	–	15	2.5						2.5	
Input Low Voltage: V_{IL} Max. CD4050B	0.5	–	5	1.5				–	–	1.5	
	1	–	10	3				–	–	3	
	1.5	–	15	4				–	–	4	
Input High Voltage: V_{IH} Min. CD4049UB	0.5	–	5	4				4	–	–	
	1	–	10	8				8	–	–	
	1.5	–	15	12.5				12.5	–	–	
Input High Voltage: V_{IH} Min. CD4050B	4.5	–	5	3.5				3.5	–	–	
	9	–	10	7				7	–	–	
	13.5	–	15	11				11	–	–	
Input Current, I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm10^{-5}$	±0.1	µA

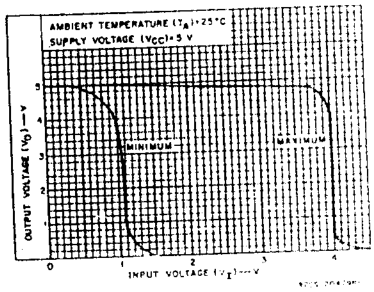


Fig. 2 – Minimum and maximum voltage transfer characteristics for CD4049UB.

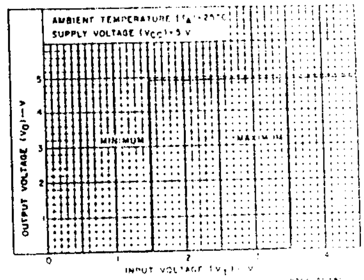


Fig. 3 – Minimum and maximum voltage transfer characteristics for CD4050B.

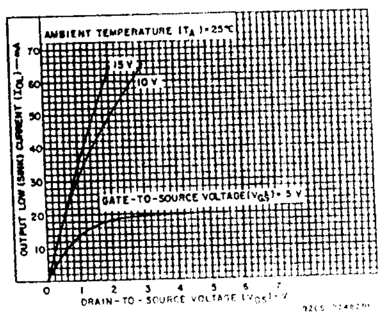


Fig. 4 – Typical output low (sink) current characteristics.

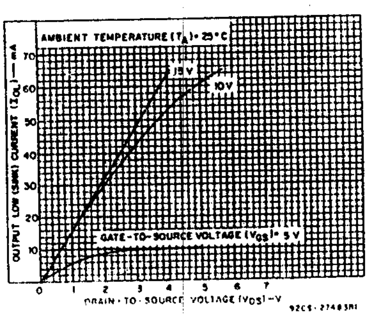


Fig. 5 – Minimum output low (sink) current drain characteristics.

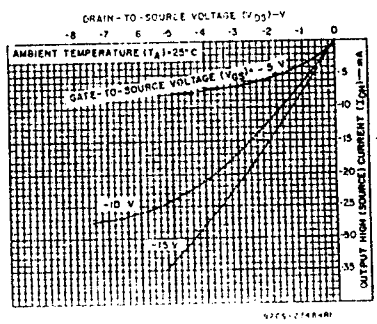


Fig. 6 – Typical output high (source) current characteristics.

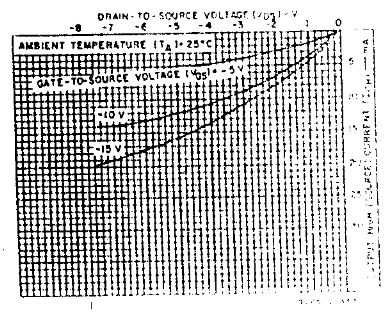


Fig. 7 – Minimum output high (source) current characteristics.

CMOS Hex Buffer/Converters

High-Voltage Types (20-Volt Rating)

CD4049UB—Inverting Type

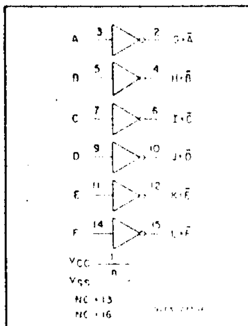
CD4050B—Non-Inverting Type

Features:

- High sink current for driving 2 TTL loads
- High-to-low level logic conversion
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- 5-, 10-, and 15-volt parametric ratings

Applications:

- CMOS to DTL/TTL hex converter
- CMOS current "sink" or "source" driver
- CMOS high-to-low logic-level converter

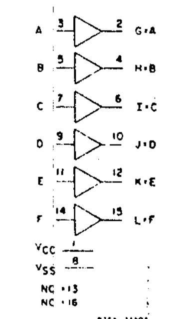


CD4049UB FUNCTIONAL DIAGRAM

The RCA-CD4049UB and CD4050B are inverting and non-inverting hex buffers, respectively, and feature logic-level conversion using only one supply voltage (V_{CC}). The input-signal high level (V_{IH}) can exceed the V_{CC} supply voltage when these devices are used for logic-level conversions. These devices are intended for use as CMOS to DTL/TTL converters and can drive directly two DTL/TTL loads. (V_{CC}=5 V, $V_{OL} \leq 0.4$ V, and $I_{OL} \geq 3.3$ mA.)

The CD4049UB and CD4050B are designated as replacements for CD4009UB and CD4010B, respectively. Because the CD4049UB and CD4050B require only one power supply, they are preferred over the CD4009UB and CD4010B and should be used in place of the CD4009UB and CD4010B in all inverter, current driver, or logic-level conversion applications. In these applications the CD4049UB and CD4050B are pin compatible with the CD4009UB and CD4010B respectively, and can be substituted for these devices in existing as well as in new designs. Terminal No. 16 is not connected internally on the CD4049UB or CD4050B, therefore, connection to this terminal is of no consequence to circuit operation. For applications not requiring high sink-current or voltage conversion, the CD4069UB Hex Inverter is recommended.

The CD4049UB and CD4050B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).



CD4050B FUNCTIONAL DIAGRAM

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{CC})
(Voltages referenced to V_{SS} Terminal) . . . -0.5 to +20 V

INPUT VOLTAGE RANGE, ALL INPUTS . . . -0.5 to +20.5 V

DC INPUT CURRENT, ANY ONE INPUT . . . ±10 mA

POWER DISSIPATION PER PACKAGE (P_D):

For T_A = –40 to +60°C (PACKAGE TYPE E) . . . 500 mW

For T_A = +60 to +85°C (PACKAGE TYPE E) . . . Derate Linearly at 12 mW/°C to 200 mW

For T_A = -55 to +100°C (PACKAGE TYPES D, F, K) . . . 500 mW

For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . 100 mW

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPES D, F, K, H . . . -55 to +125°C

PACKAGE TYPE E . . . -40 to +85°C

STORAGE TEMPERATURE RANGE (T_{stg}) . . . -65 to +150°C

LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . +265°C

RECOMMENDED OPERATING CONDITIONS at T_A=25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS Min.	LIMITS Max.	UNITS
Supply-Voltage Range (V_{CC}) (For T_A=Full Package-Temperature Range)	3	18	V
Input Voltage Range (V_{IN})	V_{CC}*	18	V

*The CD4049 and CD4050 have high-to-low-level voltage conversion capability but not low-to-high-level; therefore it is recommended that $V_{IN} \geq V_{CC}$.

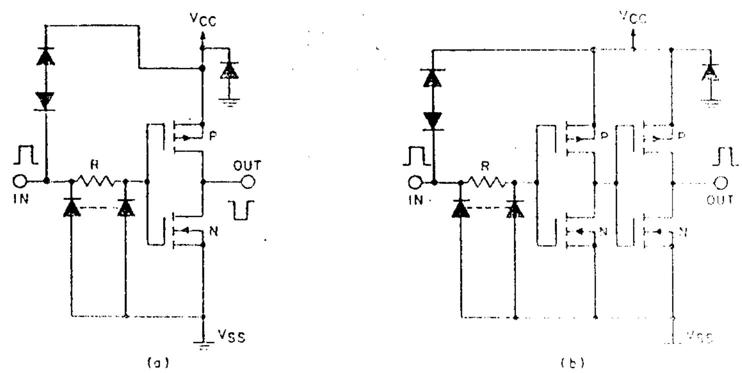


Fig. 1—a) Schematic diagram of CD4049UB, 1 of 6 identical units; b) Schematic diagram of CD4050B, 1 of 6 identical units.

RECOMMENDED OPERATING CONDITIONS *at $T_A = 25°C$, Except as Noted.*
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS MIN.	LIMITS MAX.	UNITS
Supply-Voltage Range (For T_A=Full Package-Temperature Range)		3	18	V
Data Setup Time, t_S	5 10 15	125 55 35	– – –	ns
Clock Pulse Width, t_W	5 10 15	200 100 83	– – –	ns
Clock Input Frequency, f_{CL}	5 10 15	dc	1.25 2.5 3	MHz
Clock Input Rise or Fall time, t_rCL, t_fCL:*	5 10 15	–	15 5 5	µs
Strobe Pulse Width, t_W	5 10 15	200 80 70	– – –	ns

*If more than one unit is cascaded t_fCL (for Q_S only) should be made less than or equal to the sum of the fixed propagation delay at 50 pF and the transition time of the output driving stage for the estimated capacitive load.

TRUTH TABLE

CL▲	Output Enable	Strobe	Data	Parallel Outputs Q1	Parallel Outputs QN	Serial Outputs QS*	Serial Outputs Q'S
↑	0	X	X	OC	OC	Q7	NC
↓	0	X	X	OC	OC	NC	Q7
↑	1	0	X	NC	NC	Q7	NC
↑	1	1	0	0	QN-1	Q7	NC
↑	1	1	1	1	QN-1	Q7	NC
↓	1	1	1	NC	NC	NC	Q7

▲ = Level Change
X = Don't Care
NC = No Change
OC = Open Circuit
Logic 1 = High
Logic 0 = Low

* At the positive clock edge information in the 7th shift register stage is transferred to the 8th register stage and the QS output.

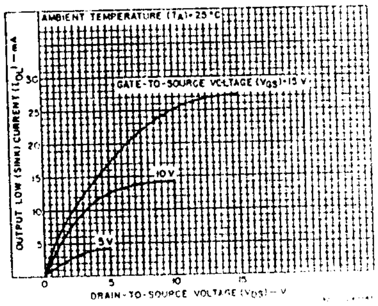


Fig. 4 – Typical output low (sink) current characteristics.

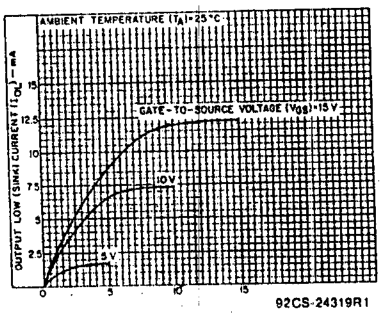


Fig. 5 – Minimum output low (sink) current characteristics.

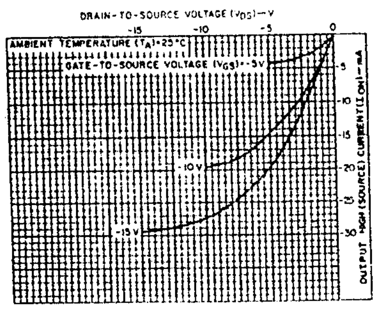


Fig. 6 – Typical output high (source) current characteristics.

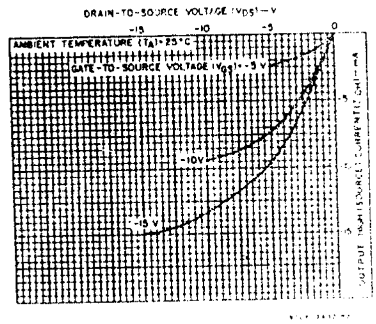


Fig. 7 – Minimum output high (source) current characteristics.

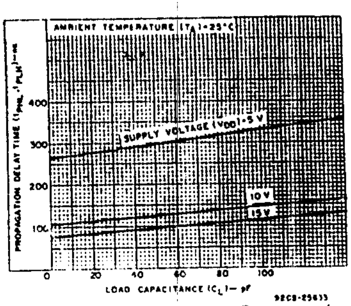


Fig. 8 – Clock-to-serial output Q_S propagation delay vs C_L.

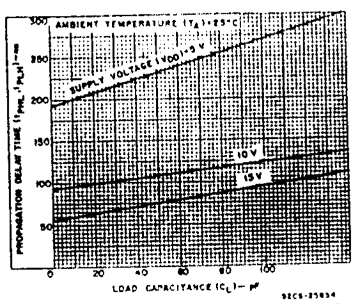


Fig. 9 – Clock-to-serial output Q'_S propagation delay vs C_L.

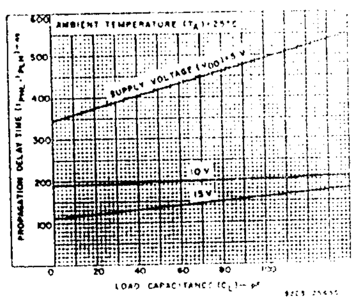


Fig. 10 – Clock-to parallel output propagation delay vs C_L.

Semiconductor

M555/LM555C Timer

neral Description

LM555 is a highly stable device for generating ... time delays or oscillation. Additional terminals ... provided for triggering or resetting if desired. In the ... delay mode of operation, the time is precisely con... by one external resistor and capacitor. For astable ... as an oscillator, the free running frequency and ... cycle are accurately controlled with two external ... and one capacitor. The circuit may be triggered ... reset on falling waveforms, and the output circuit ... source or sink up to 200 mA or drive TTL circuits.

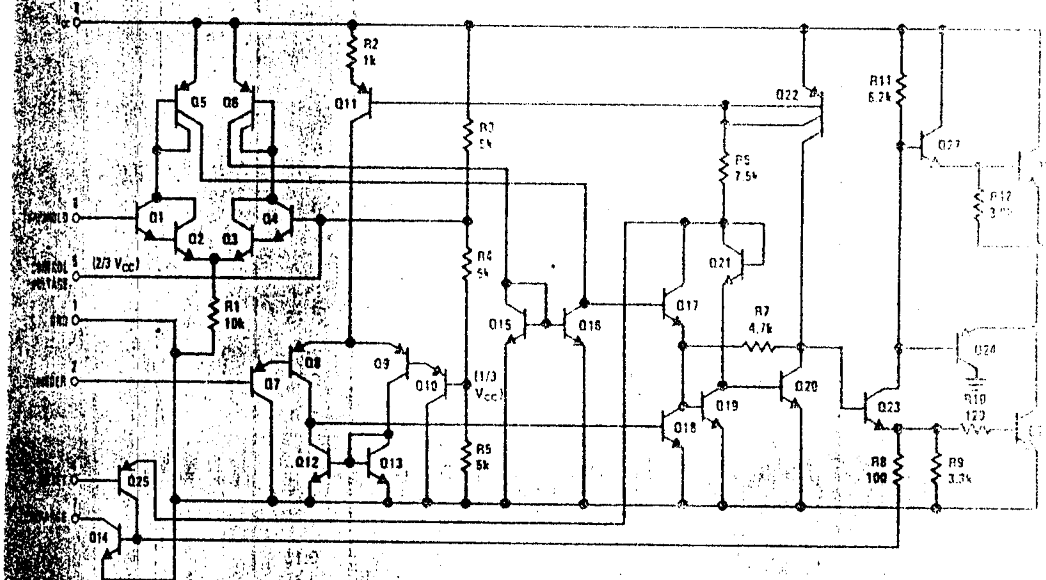
Features

- Direct replacement for SE555/NE555
- Timing from microseconds through hours
- Operates in both astable and monostable modes
- Adjustable duty cycle
- Output can source or sink 200 mA
- Output and supply TTL compatible
- Temperature stability better than 0.005% ...
- Normally on and normally off output

Applications

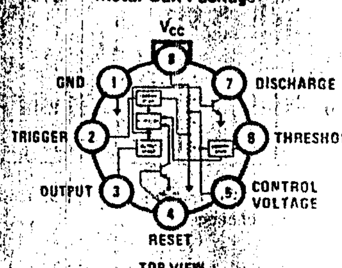
- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Linear ramp generator

Schematic Diagram



Connection Diagrams

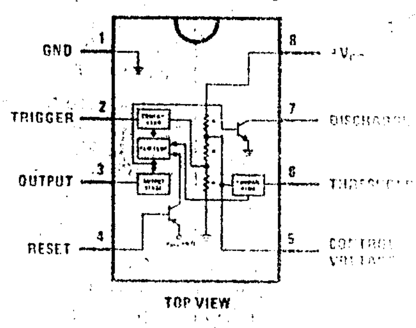
Metal Can Package



TOP VIEW

Order Number LM555H, LM555CH
See NS Package H08C

Dual-In-Line Package

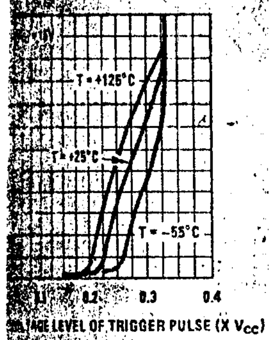


TOP VIEW

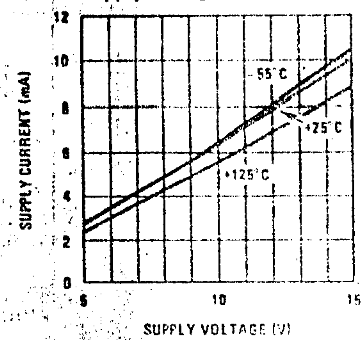
Order Number LM555CN
See NS Package N08B
Order Number LM555J or LM555CJ
See NS Package J08A

Performance Characteristics

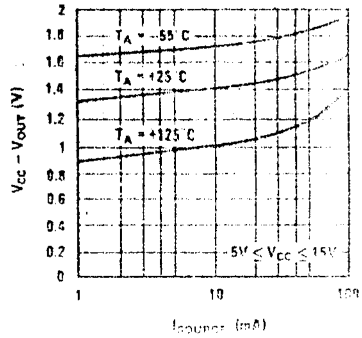
Pulse Width
for Triggering



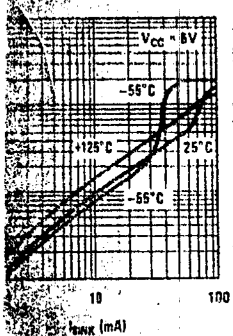
Supply Current vs Supply Voltage



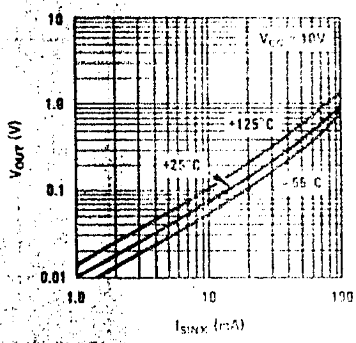
High Output Voltage vs Output Source Current



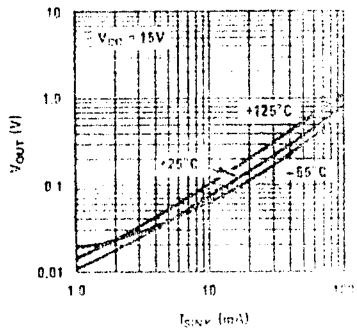
Output Voltage vs
Sink Current



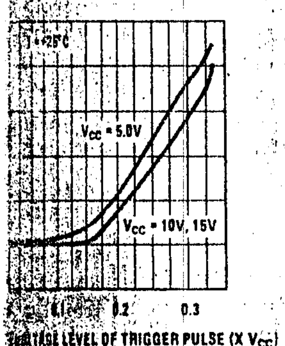
Low Output Voltage vs Output Sink Current



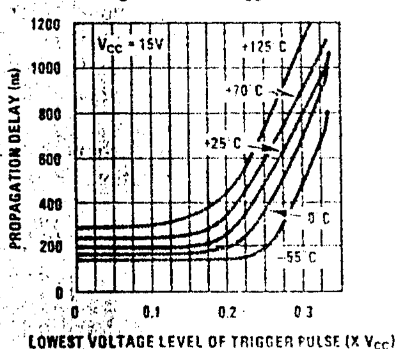
Low Output Voltage vs Output Sink Current



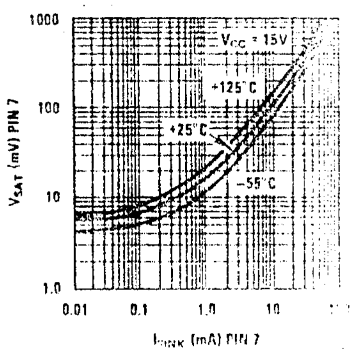
Output Propagation Delay vs
Voltage Level of Trigger Pulse



Output Propagation Delay vs Voltage Level of Trigger Pulse



Discharge Transistor (Pin 7) Voltage vs Sink Current



Discharge Transistor (Pin 7) Voltage vs Sink Current