Ultrasonic Surveillance System

PROJECT REPORT

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Name.. **Roll No.**....................

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This is Bonafide Record of the Project Work Titled

'ULTRASONIC SURVEILLANCE SYSTEM'

Done By

Mr. ....

During the Year 1992 - 1993

In partial Fulfilment of the requirements for the award of the Degree of Bachelor of Engineering in Electronics and Communication Engineering Branch of Bharathiar University, Coimbatore

Coimbatore.

Date :

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Submitted for the University Examination held on ....

.... Internal Examiner

.... External Examiner

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SYNOPSIS

We have attempted this project to reflect the need for a good, efficient and yet a compact surveillance system.Though the principle of Ultrosonics has been used for atleast 4 decades it finds use only in large industrial and medical fields.

Hence we sincerely hope that this project will mirror the usage of the Ultrasonic Waves whose vast potential has yet not been tapped to yet another simple but useful application.

CONTENTS

ULTRASONIC SURVEILLANCE SYSTEM

The Ultrasonic Surveillance System utilizes the property of the Ultrasonic Waves to calculate the distance of the object from the USS unit. A clock pluse generator is utilized which runs the counter at a frequency synchronous to the signal transmitted by the transduction element. At the instant of transmission the counter is activated by a clock pulse of frequency 17.05 KHz.

The Piezo Electric Crystal in the sender unit is excited by a schmitt trigger ckt. This crystal transmits sound of fequency at 40 KHz whenever an electrical signal is applied to it. These sound waves whose frequency lies above the audible range (0-20 KHz) are called Ultrasonic Waves.

The time dependant sensitive receiving unit picks up these Ultrasonic Waves during their return path. When these waves are picked up the bistable stage gets reset and thereby stopping the counting process.

Now the LCD display reads the distance between the object and the USS unit. This is done counting the number of clock pulses counted between the onset of the burst and the sensing of the echo, namely the waves reflected back by the object and this count gives a direct measure of the distance between the object and the USS unit.

Meanwhile the control unit checks whether the distance lies within a particular range and if so switches on an alarm or a buzzer thereby warning the user. Since this unit utilizes a 12 V supply it can find applications in automobiles and in industrial fields such as in Conveyor Belts.

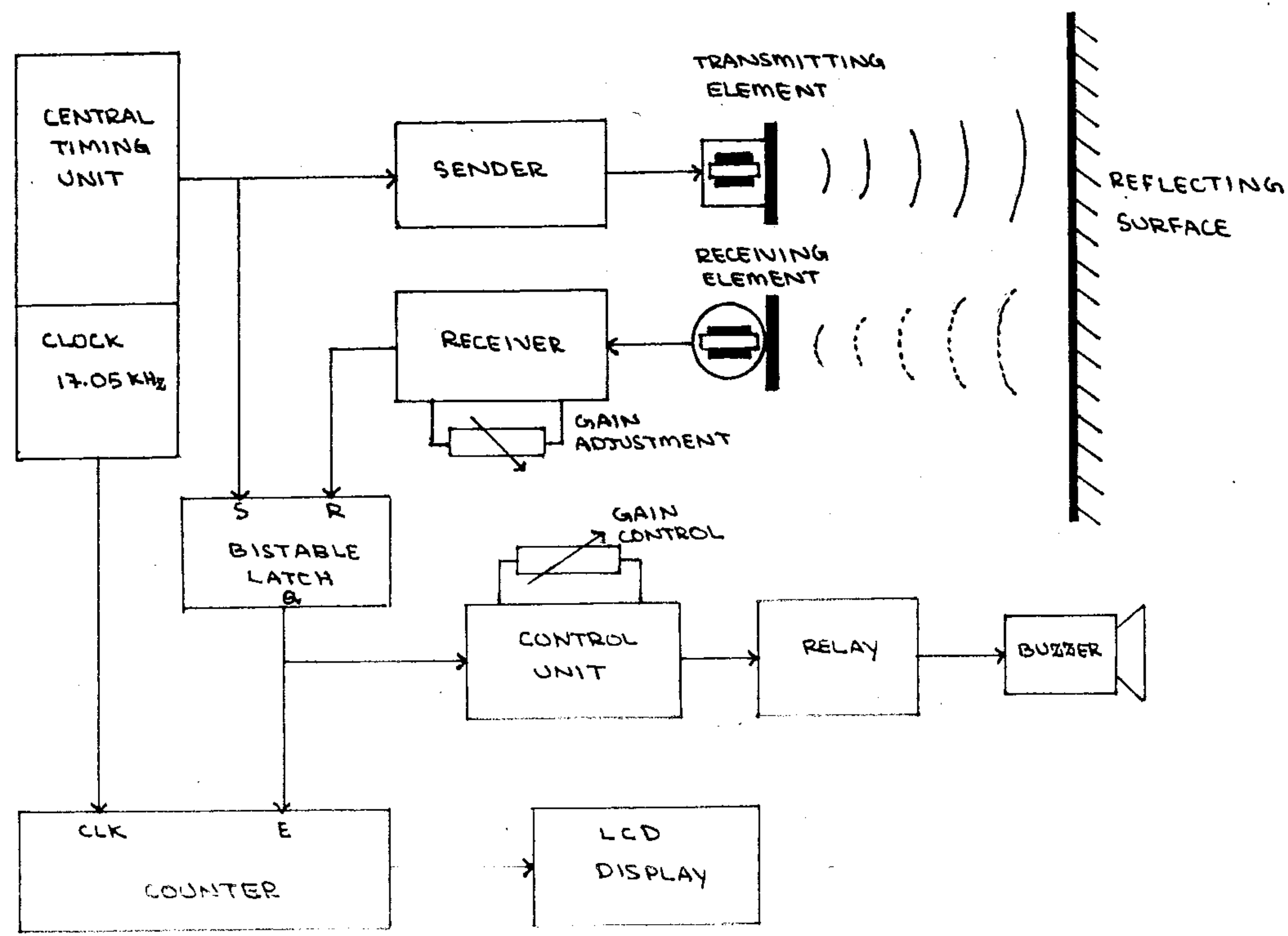


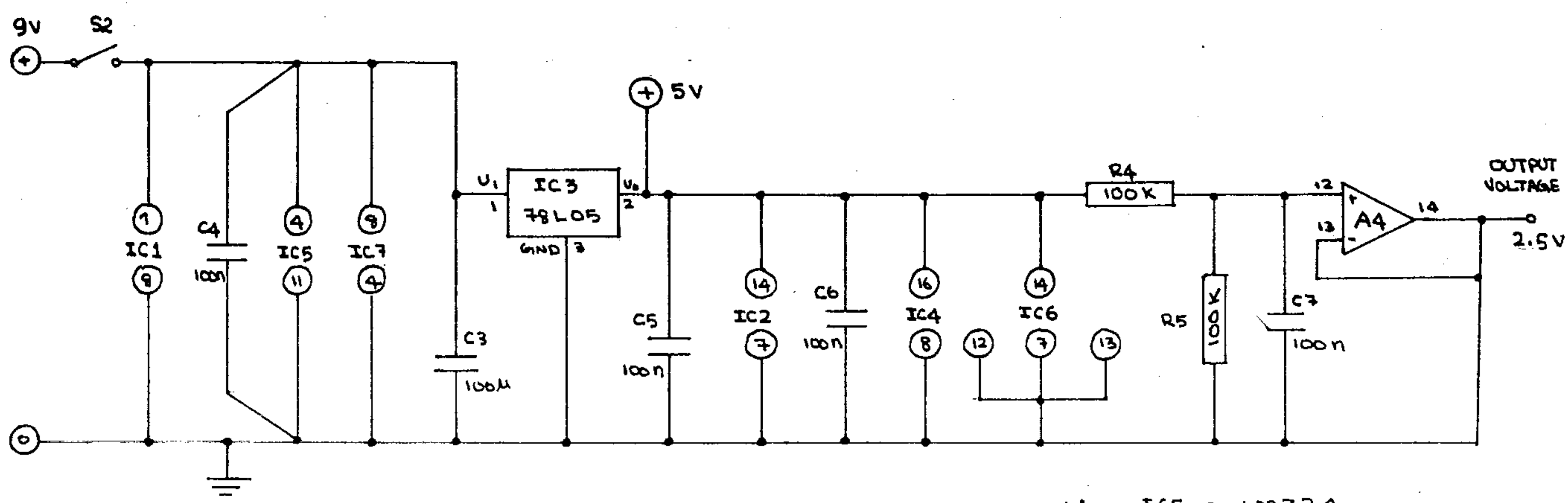
Fig: FUNCTIONAL BLOCK OF ULTRASONIC SURVEILLANCE SYSTEM

2.1 POWER SUPPLY UNIT

A 9 volt Battery is utilized to power the circuitry. The power is fed to one of the terminals of the voltage regulation chip in the 78 L 05 chip. The output of the chip is a constant voltage of 5 volts. This 5 volts is fed to a buffer amplifier designated as A4.The Buffer amplifier is used so as to reduce the input impedance.

The Buffer amplifier is a unit gain non-inverting amplifier. Thus the output of the buffer will be the same 5 volts. This desired sampled voltage is supplied to the non-inverting terminal of the comparator Op-amp A2. The power input to the circuitry should never fall below 7 volts.

Thus the battery,after a long period, will naturally become weak. Once this happens the voltage supplied by it will become low and failure of the battery is at once indicated by the LCD display. Once this happens the battery supply should be replaced.



A4 = IC5 = LM324

IC1 = 4049

IC2 = 4093

IC4 = 4060

IC5 = LM 324.

IC6 = 4030

IC7 = LM 393

Fig: POWER SUPPLY UNIT

2.2 VOLTAGE LEVELLING CIRCUIT

This circuit mainly comprises of an operational amplifier which acts as a comparator. The voltage levelling circuit is utilized for the operators information sake. It is the circuitry that enables the LOW-BAT signal light on the LCD screen to glow when the power from the Battery has dropped below requisite value, thus indicating the necessity for a replacement in the battery.

The operation of this is simple as it takes into account the principle of Comparison. The non-inverting terminal of the op-amp is connected to the output of the voltage regulator which is a contant 5 volts. The inverting terminal of the Op-amp is connected to the supply voltage of 9 V. A voltage divider circuit comprising of resistors R 16 and R 17 are present which drop the Powers' input voltage of 9 V to 5 V. Thus the two inputs of the Comparator A 21 are 5 volts and hence naturally the output of Comparator will be Zero. The input supply voltage is allowed to decrease upto a maximum value of 7 V after which the low-bat indication on the screw will glow.This is because the output of the

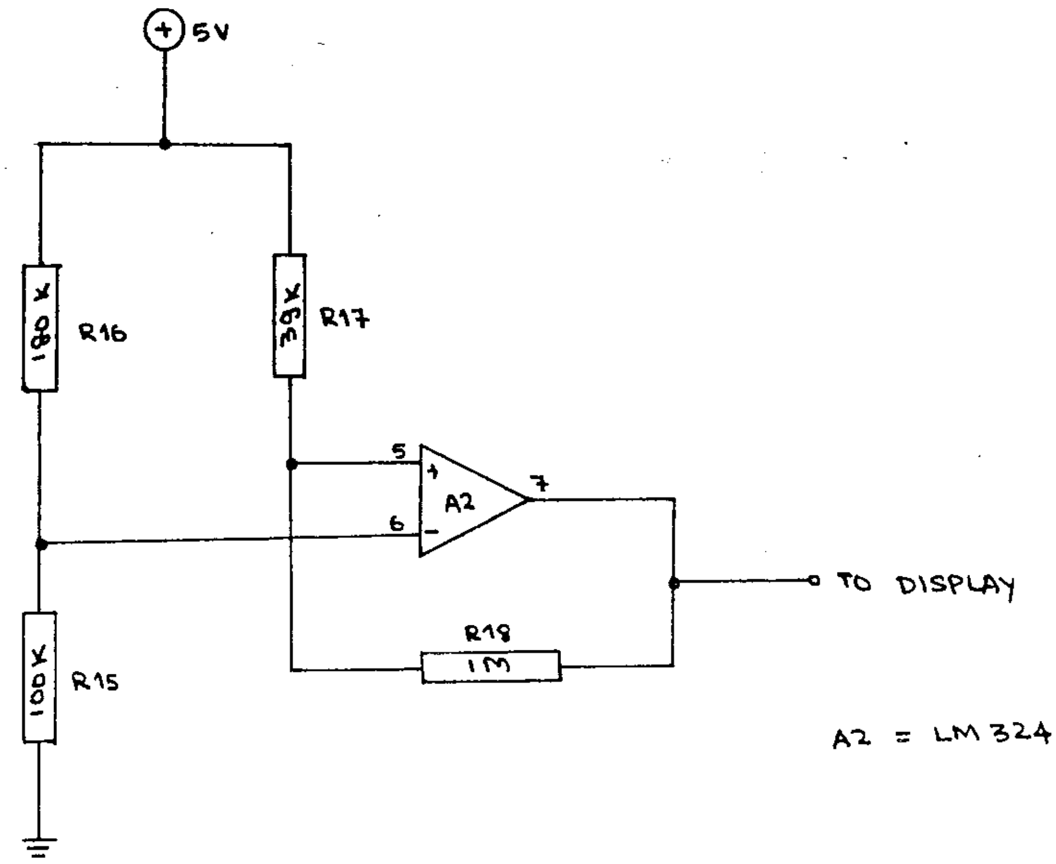


Fig: VOLTAGE LEVELLING CIRCUIT

Comparator is fed to LCD Screen is Nand gate which will have an output high when only both its inputs are high. As one input is from the 5 V supply and the other is from Comparator, the desired effect occurs only when the Comparator output is high even this happens only when the input voltage from the battery falls from its value of 9 V but drop upto 7 V is accepted after which the output goes high and hence enables the Nand gate resulting in the low-bat to start glowing.

2.3 ULTRASONIC WAVE GENERATOR

The main component of the sender unit is the tranmitter element itself. A piezo-electric crystal has the property such that whenever electrical pulses are applied to them they are stimulated. Due to this stimulation the Crystal starts vibrating and produces sound like an ordinary loudspeaker. But the vibrations are that of such high period that the sound produced is of very high frequency in the order of a few kilo hetz to as high as Megahertz.

When the frequency of the sound waves are found to be above twenty kilohertz we are brought into a new concept namely the field of ultrasonics. This ulrasonic wave is nothing but sound waves above the

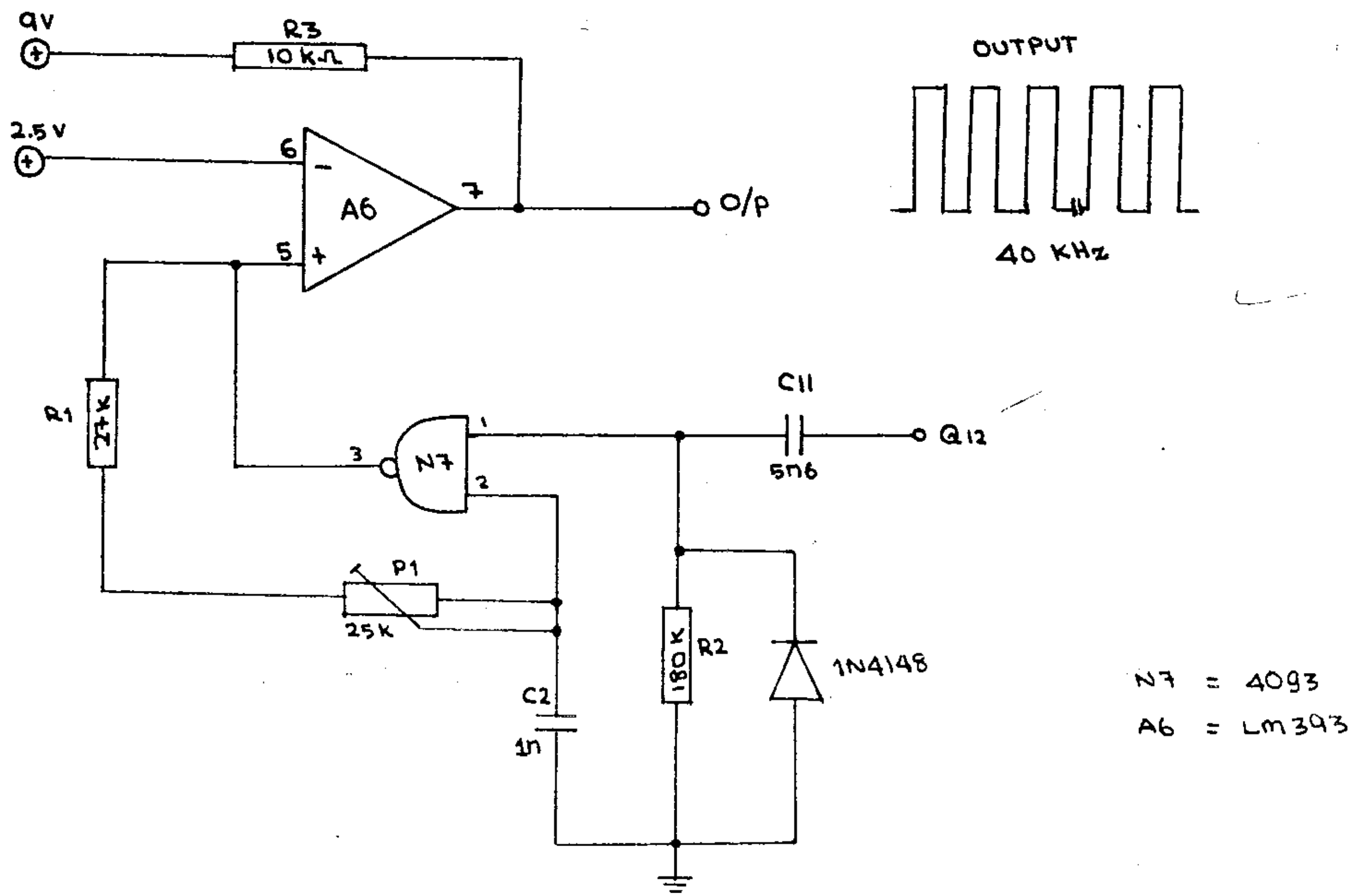


Fig: ULTRASONIC WAVE GENERATOR

audible range ie., 20 KHz. These ultrasonic waves are highly penetrative in a medium and are reflected by any material not belonging to that medium. This is the basic function of the Ultrasonic Wave Generator.

2.4 SENDER UNIT

The sender unit comprises of a schmitt trigger circuit a wave shaping circuit which are used alongwith the piezo-electric crystal so as to produce a wave of desired frequency. A comparator Op-amp designated by A 6 is used to whose non-inverting terminal the positive on going schmitt trigger is connected. To the inverting terminal the input signal is applied. Hence the op-amp compares these signals fix to it and produces the desired wave whose frequency is fixed by the design parameters of P1, which is a preset or a potentiometer whose range is 2K and capacitor C2 designed to 1nf.

The potentiometer is hence a variable quantity and this factor is utilized in order to attain the signal of value 40 KHz. This value of frequency is desired for the signal so that the transduction elements will also Oscillate at this frequency and hence will produce the ultrasonic waves of frequency 40 KHz. This circuitry acts as the Oscillaor Circuitry. The schmitt trigger is operated at its threshold voltage. The LTP points of the schmitt trigger are varied by the use of the potentiometer. This is done so as to attain the resonance frequency.

This signal shaping circuitry is made up of buffer amplifiers. It consists of four paired CMOS Buffers. The Output stage is actually a full bridge which causes the doubling of the effective voltage across the element. The capacitor C1, designed as 220 nf is used to block the DC component of the output signal during pauses in emission. To obtain bursts of signal by the transducer at maximum energy ie., IC 4049 is connected directly to the 9 volts battery. The remainder of the circuit is connected to the output of the regulator and hence operates at 5 V.

The transduction element as stated previously is a transducer made of a piezo-electric crystal. The input to the transduction element is a pulsating signal. The crystal hence undergoes contraction and rarifaction at a period similar to the input applied to it. Thus the sound waves produced are of ultrasonic nature.

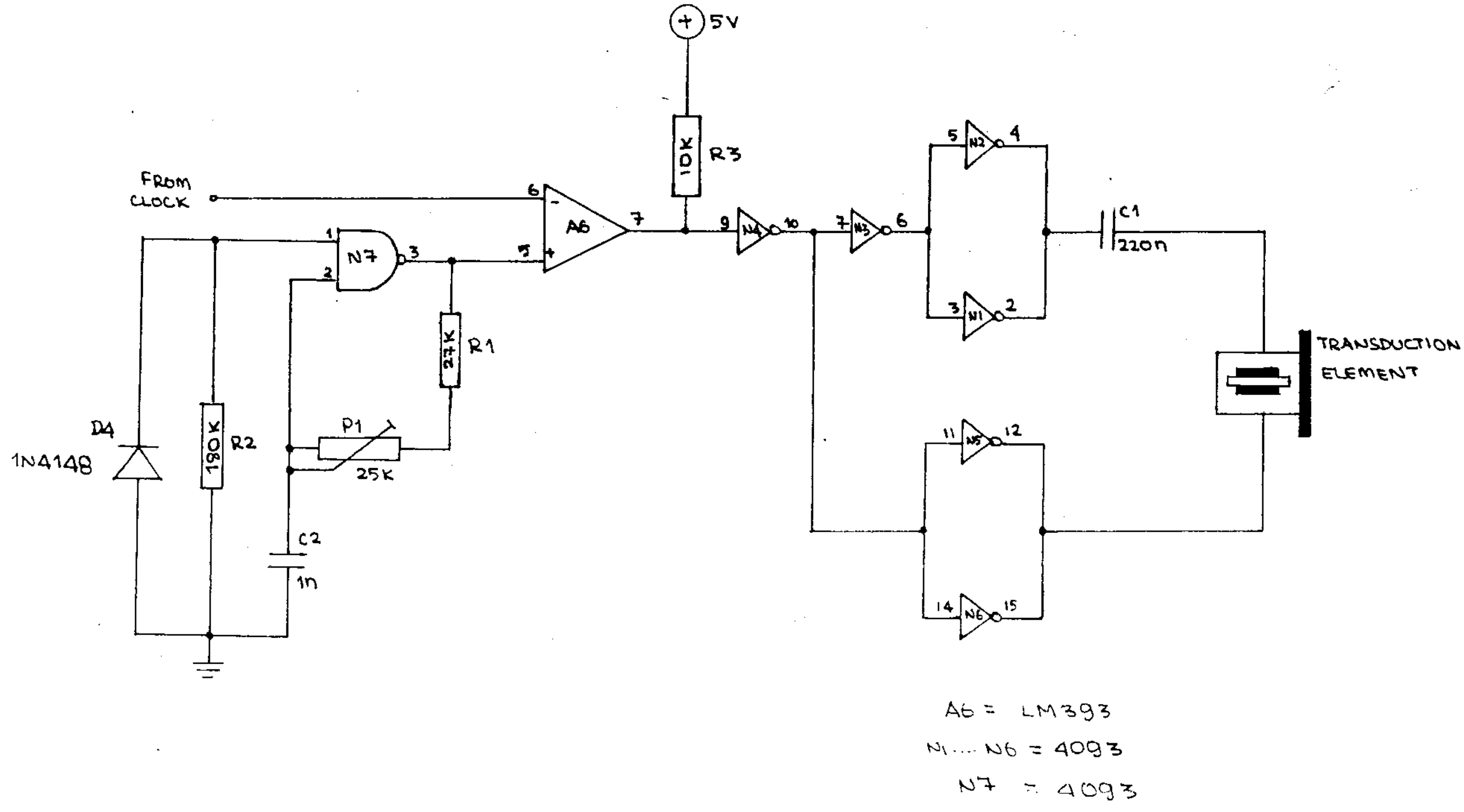


Fig: SENDER UNIT

2.5 DRIVE AMPLIFIER

Inverters N1.....N6 are playing the role of drive amplifier.The input to this circuit is 40 KHz pulse.

The inpulse pulse is branched between two path i.e., one inverted and other non-inverted. N1 and N2 are placed parallel in one path and N5 and N6 are placed parallel in the other path. This is to reduce the resistance in the path of the pulse to the transmitter.

Here, for each one input pulse, we are giving two pulses to the transmitter. Because we are reducing the path resistance and also we are giving two poulses simultaneously to the transmitter, there will be a two fold current amplification of the input pulse. Capacitor C, is there to avoid the DC signals entering the transmitter.

2.6 RECEIVER UNIT

The sensing unit or the receiver unit consists of piezo-electric transducer and an amplifier designated as A3. The sensing transducer is similar to the trans-mitting transducer is constructed but the working of it is converse to that of the transmitting antenna. Here once the ultrasound waves transmitted by

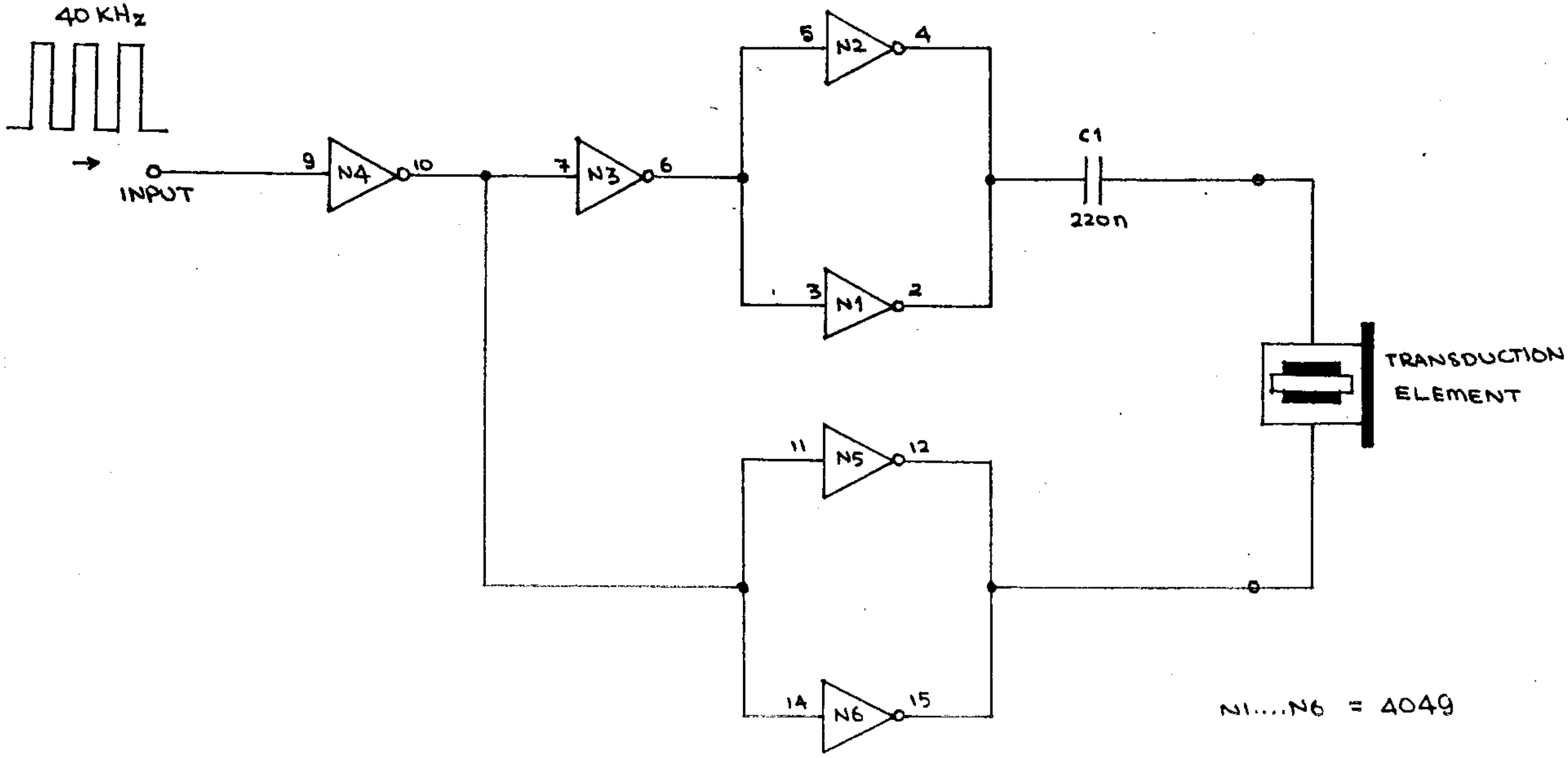


Fig: DRIVE AMPLIFIER AND TRANSMITTER

the transmitter are reflected by the object they come into contact and are hence picked up by the receiver transducer.

The receiver transducer which is also a piezo-electric crystal utilizes the converse principle namely that when external, usually in the form of rarifcation and contractions, acts on it the transducer generates an electric signal whose value corresponds to the incident pressure wave in the form of the sound waves.

The principle is similar to that of a microphone only that this transducer picks up signals of frequency in the ultrasonic range. The sensing transducer has a time dependent sensitivity.That is to say that as time elapses after the system has been operated the sensitivity of the receiving transducer increases.

This signals which are arriving at the receiver at the shortest interval will be received with a sensing element having a minimum sensitivity. But the power of the signal will be high as it has not travelled much of a distance to have grown weaker in strength. The received signal which a pulsating d.c, is applied to the op-amp designated as A3. This receiver amplifier has a gain of 33 dB derived from the relation:

Gain = 20 log R8/R9 dB

Where the designed value of R 8 is 100 K ohms and R 9 is 2 K ohm. This amplified is AC coupled as it has been seen that the transducer has a very high d.c resistance Thus the applied input voltage does not get amplified when the receiver is not functioning as it is blocked off by the transducer.

The resistor R 14 serves to minimize the offset voltage caused by the input bias current . A minimum offset voltage at the output is necessary as it alongwith the input offset voltage of A5 determines the sensitivity of the transducer which has been already explained to be a time dependent quantity.

The senitivity of the transducer is matched to the ambient conditions by adjusting the potentiometer designed to be 100 M ohm. The output of the sensing amplifier is fed to the bistable unit which sets and resets the counter by which the distance measurement is achieved.

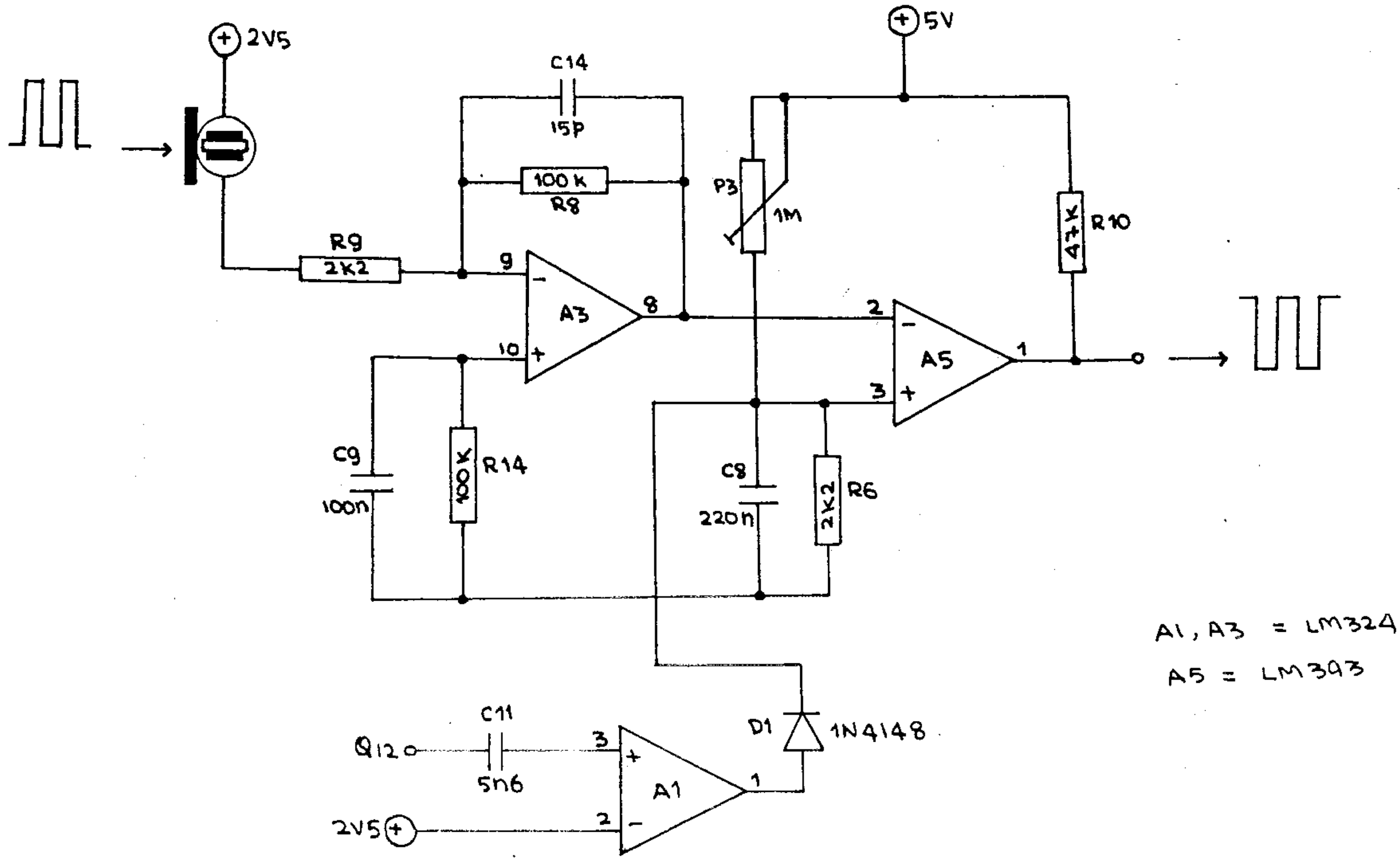


Fig : RECEIVER UNIT

2.7. CENTRAL TIMING UNIT

The reference timing unit is the heart of the whole system.It is at this region the clock pulse to drive the counter and the trigger or toggling pulses are produced which are utilised to enable the counter into functioning. The reference timing unit is built up of two sections namely

(i) Binary Clock Circuit

(ii) Bistable Unit

These divisions will be explained in detail separately.

The reference timing unit is stimulated that is to say excited by the pressing by the pressing of the switch S1 which is a push-to-make button switch. Once the triggering takes place the clock pulse generator is stimulated. This unit comprises of a preset P2 which is nothing but a rheostat. This being a variable quantity is adjusted so as to attain the desired clock pulse. The signal namely clock pulse of desired frequency is fed to the count pins of the counter. Thus the counter counts at the frequency of the clock pulse generated by this unit.

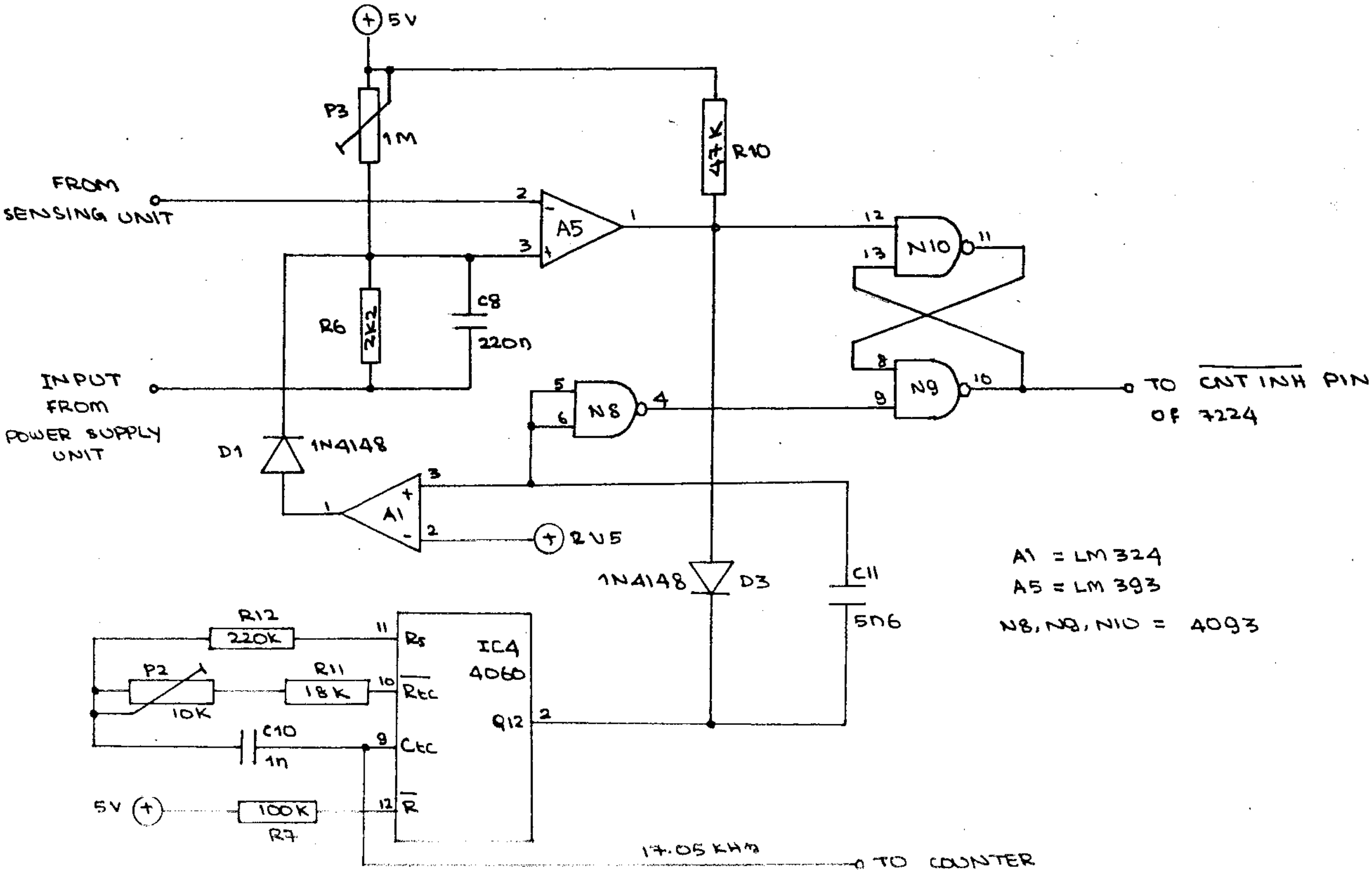


Fig: CENTRAL TIMING UNIT

The output of Q12 goes high twice in a second when the switch S1 is pressed. When this Q 12 goes high it gives a high on one terminal of the op-amp. A1 is the input voltage. The output of the comparator is the difference value. This value is used to toggle the bistable stage. To prevent toggling at other stages by the input signal we make use of the R 6-C8 connection. This drops the voltage so that the output of A1 is onl;y taken to consideration. The Bistable state will start the counter when the sound waves are transmitted and when the receiver picks up the waves on the return the counter is stopped. The actual working will be considered more deeply under their respective heading.

2.8. INTERNAL CLOCK PULSE GENERATOR

This unit is the region where the clock pulse necessary for the counter to perform in synchronism with the frequency of the signal being transmitted by the transducer. The Binary clock circuit comprises of the chip 4060 alongwith a resistor, capacitor set up. The resistor used is a preset which is nothing but a rheostat. The rheostat is adjusted so that the frequency generated is of the value 17.05 KHz. The frequency is obtained from the formula:

$$f = 1/2X3.14\ RC$$

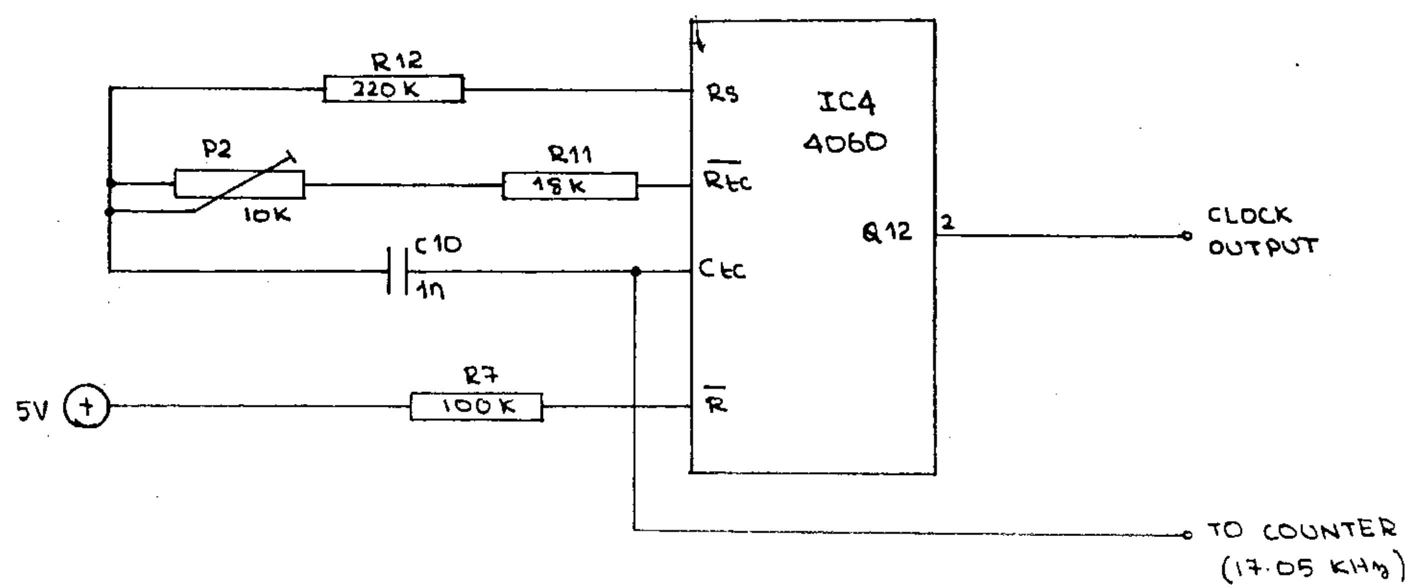


Fig : INTERNAL CLOCK PULSE GENERATOR

As the capacitor is a constant value the frequency is varied by adjusting the rheostat so as to obtain the desired value of frequency. This signal clock pulse has a time period of 0.3 ns and hence on pressing the switch due to this period manupulationg of the clock there will be a burst of twelve pulses in the duration of 0.3 ns of frequency designed as 40 KHz.

Hence the output Q 12 of the binary circuit is found to go to high twice every second.

When Q 12 goes high it will be seen that the output of the capacitor will be of requisite value which is applied to one terminal of the amplifier A 5.

The inverting terminal of the same is the signal picked up by the receiving transducer and amplified by the amplifier A 3. During emission the output of A1 is high which via D1, causes the threshold of comparator A 5 to be raised to a level that makes triggering by cross talk impossible.

2.9 BISTABLE LATCH CIRCUITRY

This crcuitry forms one block of the reference timing unit. The bistable circuit is comprised of nand gates alongwith an amplifier comparator, which compares the received signal after amplification with the clock pulse reference signal.

At the start of emission, bistable N9 and N10 is set. This disables the count inhibit input of IC5, which there upon commences counting the 17.05 KHz pulses applied to 32 by IC 4.

The receiver input amplifier has a gain of about 33 dB. The amplifier is AC coupled, because the sensing element has a virtually infinitely big DC resistance. The input offset voltage is hence not amplified further (more R14) reduces the offset voltage to a minimum value which is anyway necessary as it along with the offset voltage of amplifier A1 determines the sensitivity of the transducer which is a time dependant quantity. This is realised by A1 lowering of the trigger level of A5 via time constant R6-C8. The maximum sensitivity may be matched to the ambient conditions by P3.

When an echo is received, the output of A5 goes low, which causes the bistable to be reset, and this in turn disables the clock of IC5. At the same time a short negative pulse is applied via R13-C12 and N11 to pins 34 ie.,STORE, which results in the transfer of the counter state to the output latch of ICs. Gate N11 merely

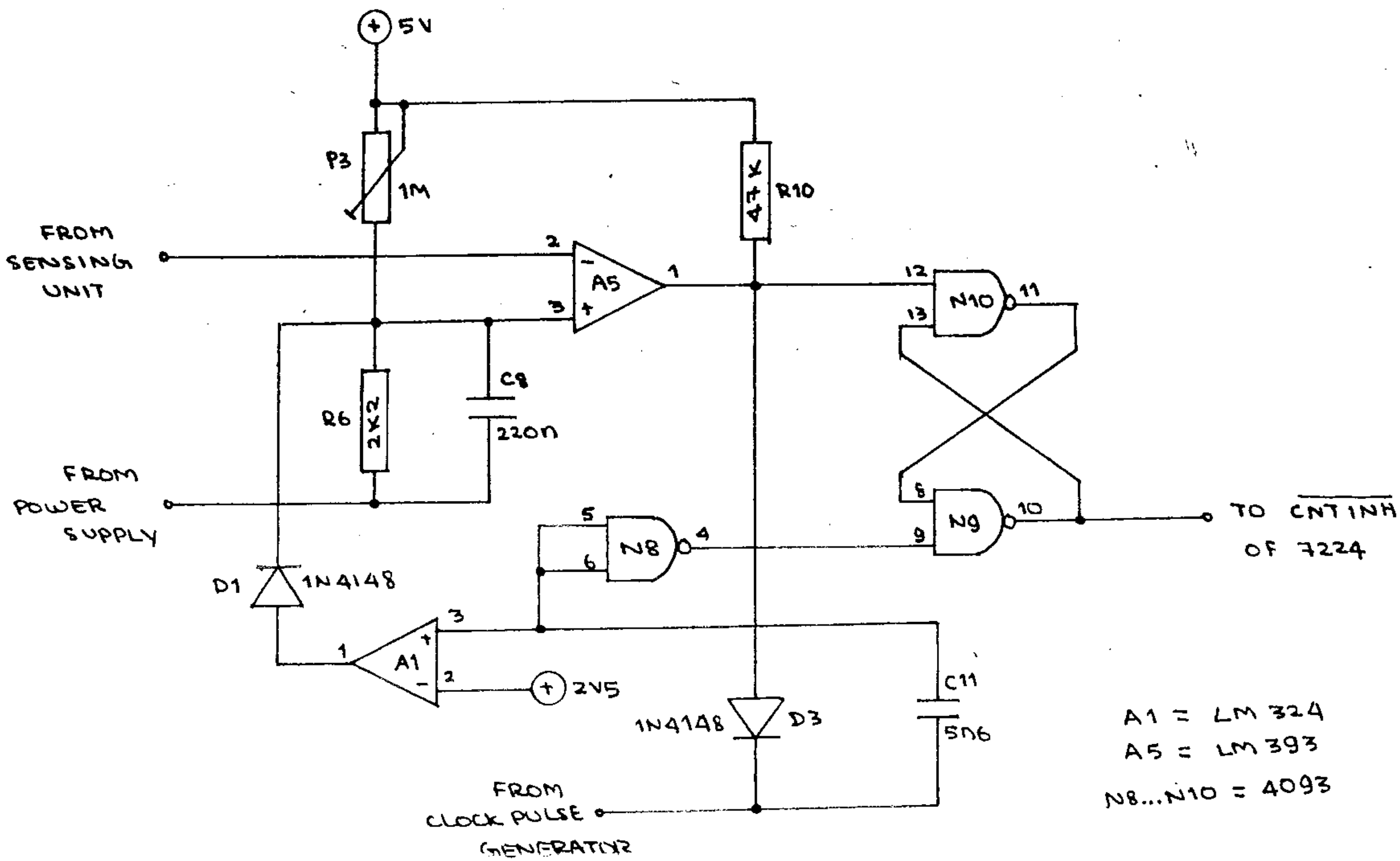


Fig: BISTABLE LATCH CIRCUITRY

buffers the low impedance store input. When the Q12 output of IC4 goes low, the counter in IC5 is reset, and the circuit is ready for the next measurement.of Q12 goes low in the absence of an echo, the counter is still reset, as is the bistable (via D3). The display will then read 0.00 to indicate an abortive measurement. Hence another pulse will have to be sent in order to study the distance of the desired object.

2.10 CONTROL UNIT

Control Unit plays a main role in the ultrasonic surveillance system. This unit consists of a comparator and a switching circuitary.

The signal which is reflected back from the object is received by the receiver and this signal is given as input to the comparator. Here, the amplitude of the received signal is compared with a threshold level. once the received signal is grater than or equal to the threshold level, a high level output is given as the comparator output. This signal now turns a transistor ON and which in turn makes a relay to operate. This relay in turn turns a buzzer to operate, which acts as an indicator that there is some obstacle in front of the system. There is a potentiometer. By varying its value

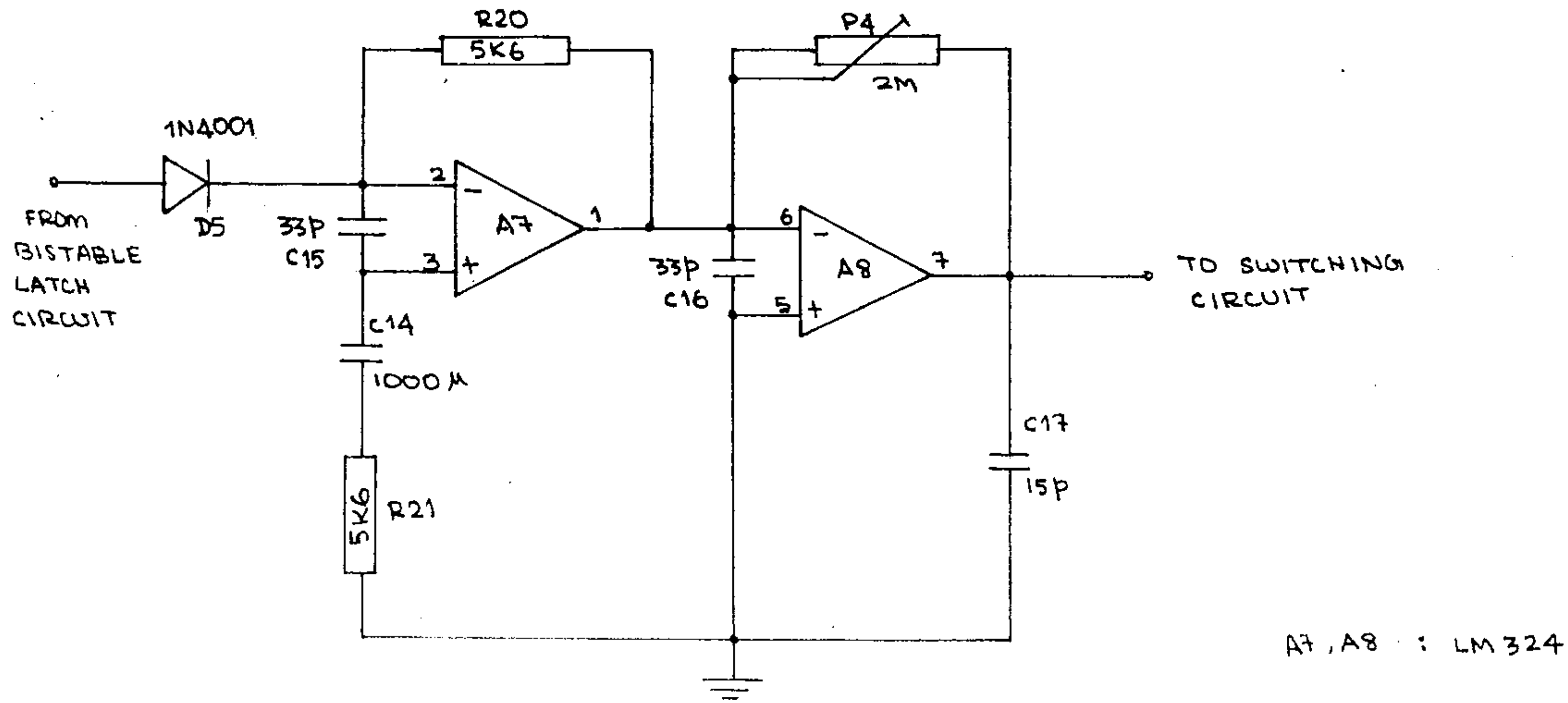


Fig : CONTROL UNIT

we can vary the gain of the surveillance system and hence the range where we are looking for obstacle.

2.11 SWITCHING CIRCUITARY

This circuit consists of a transistor, whose output is connected to relay RL1.

The high level output from the comparator will make this transistor ON. The output from the transistor makes the N/O key of RL1 to close. This gives a path to the buzzer and hence buzzer gives the indication.

In this circuit, we have a capacitor 'c' which is used as 'spike quencher'. The spike may arise due to the a.c signal input which may occur rarely. Here is also a damper diode 'D'. Both 'C' and 'D' are placed parallel to each other and also with RL1.

2,12 SOURCE BATTERY LEVEL MONITOR

The battery voltage is monitored by N13 when it drops to about 7 V, the gate's function changes from non-inverting to inverting which causes the LO BAT segment of the LCD to light. Flickering of this is prevented by the hysteresis of around 200 mV provided by R18.

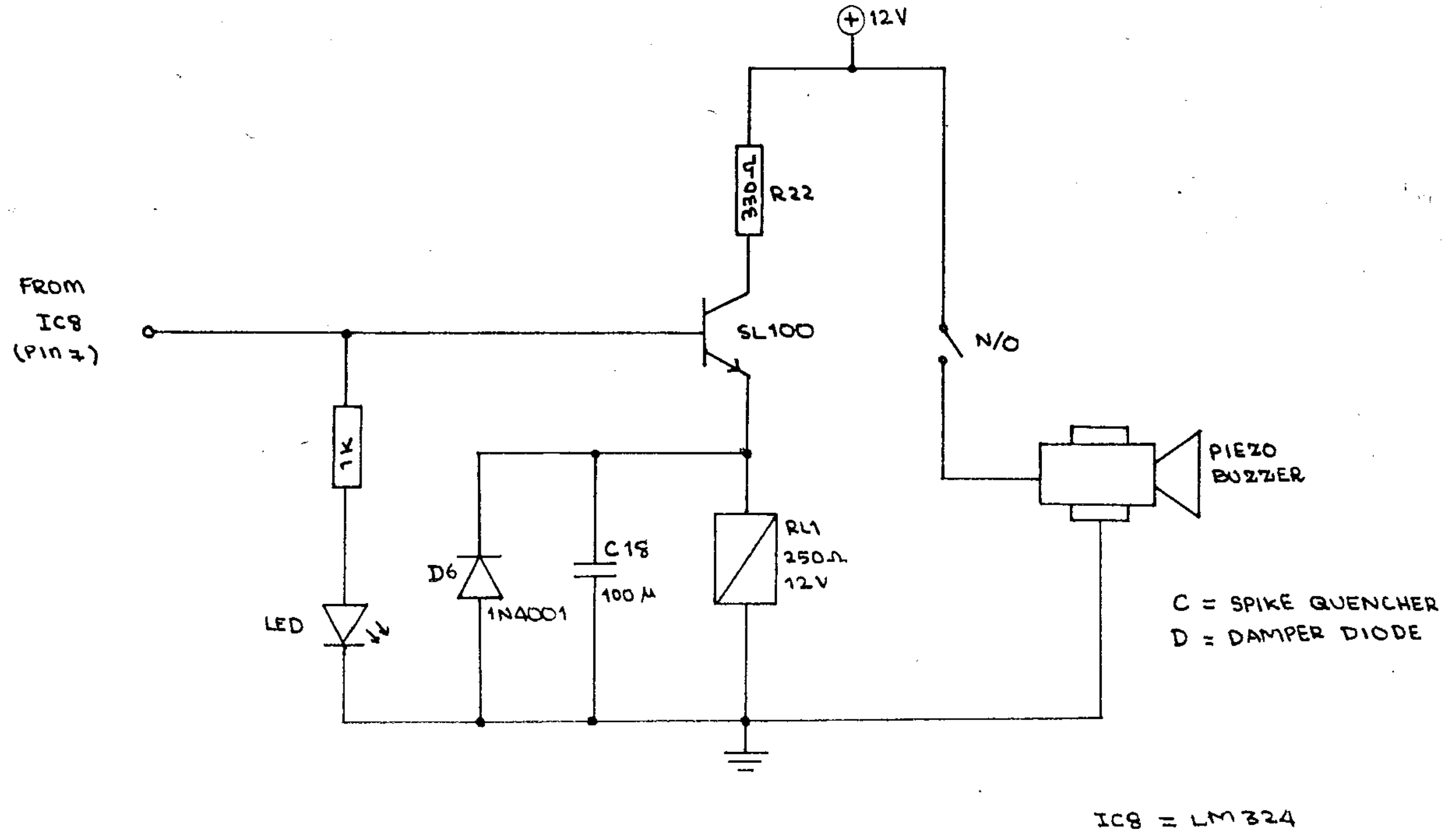


Fig : SWITCHING CIRCUITORY

3.1 OPERATIONAL AMPLIFIERS

The Operational Amplifier is today the most widely used analog sub assembly. It is safe to say that its basic properties and applications are sufficiently understood by most circuit designers and builders.

DEFIINTIONS OF PARAMETERS

Absolute Maximum Differential Voltage

Undermost operating conditions, feed back maintains the error voltage between inputs to nearly zero volts. However, in some applications such as voltage comparator, the voltage between the inputs can become large. This specification defines the maximum voltage which can be applied between inputs without causing permanent damage to the amplifier.

Common Mode Rejection

An ideal operational amplifier responds only to the difference voltage between inputs (e+ _ e-) and produces no output for a common mode voltage, that is, when both inputs are at the same potential. However, due to slightly differnt gains between the plus and minus inputs or variations in offset voltage as a function of common mode level, common mode input voltage are not eliminated at the output. If the output error voltage, due to a known magnitude of common mode voltage, is referred to the input (dividing by the closed loop gain), it reflects the equivalent common mode eror voltage between the inputs. Common mode rejection ratio (CMRR is defined as the ratio of common mode voltage to the resulting common mode error voltage. Common mode rejection is often expressed logarithmically.

CMR (in dB) = 20 log 10 (CMRR)

Common -Mode Voltage, Maximum

For differential input amplifiers, the voltage at both inputs can swing about (power supply common) level, common mode voltage is defined as any voltage is defined as any voltage (above or below ground) that could be observed at both inputs. The maximum common-mode voltage is defined as that voltage which will produce less than a specified value of common-mode error.

Full Power Response

The large signal and small signal response characteristics of operational amplifiers differ substantially. An amplifiers output will not respond to large signal changes as fast as the small signal bandwidth characteristics would predict, primarily because of slow rate limiting in the output stages. Full Power response is specified in two ways - full linear response and full peak response. Full linear response is specified in terms of the maximum frequency at unity closed loop gain, for which a sinusoidal input signal will produce full output at rated load without exceeding a pre-dertermined distortion level.

The other frequency response is the maximum frequency at which full output swing may e obtained irrespective of distortion. This is termed "Full Power Response".

Initial Bias Current

Bias current is defined as the current required at either input from an infinite source impendence to drive the output to zero (assuming zero common-mode voltage). For differential Amplifiers, bias current is present at both the negative and the positive input. All Analog devices specifications pertain to the larger of the two not the average. For single ended amplifiers (ie., chopper types) bias current refers to the current at the input terminal.

Initial Difference Current

Difference current is defined as the difference between the bias currents as the two inputs. The input circuitry of differential amplifiers is generally symmetrical, so that bias currents at both inputs tend to be equal and tend to track with changes in temperature and supply voltage. Therefore, difference current is often about 0.1 times the bias current at either input, assuming that initial bias current at either input, assuming that initial bias current has not been conpensated at the Input terminals. For amplifiers in which bias currents track, it is often possible to reduce voltage errors due to bias current and its variations by the use of equal resistance loads at both inputs.

Input Impedance

Differential input Impedance is defined as the impedance between the two input terminals at +25 C , assuming that the error voltage is nulled or very near zero volts. To a first approximation, dynamic impedance can be respresented by a capacitor in parallel with a register.

Common-mode impedance, expressed as a resistance in parallel with a capacitance, it defined as the impedance between each input and Power Supply Common, specified at + 25°C. Common mode Impedence is a non-linear function of both temperature and common mode voltage for FET input Amplifiers, common mode resistance is reduced by a factor of two for each 10 of temperature rise.

Input Offset Voltage

Offset voltage is defined as the voltage required at the input from Zero source impedence to drive the output to zero, its magnitude is measured by closing the loop (using low values of resistance to establish a large fixed gain measuring the amplified error at the output, and dividing the measured value by the gain.

The initial offset voltage is specified at +25 C and rated supply voltage. In most amplifiers, provisions are made to adjust initial offset to zero with an external trim potentiometer.

Open Loop Gain

Open loop gain is defined as the ratio of a change of output voltage to the voltage applied between the amplifier inputs to produce the change. Gain is specified at dc. In many applications, the frequency dependence of gain is important; For this reason, the typical open look gain as a fuction of frequency is published for each amplifier type.

Overload Recovery

Overload Recovery is defined as the time required for the output voltage to recover to the rated output voltage from a saturated condition caused by a 50% over drive. Published specifications apply for low impedances and contain the assumption that overload recovery is not degraded by stray capacitance in the feed back network.

Rated Output

Rated Output voltage is minimum peak output voltage which can be obtained at rated current or a specified value of resistive load before clipping or out of space non-linearity occurs. Rated output current is the minimum guaranteed value of current supplied at the rated output voltage for other specified voltage. Load impedences less than the specified value can be used, but the maximum output voltage will decrease, distortion may increase, and the open loop gain will be reduced.

Settling time

Settling time is defined as the time elapsed from the application of a perfect step input to the time when the amplifier output has entered and remained within a specified error band symmetrical about the final value. Settling time, therefore, includes the time required for the signal to propogate through the amplifier, for the amplifier to slew from the initial value, recover from slew-rate limited overload (if it occurs and settle to a given error in the linear range. It may also include a 'long tail ' due to the time required to reach thermal equilibrium or the settling time of compensation circuits. Settling time is usually specified for the condition of unity gain, relatively low impedance levels and no (or a specified value of) capacitive loading, and any specified compensation. A full scale unipolar step into is used and both polarities are tested.

Slew Rate

The slew rate of an amplifier usually in volts per microsecond defines the maximum rate of change of output voltage for a large input step change.

Unity-Gain Small Signal Response

Unity Gain Small Signal Response is the frequency at which the open loop gain falls to N/V or odB under a specified compensation condition 'Small Signal'indicates that in general, it is not possible to obtain large output voltage swing at high frequencies because of distortion due to slew-rate limiting or Signal rectification.

3.2 VELOCITY OF SOUND IN AIR

The velocity of sound, v, in a gas, such as air, for frequencies above 200 Hz is given as,

V=(VP/e)

where f=adiabalic bulk modulus of the gas (1.4 of air)
P=Pressure of the gas in Pa (air pressure at sea level is (1.01325 x 10 exp 6 Pa)
I=Density of the gas in kgm exp -3 (of air =1.29 kgm exp -3)

If a mole of air has a mass M and a volume V the density is M/V and the velocity of round V is,

V= (VP/I = (PV/M)

but PV=RT where R is the molar constant and T is the absolute temperature.

Therefore, V = (RT/M)

Since V,M and R are constants for a given gas, it follows that the velocity of sound in a gas is independant of the pressure if the temperature remains constant. It also follows that the velocity of sound is proportional to the square root of its absolute temperature. Thus if the velocity at room temperature, 20 C=293 K is calculated from,

V=291/273
=342.91 MS exp-1

3.3 PIEZO ELECTRIC OSCILLATOR

In the piezo-electric effect, if one pair of opposite faces of a crystal is subjected to pressure, the other pair of opposite faces develop opposite electric charges. The sign of the charges changes when the faces are subjected to tension instead of pressure.

The converse of piezo-electric effect is also true. According to this, if alternating voltages are applied to one pair of faces, the corresponding changes in the dimensions of the other pair of faces of the crystal are produced.

Thus, when the two opposite faces of a quartz crystal, their faces being cut perpendicular to the optic axis, are subjected to alternating voltage, the other pair of opposite faces experiences stresses and strains. The quartz crystal will continously contract and expand. Elastic vibrations are set up in the crystal.

When the frequency of alternating voltage is equal to the natural frequency of vibration of the crystal or

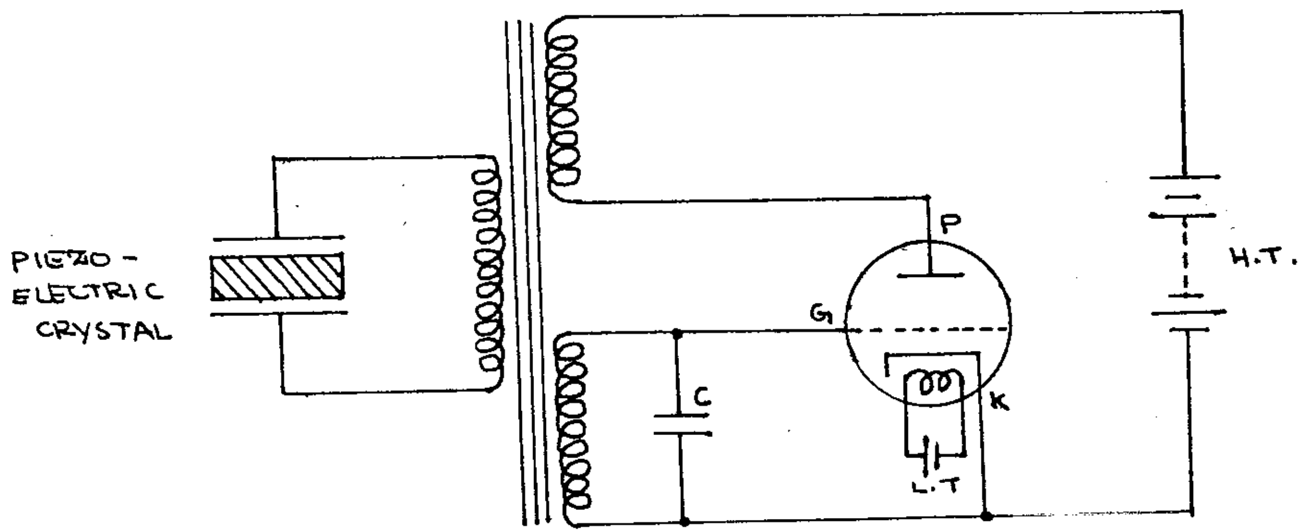


Fig : PIEZO-ELECTRIC OSCILLATOR

its simple higher multiples, the crystal is thrown into resonant vibrations and the amplitude will be large. These vibrations are longitudinal in nature.

3.4 APPLICATIONS OF ULTRASONIC WAVES

Ultrsaonic waves have a large number of practical applications.

1. Depth of Sea

Ultrasonic waves of high frequency are used to determine the depth of the sea. A Piezo-electric quartz oscillator is used. The crystal is placed between two metal plates and the plates are connected to a spark oscillator, producing damped oscillations. The frequency of damped oscillator is tuned to the natural frequency of the quartz crystal which itself acts as a transmitter and a receiver of the ultrasonic waves. These waves are transmitted towards the bed of the sea. These waves are reflected back by the bed and echo is detected by the crystal itself. The time interval between the emitted signal and the echo is determined with the help of the oscillograph. Using the known values of velocity and the time interval the depth of sea is calculated as,

$$h = (V * t)/2$$

2. Signalling

Ultrasonic waves are used for directional signalling. The frequency of ultrasonic waves is higher than the audible waves. Therefore, the wave length is small. Due to this factor they can be sent in the form of short beams. If a crystal, in the form of a disc of various r, is used the angle of cone containing these waves is given by

$$\text{Sin } \theta = 0.61/r$$

For small wave lengths 0

3. Heating Effects

When a beam of ultrasonic wave is passed through a substance it gets heated. If ultrasonic waves pass through water at $0^\circ C$, the water can be made to boil.

4. Mechanical Effects

Ultrasonic waves are used to bore holes in steel and other metals or their alloys. Here the drill oscillates with ultrasonic frequency and can bore any hard metal.

5. Crack in Metals

Ultrasonic waves can be used to detect cracks or discontinuity in metal structures. In this case, an emitter and detector of ultrasonic waves are used. The beam is directed towards the metal and the reflected beam is detected by the dector. If there is a crack or discontinuity there will be a rise in energy received by the detector.

6. Formation of Alloys

Alloys are uniform composition are obtained by subjecting the constituents to an ultrasonic beam. The two constituents are well mixed by the ultrasonic wave even though they differ in density.

7. Chemical Effect

Ultrasonic waves act like catalytic agents and accelerate chemical reactions. They bring about a number of chemical changes.

8. Soldering

Aluminium which cannot be soldered by ordinary soldering is soldered by using ultrasonic waves in addition to the solder.

9. Medical Applications

Ultrasonic waves have a large number of applications in the field of medicine. Some of the important are as follows:

a.Neuralgic pain:The affected portion of the body is exposed to ultrasonic waves which produce a soothing massage action and relieves the pain.

b.Arthritis: A small metal head vibrating the frequeny of more that 10 exp 6 hertz is moved over the skin of the patient. These vibrations after passing through the tissues, produce a deep massage action. The patient is relieved of the pain.

c. Broken teeth: Ultrasonic waves are used by dentists for the proper extraction of broken teeth.

d. Bloodless surgery: Ultrasonic waves are used in bloodless surgery. Here the waves are focussed on a sharp instrument and the tissues are destroyed without any loss of blood. Such instruments are used for bloodless brain operations.

10. Sterlization

Ultrasonic waves can destroy unicellular organisms. They are used in the sterlization of water and milk.

Ultrasonic waves are having more and more practical applications in all fields. Active research work is still in progress to study the effect of ultrasonic waves in mechanical, biological, chemical, physical and industrial fields.

3.5 COUNTERS

The ICM 7224 and ICM 7225 devices constitute a family of high performance CMOS 4 1/2 digit counters, including decoders, output latches, display drivers, count inhibit leading zero blanking , and reset circuitry.

The counter section provides direct static counting, guaranteed from DC to 15 MHz, using a 5 V + or - 10% supply over the operating temperature range. At normal ambient temperatures, the devices will typically count upto 25 Mhz. The COUNT input is provided with a schmitt trigger to allow operation in noisy environments and correct counting with slowly changing inputs. These devices also provide count inhibit, store and reset circuitry, which allow a direct interface with an ICM 7207/A, to implement a low cost, low power frequency counter with a minimum component count.

These devices also corporate several features intended to simplify cascading four digit blocks. The carry out put allows the counter to be cascaded, while the leading zero blanking input and output allows correct leading zero blanking between four decade blocks. The back plane driver of the LCD devices may be disabled, allowing the segments to be slaved to another back plane signal necessary when using an 8 or 13 digit single backplane display.

3.6 LIQUID CRYSTAL DISPLAYS

The liquid crystal display has a distinct advantage of having a lower power requirement than the LED. It is typical in the order of microwatt compared to the milli watts for LEDs.It does however require an external or internal light source, and are limited to a temperature range of 0 to 60 C.

A liquid crystal is a material that will flow like a liquid but whose molecular structure has some properties normally associated with solids. The greatest interest is in nematic liquid crystal. The individual molecules have a rod like appearance. The indium oxide conducting surface is tansparent and the incident light will simply pass through the crystal and hence appear clear. If a voltage usually between 6 and 20 V is applied across the conducting surfaces the molecular arrangements is disturbed, with the result that regions will be established with different indices of refraction. The incident light is therefore reflected in different directions at the interface between regions of different indices of refration with the result that the scattered light has a forsted glass appearance.

A digit on LCD display may have the segmented appearance. The black area is actually are cleared conducting surface connected to the terminals below for external control. If the number 2 were required the terminals 8,7,3,4, and 5 would be energised and only those regions would be forsted while the other areas will remain clear.

The field effect are twisted nematic LCD has the same segment appearance and thin layer of encapsulated liquid crystal, but its mode of operation is very different. Similar to the dynamic scattering LCD, the field affect can be operated in the reflective or transmissive mode with an internal source. The internal light source is on the right and the viewer is on the left. Only the vertical component of the entering light on the right can pass through the vertical light polarizer on the right. In the field effect LCD, either the clear conducting surface to the right is chemically etched or an organic film is applied to orient the molecules in the liquid crystal in the vertical plane,parallel to the cell wall. The opposite conducting surface is also treated to ensure that the molecules are 90 out face in the direction shown (horizontal) but still parallel to the cell wall. In between the two walls of the crystal there is a general drift from one polarization to the other. The left hand light polarizer is also such that it permits the passange of only the vertically polarized incident light. If there is no applied voltage to the conducting surfaces, the vertically polarized light enters the crystal region and follows the 90 bending of the molecular structure. Its horizontal polarization is attenuated and the viewer sees a uniformily dark pattern. When a threshold voltage is applied the rod like molecules align themselves with the field and the light passes directly through without the shift. The vertical incident light can then pass through the second vertically polarized screen and the light area is seen. Through proper excition of the segments of each digit the pattern will appear. If there is no applied voltage, there is a uniformly lit display. The application of voltage results in a vertically incident light encountering a horizontally polarized filter at the left which will not be able to apss through and be reflected. A dark area results on the crystal.

Field effect LCDs are normally used when a source of energy is prime factor since they absorb considerably less power than the light scattering types. The cost is typically higher for field effect units, and their height is limited to about 2" while light scattering units are available upto 8" in height. LCDs are characteristically much lower than LED. There is a great range of colour choice in LCD units.

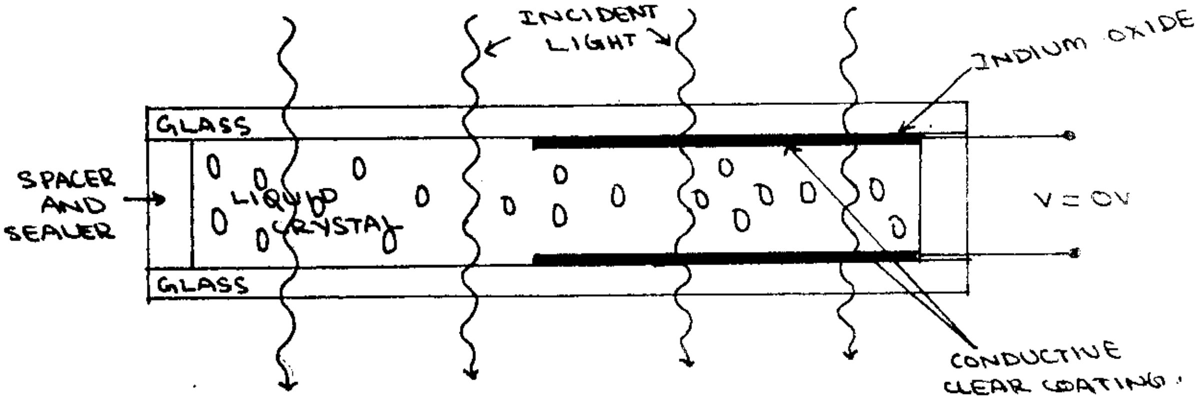


Fig : NEMATIC LIQUID CRYSTAL WITH NO APPLIED BIAS

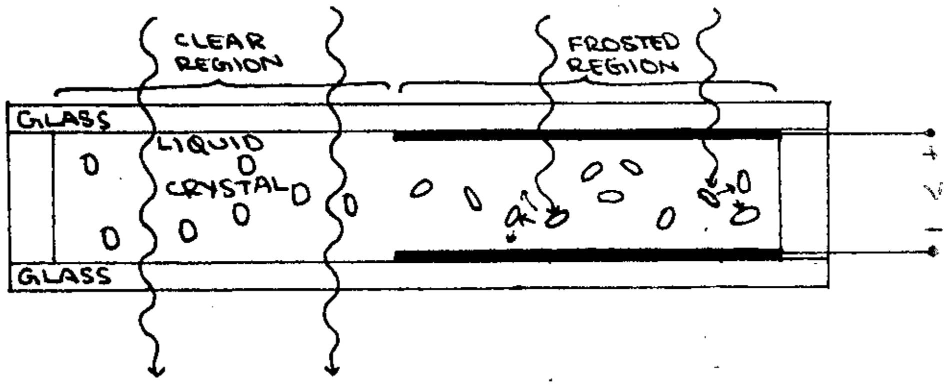


Fig : NEMATIC LIQUID CRYSTAL WITH APPLIED BIAS

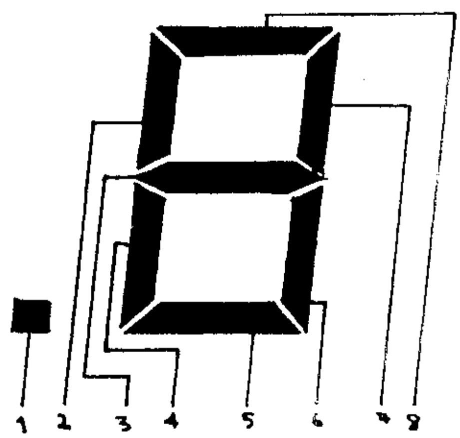


Fig : LCD EIGHT-SEGMENT DIGIT DISPLAY

4. OPERATING PROCEDURE AND CALIBRATION

A good multimeter is essential; an oscilloscope and/or frequency mater is useful.

The frequency of the 40 KHz oscillator must be matched to the reasonance frequency of the transducers. Connector temporary wire link between pins 1 and 14 of IC 2 : this will cause a transduction element to operate continuously. Turn P1 fully anti-clockwise. Measure has current drawn from the battery with the multimeter and turn P1 slowly clock-wise until the current is a maximum. The Oscillator is then set to correct frequency. Note that when P1 is turned further there is a second current peak, that is not the required oint. The Motorola version has a smaller hysteresis and this may necessitate an increase in the value of C2 to 2.2nf. The National Semiconductor version, has a higher hysteresis, so that the value of C2 may have to be reduced to 470 pf.

Remove the wire links from pins 1 and 14 IC2. Press S1 and make sure that the transduction element produces a short click twice a second.

Next, P 2 must be adjusted until the oscillator in IC 4 operates at 17.05 KHz. In the absence of a frequency meter, place the unit in the position where the distance between the front of the transducer and a good reflecting surface is exactly 1m. Press Sq and turn

P2 until the display reads 1.00. If the readng is not stable or just 0.00 turn P3 slightly until a correct, stable reading is obtained.

Adjustment of P3 (sensitivity) depends largely on the circumstances of use. In quite surroundings, the control may be set fully anti-clock wise. If, however, the display gives a spurious readings, the sensitivity is too high;: the meter then detects its own clock. This obviated by turning P3 slightly clockwise.

If the unit is used in noisy surroundings, reduce the sensitivity even further, so that it does not respond to spurious sounds. Note, however, that the maximum measurable distance is then reduced. It should be borne in mind that absorbent surfaces such as furniture, dressed people, and so on cannot be reliably be detected. This is because the echo from them is too weak to trigger the receiver. It pays, however, to experiment. The sensitivity of the receiver may be increased by reducing the value of R6. Further more, the time dependency of the sensitivity may be altered by changing the value of time constant R6-C8. Reducing that value makes the meter more sensitive over shorter distances.

5. ACCURACY

The accuracy of the measurement depends on the precision with which time is measured and on the ambient conditions. The speed of sound depends on the atmospheric pressure, the teperature, and the air density.

Larger errors caused by unit are mainly due to the incorrect triggering of the receiver. Partly because of the Q factor of the sending element, it takes a finite time (upto a few periods of the 40 KHz signal) before the received signal attain maximum amplitude and the receiver is triggered and a delayed period causes a measuring error of about half a centimeter. None the less, under normal conditions,measurements made with this prototype upto a distance will be found to be accurate to within 2% ie., 2 cm/metre.

CONCLUSION

In attempting this project, we have tried to reflect the need for a good surveillance system which should find successful applications in a wide range of areas.

Though certain impediments and hinderances go on to make our project not so foolproof, still the door is wide open for any modifications. Though adding a microprocessor to this system would be a savvy thought, we deliberately desisted in doing so because we wanted our project to be handy and cheap for easy commercialisation.

Hence in concluding our report, we would like to echo the thought that electronics has still very many areas to seep into and find interesting applications.

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DATA MANUAL - FOURCHILD	CMOS ICS 4000 SERIES.
LINEAR IC DATA MANUAL	LM SERIES.

National Semiconductor

Operational Amplifiers/Buffers

LM124/LM224/LM324, LM124A/LM224A/LM324A, LM2902 Low Power Quad Operational Amplifiers

General Description

The LM124 series consists of four independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, dc gain blocks and all the conventional op amp circuits which now can be more easily implemented in single power supply systems. For example, the LM124 series can be directly operated off of the standard +5 V_{DC} power supply voltage which is used in digital systems and will easily provide the required interface electronics without requiring the additional ±15 V_{DC} power supplies.

Unique Characteristics

- In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.
- The unity gain cross frequency is temperature compensated.
- The input bias current is also temperature compensated.

Advantages

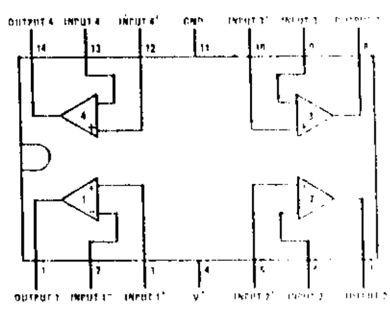
- Eliminates need for dual supplies
- Four internally compensated op amps in a single package
- Allows directly sensing near GND and V_{OUT} also goes to GND
- Compatible with all forms of logic
- Power drain suitable for battery operation

Features

- Internally frequency compensated for unity gain
- Large dc voltage gain 100 dB
- Wide bandwidth (unity gain) (temperature compensated)
- Wide power supply range:
  - Single supply 3 V_{DC} to 30 V_{DC}
  - or dual supplies ±1.5 V_{DC} to ±15 V_{DC}
- Very low supply current drain (800 μA) — essentially independent of supply voltage (1 mW/op amp at +5 V_{DC})
- Low input biasing current (temperature compensated)
- Low input offset voltage and offset current
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Large output voltage swing

Connection Diagram

Dual-In-Line Package

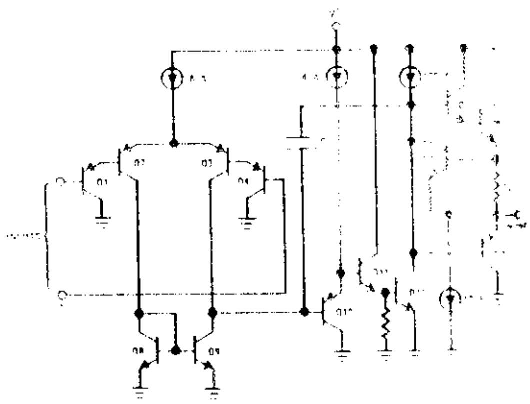


TOP VIEW

Order Number LM124J, LM124AJ, LM224J, LM224AJ, LM324J, LM324AJ or LM2902J
See NS Package J14A

Order Number LM324N, LM324AN or LM2902N
See NS Package N14A

Schematic Diagram (Each Amplifier)



National Semiconductor

Voltage Comparators

...3/LM293/LM393, LM193A/LM293A/LM393A, LM2903
... Power Low Offset Voltage Dual Comparators

...al Description

...3 series consists of two independent precision ...comparators with an offset voltage specification ...s 2.0 mV max for two comparators which were ... specifically to operate from a single power ... over a wide range of voltages. Operation from ... supplies is also possible and the low power ... current drain is independent of the magnitude ... power supply voltage. These comparators also ... unique characteristic in that the input common-... voltage range includes ground, even though ... from a single power supply voltage.

...ion areas include limit comparators, simple ... to digital converters; pulse, squarewave and time ... generators; wide range VCO; MOS clock timers; ...ibrators and high voltage digital logic gates. The ... series was designed to directly interface with ... and CMOS. When operated from both plus and ... power supplies, the LM193 series will directly ... with MOS logic where their low power drain ... distinct advantage over standard comparators.

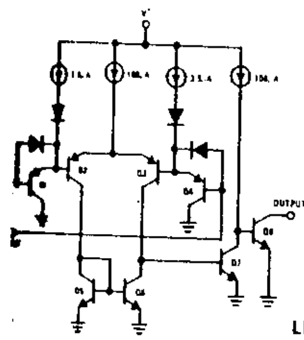
...ntages

- ...h precision comparators
- ...uced V_{OS} drift over temperature
- Eliminates need for dual supplies
- Allows sensing near ground
- Compatible with all forms of logic
- Power drain suitable for battery operation

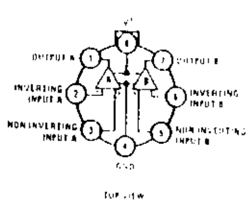
Features

- Wide single supply
  - Voltage range: 2.0 V_{DC} to 36 V_{DC}
  - or dual supplies: ±1.0 V_{DC} to ±18 V_{DC}
- Very low supply current drain (0.8 mA)–independent of supply voltage (1.0 mW/comparator at 5.0 V_{DC})
- Low input biasing current: 25 nA
- Low input offset current: ±5 nA
- and maximum offset voltage: ±3 mV
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Low output saturation voltage: 250 mV at 4 mA
- Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems

...ematic and Connection Diagrams



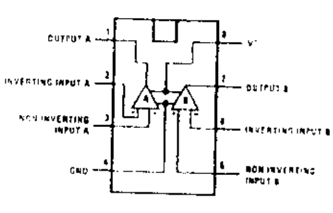
Metal Can Package



TOP VIEW

Order Number LM193H, LM193AH, LM293H, LM293AH, LM393H or LM393AH
See NS Package H08C

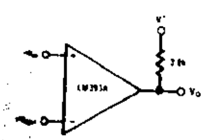
Dual-In-Line Package



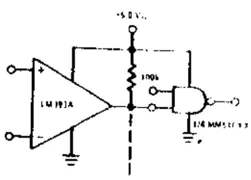
TOP VIEW

Order Number LM393N, LM393AN, or LM2903N
See NS Package N08B

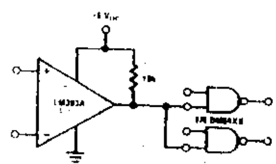
...ical Applications ($V^+ = 5.0\ V_{DC}$)



Basic Comparator



Driving CMOS



Driving TTL

National Semiconductor

Operational Amplifiers/Buffers

LM741/LM741A/LM741C/LM741E Operational Amplifier

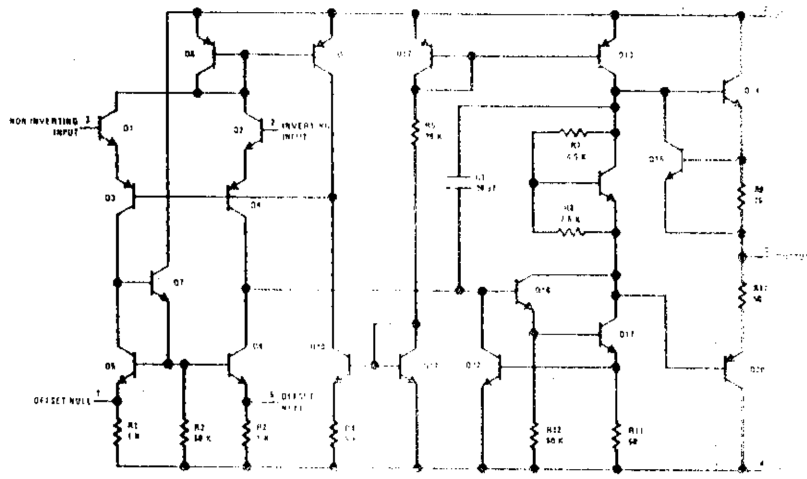
General Description

The LM741 series are general purpose operational amplifiers which feature improved performance over industry standards like the LM709. They are direct, plug-in replacements for the 709C, LM201, MC1439 and 748 in most applications.

The amplifiers offer many features which make their application nearly foolproof: overload protection on the input and output, no latch-up when the common mode range is exceeded, as well as freedom from oscillations.

The LM741C/LM741E are identical to the LM741/LM741A except that the LM741C/LM741E have their performance guaranteed over a 0°C to +70°C temperature range, instead of -55°C to +125°C.

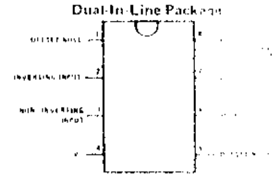
Schematic and Connection Diagrams (Top Views)



Metal Can Package

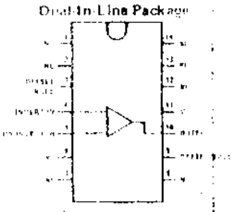
Order Number LM741H, LM741AH, LM741CH or LM741EH
See NS Package H08C

Dual-In-Line Package



Order Number LM741CN or LM741EN
See NS Package N08B
Order Number LM741CJ
See NS Package J08A

Dual-In-Line Package



Order Number LM741CN-14
See NS Package N14A
Order Number LM741J-14, LM741AJ-14 or LM741CJ-14
See NS Package J14A

LM78XX Series Voltage Regulators

General Description

The LM78XX series of three terminal regulators is available with several fixed output voltages making them useful in a wide range of applications. One of these is local on card regulation, eliminating the distribution problems associated with single point regulation. The voltages available allow these regulators to be used in logic systems, instrumentation, HiFi, and other solid state electronic equipment. Although designed primarily as fixed voltage regulators these devices can be used with external components to obtain adjustable voltages and currents.

The LM78XX series is available in an aluminum TO-3 package which will allow over 1.0A load current if adequate heat sinking is provided. Current limiting is included to limit the peak output current to a safe value. Safe area protection for the output transistor is provided to limit internal power dissipation. If internal power dissipation becomes too high for the heat sinking provided, the thermal shutdown circuit takes over preventing the IC from overheating.

Considerable effort was expended to make the LM78XX series of regulators easy to use and minimize the number of external components. It is not necessary to bypass the output, although this does improve transient response. Input bypassing is needed only if the regulator is located far from the filter capacitor of the power supply.

For output voltage other than 5V, 12V and 15V the LM117 series provides an output voltage range from 1.2V to 57V.

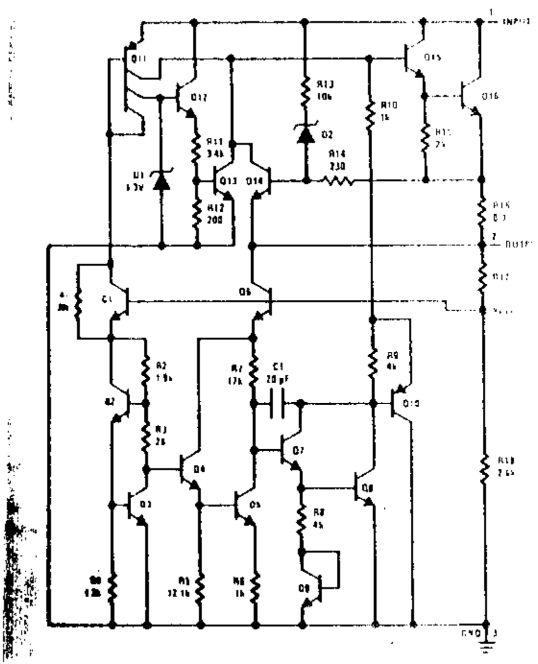
Features

- Output current in excess of 1A
- Internal thermal overload protection
- No external components required
- Output transistor safe area protection
- Internal short circuit current limit
- Available in the aluminum TO-3 package

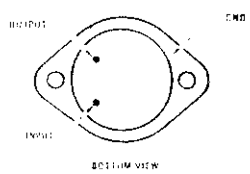
Voltage Range

LM7805C	5V
LM7812C	12V
LM7815C	15V

Schematic and Connection Diagrams

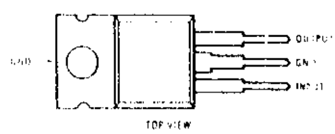


Metal Can Package
TO-3 (K)
Aluminum



Order Numbers
LM7805CK
LM7812CK
LM7815CK
See Package KC02A

Plastic Package
TO-220 (T)



Order Numbers:
LM7805CT
LM7812CT
LM7815CT
See Package T03B

CD4030B Types

CMOS Quad Exclusive-OR Gate

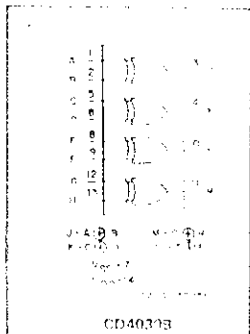
High-Voltage Types (20-Volt Rating)

The RCA-CD4030B types consist of four independent Exclusive-OR gates. The CD4030B provides the system designer with a means for direct implementation of the Exclusive-OR function.

The CD4030B types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- Medium-speed operation: t_{PHL}, t_{PLH} = 65 ns (typ.) at V_{DD} = 10 V, C_L = 50 pF
- 100% tested for quiescent current at 20 V
- Standardized, symmetrical output characteristics
- 5-V, 10-V, and 15-V parametric ratings
- Maximum input current of 1 μA at 18 V over full package temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package temperature range):
  - 1 V at V_{DD} = 5 V
  - 2 V at V_{DD} = 10 V
  - 2.5 V at V_{DD} = 15 V
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"



CD4030B FUNCTIONAL DIAGRAM

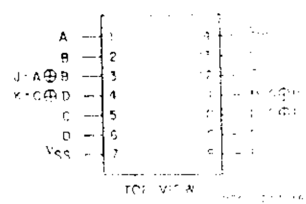
Applications:

- Even and odd-parity generators and checkers
- Logical comparators
- Adders/subtractors
- General logic functions

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) .... -0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS .... -0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT .... ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) .... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) .... Derate Linearly at 12 mW/°C to 200 mW
For T_A = -55 to +100°C (PACKAGE TYPES D, F, K) .... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) .... Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) .... 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H .... -55 to +125°C
PACKAGE TYPE E .... -40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) .... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. .... +265°C

TERMINAL DIAGRAM
Top View



RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating** conditions should be selected so that **operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

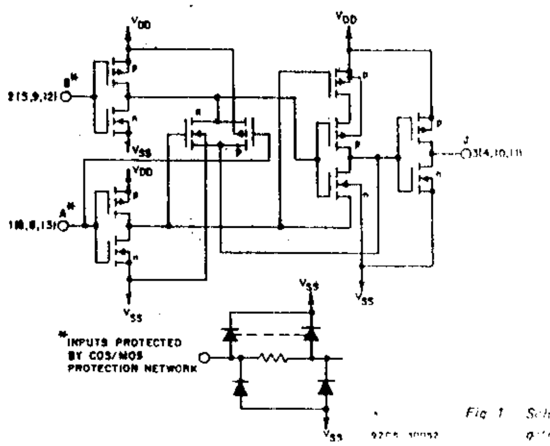


Fig. 1 – Schematic diagram (1 of 4 identical gates).

TRUTH TABLE FOR ONE OF FOUR IDENTICAL GATES

A	B	J
0	0	0
1	0	1
0	1	1
1	1	0

1 = HIGH LEVEL
0 = LOW LEVEL

CD4049UB, CD4050B Types

CMOS Hex Buffer/Converters

High-Voltage Types (20-Volt Rating)

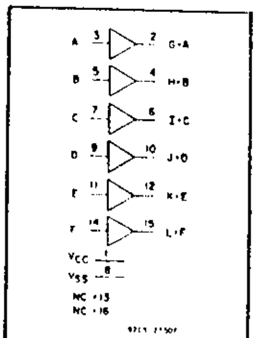
CD4049UB–Inverting Type

CD4050B–Non-Inverting Type

The RCA-CD4049UB and CD4050B are inverting and non-inverting hex buffers, respectively, and feature logic-level conversion using only one supply (voltage (V_{CC}). The input-signal high level (V_{IH}) can exceed the V_{CC} supply voltage when these devices are used for logic-level conversions. These devices are intended for use as CMOS to DTL/TTL converters and can drive directly two DTL/TTL loads. (V_{CC}=5 V, $V_{OL} \leq 0.4$ V, and $I_{OL} \geq 3.3$ mA.)

The CD4049UB and CD4050B are designated as replacements for CD4009UB and CD4010B, respectively. Because the CD4049UB and CD4050B require only one power supply, they are preferred over the CD4009UB and CD4010B and should be used in place of the CD4009UB and CD4010B in all inverter, current driver, or logic-level conversion applications. In these applications the CD4049UB and CD4050B are pin compatible with the CD4009UB and CD4010B respectively, and can be substituted for these devices in existing as well as in new designs. Terminal No. 16 is not connected internally on the CD4049UB or CD4050B, therefore, connection to this terminal is of no consequence to circuit operation. For applications not requiring high sink-current or voltage conversion, the CD4069UB Hex Inverter is recommended.

The CD4049UB and CD4050B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).



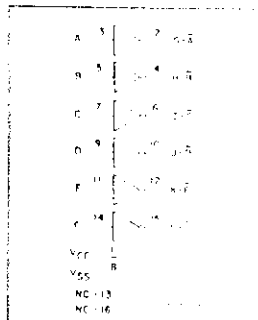
CD4050B
FUNCTIONAL DIAGRAM

Features:

- High sink current for driving 2 TTL loads
- High-to-low level logic conversion
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- 5-, 10-, and 15-volt parametric ratings

Applications:

- **CMOS to DTL/TTL hex converter**
- **CMOS current "sink" or "source" driver**
- **CMOS high-to-low logic-level converter**



CD4049UB
FUNCTIONAL DIAGRAM

MAXIMUM RATINGS, *Absolute Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{CC}) (Voltages referenced to V_{SS} Terminal)	-0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5 to +20.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = –40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = –55 to +100°C (PACKAGE TYPES D, F, K)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, K, H	-55 to +125°C
PACKAGE TYPE E	-40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING): At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max	+265°C

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range (V_{CC}) (For T_A = Full Package Temperature Range)	3	18	V
Input Voltage Range (V_{IN})	V_{CC}*	18	V

*The CD4049 and CD4050 have high-to-low level voltage conversion capability but not low-to-high-level; therefore it is recommended that $V_{IN} \geq V_{CC}$.

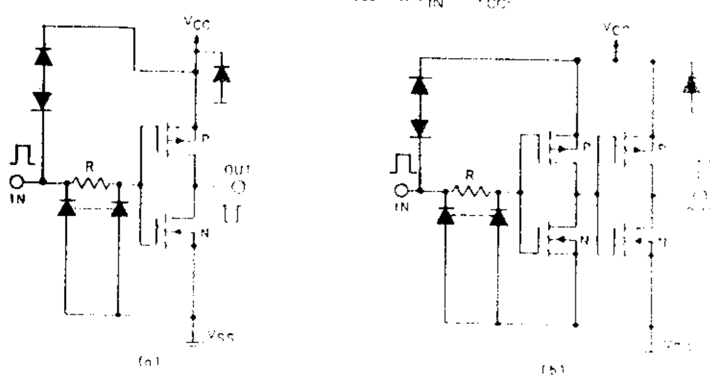


Fig. 1 – a) Schematic diagram of CD4049UB, 1 of 6 identical units.
b) Schematic diagram of CD4050B, 1 of 6 identical units.

CD4093B Types

CMOS
Quad 2-Input NAND Schmitt Triggers

High-Voltage Types (20 Volt Rating)

The RCA-CD4093B consists of four Schmitt-trigger circuits. Each circuit functions as a two-input NAND gate with Schmitt-trigger action on both inputs. The gate switches at different points for positive- and negative-going signals. The difference between the positive voltage (V_P) and the negative voltage (V_N) is defined as hysteresis voltage (V_H) (see Fig. 2).

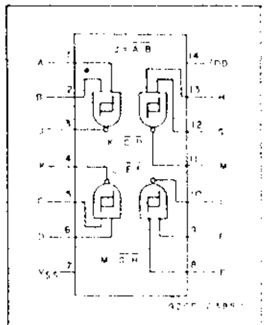
The CD4093B types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic package (E suffix), 14-lead ceramic flat package (K suffix), and in chip form (H suffix).

Features:

- Schmitt-trigger action on each input with no external components
- Hysteresis voltage typically 0.9 V at V_{DD} = 5 V and 2.3 V at V_{DD} = 10 V
- Noise immunity greater than 50%
- No limit on input rise and fall times
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package-temperature range, 100 nA at 18 V and 25°C
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Wave and pulse shapers
- High-noise-environment systems
- Monostable multivibrators
- Astable multivibrators
- NAND logic



FUNCTIONAL DIAGRAM

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

CHARACTERISTIC	MIN.	MAX.	UNITS
Supply-Voltage Range (T_A = Full Package Temp. Range)	3	18	V

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . -0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . -0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = -55 to +100°C (PACKAGE TYPES D, F, K) . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . -55 to +125°C
PACKAGE TYPE E . . . -40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . +265°C

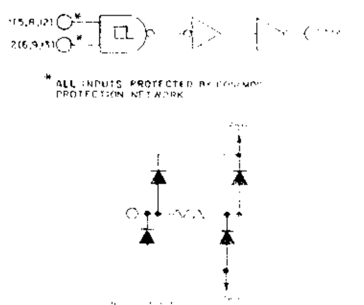
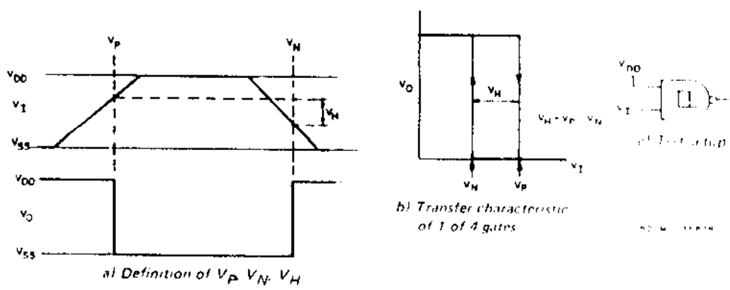


Fig. 1 – Logic diagram (1 of 4 Schmitt triggers).



a) Definition of V_P, V_N, V_H

b) Transfer characteristic of 1 of 4 gates

Fig. 2 – Hysteresis definition, characteristic, and test setup.

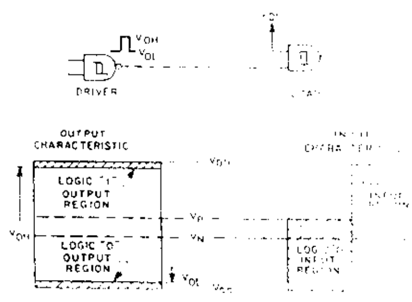


Fig. 3 – Input and output characteristics.

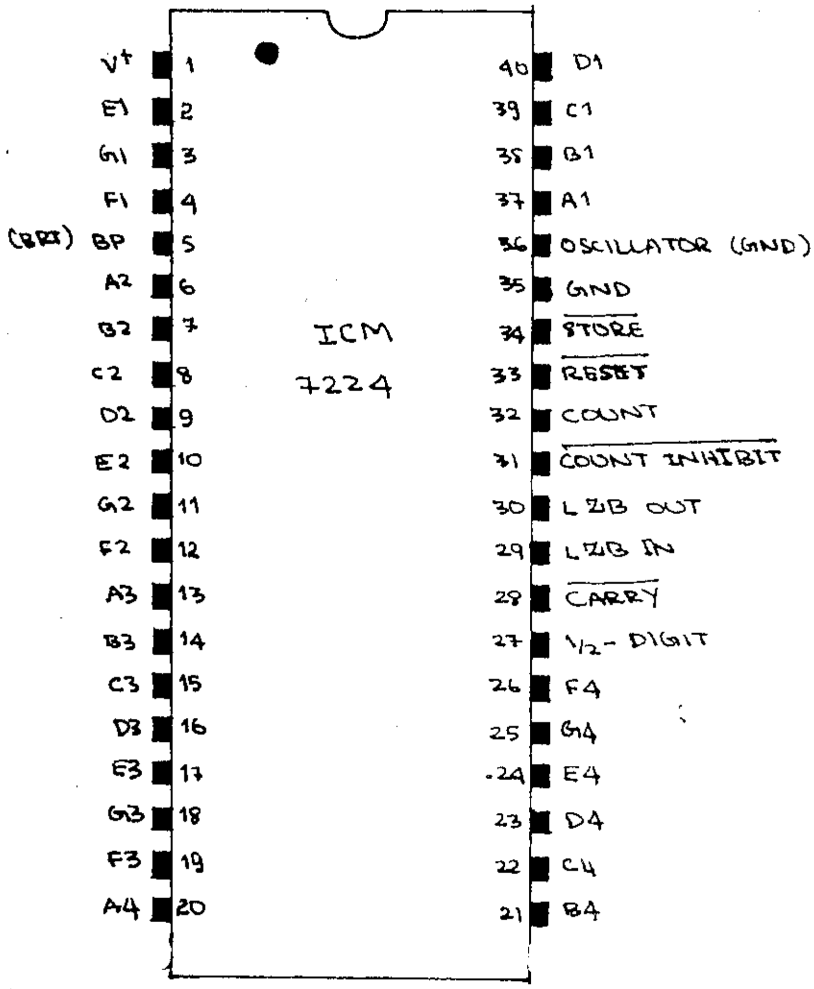


Fig : PIN CONFIGURATION OF ICM 7224