8-Digit Frequency Meter

PROJECT REPORT

Submitted in partial fulfilment of the requirements for the award of the degree of Bachelor of Engineering in Electrical & Electronics Engineering of the Bharathiar University. Coimbatore-641 046

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Certificate

This is to certify that the Report entitled

8-DIGIT FREQUENCY METER

has been submitted by

Mr. Mathews. C. Simon, K. Saravanan & S. Lakshmanan

in partial fulfilment for the award of Bachelor of Engineering in the Electrical and Electronics Engineering Branch of the Bharathiyar University Coimbatore-641 046 during the academic year 1990–91

16/3/91

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Team Members,

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SYNOPSIS

Frequency measurement is required as part of those instruments which converts the measured physical quantity into a frequency change, such as the variable-reluctance velocity transducer, stroboscopes. The vibrating wire force sensor, resonant-wire pressure measuring instruments and the quartz thermometer. The output relationship of some forms of A.C. bridge circuit used for measuring inductance and capacitance also requires the excitation frequency to be known.

In this project a frequency meter module is fabricated using 8digit,7 segment LED indicator with a resolution of 10 Hz and accepts input frequencies of upto 3.5 MHz. Its presetting facility makes this simple-to-build module for incorporating in a radio receiver. The module uses two ICM 7217IPI Cmos presettable up and down counters.

CHAPTER 1

INTRODUCTION

1.1 Electronics Frequency Measurements:

It is needless to say that a frequency meter finds a very wide range of apllication, in a power house, receiving station, sub stations, radio stations and Television stations. As it goes hand in hand with financial involvement the meter should have a fair accuracy and fast response. Electronic tehniques are widely used in the measurement of variables with greater accuracy. In this project, measurement of frequency by electronic circuit is taken. The design of digital frequency meter is carried out and the frequency meter is fabricated to give a numerical read out. Accordng to the mathematical equation $f = 1/T$ where f is the frequency in Hz and T is the time period in seconds.

1.2 Advantages of digital frequency measurements:

The digital instruments which are naturally based on electronic circuits have several advantages as mentioned below.

1. The digital instruments indicate the readings directly in decimal numbers and therefore errors an account of

human factors like errors due to parallex and approximation are eliminated.

2. The readings may be carried to any number of significant figures by merely positioning the decimal point.

3. Since the output of digital instruments is in digital form and therefore the output may be directly fed into memory devices like tape recorders,printers and digital computers etc, for storage and future computations.

4. Electronically operating measuring scheme draw very minute current which the signal source can supply without affecting accuracy that is the signal source is not loaded as the electronics circuit provides high input impedance which is essential to reduce error.

5. When manipulating the signal by electronic circuits, the signal can be amplified or attenuated to the required level.

1.3 Resolution in Digital Meters:

The number of digit positions used in a digital meter determines the resolution. In practice a fourth digit usually capable of indicating either 0 or 1 only, is placed to the left or active digits. This permits going above 999 to 1999 to give overlap between ranges for convenience. This is called over ranging.

This type of display is known as a 31/2 digit display.

The resolution of a digital meter is determined by the number of active or full digits used. If n = number of full digits used in the meter.

Resolution = $1 / 10^n$

Therefore a 4 digit display has a resolution of $1/10^4$ = 0.0001 (or) 0.01 percent.

1.4 Sensitivity of Digital meters:

Sensitivity is the smallest change in input which a digital meter is able to detect. Therefore it is lowest ranges full scale value multiplied by meter's resolution.

Sensitivity S = (f.s) mini x R

Where (f.s)mini = lowest full scale value of meter and R = resolution expressed as decimal.

1.5 Scheme of the Project:

Alternative methods of measurements of frequency is explained in chapter 2. The proposed digital frequency meter is explained in chapter 3. This module is based on two ICM 7217 CMOS presettable UP/DOWN counters. Two of these chips are cascaded to obtain 8 digit read out on common anode 7 segmoent LED displays.

CHAPTER 2

FREQUENCY METERS

2.1 Types of frequency Meters:

The different types of frequency meters are available based on different principles as follows:

1) Mechanical & resonance type
2) Electrical resonance type
3) Electrodynamometer type
4) Weston type
5) Ratiometers type
6) Saturable core type.

The frequency can also be measured and compared by other arrangements like electronic counters, frequency bridges, stroboscopic methods and cathode ray oscilloscopes.

2.2 Mechanical Resonance type frequency meter (vibrating read type)

This meter consists of a number of thin steel strips called reeds. These reeds are placed in a row alongside and close to an electromagnet which has a laminated iron core and its coil is connected in series with a resistance, across the supply whose frequency is to be measured.

When the frequency meter is connected across the supply whose frequency is to be measured, the coil of electromagnet carries a current which alternates at the supply frequency. The force of attraction between the reeds and the electromagnet is proportional to i*i and therefore this force varies at twice the supply frequency.

Frequency Range.

The usual frequency span of these meters is 6 Hz to 53 Hz. The range of frequency meter can be doubled with polarization. The polarization may be accomplished by using a DC winding in addition to the A.C winding or by using a permanent ,magnet.

Advantages and disadvantages.

An advantage of the reed type of frequency meter is that the indication is virtually independent of the waveform of the supply voltage. The indication is independent of magnitude of applied voltage also provided the voltage is not too low , as at low voltages, the amplitude of vibrations will not be sufficient and thus the readings will not be reliable.

The disadvantages is that such instruments cannot be read much closer than half the frequency difference between adjacent reeds. Thus they cannot be used for precision measurements.

2.3 Electrical Resonance type frequency meters:

Two types of electrical resonance frequency meters are

(i) Ferrodynamo type

(ii) electrodynamo meters type.

(i) Ferrodynamo Type:

The operation of this instrument, the magnetising coil carries a current I and this current produces a flux. If we reflect the resistance of the coil and the iron losses in the core, flux ϕ, is in phase with current I. Flux being alternating in nature induces an enforce in the moving coil. This emf lags behind the flux by 90°. The emf induced circulates a current in the moving coil. The phase of this current depends upon the inductance L of the moving coil and the capacitance C.

(ii) Electric dynamometer Type frequency meter:

The torque on the movable element is proportional to the current through the moving coil. This current is the sum of the currents in the two parts of the fixed coil. For applied frequency within the

limits of the frequency range of the instrument, the circuit of fixed coil 1 operates above resonant frequency (as XL1>XC1) with current through it, lagging the applied voltage. The circuit of fixed coil 2 operates below the resonant frequency (as XC2 > XL2) with current in leading the aplied voltage. One fixed coil circuit is inductive and the other is capacitance and therefore the torques produced by the two currents I1 and I2 acts in opposition on the moving coil. The reluctant torque is a function of frequencoy of the applied voltage and therefore the meter scale can be calibrated in terms of frequency. The instrument scale spread over an angle of about 90. This meter is used only for power frequency measurements and is used in power systems for mentioning the frequency.

2.4 Weston Frequency Meter:

This frequency meter conists of two coils mounted perpendicular to each other. Each coil is divided into two sections.

The meter is connected accross the supply and the two coils carry currents, and these currents setup two magnetic fields which are at right angles to each other. The meter is so designed that the values of various resistance and inductances are such that for normal frequency of suply the value of voltage drops across resistance La and resistance Rb send equal currents through coils A and B. Therefore the needle takesup a position which is at 45° to both the coils and the pointer is at the centre of the scale.

Now if the frequency increases above its normal value, reactance of coil A and Coil B increased. While resistances coil A and coil B remain the same. This means that with an increase in frequency. The voltage impressed upon coil A increases as compared with that across coilB. Hence the current in coil A increases while it decreases in coil B (owing to increase in reactance of Lb) thus the field of coil A becomes stronger than that of coil B. The tendency of the needle is to deflect towards the stronger field and therefore,it tends to set itself in line with axis of coil A. Thus the pointer deflects to the left.

When the frequency decreases, an opposite action takesplace and the pointer deflects to the right.

2.5 Ratiometer Type Frequency Meter:

A ratiometer type freqnency meter consists of a ratiometer which gives a linear relationship between the current ratio and the deflection. The two coils of this ratiometer are fed with rectified output currents of two separate bridge rectifiers. The input sides of the two bridge rectifiers are connected to alternating current supply whose frequency is to be measured. Input side of one bridge rectifier has a series capacitance C and the other has series resistance R.

Theory and operation.

Let V be the supply voltage and F be its frequency output currents of bridge rectifier 1 is I1 is proportinal to 2*3.14159*V*C

Output current of bridge rectifier 2 I2 is proportional to V/R.

Therefore deflection Theta = K*I1/I2

= (K * 2* 3.14159 *f*V*C)/(V/R)

= 2 * 3.14159 * K1*C*R*f

Now K1, C and R are constants.

Therefore theta=K2*f.

Thus the instrument has a linear scale of frequency in case the ratiometer is so designed that the deflection is directly proportional to the ratio of two currents.

It is clear from above that the supply voltage V does not appear in the expression for deflection. Thus the instrument may be used for a fairly wide range of voltage below the maximum specified. However, the voltage should not be too low otherwise distortions are introduced which make the meter read wrongly.

This meter may beused upto a frequency of 5000 Hz. Having discussed the various analog type of frequency meter, the next chapter deals with digital frequency meters.

CHAPTER 3

DIGITAL FREQUENCY METER

3.1 Frequency Measurements:

The instrument which is now most widely used for measuring frequency which is measured in hertz, is the digital counter timer. The osciloscope is also commonly used for obtaining approximately measurements of frequency especially in circuit test and fault diagnosis applications. Within the audio frequency range, the wien bridge is a further instrument which is often used certain other frequency measuring instruments also exist which are used in some special applications. These include the dynamometer frequency meter, the zero beat meter, the grid dip meter, compbells circuit and maxwell's comutator bridge. Digital counter-times are the most accurate and flexible instrument available for measuring frequency.

3.2 Principle of operation of Digital frequency meter:

The signal whose frequency is to be measured is converted in to a train of pulses one pulse for each cycle of the signal. Then the number of pulses appearing in a definite interval of time is counted by means of an electronic counter. Since the pulses represent the cycles of unknown signals, the number appearing on the counter is a direct indication of frequency of the unknown signal. Since the elctronic counters are extremely fast the frequency of high frequency signals may be known.

3.3 Basic circuit:

The block diagram of the basic circuit of a digital frequency meter is shown in fig (3.1) The unknown frequency signal is fed to a schmit trigger.

The signal may be amplified before being applied to schmitt trigger the signal is converted in to a square wave with very fast rise and fall times then differentiated and clipped. As a result the output from a schmitt trigger is a train of pulses, for each cycle of the signal.

The output from the schmitt trigger are fed to start stop gate. When this gate opens (starts), the input pulses psses through this gate and are fed to an electronic counter which starts registering the input pulses. When the gate is closed (stop), the input pulses to counter ceases and it stop counting.

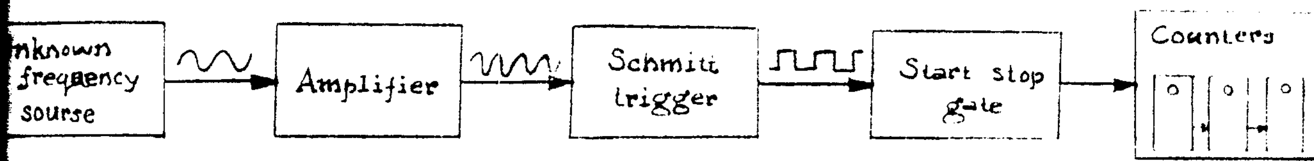


Fig. 3.1 Basic circuit of a digital frequency meter

The counter displays the number of pulses that have passed through it in the time interval between start and stop. If this interval is known, the pulse rate and hence the frequency of the input signal can be known suppose 'F' is the frequency of unknown signal 'N' the number of counts displayed by counter and 't' is the time interval between start and stop gate. Therefore frequency of unknown of signal $f = N/t$.

3.4 Time Base:

It is abundantly clear that in order to know the value of frequency of input signal, the time interval between start and stop of gate must be accurately known. This time interval known as time base can be determined by the circuit given in fig (3.2). The time base consists of a fixed frequency crystal oscillator. This oscillator which is known as clock oscillator must be very accurate. In order to insure its accuracy the crystal is enclosed in a constant temperature over. The output of this constants frequency oscillator is fed to a schmitt trigger which converts the input to an output consisting of a train of pulses at a rate equal to the frequency of the clock oscillator. The train of pulses then passes through a series of frequency divider decade assemblies connected in cascade. The connections are taken from the outpt of each decade in the series chain, and by means of a selector switch, any output may be selected. In the block diagram of fig 3.2 the clock oscillator frequency is IMHz. Thus the output of the schmitt trigger is 10^{6} pulses per second. At the X1 tap of the switch there are 10^{6} pulses per second, and thus the time inverval between two consequtive pulses is 10^{-6} sec or 1 micro secs.

At $1x10^{-1}$ tap the pulses,having gone through decade divider, are reduced by a factor 10 and now there are 10^{5} pulses per second. Therefore the time intervel between them is 10 us . Similarly there are 10^{4} pulses per second at tap 10^{-2} and the time interval is 100 us 10^{3} pulses at tap 10^{-3} and the time interval 100 ms. 10 pulses per second at tap 10^{-6} and the time interval 1 sec. One pulse per second at tap 10^{-6} and the time interval is 1 second. The time interval between the pulses is the base and it can be selected by means of the selector switch.

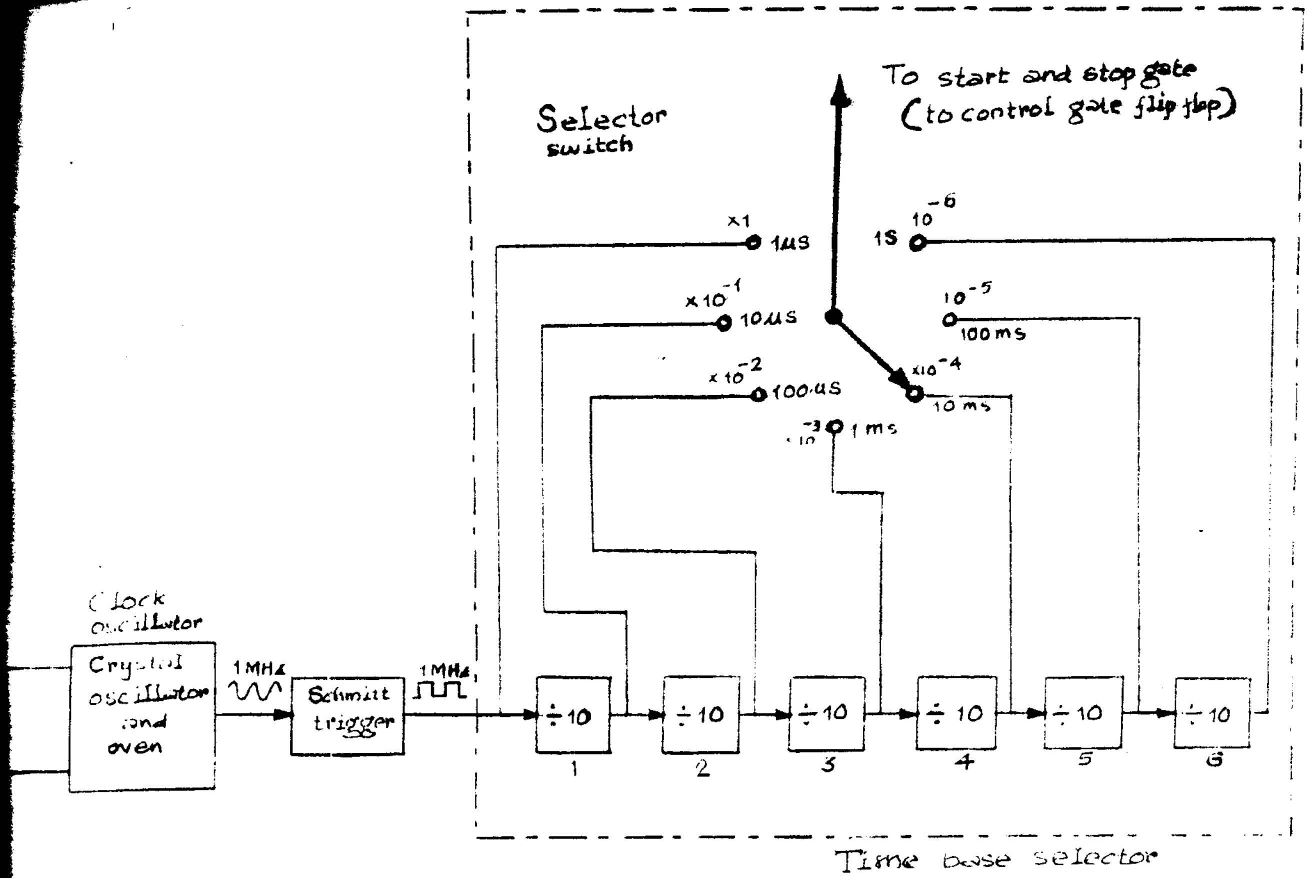
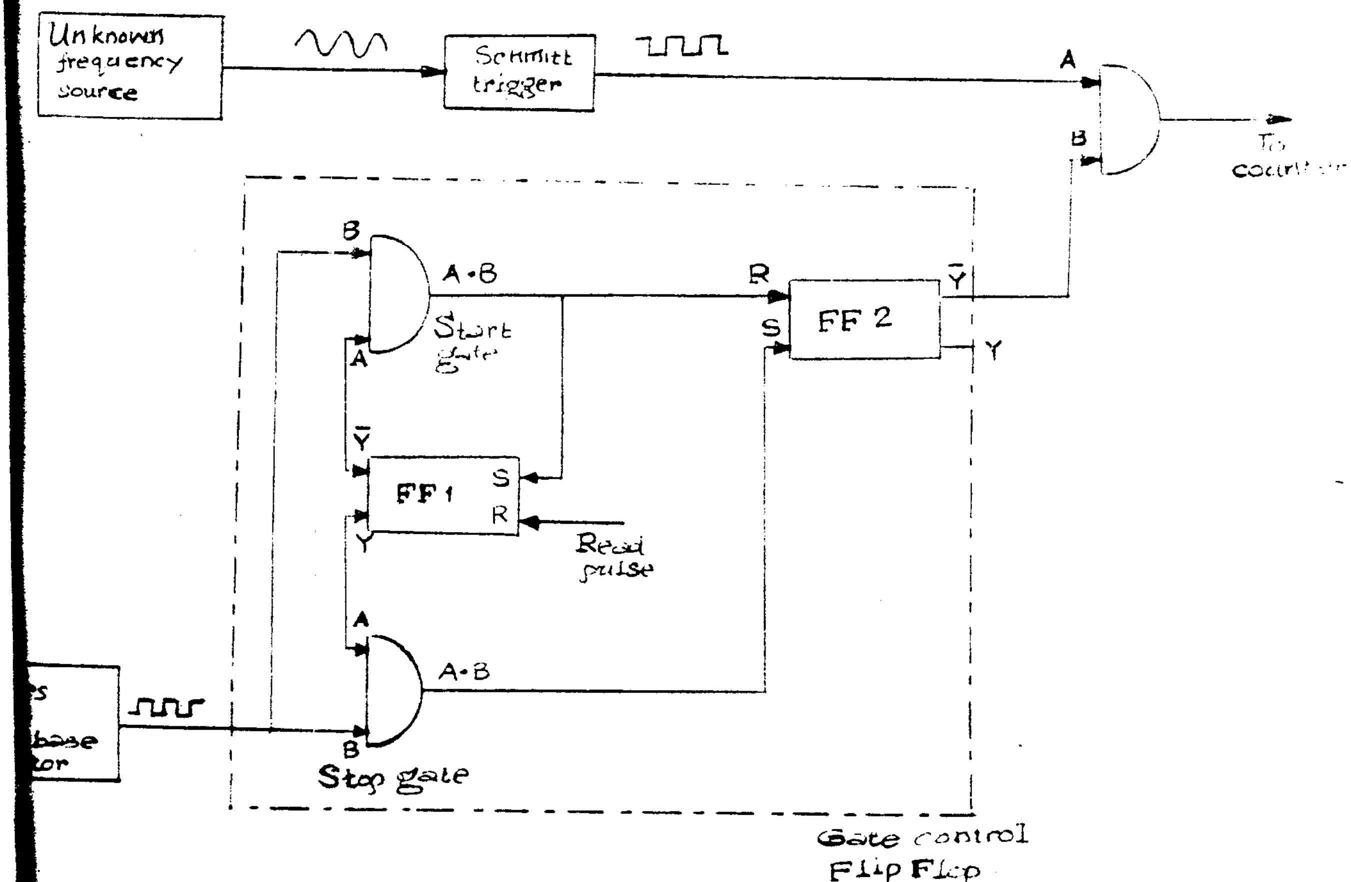


Fig. 3.2 Time base selector



g. 3.3 Circuit for measurement of frequency.

3.5 Circuit for measurement of frequency:

The complete circuit for measurement of frequency is shown in the fig (3.3) The positive pulses from the unknown source called counted signal are arriving at input A of the main gate and positive pulses from the base sellector are arriving at input B of the start gate and at input B of stop gate. Initially the FF1 is its 1 state. The resetting voltage from output volt of flip flop FF1 applied to input A of stop gate opens this gate. The zero voltage from output Y of flip flop FF1, applied to input A of stop gate closes that gate.

As stop gate is open the positive pulses from the time base, can get through to set input terminal 's' of flip flop FF2 and keep it in state 1. The resulting zero output voltage from Y is applied to terminal 'B' of main gate. Hence no pulses from unknown source can pass through the main gate.

In order to start the operation, a positive pulse called read pulse is applied to reset terminal, R of FF1 this causes FF1 to reverse its state from 1 to 0. Now its output Y is positive voltage and output Y is 0. As a result the stop gate is closed and start gate is opened. The same read pulse is applied to the decades of the counters bring them to zero and thus the count can start now.

When the nextpulse from the time base arrives it is able to pass through the start gate to the reset terminal of FF2 flipping it from its 1 state to 0 state. The resulting positive voltage from its input Y is applied to input B of main gate operating that gate. Now the pulses from the unknown frequency source are able to pass through and they are registered on the counter. The same pulse that passes through the start gate is applied to the set input S of FF1 changing its state from 0 to 1. This results in closing of start gate and the stop gate is opened.

The next pulse from the time base selector passes through the open stop gate to the set input terminal S of FF2 changing it back to its 1 state. Its output from terminal Y is zero and so the main gate is closed and the counting stops the assembly consisting of the two AND gate and the two flip flops is known as gate control flipflop.

3.6 Simplified composit diagram of a digital frequency meter:

A simplified compositive circuit of a digital frequency meter is shown in fig(3.4) There are two signal to be traced.

(i)Input signal - The frequency to be measured.

(ii)Gating signal - This determines the length of time during which the counters are allowed to totalize the pulses.

The input signal is amplified and is applied to a schmitt trigger where it is converted to a train of pulses.

The time base is shapped by a schmitt trigger in to positive pulses, 1μs apart. These pulses are applied to 6 decade driven assemblies. A selector switch allows the time interval to be selected from 1 μs to 1 sec. The input to othe time base is provided by a clock oscillator and a schmitt trigger.

The first output pulse from the time base selector switch passes through the schmitt trigger to the gate control flipflop. The gate control flipflop assures a state such that an enable signal is applied to the main gate. The main gate being an AND gate, the

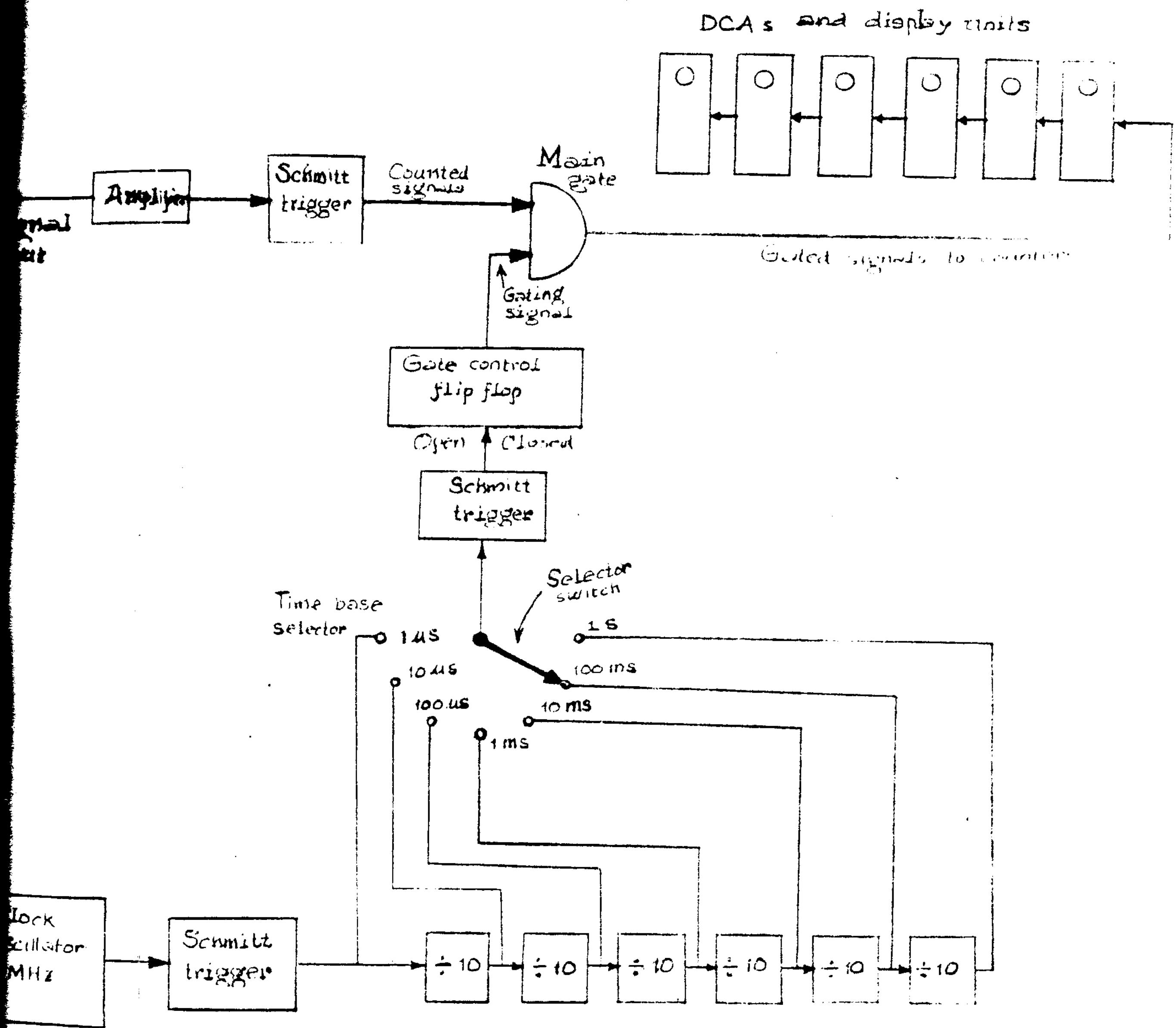


Fig. 3.4 Circuit of a digital frequency meter

input signal pulses are allowed to enter the DCAs where they are totalized and displayed. This process continues till a second pulse arrives at the control gate flip flop from the DDAs (Decade Dividing Assemblies) The control gate reverses its state which removes the enabling signal from the main gate and no more pulses are allowed to go to counting assemblies since the main gate closes. Thus the number of pulses which have passed during a specific time are cunted and displayed on the DCAs. The frequency can be read directly in case the time base selector moves the decimal point in the display area.

High frequency measurement:

The direct count range of digital frequency meters extend from D.C to a few hunder MHz. The limitations on account of the counters used. High frequency measurement demands very high rate of counting.

3.7 8Digit Frequency Meter Introduction:

The module is based on two ICM 7217 IJI CMOS presettable up and down counters. Two of these chips are cascaded to obtain an 8 digit readout on common anode 7 segment LED displays.

The counters presetting facility makes if eminently suitable for use as a frequency read out in receivers the intermediate frequency (e.g 455Hz or 99MHz) can be progarammed as an off set. In this manner, the output frequency of the local oscillataor (LO) may be measured by the counter module, when driven by a suitable prescaler. Depending on whether the L.O frequency is lower or higher than the received frequency the IF off set is divided by the pre scale ratio and then programmed as a pre set value which is automatically added to or subtracted from the module's input frequency to ensure that the received frequencoy is shown on the display.

An example might help to illustrate the above procedure. A super heterodyne VHF FM broad cast receiver has an intermediate frequency of 10.7MHz. The LO frequency is higher than the received frequency. Assuming the receiver is tunned to a station 100MHz the LO generates 110.7 MHz. This signal is applied to a divide by 100 pre scaler, which drives the frequency meter moudule. To ensure that the display reeds 100 MHz, the counter must be programmed for an IF off set of 10.7 Mhz/100 =107 KHz . Since the counter will normally count up, it must be set to a negative off set, the one's complement of this frequency, which is simple to calculate as, 10 000 000 - 0 107 000 = 0 9 893 000

Shift right (10MHz), MSD borrow;

preset = 99 989 300

The counter module has an up and down input and a separate, but optimal. Circuit for programming the off set. Resolution and gating times are simple to change, if desired. The maximum input frequency of the counter module is about 3.5MHz at a senstivity of 60 mVrms.

3.8 The Counter Chip:

The ICM 7217 IJI is a CMOS decade counter is a 28 pin plastic enclosure, intended for being programmed with the aid of switches or fixed logic configurations and driving comon anode displays. The device from GE intersil is are of a family of single chip 4 bit programmable up down counters with an on chip multiplex scan oscillator for simple driving of 7 segment LED displays.

The internal structure of the ICM 7217 is given in fig 3.5. Three main outputs are provided. CARRY/BARROW for cascading with further 4 bit counters, zero which indicates when counter state zero (0000) is counter state equals the value loaded in to the internal

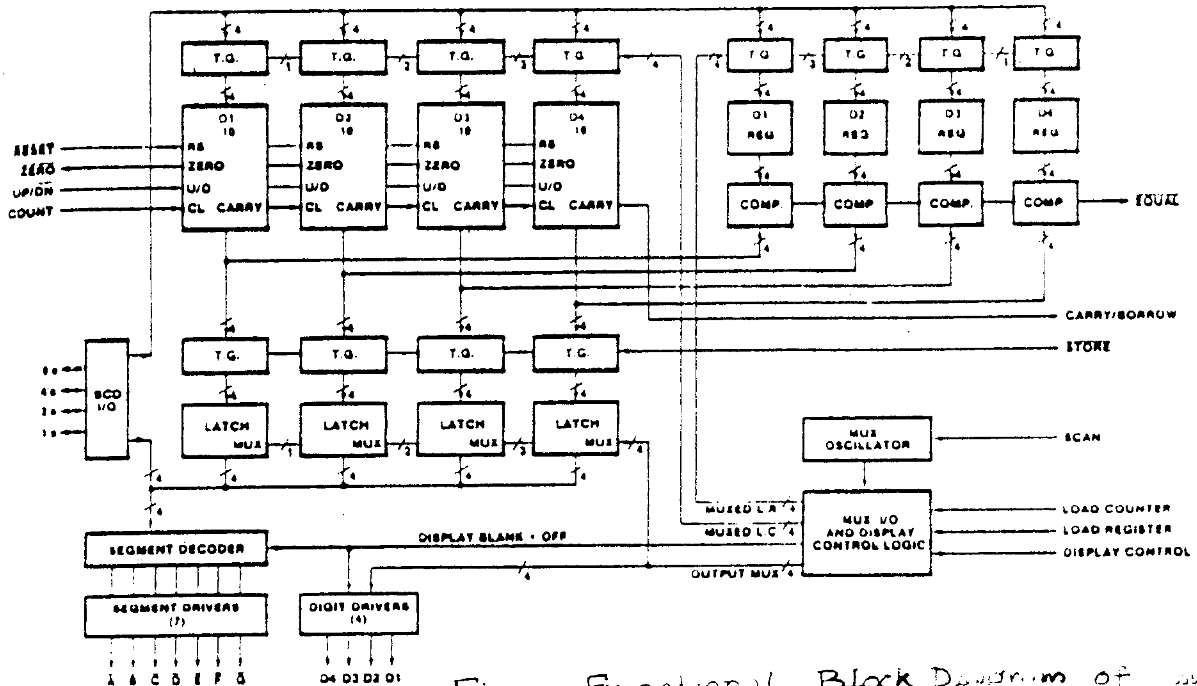


Fig. 3.5 Functional Block Diagram of ICM 7217

register via the BCD I/O pins. The three outputs and the BCD ports are TTL - compatiable and internally multiplexed. Output CARRY/BORROW goes high when the counter is clocked from 9999 to 0000 when counting up (input up and down logic high) or from 0000 to 9999 when counting down (input up and down logic low) The schmit trigger to prevent double clocking on slow rising edges.

The counter contents are transfered to the multiplexed 7 segment and BCD outputs when input STORE is pulled low. A low level at the RESET input courses the counter to be asynchronously reset to 0000.

As already noted, the BCD port can function as an input or an output. These functions are selected with the logic levels applied to the three level load counter (LD) and LOAD REGISTER (LR) inputs. When both are open, the BCD port provides the multiplexed BCD display selection signals, scanning from MSD (most significant display) to LSD (least significant display). When either LR or LC is taken high, the BCD port is turned into a 4- bit input for loading the counter (LC) or register (LR) data. Since the ICM 7217 IJI is designed to drive common anode displays, the levels applied to or provided by the BCD port are 'high true'.

When input LR is made low the BCD I/O lines are switched to the high impedence state and the digit and segment drivers are turned off. The counting operation continues, however, and the remaining input and output functions normally. The displays are normally switched off with the aid of input LR to reduce power consumption during stand by conditions.

The on board multiplex scan oscillator controls the internal timing of the ICM 7217. The operation frequency of 2.5 KHz may be reduced by connecting a capacitor between input scan and the positive suply line. The oscillator output signal has a relatively low duty factor to delay the digit driver outputs and then prevent 'ghosting' effects on the display.

The digital and segment drivers on board the ICM 7217 are capable of directly driving common anode 7 segment LED display at a peak segment current of 40 mA. At a peak segment current of 40 mA. At a duty factor of 0.25 this corresponds to 10 mA per segment.

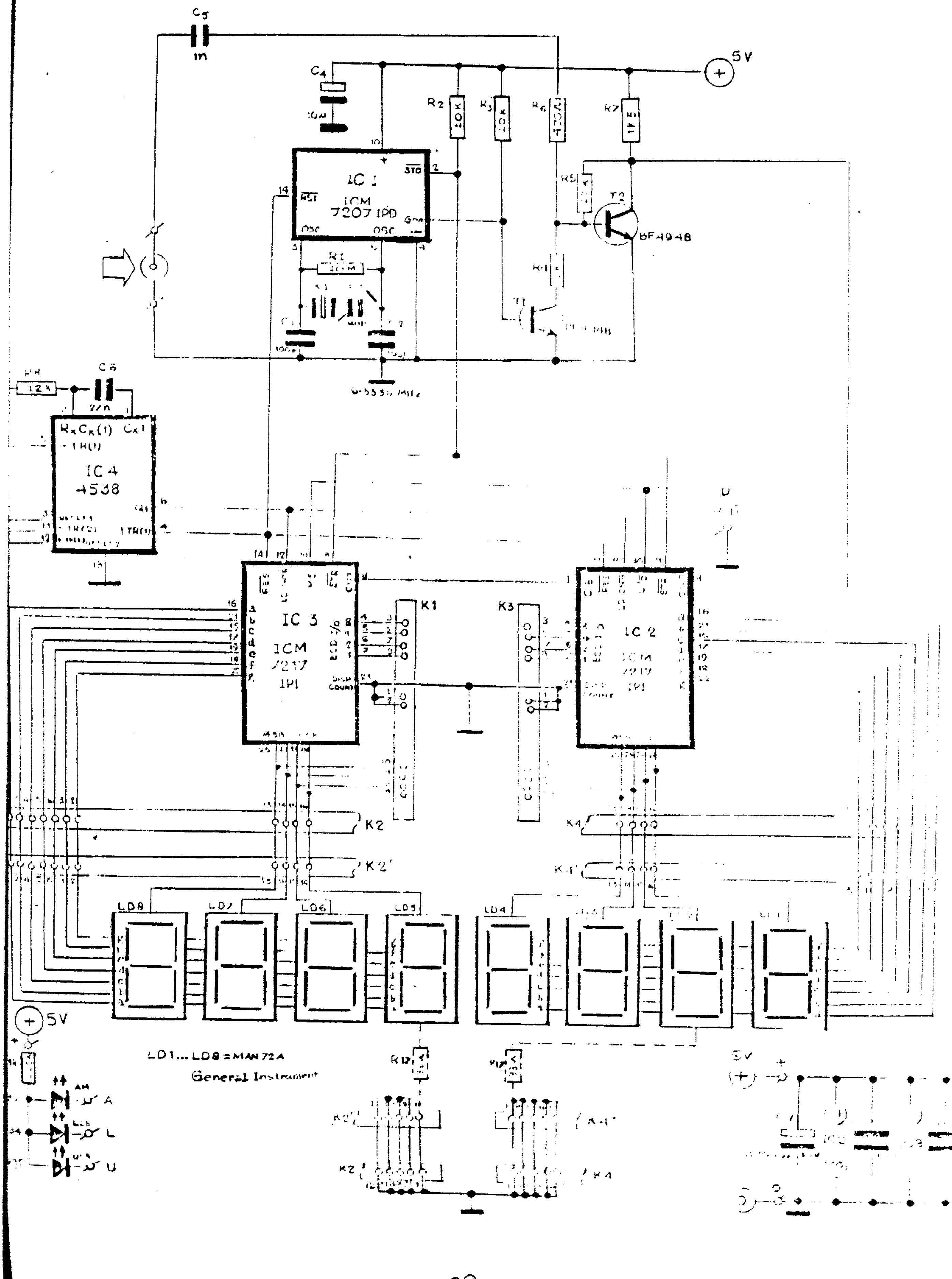
Finally the DISPLAY CONTROL input recognizes 3 logic levels. When it is logic high, the display segments are inhibited. When it is logic low, the leading zero blanking feature is tuned off. Displays on with leading zero suppression is achieved by leaving output open.

3.9 PRACTICAL CIRCUIT:

As shown in the circuit diagram of fig 3.6 a pair of ICM 7217 IPI is used in conjunction with a central timing generator type ICM 7207 IPD (IC1). This chip controls the gating of the input signal with the aid of an external quartz crystal X1, inverter T1 and input amplifier T2. In addiion, the ICM 7207 IPD provides the STORE and RESET signal for the counter chips, IC2 and IC3. Although the STORE output of the ICM 72071 IPD is of the open drain type, and the associated inputs of the ICM 7217s have 75 mA pull-up resistors, an external pul up resistor R2 is fitted to ensure immunity to noise. The U/d and RESET inputs also have internal pull up resistors, and may, be leftopen for normal operation as an up counter. The block diagram of the ICM 7207 is given in fig 3.8.

Monostable IC4 enables the counter to load the preset word. The LOAD COUNTER pulse is delayed with respect to the RESET pulse because the counter can only preset with data other than 000 when RESET is inactive.

Fig 3·6 8 - DIGIT FREQUENCY ME



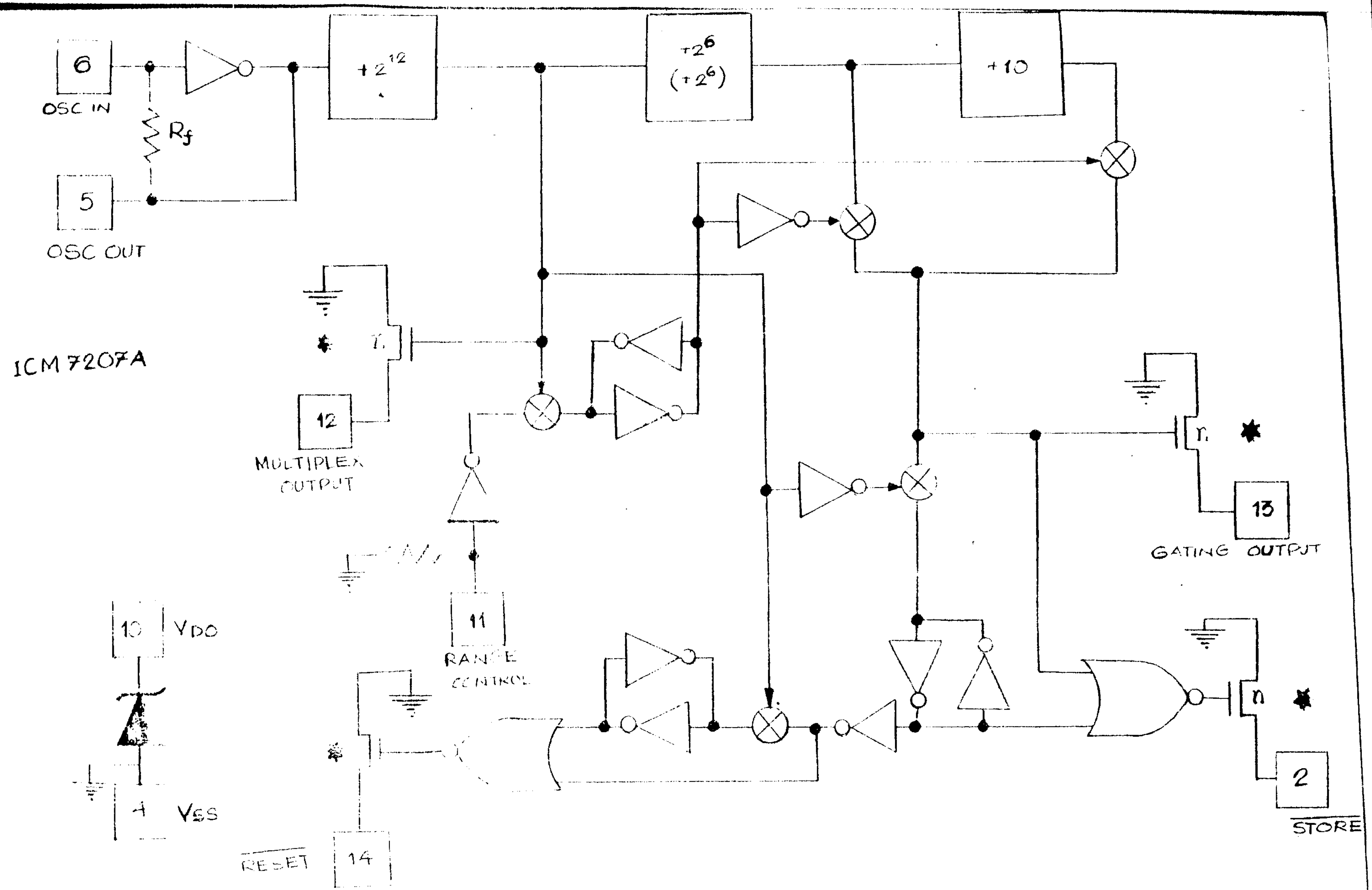


Fig. 3.8 Internal structure of the ICM7207 timing generator

The preset frequency is set with two block of 4 way DIP switch blocks. The circuit diagram of these (optional) units are given in fig 3.7 BCD thumbwheel switches may be used as a more ergonomical alternative to the DIP switches. Alternatively, wire link may be used if the counter works with one, fixed preset frequency.

The BCD port lines and the scanning digit selection signals are available on K1 and K3 for connecting to the preset unit.

A few suggestions are give for those who want to experiment with the circuit. The duration of the count window may be reduced from 100 ms to 10ms by typing pin 11 of the ICM 7207 IPD (RANGE CONTROL) to the positive suplly one.. This modification results in a corresponding reduction of the counter's resolution, however, with pin 11 at + 5v this is 100 Hz instead of 10 Hz. In both cases a good quality 6.5536 MHz quartz crystal is required. For optimum stability of the read out a type with 10 ppm tolerance or better is recommended (most inexpensive computer crystals do not meet this specification).

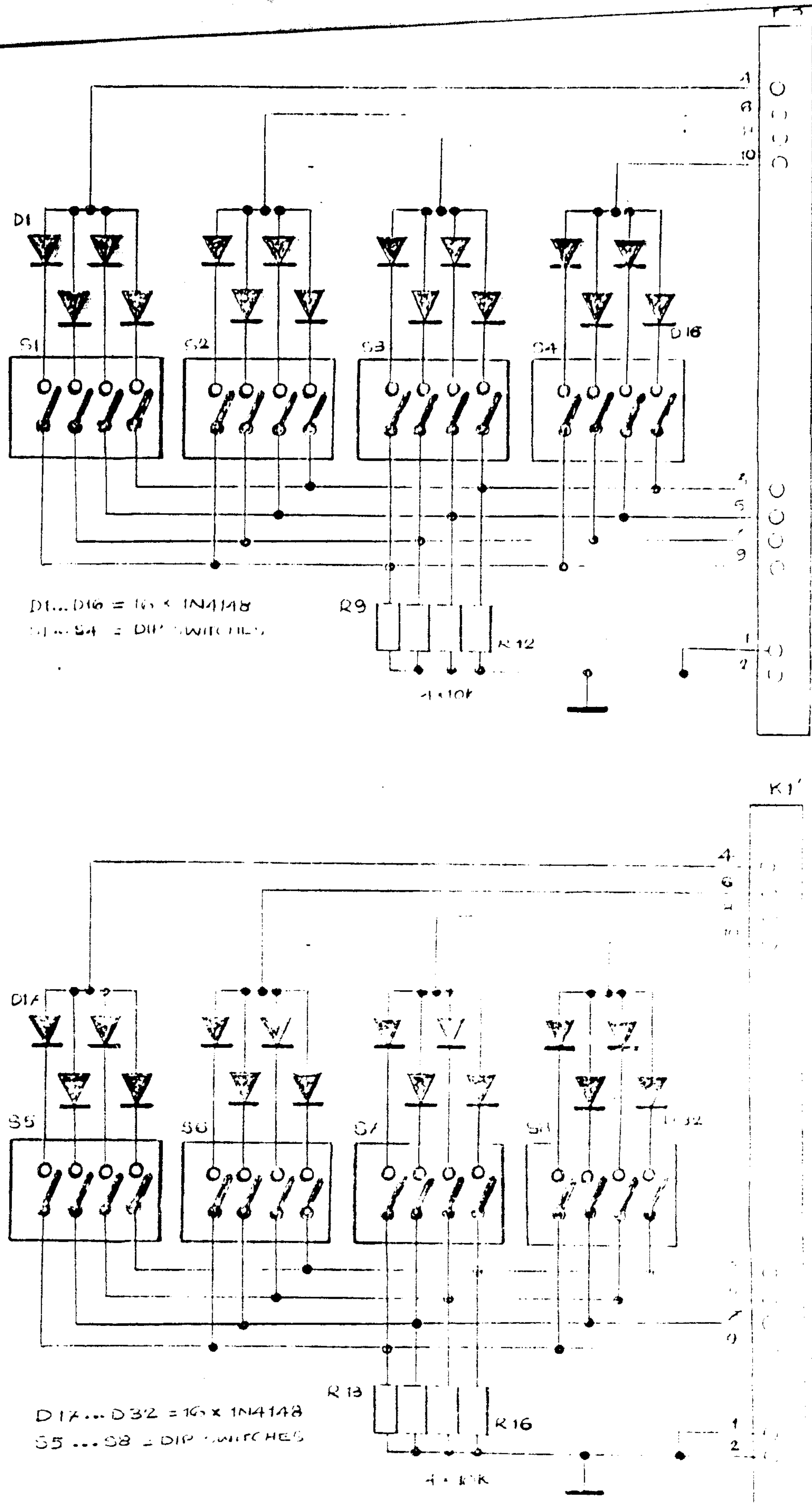


Fig. 3.7 Circuit [illegible]

For high resolution applications the duration of the count window may be increased by a factor 10 (100 ms or 1s) by using a 5.24288 MHz quartz crystal. Unfortunately, this is not standard frequency. So that this crystal have to be made to order.

Pin 23 of both counter chips is connected to ground so that leading zero suppression is not used. As already discussed, this feature may be useful in a number of applications. Where it is required, pin 23 of IC 3 may be left open to achieve leading zero suppression of the full 8 digit display may realized by the driving the display CONTROL input pin of the LS group driver IC 2 with the collector signal of a NPN transistor whose base is driven by the ZERO output of the us group driver IC 3. In a number of cases it may be posible to omit the two us displays at together.

Resistor R17 is only required when the module is used without a prescaller. Depending on whether a MHz or KHz indication is required the resistor lights the decimal point on LD5 (MHz read out) or LD2 (KHz read out).

Three receiver mode indicators D33 D34 and

D35 are provided on the display board. The LEDs may be controlled from the mode selection switch in the receiver.

3.10 Three Boards: A compact frequency read out.

The PCB is cut in to three to separate the preset unit (at the top) the main counter board (at the centre), and the readout section (at the bottom). the receiver mode indication board forms a separate unit, which need,however, not be cut from the display board.

Populating the board is straight forward and requires hardly any comment. It is strongly recommended to use sockets for all integrated circuits, displays and DIP switches. K2' and K4' on the display board and K2 and K4 on the main counter board, are 16 way sockets with turned pins. There receive 16 way IDC pin headers fitted at the ends of an approximately 5 cm long flat ribbon cable.

Insert the cable between the socket or plug and the associated plastic cap and align the individual wires with the clip type connectors check the continuity at all pins. The completed sub assembled are then ready for mounting together in a sandwich construction. The read out board is mounted on top of the main counter board with the aid of three 25 mm long spares or lengths of M3 threading. Make sure that the soldering connections of the receiver mode LEDs and those for the near by terminal posts do not touch the body of the large electrolytic capacitor, C7 underneath. The preset board is fitted back to back below the main counter board with the aid of 20 mm long PCB spacers with internal threading.

The unit may be installed in a receiver and connected to a regulated and well decoupled 5 v. power supply. In some cases it may be necessary to screen the module to prevent interfrence in the receiver. The readablity of the displays may be improved by fitting them behind a red bezel.

Calibration is simple if a frequency meter is available, adjust timmer C3 for 6.5536 MHz measured at pin 5 of the ICM 7207. Alternatively tune the receiver for zero beat against a frequency reference station and adjust the timmer until the correct received frequency is displayed.

CHAPTER 4

UP/DOWN COUNTER

4.1 GENERAL DESCRIPTION OF COUNTER CHIP :-(ICM 7217)

The ICM 7217 and ICM 7227 are 4 digit resetable UP/DOWN counters each with an on board presetable register continuously compare to the counter.The ICM 7217 versions are intended for use in hard-wired applications whose thumwheel switches are used for loading data and simple SPDT switches are used for chip control. The ICM 7217 versions are for use in processor based system, where preseting and control function are performed under processor control.

These circuits provide multiplexed 7 segment LED display outputs, with common anode or common cathode configurations available. Digit and segment drives are provided to directly drive displays of up to 0.8 inch character hight (common anode) at a 25% duty cycle. The frequency of the on board multiplexed oscillator may be controled with a single capacitor or the oscillator may be allowed to free run. Leading zeros may be blanked. The data appearing at the 7 segment and BCD output is latched, the content of counter is transfered in to latches under external control by means of the store pin.

The ICM 7217/7227 (common anode) and ICM 7217A/7227A (common cathode) versions are decade counters, providing a maximum count of 9999, while the ICM 7217B/7227B (common anode) and ICM 7217C/7227C (common cathode) are intended for timing purposes, providing maximum count of 5959.

4.2 FEATURES:-

1. Four decade, presettable UP-DOWN counter with parellel zero direct.
2. Settable register with contents continiously compared to counters.
3. Directly drives multiplexed 7 segment common anode or common cathode LED display.
4. On-Board multiplex scan oscillator.
5. Schimitt trigger counter inputs.
6. TTL compatible VCD I/O port, CARRY/BORROW, equal, zero outputs.
7. Display bank control for lower power operations; quiescent power dissipation 5 mW.
8. All terminals fully protected against static

discharge.

9. Single 5 volt supply operations.

4.3 OUTPUTS:-

The CARRY/BORROW output is a positive going pulse occuring typically 500 ns after the positive going edge of the COUNT INPUT. It occurs when the counter is clocked from 9999 to 0000 when counting up and from 0000 to 9999 when counting down. This output allows direct cascading of counters.

The $\overline{\text{EQUAL}}$ output assumes a negative level when the counter and register are equal.

The $\overline{\text{ZERO}}$ output assumes a negative level when the counter of counter is 0000.

The CARRY/BORROW, $\overline{\text{EQUAL}}$ and ZERO outputs will drive a single TTL load over the full range of supply voltage and ambient temperature; for a logic zero, these outputs will sink 1.6 mA @ 0.4V, and for a logic one, the output will source 60 uA. A 10 K pull-up register to VDD on the $\overline{\text{EQVAL}}$ or $\overline{\text{ZERO}}$ outputs is recommended for highest speed operation, and on the CARRY/BORROW output when it is being used for cascading.

The digit and segment drivers provide a

decoded 7 segment display system. capable of directly driving common anode LED displays at typical peak currents of 40 mA/Seg. This corresponds to average current of 10 mA/seg at a 25% multiplex duty cycle. Fig (4.1) shows the multiplex timing, while fig (4.2) shows the output timings.

The DISPLAY pin controls the display output using three level logic. The pin is self biased to a voltage approximately 1/2(VDD); this corresponds to VDD, the segments are inhibited, and when connected to VSS, the leading zero blanking feature is inhibited. For normal operation (Display on with leading zero blanking) the pin may be left open.

4.4 COUNTING CONTROL:-

As shown in fig (4.2) the counter is incremented by the rising edge of the COUNT INPUT signal when UP/$\overline{\text{DOWN}}$ is high. It is decremented when UP/$\overline{\text{DOWN}}$ is low . A schmitt trigger on the COUNT INPUT provides hysteresis to prevent double triggering on slow rising edges and permits operation in noisy environments. The COUNT INPUT is inhibted during reset and load counter operations.

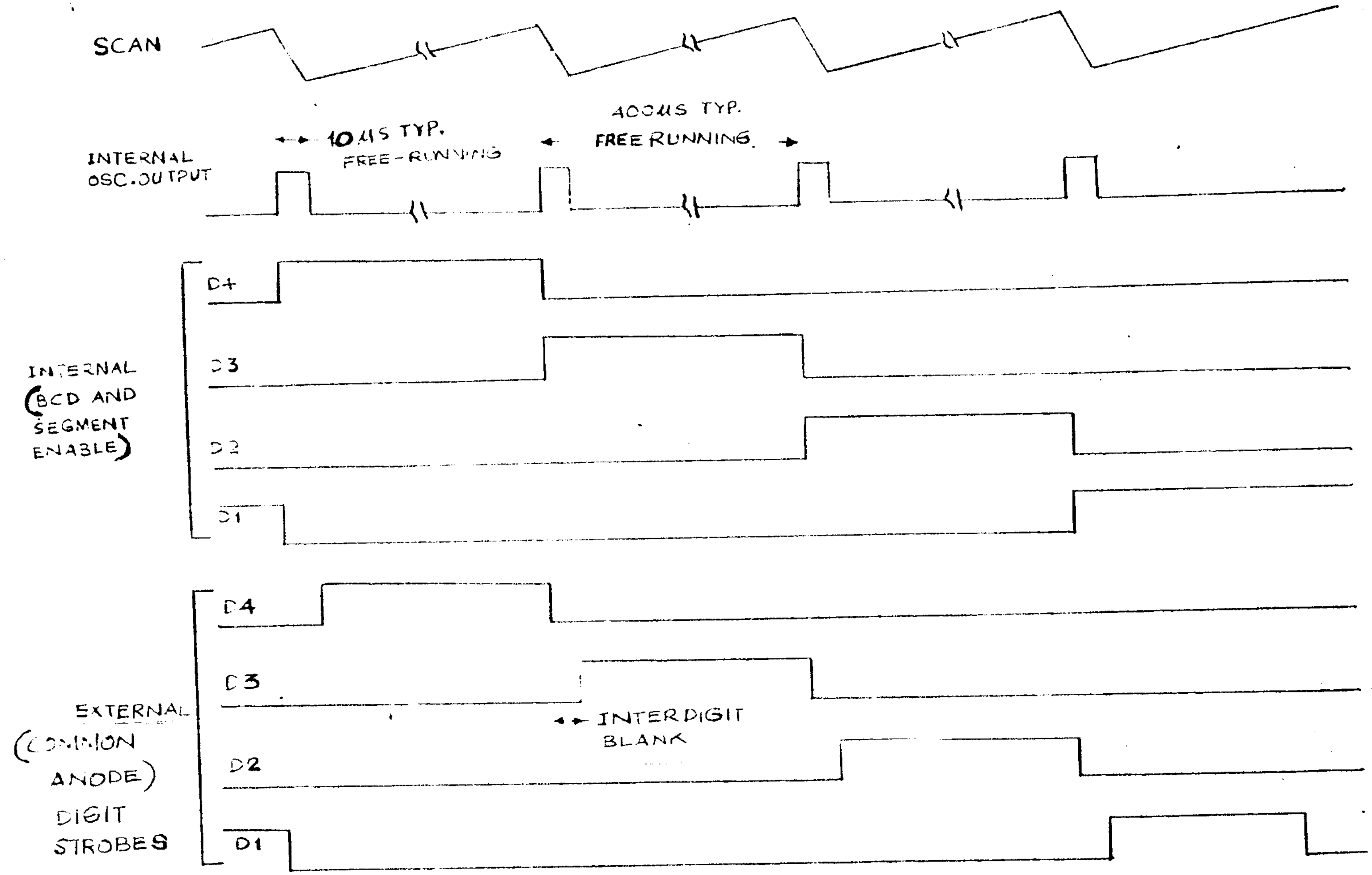
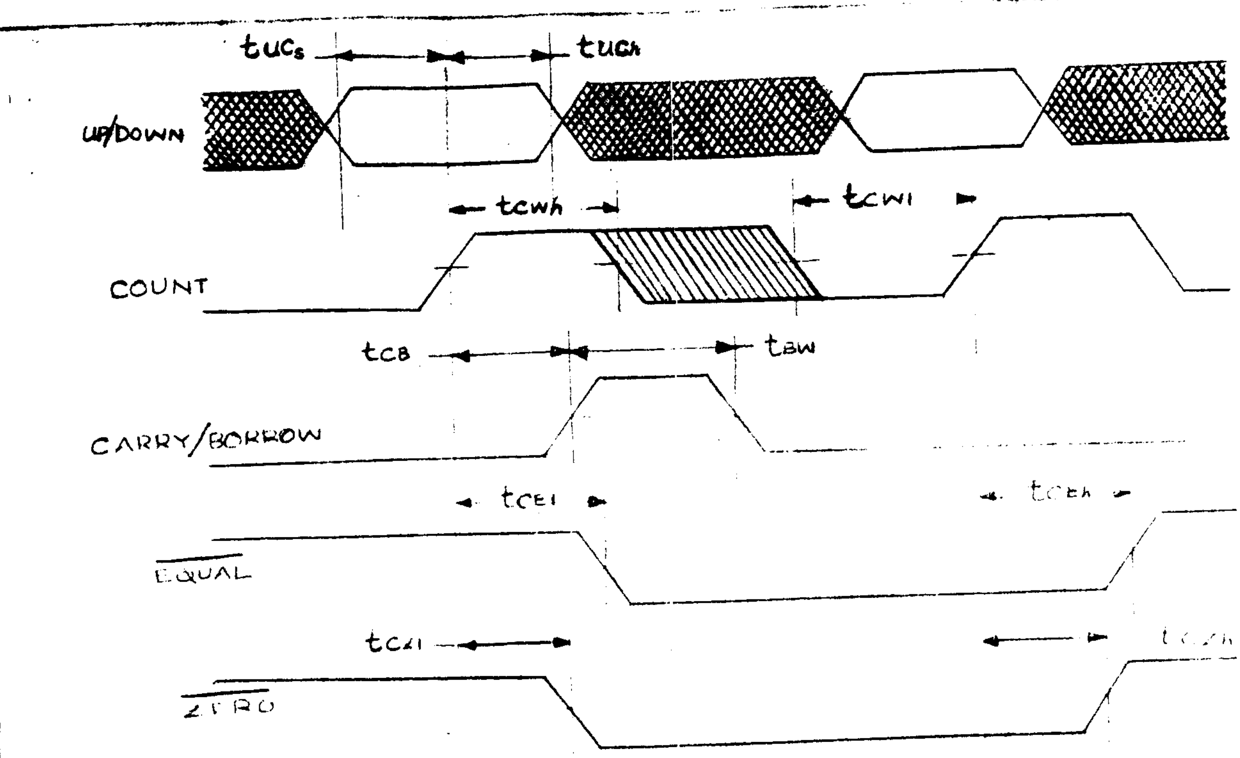


Fig. 4-1 Multiplex Timing



Symbol	Description	Min	Typ	Max	Unit
tUCs	UP/DOWN setup time (min)		300		
tUCh	UP/DOWN hold time (min)		0		
tCUh	COUNT pulse high (min)		100	250	ns
tCUl	COUNT pulse low (min)		100	250	
tCB	COUNT to CARRY/ BORROW delay		750		
tBW	CARRY/BORROW pulse width		100		
tCEl	COUNT to EQUAL delay		500		
tCZl	COUNT to ZERO delay		300		

Fig 4.2 ICM 7217 COUNT and Output Timing

The $\overline{STORE}$ pin controls the internal latches and consequently the signals appearing at the 7 segments and BCD outputs. Bringing the $\overline{STORE}$ pin low transfers the content of the counter in to the latches.

The counter is asynchronously reset to 0000 by beginig the $\overline{RESET}$ pin low. The circuit performs the reset operation by forcing the BCD input lines to zero, and "Presetting" all four decades of counter in parallel. This affects register loading. If LOAD REGISTER is activated when the $\overline{RESET}$ input is low, the register will also be set to zero. The STORE, RESET and UP/DOWN pins are provided with pull up registers of approximately 75K

4.5 BCD I/O PINS:-

The BCD I/O port provides a means of transferring data to and from the device. The ICM 7217 versions can multiplex data in to the counter or register via thumbwheel switches, depending on inputs to LOAD COUNTER or LOAD REGISTER pins. When functioning as outputs, the BCD I/O pins will drive one standard TTL load. common anode versions have internal pull down registers and common cathode versions have internal pull up registers on the four BCD I/O lines when used as inputs.

4.6 LOADING THE COUNTER :-

The BCD I/O pins. the LOAD COUNTER to provide presetting and compare functions. LC have three-level inputs, being self biased at approximately 1/2 VDD for normal operations. With LC open, the BCD output of the latch contents, scanned from MSD to LSD by the display multiplex.

When LOAD COUNTER is taken high, the drivers are tunned off and the BCD pins become high input impedence. When LC is connected to VDD, the COUNT INPUT is inhibited and the levels at the BCD pins are multiplexed into the counter. The ICM 7217 have been designed to drive common anode displays. The BCD inputs are high true, as are the BCD outputs.

4.7 THUMBWHEEL SWITCHES & MULTIPLEXING:-

The thumbwheel switches used with these circuits are TRUE BCD coded i.e all switches open corresponds to 0000. Since the thumbwheel switches are connected in parallel, diodes must be provided to prevent cross talk between digits. In order to maintain reasonable noise marigins, these diodes should be specified with low forward voltage drops. Similarly if

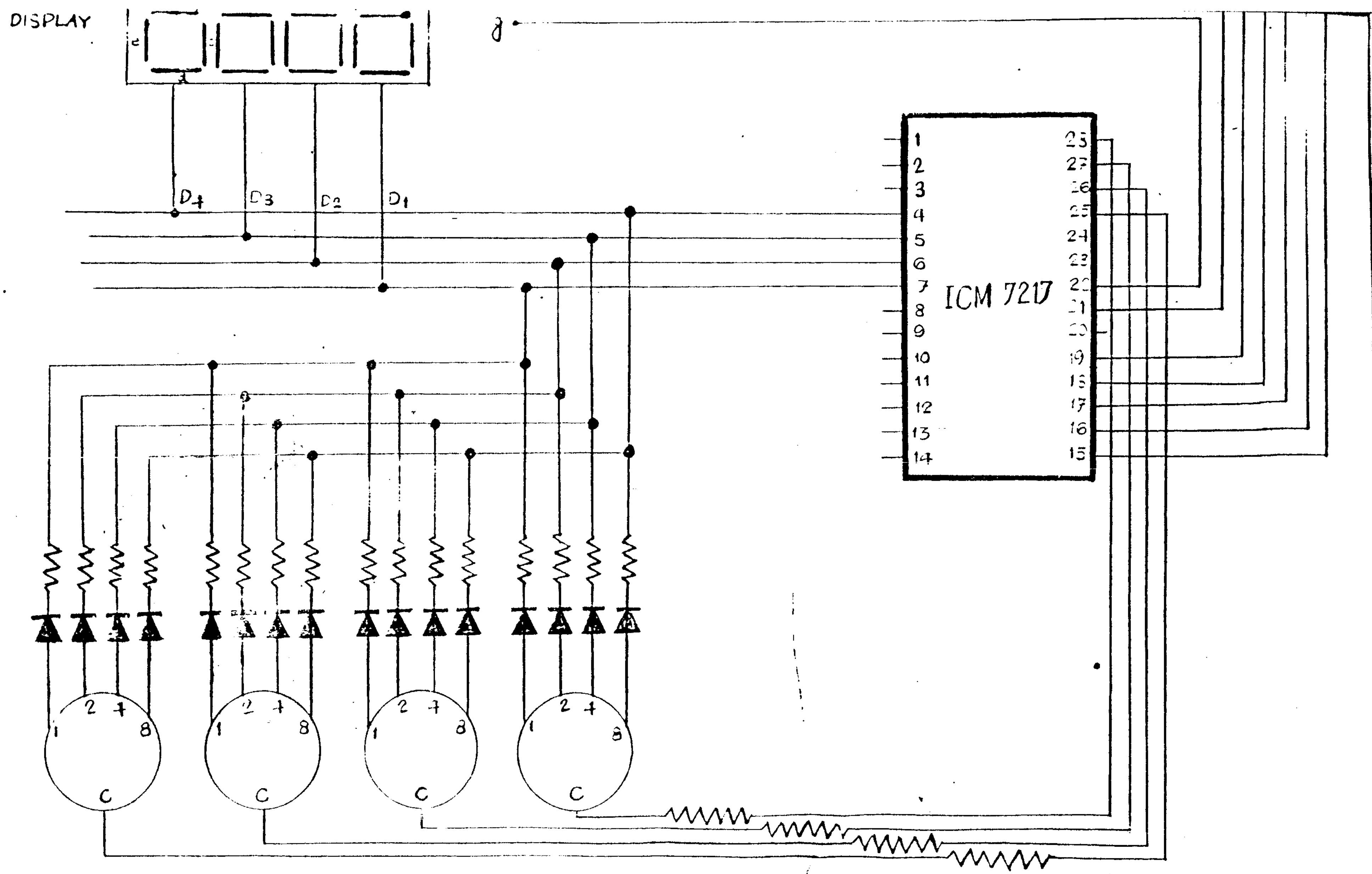


Fig.(4.3) LED Display with Thumbwheel switches the BCD outputs are to be used, resistors should be inserted in the digit lines to avoid loading problems.This is shown in fig (4.3)

4.8 OUTPUT AND INPUT RESTRICTIONS:-

The CARRY/BORROW output is not valid during load counter and reset operations.

The $\overline{\text{EQUAL}}$ output is not valid during load counters or load register cperations.

The $\overline{\text{ZERO}}$ output is not valid during a load counter operation.

The RESET input may be susceptible to noise if its input rise time is greater than about 500 us. This will prevent no problems when this input is driven by active devices (i.e TTL or CMOS logic) but in hardwired systems adding virtually any capacitence to the RESET input can cause with the circuit is configured to reload the counter with new value from the BCD lines, loading time will be digit 'ON' time multiplexed by four. If time is larger than one period of the input count, a count can be lost.

4.9 8 DIGIT UP/DOWN COUNTER :-

This circuit shows (Fig 4.4) how to cascade counters and retain correct leading zero blanking. The NAND gate detects whether a digit is active since one of the two segments $\bar{a}$ or $\bar{b}$ is active on any unblanked numbers. The flip-flop is clocked by the least significant digit of the higher order counter, and if this digit is not blanked, the Q output of the flip-flop goes high and turns on the NPN transistors, thereby inhibiting leading zero blanking on the low order counter. It is possible to use seperate thumbwheel switches.

4.10 PRECISION FREQUENCY COUNTER

The circuit in fig (4.5) shows a simple implementation of a four digit frequency counter, using an ICM 7207A to provide the one second gating window and the STORE and RESET signals. In this configuration, the display reads hertz directly. With pin 11 of the 7207A connected to VDD, the gating time will be 0.1 seconds, this will display tens of hertz as the least significant digit . For shorter gating times an ICM 7207 may be used, giving a 0.01 second gating with pin 11 connected to VDD and a 0.1 second gating with pin 11 open.

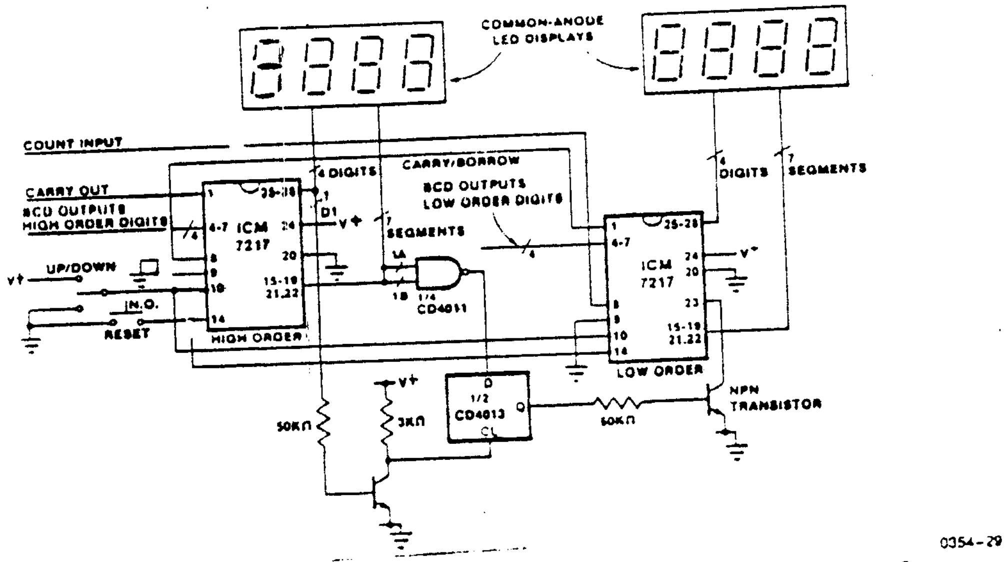


Fig. 4.4 Digit Up/Down Counter

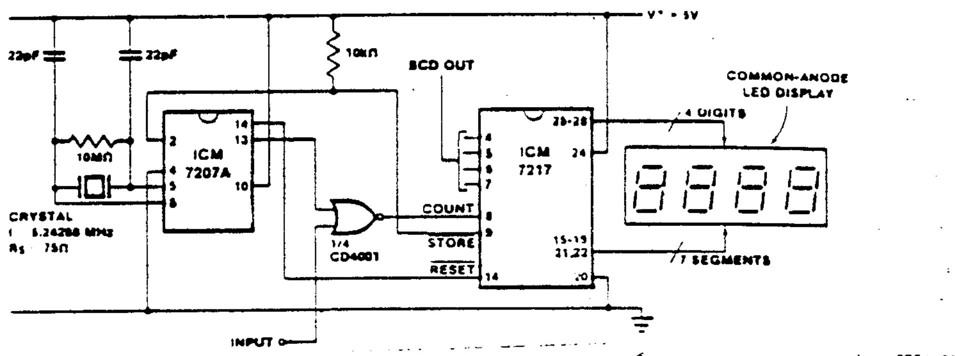


Fig. 45 Precision Frequency Counter (MHz Maximum)

4.11 GENERAL DESCRIPTION:-

(ICM 7207/A - CMOS Time base generator)

The ICM 7207/A consists of a high stability oscilattor and frequency divider providing four control outputs suitable for the frequency counter time bases. Specifically when used as a frequency counter time base in conjunction with the ICM 7208 frequency counter the four outputs provide the gating signals for the count window, store function, reset function and multiplex frequency reference. Additionally the duration of the count may be changed by a factor of 10 to provide a two decade range counting system.

The normal operating voltage of the ICM 7207/A is 5 volts. The typical power dissipation is less than 2mW when using an oscillator frequency of 6.5536 MHz with the 7207 and 5.24288 MHz with the 7207 A.

In the 7207/A the gatting output. $\overline{\text{RESET}}$, and the MULTIPLEX output provide both pull up and pull down eliminating the need for three external resistors, although , buffering must be provided if interfacing with TTL is required.

FEATURES:-

1. Stable HF oscillator
2. Low power dissipation < 2mW with 5 volt supply.
3. Counter chain has output at $\div 2^{12}$ and $\div 2^{n}$ or $\div (2^{n} * 10)$: n=17 for 7207 and 20 for 7207A.
4. Low impedence output drives $\leq$ 100 ohm.
5. Count windows of 10/100 ms (7207 with 6.5536 MHz crystal) or 0.1 / Sec.(7207 A with 5.24288 MHz crystal).

APPLICATIONS:-

1. System time bases.
2. Oscilloscope calibration generators.
3. Marker generator strobes.
4. Frequency counter controllers.

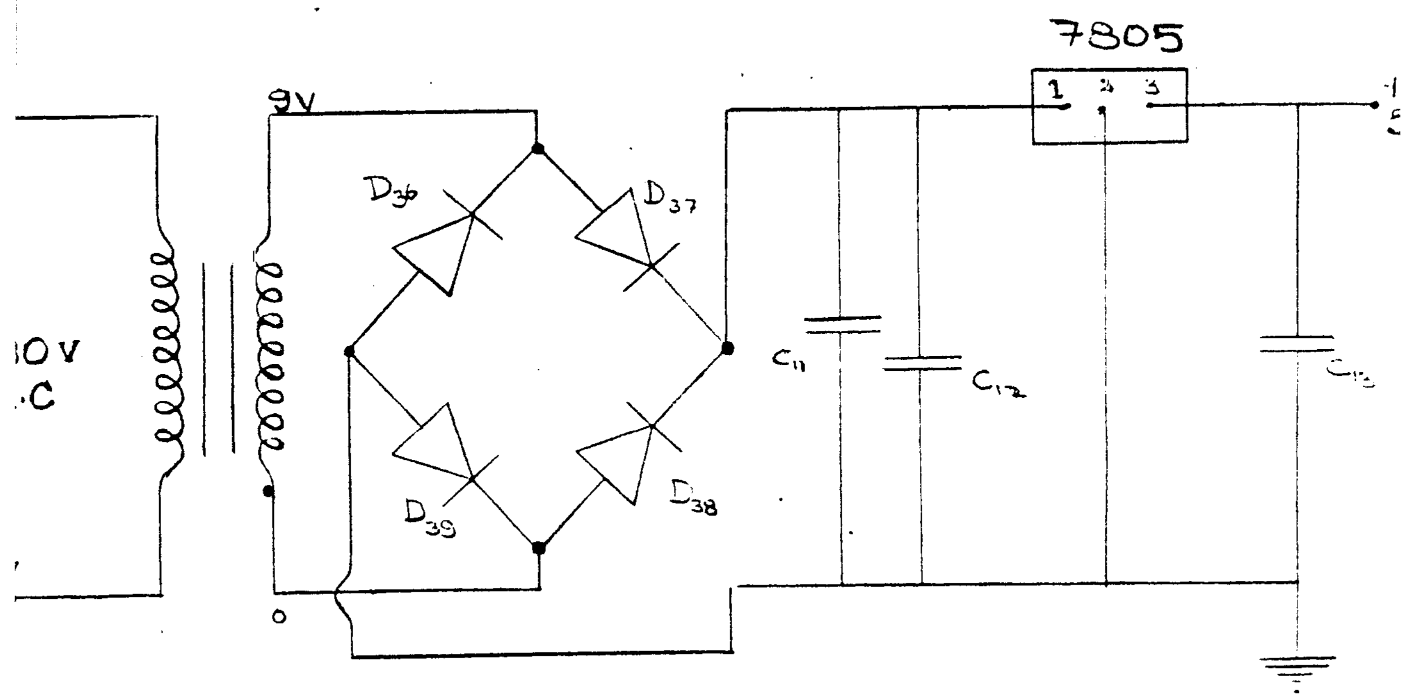
CHAPTER 5

POWER SUPPLY

For operating the circuit, +5 volt regulated power supply is necessary . The circuit for the same is explained in the following lines.

+5 VOLT POWER SUPPLY:-

The rating of the transformer is 230V/9V, 500mA is selected for this purpose. The secondary of the transformer is connected to the AC input of the bridge rectifiers. The output is filtered. That filtered output is given to the input of the regulated IC's as shown in fig 5.1. The output of the regulating IC's is a pure filtered regulated power supply.



'ig 5.1 Power Supply (+5 V)

CHAPTER 6

TESTING OF THE METER

Since 5V supply is designed within the unit, we have given direct A.C supply to frequency meter for circuit operation. The unknown frequency which is to be measured is applied to the input terminal.

For testing purpose we have given different input frequencies from a function generator and the obtained results are tabulated as follows.

Given Frequency	Read Out Frequency
70 Hz	75 Hz
2.5 KHz	2.55 KHz
7 KHz	7.37 KHz
14 KHz	14.24 KHz
18 KHz	18.07 KHz
43.67 KHz	43.70 KHz
79.3 KHz	79.53 KHz
90.11 KHz	91.34 KHz

CONCLUSION

CHAPTER 7

CONCLUSION

It is needless to say that the conventional frequency meter cannot register the frequency to the required accuracy. Since digital frequency meter developed in the project measures resolution, versatability and ofcourse range are greatly increased. Sensitivity of the prototype was 35 mVrms over 200 KHz to 1 MHz and 60 mVrms at an input frequency of 3 MHz. Average current consumption with eight displays on (indication : 8 x '8'), but the reciver mode LED's off, was at approximately 450 mA.

Assuming that the counter operates in the UP mode, and that the load oscillator frequency is higher than the recived frequency, the required preset value is first converted to its eight digit one's complement. Next the corresponding DIP switches are set until the preset appears on the displays. However, the counter cannot handle input frequencies higher than the 3.5 MHz, so that the effectively programmed offset is the IF frequency divided by the physical factor. For most SW and general coverage receivers, a ÷ 10 prescaler is suitable; for the VHF receivers a ÷ 100 prescaler.

APPENDIX

Fig (8.1) PIN CONFIGURATION OF ICM 7207

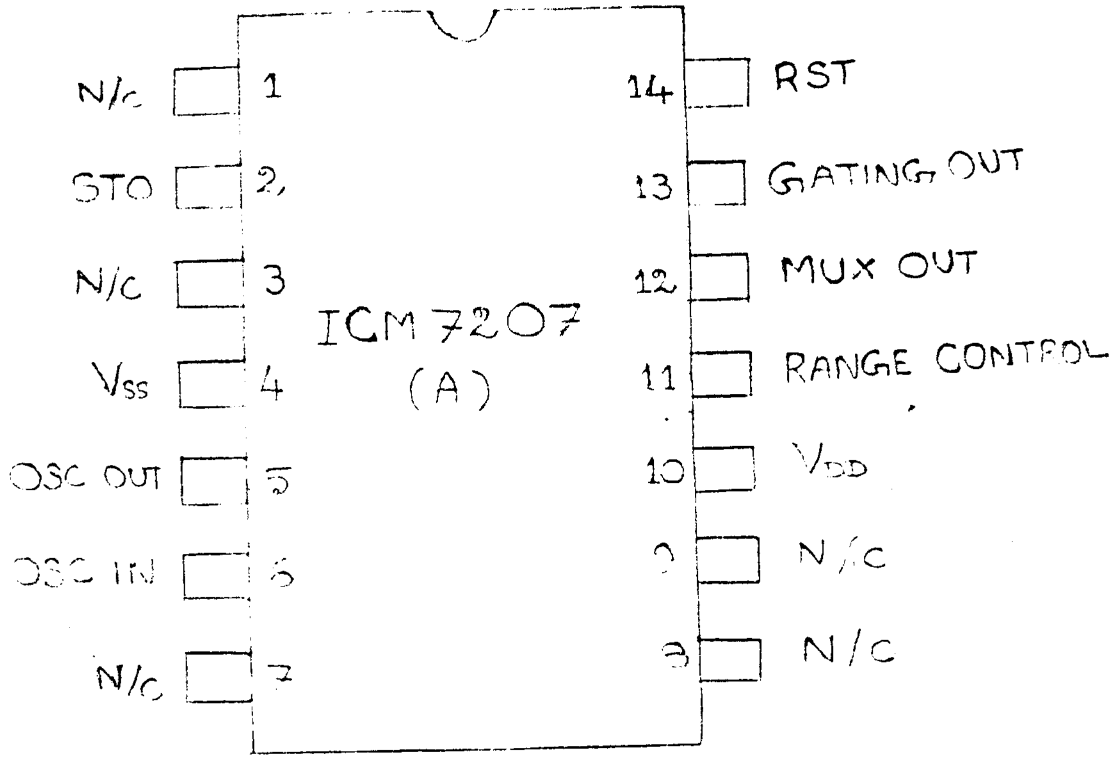


TABLE (8.1) ORDERING OF 7207 (7207A)

Order Number	Temp Range	Package
ICM 7207 IJD	-25°C to +85°C	14 pin CER DIP
ICM 7207 IPD	-25°C to +85°C	14 pin PLASTIC DIP
ICM 7207 EV/kit	—	EV/kit
ICM 7207A IJD	-25°C to +85°C	14 pin CER DIP
ICM 7207A IPD	-25°C to +85°C	14 pin PLASTIC DIP
ICM 7207A EV/kit	—	EV/kit

Those EV/kit contain just the IC and the Corresponding Crystal

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ($V_{DD}-V_{SS}$) 6.0V
Input Voltages .... $V_{SS}-0.3V$ to $V_{DD}+0.3V$
Output Voltages:
7207 .... V_{SS} to +6V
7207A .... V_{DD} to V_{SS}

Output Currents 25mA
Power Dissipation @ 25°C Note 1 .... 200mW
Operating Temperature Range .... −25°C to +85°C
Storage Temperature Range .... −65°C to +125°C
Lead Temperature (Soldering, 10sec) .... 300°C

NOTE 1: Derate by 2mW/°C above 25°C.
Absolute maximum ratings refer to values which if exceeded may permanently change or destroy the device.
NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

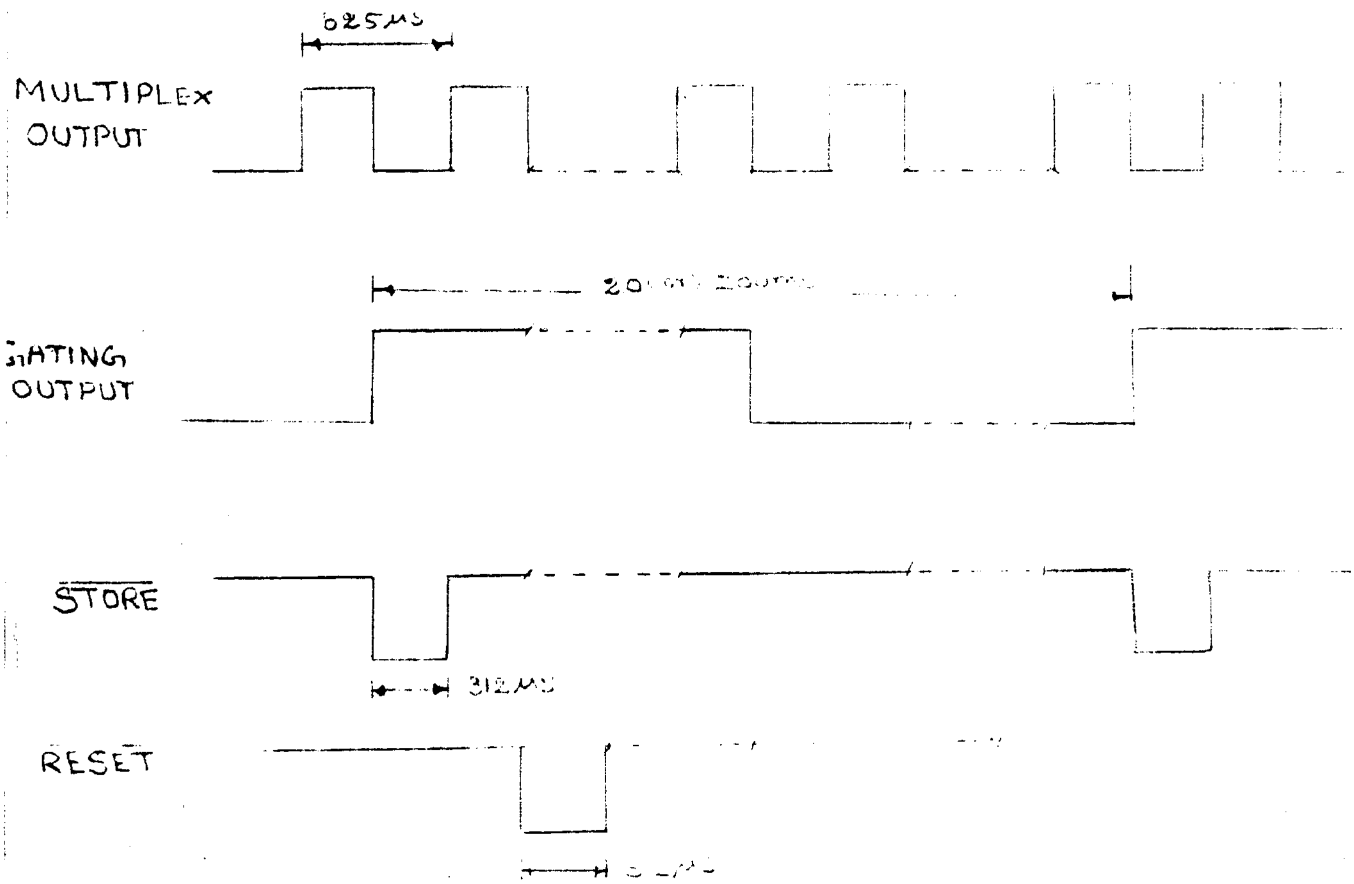
ELECTRICAL CHARACTERISTICS

f_{osc} = 6.5536MHz(7207), 5.24288MHz(7207A), V_{DD} = 5V, T_A = 25°C, V_{SS} = 0V, test circuit unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{DD}	Operating Voltage Range	−20°C to +85°C	4		5.5	V
I_{DD}	Supply Current	All outputs open circuit		260	1000	µA
$R_{ds}(on)$	Output on Resistances	Output current = 5mA All outputs		50	120	Ω
I_{OLK}	Output Leakage Currents	All outputs (STORE only)			50	µA
(R_{OUT})	(Output Resistance Terminals 12,13,14)	Output current = 50µA, 7207A only			33K	Ω
I_{pd}	Input Pulldown Current	Terminal 11 connected to V_{DD}		50	200	µA
	Input Noise Immunity		[illegible]			% supply voltage
f_{osc}	Oscillator Frequency Range	Note 2	2		10	MHz
f_{STAB}	Oscillator Stability	$C_{IN}=C_{OUT}$ = 22pF		0.2	1.0	ppm/V
r_{OSC}	Oscillator Feedback Resistance	Quartz crystal open circuit Note 3	3			MΩ

NOTES: 2. Dynamic dividers are used in the initial stages of the divider chain. These dividers have a lower frequency of operation determined by transistor sizes, threshold voltages and leakage currents.
3. The feedback resistor has a non-linear value determined by the oscillator instantaneous input and output voltage voltages and the supply voltage.

Fig(8.2) OUTPUT TIMING WAVEFORMS OF 7207



Fig(83)- PIN CONFIGURATION OF ICM 7217

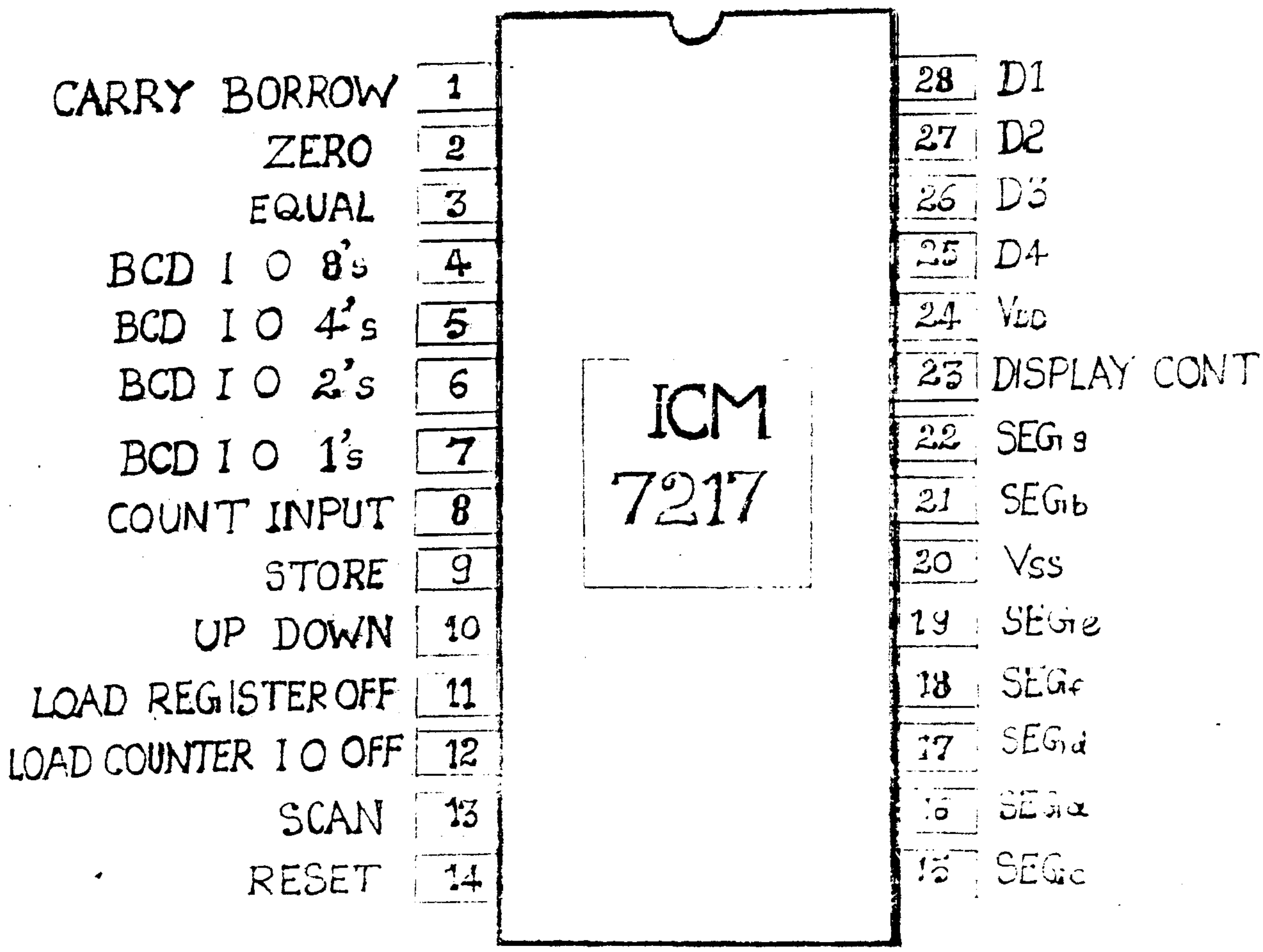


TABLE 8-4

ELECTRICAL CHARACTERISTICS (V_{DD} = 5V, V_{SS} = 0V, T_A = 25°C, Display Diode Drop 1.7V, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{DD} (7217)	Supply Current (Lowest power mode)	Display Off, LC, DC, UP/DN, ST, RS, BCD I/O Floating or at V_{DD} (Note 3)		350	500	μA
I_{DD} (7227)	Supply current (Lowest power mode)	Display off (Note 3)		300	500	μA
I_{OP}	Supply Current OPERATING	Common Anode, Display On, all "8's"	140	200		mA
		Common Cathode, Display On, all "8's"	50	100		mA
V_{DD}	Supply Voltage		4.5	5	5.5	V
I_{DIG}	Digit Driver output current	Common anode, $V_{OUT} = V_{DD} - 2.0V$	140	200		mA peak
I_{SEG}	SEGment driver output current	Common anode, $V_{OUT} = +1.5V$	−20	−35		mA peak
I_{DIG}	Digit Driver output current	Common cathode, $V_{OUT} = +1.0V$	−50	−75		mA peak
I_{SEG}	SEGment driver output current	Common cathode $V_{OUT} = V_{DD} - 2V$	9	12.5		mA peak
I_P	$\overline{ST}$, $\overline{RS}$, UP/$\overline{DN}$ input pullup current	$V_{OUT} = V_{DD} - 2V$ (See Note 3)	5	25		μA
Z_{IN}	3 level input impedance		40		350	kΩ

ELECTRICAL CHARACTERISTICS (Continued) (V_{DD} = 5V, V_{SS} = 0V, T_A = 25°C, Display Diode Drop 1.7V, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
[illegible]	BCD I/O input high voltage	ICM7217 common anode (Note 4)	1.5			V
		ICM7217 common cathode (Note 4)	4.40			V
		ICM7227 with 50pF effective load	3			V
[illegible]	BCD I/O input low voltage	ICM7217 common anode (Note 4)			0.60	V
		ICM7217 common cathode (Note 4)			3.2V	V
		ICM7227 with 50pF effective load			1.5	V
I_{PU}	BCD I/O input pullup current	ICM7217 common cathode $V_{IN} = V_{DD} - 2V$ (Note 3)	5	25		μA
I_{PD}	BCD I/O input pulldown current	ICM7217 common anode $V_{IN} = +2V$ (Note 3)	5	25		μA
V_{OH}	BCD I/O, $\overline{ZERO}$, $\overline{EQUAL}$ Outputs output high voltage	$I_{OH} = 100μA$	3.5			V
V_{OL}	BCD I/O, CARRY/BORROW $\overline{ZERO}$, $\overline{EQUAL}$ Outputs output low voltage	$I_{OL} = -1.6mA$			0.4	V
f_{in}	Count input frequency (Guaranteed)	−20°C < T_A < +70°C	0	5	2	MHz
V_{TH}	Count input threshold	(Note 5)		2		V
V_{HYS}	Count input hysteresis	(Note 5)		0.5		V
V_{CIL}	Count input LO				0.40	V
V_{CIH}	Count Input Hi		3.5			V
f_{ds}	Display scan oscillator frequency	Free-running (SCAN terminal open circuit)			10	kHz

NOTES: 1. These limits refer to the package and will not be obtained during normal operation.

2. Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to a voltage greater than V_{DD} or less than V_{SS} may cause destructive device latchup. For this reason it is recommended that the power supply to the device be established before any inputs are applied and that in multiple systems the supply to the ICM7217/7227 be turned on first.

3. In the ICM7217 the UP/DOWN, $\overline{STORE}$, $\overline{RESET}$ and the BCD I/O as inputs have pullup or pulldown devices which consume power when connected to the opposite supply. Under these conditions, with the display off, the device will consume typically 750 μA. The ICM7227 devices do not have these pullups or pulldowns and thus are not subject to this condition.

4. These voltages are adjusted to allow the use of thumbwheel switches for the ICM7217 versions. Note that a positive level is taken as an input logic zero for ICM7217 common-cathode versions.

5. Parameters not tested (Guaranteed by Design).

TABLE 8.5

PARTS LIST

RESISTORS (+ or - 5%)

R1 = 10 M

R2;R3; R9 - R16 ind = 10 K

R4 = 1 K

R5 = 27 K

R6 = 470 R

R7 = 1.5 K

R8 = 12 K

R17 = 33 ohm

R18 = 220 ohm

CAPACITORS:-

C1;C2=100 PF

C3 = 80 p trimmer

C4 = 10 UF ; 25V tantlum

C5 = 1 nF

C6 = 27 nF

C7 = 4700 uF; 10V

C8,C9;C10 = 100nF

C11 = 2200 uF

CI2 = 0.1 uF

SEMICONDUCTORS:-

D1-D33 ind = IN4148

D33,D34,D35 = LED

IC1 = ICM 7207 IPD (GE InteNsil (or) maxim)

IC2;IC3 = ICM 7217 IJI (or) ICM 7217 IPJ (GE intensil (or) mAXIM)

IC4 = 4538

IC5 = 7805

LD1 - LD8 ind = MAN72A

T1;T2 = BF494B

D36-D39-BY127

MISCELLANEOUS:-

K2;K2';K4;K4' = 16 way DIL socket with mating IDC plug.

K1;K1';K3;K3' = 10 way pin header with mating IDC socket .

S1-S8 ind = 4 way DIL switch block

X1 = 6.5536 MHz quartz crystal .

Transformer 230/9V;500mA.

REFERENCES

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   & Electronics Measurements
   & Instrumentation by A. K. Sawhney

2. Elector - India 1989.

3. Intersil Data Book.