Micro Controller Based Digital Energy Meter

Project Work
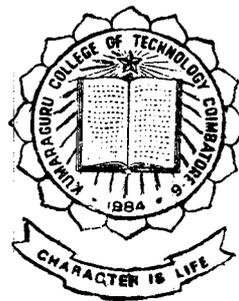
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in partial fulfilment of the requirements
for the award of the degree of
BACHELOR OF ENGINEERING
in Electronics and Communication Engineering

Department of Electronics and Communication Engineering
Kumaraguru College of Technology
Coimbatore-641 006

1994

Department of Electronics and Communication Engineering

Kumaraguru College of Technology

Coimbatore - 641 006

CERTIFICATE

This is to certify that this project entitled

Micro Controller Based Digital Energy Meter

has been done by

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Branch of the Bharathiar University, Coimbatore
During the academic year 1994

Guide

Head of the Department

Certified that the Candidate was examined by us in the Project-Work

Viva-Voce Examination held on.............................

and the University Register Number was.............................

Internal Examiner

External Examiner

ACKNOWLEDGEMENT

ACKNOWLEDGEMENT

We are solemnly indebted to the Department of Electronics and Communication Engineering. We express our gratitude to our Principal, Dr.**S.Subramanian** for the ample facilities provided to us for carrying out our project work.

It is indeed a matter of great pleasure to thank our Head of the Department, **Prof.K.Palaniswami**,M.E, M.I.E.E.E, M.I.S.T.E, F.I.E.T.E, who extended us kind co-operation and continued support during the course of our project work.

We are greatly indebted to the Kerala State Science and Technology Museum for having consented to provide us the facilities required to carry out this project. We are grateful to Mr.C.H.Abdul Buhari (Director) and Mr.Arul Jerald Prakash (Senior Technical Officer) for having assisted us in our endeavour.

A special thanks goes to our guide Miss.**G.Shanthi**,M.E. for helping us by providing constructive suggestions.

We would like to express our lasting gratitude advisor and all staff members of our department who helped us directly or indirectly in the completion of our project.

<div align="right">(Authors)</div>

SYNOPSIS

SYNOPSIS

Our project, which is the Microcontroller based energy meter is a purely digital system. The heart of the system is the MCU 8748. It also employs an analog multiplier. The inputs to this four quadrant multiplier are obtained from voltage and current sensing circuits. The use of XR2208 as the multiplier makes the system efficient and accurate.

The average power is fed to the kernel of the system which is the microcontroller. Before this, it is converted into digital signal by means of the A/D converter.The power is integrated over a time period to compute energy in Kilowatt hour using software computation routines.

A five digit seven segment display has been interfaced with the system to display the energy consumed.The use of MCU 8748 has made the system accurate and efficient.

Our project has been designed, solely to satisfy the long standing demand of the consumers for an efficient, reliable and accurate digital energy meter. This objective has been successfully achieved by our proposed energy meter.

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INTRODUCTION

CHAPTER ONE - INTRODUCTION

1.1 General

There has been rapid changes in technology all over the world. This advancement of science and technology is dependent largely upon a parallel progress in measurement techniques. One of the quickest ways to access the Science and Technological progress in a nation is to examine the measurement techniques used. As energy measurements go hand in hand with revenue and also as it forms an integral part of the nation's financial status, this meter should be fairly accurate. Furthermore, the power consumed by such meters must also be reduced.

Considering all these requirements and also taking into acccunt the errors and disadvantages of the conventional energy meters that are in use, the development of a digital energy meter with greater accuracy, reliability and flexibility has been attempted in this project.

1.2 Energy meter

Energy meters are integrating instruments and hence, measure either the total quantity of electricity in ampere hour or the total amount of energy in KWh supplied to the load circuit in a given time. Thus an energy meter differs from a wattmeter in the sense the former does not merely indicate the power or rate of energy supplied, but takes also into account the length of time for which the energy is supplied. The registrations of energy meters are always the same, for a given amount of energy supplied

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to a circuit, no matter what the instantaneous values of the power, during the time in which the energy is supplied may be.

Electrical energy developed as work or dissipated as heat may be expressed as :

$$W = \int_{0}^{t} V \times I dt$$

The unit of energy is joule or watt second. If the unit of time is taken as hour, energy is then expressed in watt hours. One unit = 1 KWH, that is, energy consumed when power is delivered at an average rate of 1000 watts for one hour.

1.3 Conventional induction type energy meter

Induction meter is almost universally used as the a.c. energy meters. The moving system of this type, in absence of control system, also continuously rotates instead of rotating through a fraction of one revolution as in the wattmeter.

Construction and theory of induction meter

An insight on the construction and theory of these meters are required to understand the inherent disadvantages of these systems.

In the induction meters, the core of electromagnets are built up from silicon iron stamping. The construction is of a very rigid form giving a constant gap between the poles of current and voltage coils. The rotor or moving system consists

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of an aluminium disc mounted on a light alloy shaft with a pinion on its upper part. There are two braking permanent magnets at the front edge of the disc. When the disc rotates in the gap between the poles of braking magnets, eddy currents are set up in the disc. The function of the recording mechanism is to record continuously a number which is propotional to the revolutions made by the disc.

Deflecting torque,	T_d	$\propto$	VI cos
Braking torque,	T_d	$\propto$	N
For steady speed,	T_B	$=$	T_D
	N	$\propto$	VI cos

Thus the total revolution in a given time is propotional to the energy supplied in that time.

Errors : The errors may be caused by the driving system or by the braking system. The errors caused by the driving system are :

i)   Incorrect magnitude of fluxes :

This may be due to abnormal values of current or voltage. The shunt magnet flux may be in error due to changes in resistances of coil or due to abnormal frequencies.

ii)   In correct phase angles :

There may not be proper relationship between the various phasors. This may be due to improper lag adjustments, abnormal frequencies, change in resistance with temperature etc.

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iii) Lack of symmetry in magnetic circuit :

In case the magnetic circuit is not symmetrical, a driving torque is produced which makes the meter creep.

The errors caused by the braking system are :

i)   changes in strength of brake magnet

ii) changes in disc resistance

iii) self-braking effect of series magnet flux

iv) Abnormal friction cf moving parts.

Compensation of Errors :

i)   Friction or low load compensation

ii)   Over lcad compensation

iii) phase error compensation

iv)   Inductive load compensation

v)   Compensation for creeping action of meter.

vi)   Quadrature adjustment

vii) Voltage compensation

viii) Temperature compensation.

Disadvantages and limitations of conventional meters:

The necessity of the evolution of an alternative for the already existing meter can be clearly understood when we consider the following limitations :

i)   This meter requires certain minimum amount of power from the signal source for their operation. Hence cannot be used for low power measurement.

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ii) Pointer type indicators cause human errors in energy measurements.

iii) Energy consumed by the load is in the order of watts and hence is a source of power wastage.

iv) Presence of moving parts like discs cause friction losses.

v) Power factor variations not taken care.

vi) Increased voltage causes saturation of iron path and hence proper linearity is lost at high voltages.

vii) Due to magnetic drag and deteriorating nature of magnetic parts, they require calibration once in 5 years.

viii) Needs more space due to the presence of mechanical and electrical components that are bulky.

ix) Wear and tear causes degradation in accuracy.

x) One of the important disadvantages is that the meter readings can be altered by illegal means.

xi) Visualisation of meter readings, especially during the night becomes a problem.

1.4 Microcontroller based energy meter :

The proposed energy meter is a completely digital instrument and hence has all the inherent advantages of a digital circuit. The signal source is not loaded as the electronic circuit provides high input impedance which is essential to reduce the error. The measuring system incorporated has the additional advantage of numerical readout. Hence it reduces human errors in reading and increases reading speed.

INTRODUCTION

The proposed meter employs simple electronic circuits to sense the supply voltage and load current. The VI cos computation is carried out using a hardware analog multiplier. The average power is then digitised using an A/D converter. Other mathematical calculation involved for computing the units consumed are performed in software with the help of 8748 - single chip microcontroller.

Advantages :

The digital energy meter has an edge over all existing energy meters. The solid state nature of this meter suits very well with all the needs of the ordinary customer as well with the electricity department due to the following advantages :

i) Use of electronic components has reduced the amount of power required. Hence it can very well measure at low power consumption.

ii) Low power requirements is a considerable source of revenue for the electricity board involved in domestic power distribution.

iii) Use of hardware multiplier increases accuracy by taking into account power factor variations.

iv) Use of 8748 microcontroller has increased the reliability and flexibility.

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v)   Wide range of operating voltages and currents can be handled by software and hardware adjustments.

vi) Versatility has been increased.

vii) Accuracy has been greatly improved.

viii) Since there are no rotating or moving parts frictional errors have been completely eliminated.

ix) Calibration is required only during installation.

x)   LED's used in display increases the visuability.

xi) Use of multiplexed display has reduced the power requirements.

xii) Future expansion is easily possible.

xiii) Light weight and attractive look.

Chapter Description :

Chapter 2 gives a general description about microcontrollers - their architecture, instruction set and wide range available.

Chapter three deals with the general description of the entire system with the block diagram. Chapter four describes in detail about the first and foremost part of our system - Signal conditioning and power sensing.

A detailed description of the microcontroller 8748, its selection from the wide range of processors available and its architecture follows in Chapter five. System design and hardware details come under the chapter six. Software computation with flowcharts are explained in chapter 7. Appendices contain the details and characteristics of the chips used in our project.

MICRO CONTROLLER

CHAPTER TWO - MICROCONTROLLERS

2.1 General

As the heart of the system revolves around the microcontrollers and the units computation is done using software, a general understanding of the architecture, their instruction sets and comparison between some microcontrollers are imperative before system description. All these features are dealt with in this chapter.

2.2 Single-chip micro computers : Architecture.

A single chip micro computer, of which microcontrollers are a subset, is a single integrated circuit that contains the five essential elements of a computer : input, output, memory, ALU and a control unit. The primary difference among the various models is the type of on-chip program storage, the two options being no program ROM, or 1024 bytes of EPROM (8748). The amount of RAM is limited to 64 (8048), 128 (8049) or 256 (8050) bytes, but this is adequate for a number of applications. The on-chip I/O is implemented as 27 programmable lines consisting of three ports of eight bits each and three test inputs that can be tested by conditional jump instructions.

A major architectural difference among microcontrollers and computers in general is the method of accessing I/O ports. The three different approaches are memory mapped I/O, separate I/O and I/O processors. Memory mapped I/O means that all I/O is

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performed as if the I/O devices were memory addresses. Separate I/O has, in addition to a read/write control line, an I/O/memory control line. This method can use identical address decoders for both I/O and memory with the final determination of which of these is accessed determined by the status of the (I/O)/memory control line.

Another important feature is that most MCU's have versatile timers that can be configured in real time by writing approximate codes to control registers. These timers can be reprogrammed as to the duration that they will measure, the type of interrupt, if any, that they will generate; and whether they will reload and continue to time the next period automatically. They can also usually be reconfigured, again in real time, to act as event counters or to count the duration between transitions on the inputs.

Some MCU's make no provision for external memory and are designed to operate autonomously. Others allow for the possibility of adding external memory. A disadvantage of this approach is that the I/O ports are lost, and this may not be acceptable. Another need for external memory is during the development phase, in which it is inconvenient continually to erase and reprogram on-chip EPROM program memory.

Comparison of various microcontrollers :

An illustration of a variety of microcontrollers available from two major manufacturers - Motorola and Intel are given below in the next page.

2.3 Instruction set :

The actual selection of the instruction set for an MCU is a complex inter action of five fundamental issues.

i) Operation repertoire : The number and complexity of the operations selected.

ii) Data types : Which types of numerical, character, or logical data types are desired as operands.

iii) Instruction formats : The structure of the instruction including the number of opcodes, number of addresses and whether it is a fixed or variable size.

iv) Registers : The amount of on chip, directly addressable storage.

v) Addressing : The modes of addressing that are allowed.

This chapter has given an insight on microcontrollers and hence the choice of microcontrollers instead of opting for microprocessor which requires the use of additional peripheral devices like program memory, data memory, 8255 PPI etc is justified.

TABLE 1.0 Capabilities of Representative-8bit microcontrollers from Two Families

Chip	RAM	ROM/EPROM EAROM/EEPROM	Clocks	I/O Ports	A/D	Timers
M68HC11A0	256	--	0.476	4x8 1x6	4/8	9
M68HC11A1	256	512 EEPORM	0.476	4x8 1x6	4/8	9
M68HC11A2	--	2048 EEPORM	0.476	4x8 1x6	4/8	9
M68HC11A8	256	8k ROM, 512 EEPROM	0.476	4x8 1x6	4/8	9
M68HC11E0	512	--	0.476	4x8 1x6	4/8	9
M68HC11E1	512	512 EEPORM	0.476	4x8 1x6	4/8	9
M68HC11E2	256	2048 (EE)	0.476	4x8 1x6	4/8	9
M68HC11E9	512	12k (ROM), 512(EE)	0.476	4x8 1x6	4/8	9

Chip	RAM	ROM/EPROM EAROM/EEPROM	Clocks	I/O Ports	A/D	Timers
M68HC11D3	192	4096 (ROM)	0.476	4x8 1x6	8	9
M68HC11F1	1024	512 (EEPROM)	0.476	4x8 1x6	8	9
Intel 8021	64	1024 (ROM)	2.5	2x8 1x4	-	2
Intel 8022	64	2048 (ROM)	2.5	3x8	-	2
Intel 8035	64	--	2.5	3x8	-	2
Intel 8039	128	--	1.4	3x8	-	2
Intel 8041	64	1024 (ROM)	2.5	3x8	-	2
Intel 8048	64	1024 (ROM)	2.5	3x8	-	2
Intel 8049	64	2048 (ROM)	1.4	3x8	-	2
Intel 8748	64	1024 (EPROM)	2.5	3x8	-	2
Intel 8y031	128	--	1	4x8	-	2
Intel 8051	128	4096 (ROM)	1	4x8	-	2
Intel 8751	128	4096 (EPROM)	1	4x8	-	2

SYSTEM DESCRIPTION

3.1 Introduction :

A general idea of the entire system can be obtained from the block diagram. It mainly consists of

i)   Power sensing and signal conditioning

ii) System control and hardware

iii) Software computation

iv) Display.

3.2. System Description

A general description about the system is given below with specifications listed at the end.

Power sensing

Real power is defined as the product of rms voltage applied and rms current in the circuit. The voltage sensing and current sensing is done as follows :

Voltage sensing:

Load voltage can be sensed by using either a step down transformer or a potential divider. A resistive potential divider is a better choice. The voltage sensing circuit has been designed to produce an output of 5V peak for an input of 260V rms.

SYSTEM DESCRIPTION

Current sensing :

A voltage propotional to the current consumed by the load is to be developed in the current sensing circuit for this we use three .1 Ω resistors and this circuit produces an output of 5V peak for a maximum load current of 15A (rms)

Analog multiplier :

The inputs to the analog multiplier are the two voltages from the current sensing and voltage sensing circuits. XR - 2208 is a chip that is used for analog multiplication. Since the multiplication is instantaneous, the power factor is taken into account.

Averaging filter :

The averaging filter is basically a low pass filter and averages power waveform that is obtained from the output of the multiplier. The output, which is the average power, is fed to the A/D converter. All the stages upto this are included in the signal conditioning and power sensing hardware. This will be dealt with in detail in Chapter four.

A/D conversion :

The average analog power is digitised using the A/D converter. The technique followed is A/D using D/A and the method used in D/A conversion is using the R-2R ladder networks. The A/D output range is from 0-FF for an input of 0-5 Volts.
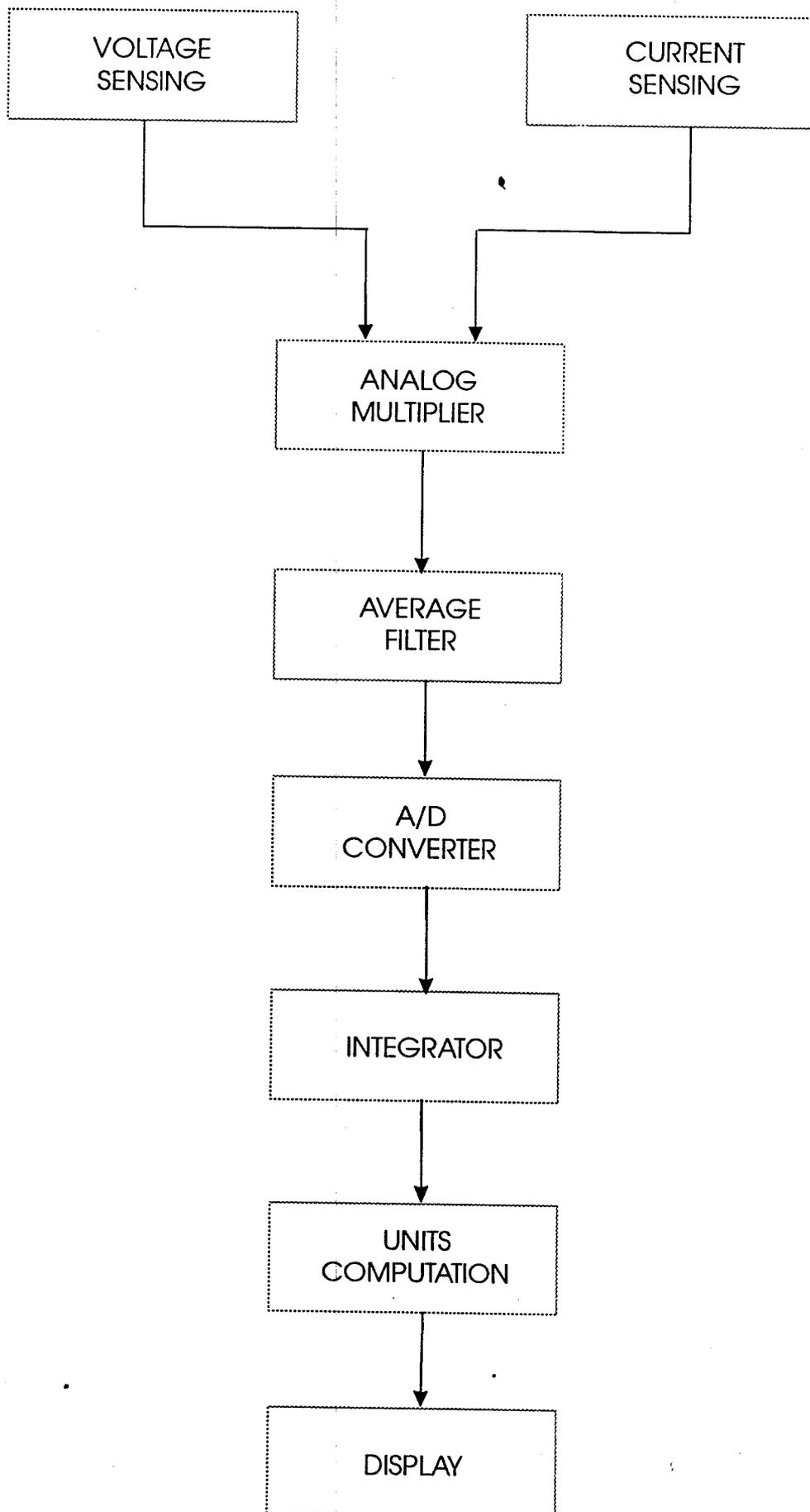
```
┌─────────────────┐                    ┌─────────────────┐
│    VOLTAGE      │                    │    CURRENT      │
│    SENSING      │                    │    SENSING      │
└────────┬────────┘                    └────────┬────────┘
         │                                      │
         └──────────────┐      ┌────────────────┘
                        ▼      ▼
                 ┌─────────────────┐
                 │     ANALOG      │
                 │   MULTIPLIER    │
                 └────────┬────────┘
                          ▼
                 ┌─────────────────┐
                 │    AVERAGE      │
                 │    FILTER       │
                 └────────┬────────┘
                          ▼
                 ┌─────────────────┐
                 │      A/D        │
                 │   CONVERTER     │
                 └────────┬────────┘
                          ▼
                 ┌─────────────────┐
                 │   INTEGRATOR    │
                 └────────┬────────┘
                          ▼
                 ┌─────────────────┐
                 │     UNITS       │
                 │  COMPUTATION    │
                 └────────┬────────┘
                          ▼
                 ┌─────────────────┐
                 │    DISPLAY      │
                 └─────────────────┘
```

Fig: System Block diagram

SYSTEM DESCRIPTION

Units computation :

    Energy is defined as the amount of average power consumed over a time period. Integration and units computation are done fully using software. Dedicated microcontroller 8748 is used for this. The unit of energy is KWH.

Display :

    The energy obtained as units is given for display. The display used is a 5 digit seven segment LED. Common anode configuration is employed. The display section will display from 0000.0 to 9999.9.

Energy meter specifications

Supply voltage	:	220 - 15% + 10%
Supply Frequencies	:	50 + 5% Hz
Operating temperature	:	$0 - 55^{0}$ C
Humidity	:	95%
Power consumption	:	10 VA
Load voltage	:	260 V
Load current	:	15 V
Operating life of meter	:	Infinite
Calibration	:	Required only during installation.

SYSTEM DESCRIPTION

Power supplies : Power supplies required are

i)   + 12 V and - 12 V split supply

ii) + 5 V supply

iii) + 2.71 V reference voltage

These power supplies are generated using three terminal IC
regulators IC 7812, IC 7912 and IC 7805.

The dual power supply is used for XR - 2208, LM 324 and
LM 339. A 5V supply is used for MCU 8748, 74 HC 373, 7414 and
7406.

The next chapter deals in detail about power sensing and
signal conditioning circuits.

POWER SENSING AND
SIGNAL CONDITIONING

CHAPTER FOUR - POWER SENSING AND SIGNAL CONDITIONING

4.1 Introduction

Power sensing forms the first major building block of our project. All further calculations are based on this part. Hence utmost care is taken to maintain a very high degree of accuracy and sensitivity. Power sensing, is divided into two main parts : Voltage sensing and current sensing. In the power sensing and signal conditioning part of the hardware op-amp has been used. Op-amps are employed for the reasons stated below :

i)   Provides gain adjustments

ii)   Offers low output impedance

iii) acts as a buffer

iv)   prevents loading.

The op-amp used in this particular case is LM 324.

4.2 LM 324 ;

This series consists of four independent high gain, internally frequency compensated, operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltages.

The advantages of using this Op-amp are :

i)   It eliminates use of dual supplies

ii)   Four internally compensated op-amps in a single package.

iii) Allows directly sensing near ground.

POWER SENSING AND SIGNAL CONDITIONING

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iv) Compatible with all forms of logic

v) Power drain suitable for battery operation.

The features of the op-amp LM 324 include internal frequency compensation for unity gain, wide band width of 1 MHz, low input biasing current, very low supply current drain etc. Further electrical characteristics are given in the Appendix.
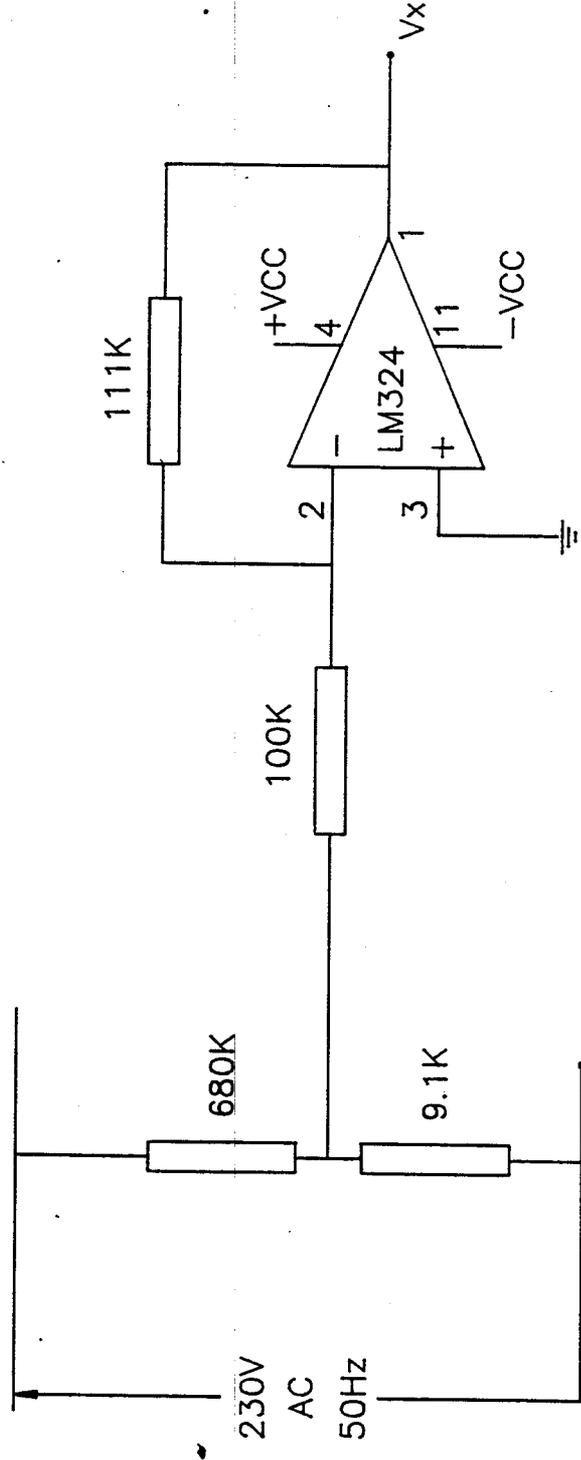
Voltage sensing :

The voltage can be stepped down either by a step down voltage transformer or by a potential divider network. The step down voltage transformer apart from being costly is also bulky and hence the latter method is adopted.

The voltage is stepped down using a resistive potential divider network of 680 K and 9.1 K. The output is taken across the 9.1 K resistor. The exact output voltage can be obtained using the op-amp gain adjustments.
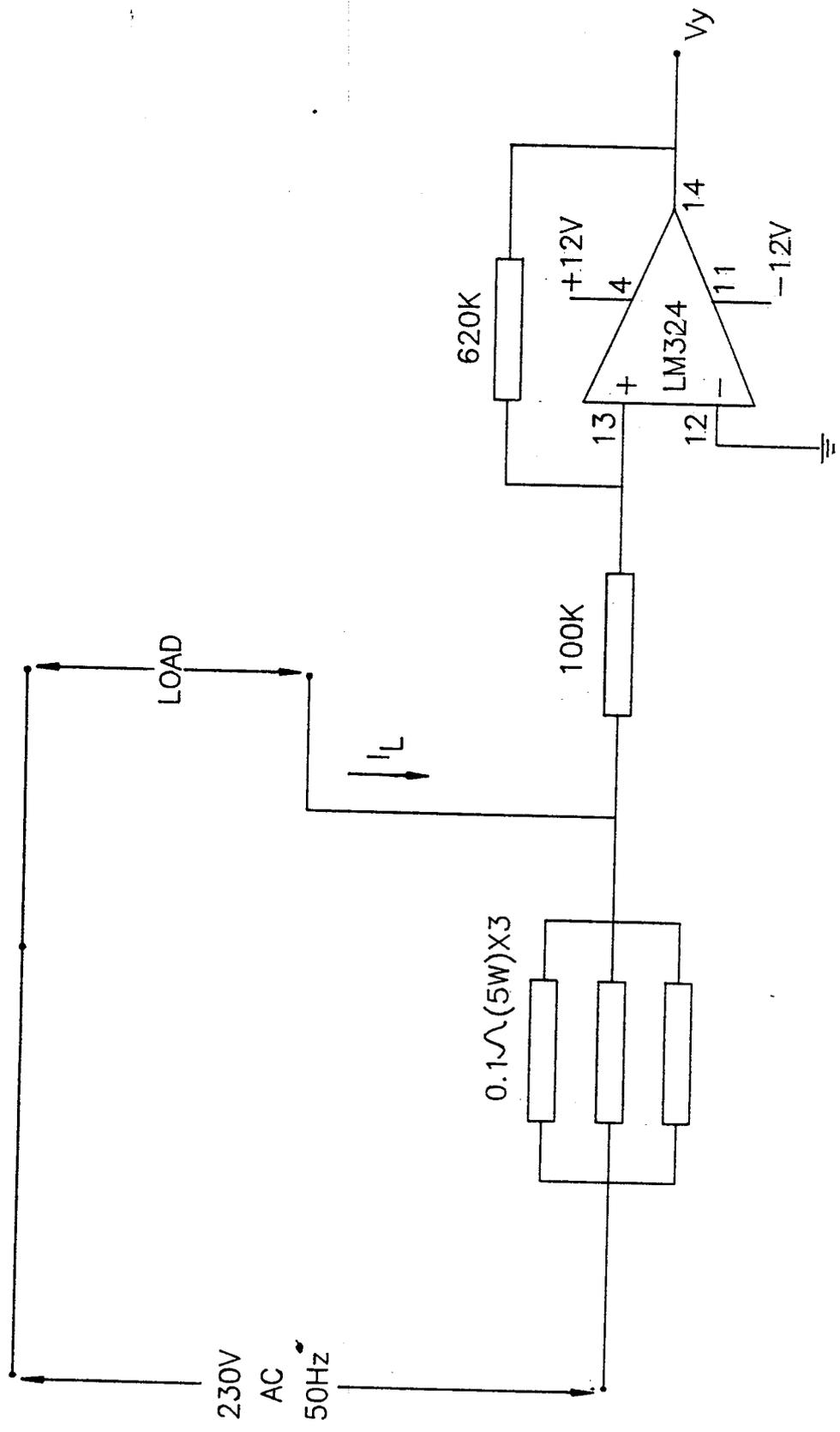
Current sensing :

The other signal that is sensed is the current. Current here is measured using the current to voltage converter.

This system has been designed to support a load of maximum 15 A rms. The choice of resistances involved in this circuit are made taking into consideration both the value and its power rating, given the large current that it has to handle.

+VCC

4

1

Vx

2

−

LM324

111K

3

+

11

−VCC

100K

680K

9.1K

230V
AC
50Hz

VOLTAGE SENSING

CURRENT SENSING
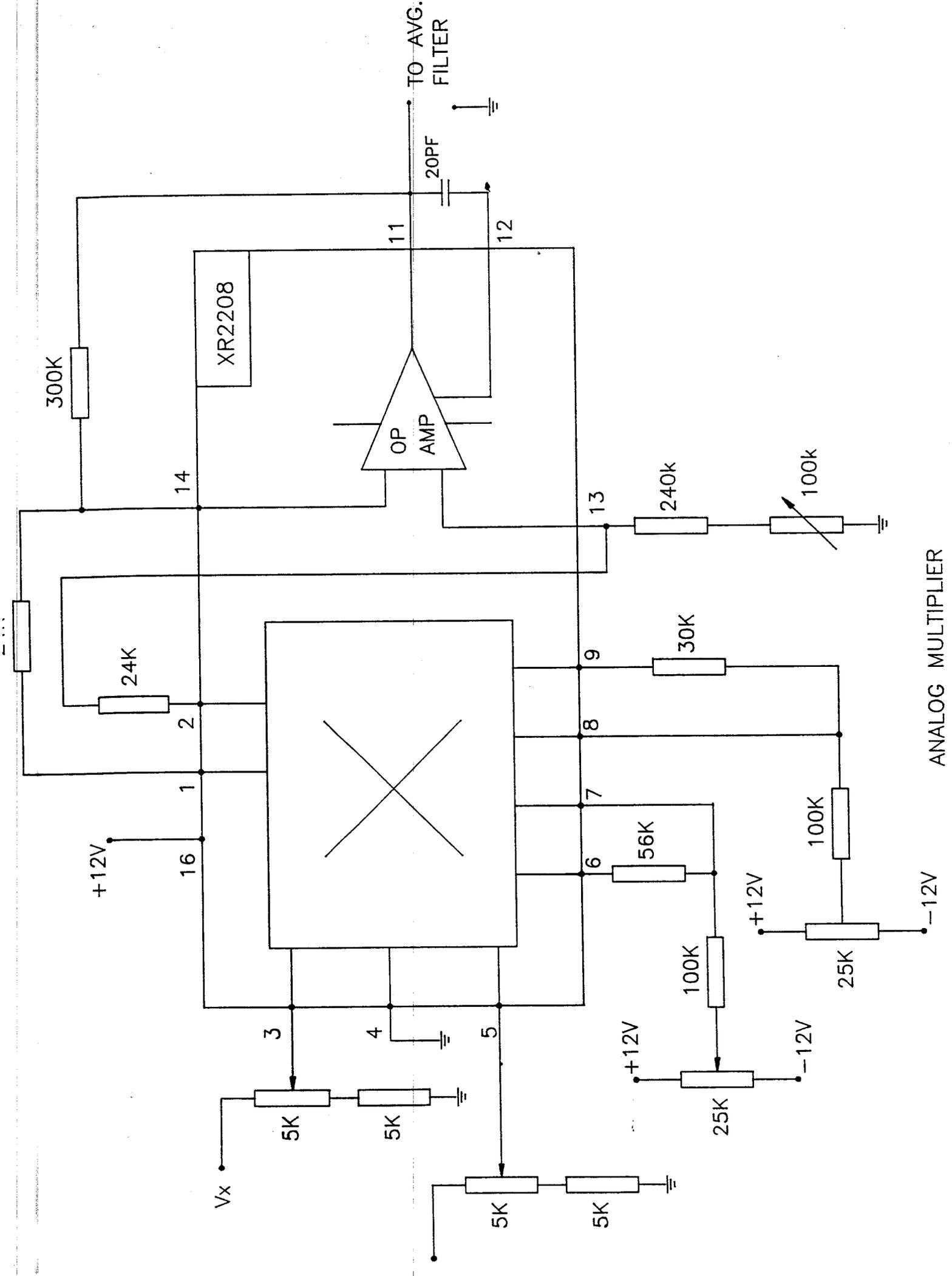
POWER SENSING AND SIGNAL CONDITIONING

The resistors used are three .1 Ω with a power rating of 5 watts. The current flowing through the load is equally divided among these three resistors. The voltage developed across these resistances is propotional to the load current which is then adjusted such that an output of 10V p-p is obtained for a maximum of 15 A rms.

Analog multiplier :

A multiplier is an active network the output of which is propotional to the product of two input signals. The output is basically given by Z = Kxy where x and y are the two input signals with K being the multiplier scale factor. All the signals are measured with respect to ground.
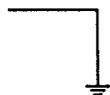
The signals can be voltages or currents. In our case both the signals are voltages from the output of the current and voltage sensing circuits. For ideal circuits, the output voltage is zero if either input voltage is zero. In other words, the offset, drift and noise voltages are also zero.

The multiplier may be analogue or digital. As the main emphasis has been laid on accuracy, analogue multiplication is chosen. This, apart from multiplying the two signals accounts for the power factor as well. Analogue multipliers are most versatile building blocks.

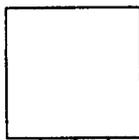ANALOG MULTIPLIER

7912

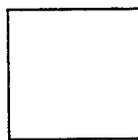1 3 2

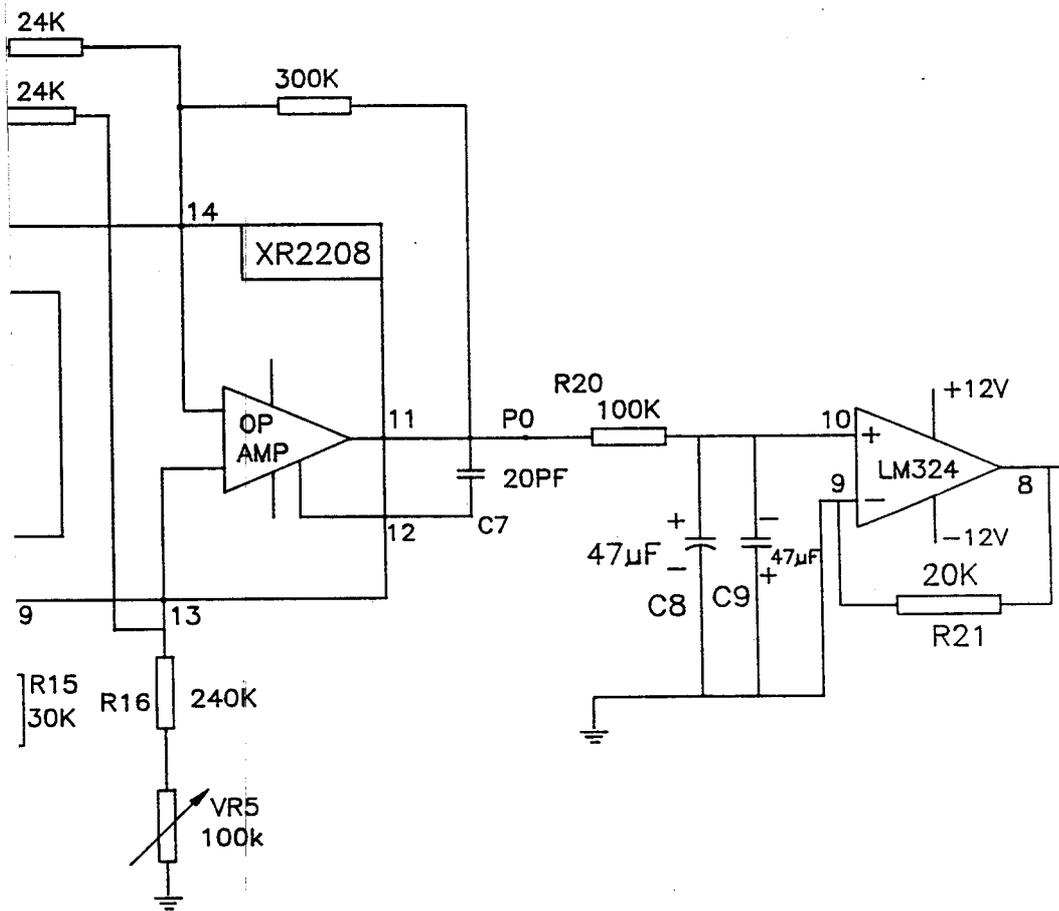GND 1/p 0/p

12V

12V

7812

1 3 2

1/p GND 0/p

24K

24K

300K

14

XR2208

OP
AMP

11

PO

R20
100K

10

+12V

LM324

8

20PF

9

C7

12

9

+
47µF

C9

+
47µF

20K

R21

9

13

C8

R15
30K

R16

240K

VR5
100k

S

POWER SENSING AND SIGNAL CONDITIONING

They may be used for the following applications.

*   Multiplication, division, squaring and square root extraction as required in instrumentation and control.

*   Frequency and phase detections, amplitude, frequency and phase modulation.

*   Gain control stages, bandwidth control stages, frequency multiplication etc.

A four quadrant multiplier is one that can accept input voltages of either polarity and can produce output voltages of both positive and negative polarity. In contrast a one quadrant multiplier can operate with only one polarity of input and consequently the output voltage will have only one possible polarity.

4.3 XR - 2208 :

General description :

The XR - 2208 operational multiplier combines a four quadrant analog multiplier, a high frequency buffer amplifier and an operational amplifier in a monolithic circuit that is ideally suited for both analog computation and communication signal processing equipment. For maximum versatility the multiplier and operational amplifier sections are not internally connected. They can be interconnected with a minimum number of external components to perform arithematic computations.

POWER SENSING AND SIGNAL CONDITIONING

This four quadrant multiplier has fully differential x and y inputs and outputs. Both inputs have 3 MHz dynamic response and 100 MHz trans conductance bandwidth. The operational amplifier features high gain and a large common mode range. The device is powered by 4.5 V to 16 V split supplies. Current and voltage levels are internally regulated to provide excellent power supply rejection and temperature stability. The XR - 2208 operates over a 0^0 to 70^0 temperature range.

Multiplier Characteristics

Offset terms

Since output of a multiplier is a function of two independent input variables, its operating characteristics must be defined with respect to the offset voltages associated with each input and also include any offset associated with the output stage. When these finite offset terms are considered, the actual transfer function becomes

$$Vs = K(Vx + \phi x)(Vy + \phi y) + \phi_o$$

Where ϕx and ϕy are the offset associated with the x and y i/ps respectively, and ϕ_o is the output offset voltage of the multiplier. This implies that for high-precision multiplication, four seperate adjustments are required, three of these to 'null' out the internal offset and the fourth to set the multiplier gain.

POWER SENSING AND SIGNAL CONDITIONING

In most applications, the multiplier gain is set at 0.1. This permits either or both i/p to have a value around the 10V range without causing the output to exceed 10V. Once the offsets have been trimmed and the value of K set to 0.1, the transfer function becomes

$$Vz = \frac{Vx\ Vy}{10}$$

An actual multiplier will, however, have an output voltage given by

$$Vz = \frac{(Vx + \phi x)\ (Vy + \phi y)}{(10\ V)\ \ \ \ \ (1 + E)} + \phi_0$$

Where E is the error in K. Most multipliers have provision for trimming or nulling out the offset voltages and the scale factor so that the various error terms can be reduced down to the range of 0.1%. The offset voltages can be nulled out at a given operating temperature so that only the subsequent drift in the temperature and the long term offset voltage drift will contribute to the offset error. The equation also contains non linear terms in $Vx^n\ Vy^n$. However these are much more difficult to compensate for, and will represent the ultimate limitations on the accuracy of the multiplier.

The temperature stability is normally measured in terms of the temperature drift of the null-offset term ϕ_c (in mV/C) and the scale factor K (in ppm/c).

POWER SENSING AND SIGNAL CONDITIONING

Accuracy : Accuracy is specified as the deviation of the actual o/p from that of the ideal, for any combination of x and y i/ps within the specified operating range of the multiplier.

Therefore if a multiplier with + 10V output swing is specified with 0.5% full scale accuracy, the o/p would be within + 50 mV of its predicted value. Accuracy normally, ranges from fraction of a percent to 3 percent.

Linearity : The accuracy of a multiplier is usually expressed in terms of its linearity. A graph of the output voltage Vz as a function of one of the input voltages such as Vx is obtained, with the other input voltage kept at some constant value. The input voltage that is kept constant is usually set to its maximum or full-range value.

Linearity is most commonly defined as the maximum percentage deviation from best straight line data at the output. Corresponding to equal magnitude inputs at the x and y terminals.

Linearity error is plotted different for x and y inputs, when these plots are combined, they present an error surface. Hence linearity error can also be defined as the maximum absolute deviation of the error surface.

POWER SENSING AND SIGNAL CONDITIONING

Some times, linearity error is defined as a percentage of full scale output as the maximum deviations from linearity occur at the extreme ends of the multiplier dynamic range. Thus, if a multiplier has 10V inputs and an output given 1% linearity would mean a maximum deviation of + 100 mV from a 'best fit' straight line.

Linearity error cannot be reduced and places a lower limit on the multiplier accuracy.

Typically, linearity error values for IC analogue multiplier with a full - scale output voltage of 10V are generally in the range 0.1 to 1% with the lower figure being representative of multiplier in which the offset voltages have been trimmed.

Squaring Mode Accuracy : This is another index of multiplier accuracy. In this case both inputs are tied together, ie, $V_x = V_y$, and a graph of $V_1 = V_x = V_y$ is obtained as shown in figure. The Squaring mode accuracy is the maximum deviation of the output voltage from an ideal best fit square law curve, usually expressed as a percentage of the full scale output voltage.

Band Width : Band width indicates the high frequency capability of an analog multiplier. The definition depends upon the application of multiplier. Hence several band width are defined as below.

POWER SENSING AND SIGNAL CONDITIONING

Small signal 3 - dB band width (fo) : It is defined as the frequency fo, at which the output is 3 dB down from its low frequency value, for a constant input level. This is seperate for the x-channel and the y-channel. fo, thus indicates the frequency at which the amplitude is in error by 3 dB.

1 Present absolute error band width (f1%) : It is defined as the frequency where the output Z (jw) is down by 1 percent from its low frequency value. Thus it is the frequency at which the amplitude is in error by 1%.

For multiplier co-integrated with output converter, the full power frequency f_{fv} is usually, also specified.

1 Percent phase vector error band width : It is an alternate band with criterian and is the frequency where the o/p in phase is shifted by 0.57^{o} or 0.01rad from its low frequency value, resulting in 1 percent vector difference between Z(0) and Z (jw). The vector error band width is always much smaller than the corresponding absolute error band width.

3 phase shift band width : It is the frequency where the net phase shift across the multiplier is 3° .

Transconductance band width : It is the frequency where the transconductance of the multiplier drops 3 - dB below its low frequency value. This band width defines the frequency range for operation as a phase detector or synchronous AM detector.

POWER SENSING AND SIGNAL CONDITIONING

Feed through : It is the amount of peak to peak voltage with one input grounded. The ideal multiplier provides no output voltage if either input voltage is Zero. Real multiplier always exhibit a small residual signal under such conditions, no matter how thoroughly they have been trimmed.

Two values of feed - Through are specified one with the X input grounded and another with the y input grounded. The test voltage applied to the ungrounded input is a low frequency sine wave. Thus the feed through voltages are the peak - to peak voltages at the output, as measured under the above conditions.

Feed-through provides a measure of the output error due to the input signal being coupled to the output.

Zero Trim : This is the ability to set the output voltage to zero if one or both inputs is grounded.

Quadrant : This indicates whether the device will accept bipolar signals. If it accepts only positive signals, it is a first quadrant device; if it accepts only one bipolar signal, it is a two quadrant device; if it accepts two bipolar signal, it is a four quadrant device.

POWER SENSING AND SIGNAL CONDITIONING

Scale factor (k)

Scale factor is defined to be the proportionality constant, relating the output voltage and the product of the input voltages.

$$K = \frac{Vz}{Vx \ Vy}$$

In above equation, K is found at particular value of Vx, Vy and Vz.

The slight temperature dependence of K is specified as

$$\frac{\triangle K/K}{\triangle T} \ \% \ per \ ^{\circ}C \ and$$

its slight supply voltage dependence is specified as

$$\frac{\triangle K/K}{\triangle Vs} \ \% \ per \ V$$

Scale Factor Trim : It indicates the ability to set the output voltage to its positive and negative maximum, Which are equal in magnitude.

The power supply of the multiplier is usually ± 15V, it is desirable to limit the output to ± 10V. Since each input can reach 10V, the scale factor is chosen as 1/10, there by limiting the output to the desired range.

POWER SENSING AND SIGNAL CONDITIONING

Study of XR 2208 :

The pin details and the trimming procedure that is followed when using XR - 2208 are dealt with in this section.

4.4 Description of circuit controls :

The x and y inputs to the multiplier are applied to pins 3 and 5 respectively. The third input - pin 4 is common to both x and y portions of the multiplier. This pin in most applications serves as a 'reference' or ground terminal. The typical bias current at the multiplier input is 3μ A for the x and y input and 6μ A for the common terminal. In ckt. applications such as synchronous AM detection or "frequency doubling" where the same input signal is applied to both x and y inputs, pin 4 can be used as the input terminal since it is common to both x & y sections of the multiplier.

Multiplier Outputs (Pin 1 & 2)

The differential output voltage Vo, across these terminals is proportional to the linear product of voltage Vx and Vy applied to the inputs Vo can be expressed as :-

$$Vo = \frac{25}{(Rx)\ (Ry)}(Vx\ Vy)$$

where all the voltages are in volts and all the resistors are in $K \Omega$. Rx and Ry are gain control resistors for x and y sections of multiplier.

POWER SENSING AND SIGNAL CONDITIONING

The common mode dc potential at the multiplier output is approximately 3 volts below the positive supply. One of the multiplier outputs is internally connected to a unity gain buffer amplifier input for high frequency applications. In most analog computation operations, such as multiplication, division etc. Pin 1 and pin 2 are dc coupled to op-amp inputs. The final output, Vz is then obtained from the op-amp output at pin 11.

X & Y Gain Adjust (Pins 6,7,8,9)

The gains of the X & Y sections of the multiplier are inversely proportional to resistors Rx and Ry connected across the respective gain terminals. The multiplier conversion gain, Km can be expressed as :-

$$Km = \frac{25}{RxRy}(Volts)^{-1}$$

X & Y offset adjust (Pins 7 & 8)

Two of the gain control pins 7 & 8 are also used for adjusting x & y offsets. The typical adjustment circuitry which can be connected to the pins to null out input offsets is shown in Appendix   .

Op-amp Inputs (Pin 13 and 14)

Pin 13 is the non-inverting and pin.14 the inverting inputs for the op-amp section. In most multiplier applications, the terminals are connected to the multiplier outputs. If these terminals are not used, they should be grounded.

POWER SENSING AND SIGNAL CONDITIONING

Op-Amp compensation (Pin 12)

The op-amp section can be compensated for unconditional stability with a 20 pf capacitor connected between pin 11 and pin 12.

Op-Amp Output (Pin 11)

This terminal serves as the o/p for the op-amps section. It is internally protected against accidental short ckt. conditions and can sink or source 10 mA of current into a resistive load.

Buffer Amplifier Output (Pin 15)

The buffer amp is internally connected to the multiplier sections. It has unity voltage gain, and provides a low impedance output at pin 15 for the multiplier sections.

Application Information

Multiplication

For most multiplication applications, the multiplier and op-amp sections are interconnected as shown in Fig included in Appendix to provide a single ended analog output with a wide dynamic range. The ckt of fig. provides a linear output swing of 10V for maximum input signals of 10V, with a scale factor K=0.1. The trimming procedure for the ckt is as follows :-

1. Apply OV to both inputs and adjust the o/p offset to OV using the o/p offset adjust.

POWER SENSING AND SIGNAL CONDITIONING

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2.   Apply   20 Vp-p at 50 Hz to the x - input and   OV   to   the

input.   Trim   the   Y-offset adjust for Y-offset.   Adjust   for

minimum peak to peak o/p.

3.   Apply   20 Vpp to the Y-input   and OV to the   x-input.   Trim

x-offset adjust for minimum peak to peak output.

4.   Repeat step 1.

5.   Apply + 10 V to both inputs and adjust   scale   factor   for

Vo=+10V. This step may be repeated with different amplitude   and

polarities of input voltages to optimize   accuracy over the

entire range of input voltages, or   over any specified portion of

input voltage range.

     The   circuits and curves associated   with XR-2208 have   been

grouped in Appendix.

4.5 Averaging Filter :

     Energy   is defined as the average power over a   period of

time. Hence the output power waveform attained from   the

multiplier is averaged using an averaging filter. The   gain   of

the filter is chosen such that for an input of 260 V rms and 15 A

rms it gives 5 V dc output.

     In the circuit used for averaging two capacitors are

connected in parallel with opposite polarities. One capacitor

AVERAGE FILTER

Circuit labels:

AVERAGE POWER (P_c^1)

8

4 +

11 −

LM324

10 +

9 −

20K

91K

100K

47μF / 25V

MULTIPLIER OUTPUT (Po)
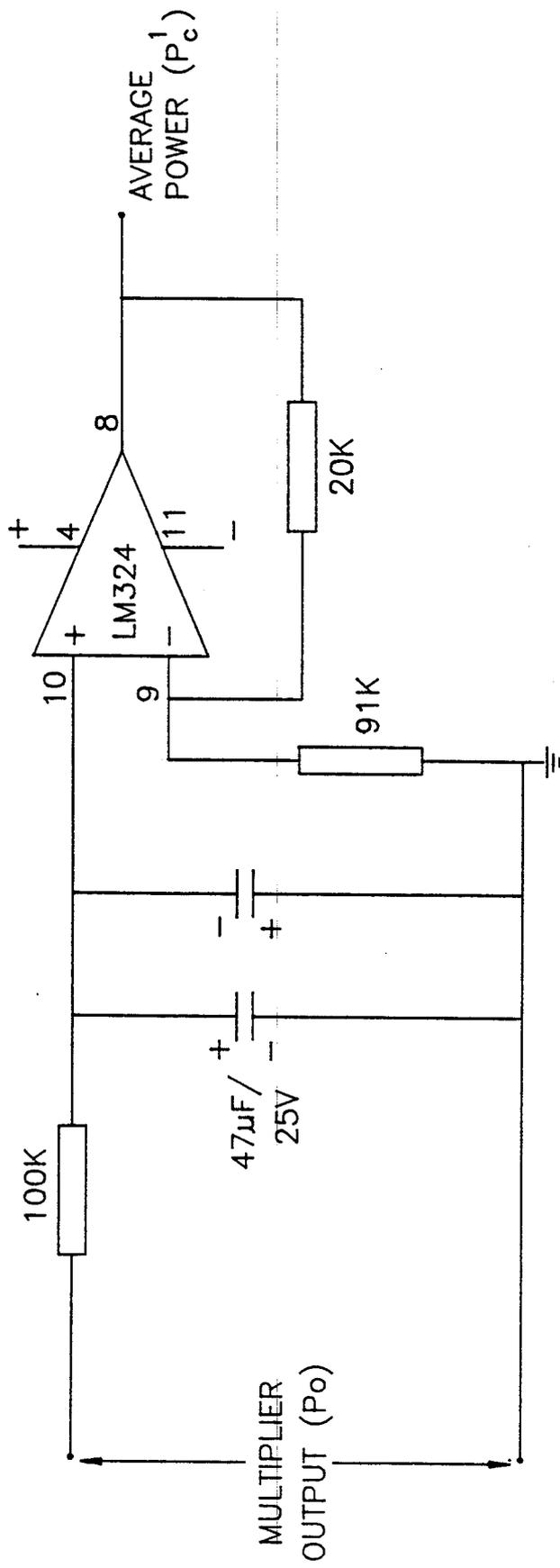
POWER SENSING AND SIGNAL CONDITIONING

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charges upto 31.8% of positive peak and the other capacitor charges upto 31.8% of the negative peak. The difference between these two voltages is the average power which is fed to the op-amp. In this the average power is amplified so as to obtain a 5 Volts dc for maximum load current and maximum voltage.

Average power = .318 (Vpp - Vnp)

where Vpp is the positive peak voltage

Vnp is the negative peak voltage.

μC 8748

CHAPTER FIVE - MICROCONTROLLER 8748

5.1 Introduction

The heart of the system and the software computation re-volves around the microcontroller. A brief introduction to the microcontrollers, their architecture and instruction set has already been given in chapter 2. A more detailed understanding of MCU - 8748 is done in this chapter.

Some benefits that arise a from having a one-chip microcontroller are as follows :

i) Small size and power for the controller portion of an instrument.

ii) The opportunity to identify one chip as a kernel for the digital portion of an instrument for test purposes.

iii) The definition of an efficient instruction set with 70% one byte instructions.

5.2 Selection

It is indeed a great task in selecting a particular controller for our needs from the wide range of MCU's available today. Most of the MCU available are 8 bit like Intel 8048 and 8051 series, Motorola M6801 series etc except TMS 1000 from Texas instruments which has a word length of 4 bits.

Of all these microcontrollers, a final choice was made on 8748 as this has been designed to be an efficient controller as

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well as an arithmetic processor. The 8748 chip has extensive bit handling capacity as well as facilities for both binary and BCD arithmetic. It has a program memory of 1 K bytes and a data memory of 64 bytes. It has 2 ports of eight pins each and a bidirectional databus. It also has an inbuilt timer/counter. With all these, as well as the low cost of this MCU, the choice has been made.

5.3 Architecture of 8748

Intel single chip 8748 is pin compatible with 8048 which is considered to be the head of Intel's-MCS-48 family of MUCs. The instruction set for both of them are same.

8748 is provided with a 8-bit CPU, 1 K x 8 ROM programe memory, 64 x 8 RAM data memory, 27 I/O lines and an 8-bit timer/event counter. The main advantage is that either the capacity of program memory or data memory or even both can be expanded by connecting memory chips externally.

MCU - 8748

ARCHITECTURE

ARITHMETIC SECTION

The arithmetic section of the processor contains the basic data manipulation function of 8748 and can be divided into the following blocks :

1.   Arithmetic Logic unit

2.   Accumulator

3.   Carry flag

4.   Instruction decoder.

Instruction Decoder

The operation code portion of each program instruction is stored in the instruction decoder and converted to outputs which control the function of each of the blocks of the Arithmetic section. There lines control the source of data and destination register as well as the function performed in the ALU.

ALU

The ALU accepts 8-bit data words from one or two sources and generaly an 8-bit result under control of the instruction decoder. The ALU can perform functions like Add with or without carry, AND, OR, EX-OR, Increment/Decrement, Bit complement, Rotate left, right, swap nibbles BCD decimal adjust etc. If the operation performed by the ALU results is a value represented by more than 8-bits, a carry flag is set in the program status word.

MCU - 8748

ACCUMULATOR

Accumulator is the single most important data register in the processor, being one of the sources of input to the ALU and often the destination of the result of operations performed in the ALU. Data to and from I/O ports and memory also normally passes through the accumulator.

Program Memory

Resident program memory consists of 1024, 2048 & 4096 words eight bits wide which are addressed by the program counter. In the 8748 this memory is user programmable and erasable EPROM. There are three locations in program memory of special importance. They are :

1. Location 0 : Activating the reset line of the processor causes the first instruction to be fetched from location 0.

2. Location 3 : Activating the interrupt input line of the processor causes a jump to subroutine at location 3.

3. Location 7 : A timer/counter interrupt resulting from timer/counter overflow causes a jump to subroutine at location 7.

Therefore the first instruction to be executed after initialization is stored is location 0, the first word of the interrupt service subroutine is stored in location 3 and the

first word of a timer/counter service routine is stored in location 7.

Program memory can also be used to store constants as well as program instructions. The program memory map has been shown in Appendix.

Data Memory

Resident data memory is organized as 64 words 8-bit wide. All locations are indirectly addressable through either of RAM or the pointer registers which reside at address 0 and 1 of the register array. In addition, the first eight locations of the register array are designated as the working registers and are directly addressable by several instructions. Since these registers are easily addressed they are used mostly to store more frequently accessed intermediate results.

By executing a register bank switch instruction SEL RB loc 24 - 31 over designated as working registers in place of loc 0-7 and are then directly addressable. This second bank of registers may be used as an extension of the first bank or unserved for use during interrupt service subroutines allowing the registers of bank 0 used in the main. program to be instantly 'saved' by a bank switch. Registers RO & R1 are a part of the working register array, bank switching effectively creates two more pointer registers which along with RO & R1 can be

MCU - 8748

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effectively used to access up to four separate working areas in RAM at a time.

RAM locations (8-23) also serve a dual role in that they contain the program counter stack. These locations are addressed by the stack pointer as well as by the pointers R0 & R1. The data memory map has been shown in Appendix B.

Input/Output :

It has got 27 lines which can be used for input or output functions. These lines are grouped as 3 ports of 8 lines. These serve as either I/P, O/P or bidirectional ports and 3 test I/Ps which can alter the program sequences when listed by conditional jump instruction.

Ports 1 and 2 are each 8-bit wide and have identical characteristics. As input ports these are non-latching ie., inputs must be present until read by an input instruction. The lines of port 1 and 2 are called quasi-directional because of a special output circuit structures which allows each lines to serve as an I/P, O/P or both, even though O/Ps are statically latched. Each lines is continuously pulled up to Vcc through a resistive device of relatively high impedance.

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It is important to note that the ORL & ANL are read/write operations. When executed, the C "reads" the port, modifies the data according to the instructions, then "writes" the data back into the port. The "writing" enables the low impedance pull-up momentarily again even if the data was unchanged from a "1". This specifically applies to configuration that have inputs and 1 outputs mixed together on the same port.

BUS

Bus is also an 8-bit port which is a true bidirectional port with associated input and output strobes. If the bidirectional feature is not needed, bus can serve as either a statically latched output port or non-latching input port. I/P & O/P lines on this port cannot be mixed however.

As static port, data is written and latched using the OUTL instruction and inputted using the INS inst. The INS and OUTL unit generate pulses on the corresponding RD and WR output strobe lines, however, in the static port mode they are generally not used. As a bidirectional port the MOVX instructions are used to read and write port. A write to the port generates a pulse on the WR output line and output data generates a pulse on the RD output line and input data must be valid at the trailing edge of RD. When not being written or read, the BUS lines are in a high impedence state.

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Test & Int. Inputs

Three pins serve as inputs and are testable with the conditional jump inst. These are T0, T1 & INT. These pins allow inputs to cause program branches without the necessity to load an input port into the accumulator. The T0, T1 & INT pins have other possible functions as well.

Program Counter & Stack

The program counter is an independent counter and the program counter stack is implemented using pairs of registers in the data memory array. The program counter is initialized to zero by activating the RESET line.

An interrupt or CALL to a subroutine causes the contents of the Program Counter to be stored in one of the 8-register pairs of the Program Counter stack as shown.

The pair to be used is determined by a 3 bit stack pointer which is part of the program status wors (PSW) data RAM locations 8-23 are available as stack registers and are used to store the current Program Counter value and 4 bits os PSW as shown.

Nesting of subroutines within subroutines can continue up to eight times without over flowing the stack. The end of a subroutine, which is signalled by a return instruction causes the stack pointer to be decremented and the contents of the resulting register pair to be transferred to the program counter

MCU - 8748

Program status word

An 8-bit status word which can be loaded to and from the accumulator exists called the Program Status Word. The PSW is a collection of flip-flop which can be read or written as a whole. The ability to write to PSW allows for easy restoration of machine status after a power down sequence.

The upper four bits of PSW are stored in the Program Counter stack with every call to subroutine or interrupt vector and are optionally restored upon returns with the RETR instruction. The RET instryuction does not update PSW.

PSW :

Bits 0 - 2	-	Stack pointer bits (S0, S1, S2)
Bit 3	-	Not used ('1' level when read 1)
Bit 4	-	Working register back switch bit (BS)
		0 = Bank 0
		1 = Bank 1
Bit 5	-	Flag0 bit (FO) user controlled flag which can be complemented or cleared and tested with the conditional jump instruction JFO.
Bit 6	-	Auxillary carry (AC).bit generated by an ADD instruction and used by the decimal adjust instruction DAA.
Bit 7	-	Carry (CY) carry flag which indicates that the previous operation has resulted in overflow of the accumulator.

Conditional branch logic

The conditional branch logic within the processor enables several conditional branches internal and external to the processor to be tested by the users program.

Interrupt :

An interrupt sequence is initiated by applying a low '0' level input to the INT pin. The interrupt line is sampled every instruction cycle and when detected causes a "call to subroutine" atlocation 3 in program memory as soon as all cycles of the current instruction are complete. For 2-cycle instruction the interrupt line is sampled in the 2nd cycle only. The INT must be held low for atleast 3 machine cycles to ensure proper interrupt operations. As in any CALL to subroutines, the program counter and program status word are saved in the stack. The interrupt system is single level in that once an interrupt it detected all further interrupt requests are ignored until execution of an RET reenables the interrupt input logic. This occurs at the beginning of the second cycle of the RETR instruction. This sequence holds true also for an internal interrupt generated by timer, overflow. If an internal timer/countes generated interrupt and an enternal interrupt are detected at the same time, the external source will be recognized.

Timer / Counter

The 8748 contains a counter to aid the user in counting external events and generating accurate time delays without placing a burden on the processor for these functions.

Counter

The 8-bit binary counter is presettable and readable with two MOV instructions which transfer the contents of the accumulater to the counter and vice versa. The counter content may be affected by RESET and should be initialized by software. The counter is stopped by a RESET or STOP TCNT instruction and is started by a STARTS T instruction or as an event counter by START CNT instruction. Once started the counter will increment to this maximum count (FF) and overflow to zero continueing its count until stopped by a STOP TCNT instruction. The increment from maximum count to zero results in the setting of an overflow flag flip-flop and in the generation of an interrupt request. The state of the overflow flag is testable with the conditions jump instruction JTF. The flag is reset by executing a JTF or by RESET. The timer interrupt may be enabled or disabled independently of external interrupt by the ENT CNT1 and DIS CNT1 instruction. If enabled, the counter overflow will cause a subroutine call to location 7 where the timer or counter service routine may be stored. If the timer and external interrupt occur simultaneously, the external source will be recognized and

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the call will be to location 3. Since the timer interrupt is latched it will remain pending until the external device is serviced and immediately be recognized upon return from the services routine. The pending timer interrupt is reset by the call to location 7 or may be removed by executing a DISCNT1 instruction.

Event counter

The counter input is connected with the T1 I/P pin as START CNT instruction is executed and the counter is enabled. The T1 input is sampled at the begining of state 3. Subsequent high to low transition on T1 will cause the counter to increment T1 must be held for atleast one T cycle to ensure that it wont be missed. The maximum rate at which the counter may be incremented is once per three instruction cycles. There is no minimum frequency T1 input must remain high atleast 1/5 of a T cycle after transition.

Timer :

Execution of a START instruction connects an internal clock to the counter input and enables the counter. The internal clock is derived by passing the basic machine cycle clock through a 32 prescaler. The prescalar is reset during START T instruction. The resulting clock increments the counter every 32 machine cycle. Various delay from 1 to 256 counter can be obtained by presetting the counter and detecting overflow. ALE divided by 3

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or more can serve as an external clock. Very small delays of 'fine timing' or larger delays can be easily accomplished by software delay loops.

5.4 Programming the 8748

The chip details and the functional block diagram of 8748 have been given in Appendix (b).

The following chapter gives a brief overview of the system controller (8748) architecture and its design aspects.

The MCS - 48 instruction set is extensive for machine of its size and has been tailored to be straight forward and very efficient in its use of prgram memory. All instructions are either one of two bytes in length and over 80% are only one byte long. Also, all instructions execute in either one or two cycles and over 50% of all instructions execute in a single cycle. Double cycle instructions include all immediate instructions, and all I/O instructions.

The MCS - 48 microcomputers have been designed to handle arithmetic operations efficiently in both binary and BCD as well as handle the single-bit operations required in control applications. Special instructions have also been included to simplify loop counters, table look-up routines, and N-way branch routines.

Data transfers

The 8-bit accumulator is the central point for all data transfers within the 8048. Data can be transferred between the 8 registers of each working register bank and the accumulator directly, i.e., the source or destination register is specified by the instruction. The remaining locations of the internal RAM array are referred to as Data Memory and are addressed indirectly via an address stored in either RO and R1 are also used to indirectly address external data memory when it is present. Transfers to and from internal RAM require one cycle, while transfers to external RAM require two. Constants stored in Program Memory can be loaded directly to the accumulator and to the 8 working registers. Data can also be transferred directly between the accumulator and the on-board timer counter or the accumulator and the Program Status word (PSW). Writing to the PSW alters machine status accordingly and provides a means of restoring status after an 8 interrupt or of altering the stack pointer if necessary.

Accumulator Operations

Immediate data, data memory, or the working registers can be added with or without carry to the accumulator. These sources can also be ANDed, ORed, or Exclusive ORed to the accumulator. Data may be moved to or from the accumulator and working

registers or data memory. The two values can also be exchanged in a single operation.

In addition, the lower 4 bits of the accumulator can be exchanged with the lower 4-bits of any of the internal RAM locations. This instruction, along with an instruction which swaps the upper and lower 4-bit halves of the accumulator, provides for easy handling of 4-bit quantities, including BCD numbers. To facilitate BCD arithmetic, a Decimal Adjust instruction is included. This instruction is used to correct the result of the binary addition of two 2-digit BCD numbers. Performing a decimal adjust on the result in the accumulator produces the required BCD result.

Finally, the accumulator can be incremented, decremented, cleared,or complemented and can be rotated left or right I bit at a time with or without carry. Although there is no subtract instruction in the 8048AH, this operation can be easily implemented with three single byte single-cycle instruction.

A value may be subtracted from the accumulator with the result in the accumulator by :

    Complementing the accumulator   .

    Adding the value to the accumulator

    Complementing the accumulator

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Register operations

The working registers can be accessed via the accumulator as explained above, or can be loaded immediate with constants from program memory. In addition, they can be incremented or decremented or used as loop counters using the decrement and jump, if not zero instruction, as explained under branch instructions.

All Data Memory including working registers can be accessed with indirect instructions via R0 and R1 and can be incremented.

Flags

There are four user-accessible flags in the 8048AH; Carry, Auxiliary Carry, F0, and F1. Carry indicates overflow of the accumulator, and Auxiliary Carry is used to indicate overflow between BCD digits and is used during decimal-adjust operation. Both Carry and Auxiliary Carry are accessible as part of the program status word and are stored on the stack during subroutines. F0 and F1 are undedicated general-purpose flags to be used as the programmer desires. Both flags can be cleared or complemented and tested by conditional jump instructions. F0 is also accessible via the Program Status word and is stored on the stack with the carry flags.

Branch Instructions

The unconditional jump instruction is two bytes and allows jumps anywhere in the first 2K words of program memory. Jumps to the second 2K of memory (4K words are directly addressable) are made first by executing a select memory bank instruction, then executing the jump instruction. The 2K boundary can only be crossed via a jump or subroutine call instruction, i.e., the bank switch does not occur until a jump is executed. Once a memory bank has been selected all subsequent jumps will be to the selected bank until another select memory bank instruction is executed. A subroutine in the opposite bank can be accessed by a select memory bank instruction followed by a call instruction. Upon completion of the subroutine, execution will automatically return to the original bank; however, unless the original bank is reselected, the next jump instruction encountered will again transfer execution to the opposite bank.

Conditional jumps can test the following inputs and machine status.

```
To Input pin
TI Input pin
INI Input pin
Accumulator Zero
Any bit of Accumulator
Carry Flag
F0 Flag
FI flag.
```

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Conditional jumps allow a branch to any address within the current page (2256 words) of execution. The conditions tested are the instantaneous values at the time the conditional jump is executed. For instance, the jump on accumulator zero instruction tests the accumulator itself not an intermediate zero flag.

The decrement register and jump if not zero instruction combines a decrement and a branch instructions to create an instruction very useful implementing a loop counter. This instruction can designer any one of the working registers as a counter and can elect a branch to any address within the current page of execution.

A single-byte indirect jump instruction allows the program to be vectored to any one of several different locations based on the contents of the accumulator. The contents of the accumulator points to a location to program memory which contains the jump address. The 8-bit jump address refers to the current page of execution. This instruction could be used. For instance, to vector to any one of several routines based on an ASCII character which has been loaded in the accumulator to this way ASCII key keyinputs can be used to initiate various routine.

Subroutines

Subroutines are entered by executing a call instruction. Calls can be made like unconditional jumps to any

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address in a 2K word bank, and jumps across the 2K boundary are executed in the same manner. Two separate return instruction determine whether or not status (Upper 4-bits of PSW) is restored upon return from the subroutine.

The return and restore status instruction also signals the end of an interrupt service routine if one has been in progress.

Timer Instructions

The 8-bit on board timer counter can be loaded or read via the accumulator while the counter is stopped or while counting. The counter can be started as a timer with an external clock applied to the TI input pin. The instruction executed determines which clock source is used. A single instruction stops the counter whether it is operating with an internal or an external clock source. In addition, two instructions allow the timer interrupt to be enabled or disabled.

Control Instructions

Two instructions allow the external interrupt source to be enabled or disabled. Interrupts are initially disabled and are automatically disabled while an interrupt service routine is in progress and re-enabled afterward.   .

There are four memory bank select instructions, two to designate the active working register bank and two to control programe memory banks. The working register bank switch

MCU - 8748

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instructions allow the programmer to immediately substitute second 8 - register working register bank for the one is use. This effectively provides 16 working registers or it can be used as a means of quickly saving the contents of the registers in response to an interrupt. The user has the option to switch or not to switch banks on interrupt. However, if the banks are switched, the original bank will be automatically restored upon execution of a return and restore status instruction at the end of the interrupt service routine.

A special instruction enables an internal clock, which is the XTAL frequent divided by three to be output on pin TO. This clock can be used as a general purpose clock in the user's system. The instruction should be used only to initialize the system since the clock output can be disabled only by application of system reset.

Input/Output Instructions

Ports 1 and 2 are 8-bit static 1/0 ports which can be loaded to and from the accumulator. Outputs are statically latched but inputs are not latched and must be read while inputs are present. In addition, immediate data from program memory can be ANDed or ORed directly to Port 1 and Port 2 with the result remaining on the port. This allows "masks" stored in program memory to selectively set or reset individual bits of the I/O

----

ports. Ports 1 and 2 configured to allows input on a given pin by first writing a "I" out to the pin.

An 8-bit port called BUS can also be accessed via the accumulator and can have statically latched out puts as well. It too can have immediate data ANDed ORed directly to its outputs, however, unlike ports 1 and 2, all eight lines of BUS must be treated as either input or output at any one time. In additions to being a static port, BUS can be used as a true synchronous bi-directional port using the Move External instructions used to access external data memory. When these instructions are executed, a corresponding READ or WRITE pulse is generated and data is valid only at that time. When data is not being transferred. BUS is in a high impedance state. Note that the OUTL, ANL, and the BRL instructions for the BUS are for use with internal memory only.

The basic three on-board I/O ports can be expanded via a 4-bit expander bus using half of port 2. I/O expander devices on this bus consist of four 4-bit ports which are addressed as ports 4 through 7. These ports have their own AND and OR instructions, however, combine the contents of accumulator with the selected port rather than immediate data as is done with the on-board ports. I/O devices can also be added externally using the BUS port as the expansion bus. In this case the I/O port become

---

"memory mapped", i.e., they are addressed in the same way as external data memory and exist in the external data memory address space addressed by pointer register Ro or Rl.

The instruction set has been given in the Appendix.

The chip details and the functional block diagram of 8748 have been given in Appendix.

HARDWARE DESCRIPTION

CHAPTER SIX - HARDWARE DESCRIPTION

6.1 Introduction

The 40 pin NMOs chip is the system controller. It is a totally self sufficient, 8 bit parallel computer fabricated on a single silicon chip using Intel's advanced N-channel silicon gate. MCU - 8748 is used to perform various software computations like A/D conversion, display after converting binary to BCD.

General Description

Port 1 pins are used for A/D conversion. Port 2 pins 2.0 to 2.4 are used for display of digits and remaining pins may be used for external memory. System controller clock is generated by using a 6 MHz crystal connected between XTAL 1 and XTAL 2. Pin 20 is grounded. Pin 5 (ss), Pin 26 (Vcc) and pin 40 (Vdd) are connected to 5V DC supply.

6.2 A/D converter :

A/D conversion is accomplished using DAC technique which uses R-2R ladder network. This type of converter uses resistors of only two values R and 2R. In the R-2R ladder, bits are weighted by providing paths for current division with consequent successive attenuations for bits of lower significance.

The digital data sent via port 1 is latched using a 20 pin latch 74 HC 373. This is given as input to the R-2R binary ladder network. This is a resistive network whose output voltage

HARDWARE DESCRIPTION

----

is a weighted sum of digital inputs. This output is given to the
non-inverting input of OP/AMP IC 339.

The averaged power from the averaging filter is given to the
pin 10 of the comparator. Both these voltages in Pin 10 and pin
11 are compared and the output is connected to the T1 pin of MCU
8748. If the digital data sent is greater than or equal to
multiplier output then the T1 pin will be at logic 1. The
counter ramp is terminated whenever T1 flag is set. This
indicates that the counter has reached a digital value equivalent
to the analog input. This is used for further processing done in
software routine.

6.3 Display

6.3.1   Design of resistors:

The type of display used in this energy meter is a common
anode seven segment LED display. There is one LED for each
segment. Basically there are two possible connections known as
common anode and common cathode. The displays are driven
continuously. The choice of the method selected out of common
anode and common cathode connections depends on the output of
the code converter. Common anode connections requires active low
or current sinking configuration for the code converter. The
current flow through the chosen LED should be within the current
through the chosen LED is set by a proper choise of series
resistor R1.

5X10K 5X10K 5X10K 5X10K 5X10K
5X2N2907
Q1   Q2   Q3   Q4   Q5

G1   G2   G3   G4   G5

1. 2
1. 1
1. 3
1. 5
1. 4
1. 7
2. 6
2. 8
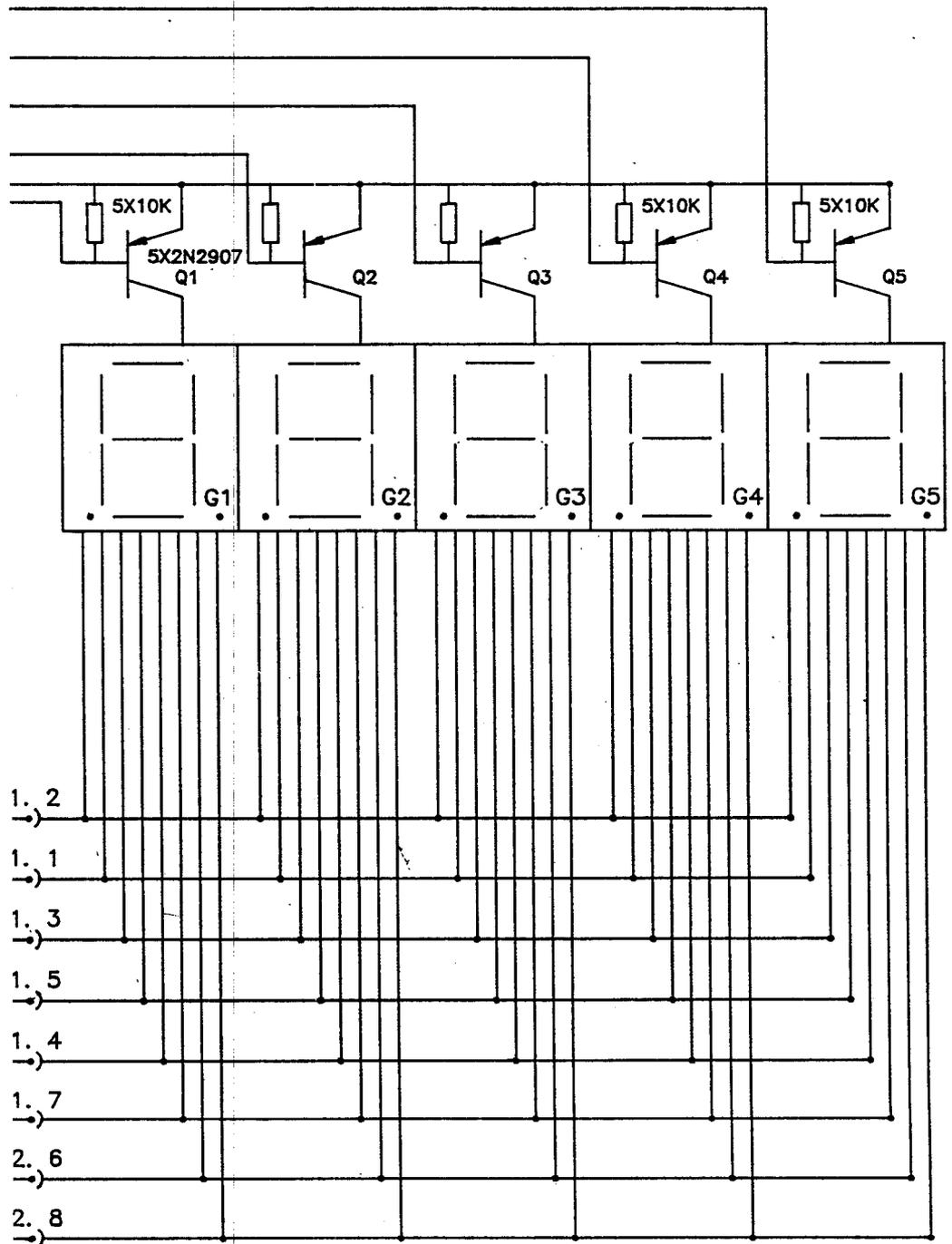
SUPPLIES USED:

V1 — +12V
V2 — +5V
VR — +2.7V

_ER WITH HARDWARE DESIGN CIRCUITS

HARDWARE DESCRIPTION

$$R1 = \frac{Vcc - VF - Vo \, (LOW)}{ILED}$$

Where Vcc is the supply voltage (5 V)
      VF is forward bias voltage (1.4 V)
      Vo(LOW) is low state output voltage of TTL output which is
      <   .4 V I LED is LED current   200 mA

        R = 150 Ω

6.3.2 Interface details :

    Port 2.0 is connected to the least significant digit   while port 2.4 pin to MSB. All the anodes of the 5 seven segment LED's are tied to a 5V supply through pnp transistors (2N2907) which acts as a switch. The emitter of the pnp transistors are tied to the 5V supply while its collector is connected to the anodes of the LED's. The base of the transistors are connected to the port two of MCU through 2.7 K resistors.

SOFTWARE COMPUTATION
FLOWCHARTS

CHAPTER SEVEN - SOFTWARE COMPUTATION

7.1 Introduction:

All the computations are achieved bying of the microcontroller. The programming is done in assembly level language. The software computation includes averaging of the A/D values, units computation, binary to BCD conversion and display.

7.2 Implementation : Software implementation has been done based on the following conditions :

1) When the power supply is made on, the processor jumps to location 0. This contains a jump to init routine. This routine initialises the processor.

2) When the timer overflows the processor is interrupted.   It jumps to location 7 of the data memory which contains a jump to TIMISR routine. This performs the display function.   The displayed is refreshed every 2 milli seconds and only one digit is refreshed at a time.

7.3 Theory of computation :

The output of the averaging filter is the average power that is analog in nature. This has to be converted into digital power before computation. This digitisation is done by A/D converter.   A/D conversion takes place every 50 ms. At the end of 1 second, 20 values are obtained and are stored in successive memory locations.   These 20 values are added and divided to get an average value. This process is done in the COMPUTE routine to

SOFTWARE COMPUTATION

----

give one byte value. This gives a propotional average power consumed.

Processing theory :

      Maximum load voltage   =   260 V (rms)

      Maximum load current   =   15 A (rms)

For resistive load,

      Maximum power consumed =   260 x 15 cos

                              =   3900 Watts

Since the unit of computation is KWh, it means that when the load consumes an average power of 3900 Watts in an hour, then the energy consumed is 3.9 units. This is the maximum power that can be consumed. But by the signal conditioning process we have scaled this such that 5 Watts corresponds to FF after A/D conversion.

Energy consumed in 1 second

$$= \frac{3.9}{60 \times 60} \text{ Units}$$

Number of units in FF H

$$= \frac{3.9}{3600} \text{ Units}$$

Number of units in 1 H

$$= \frac{3.9}{3600 \times 255}$$

$$= 4.248 \times 10^{-6} \text{ units}$$

SOFTWARE COMPUTATION

The average power consumed is in hexadecimal form and this is multiplied by this factor 4.248×10^{-6}. This value is in binary form and has to be converted into BCD form. This is done by the BCD conversion routine. Six bytes are reserved for accumulating the values and the uppermost 3 bytes are taken and displayed in the seven segment display. Thus the energy in the units Kilo watt hour is displayed. All the system flowcharts are given in this chapter.

```
                    ┌─────────────┐
                    │    START    │
                    └──────┬──────┘
                           │
                    ┌──────▼──────┐
                    │ Configure PUS in │
                    │  output mode │
                    └──────┬──────┘
                           │
                    ┌──────▼──────┐
                    │ Clear all 64 │
                    │ RAM locations│
                    └──────┬──────┘
                           │
                    ┌──────▼──────┐
                    │ Initialise timer │
                    │ to interrupt │
                    │ every 2MB    │
                    └──────┬──────┘
                           │
                    ┌──────▼──────┐
                    │ Start Timer  │
                    └──────┬──────┘
                           │
                    ┌──────▼──────┐
                    │ Enable times/│
                    │ counter interrupt│
                    └──────┬──────┘
                           │
                    ┌──────▼──────┐
                    │ Enable external │
                    │ interrupt    │
                    └──────┬──────┘
                           │
                    ┌──────▼──────┐
                    │ Initialise   │
                    │ counter 1 to 50 ms│
                    └──────┬──────┘
                           │
                    ┌──────▼──────┐
                    │ Call ATODONT │
                    │ routine      │
                    └──────┬──────┘
                           │
                         ( A )
```
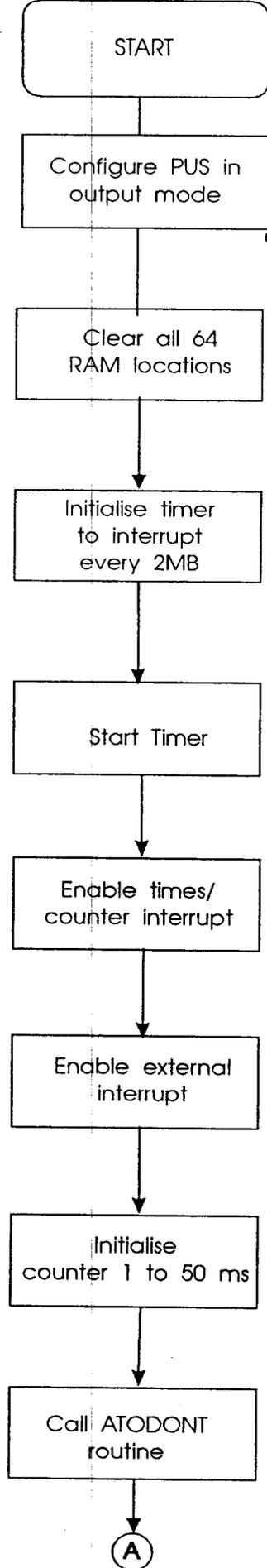
FIG - 7.1 SYSTEM FLOWCHART

FIG - 7.1 SYSTEM FLOWCHART (Contd..)

```
            ╭─────────────╮
            │    START     │
            ╰─────────────╯
                   │
                   ▼
         ┌───────────────────┐
         │     Decrement     │
         │   50 ms counter   │
         └───────────────────┘
                   │
                   ▼
         ┌───────────────────┐
         │  Push accumulator │
         │   contents into a │
         │      register     │
         └───────────────────┘
                   │
                   ▼
         ┌───────────────────┐
         │   Call Display    │
         │     Routine       │
         └───────────────────┘
                   │
                   ▼
         ┌───────────────────┐
         │ Pop Pop register  │
         │   contents into   │
         │    accumulator    │
         └───────────────────┘
                   │
                   ▼
            ╭─────────────╮
            │ RETURN AND  │
            │   STORE     │
            ╰─────────────╯
```
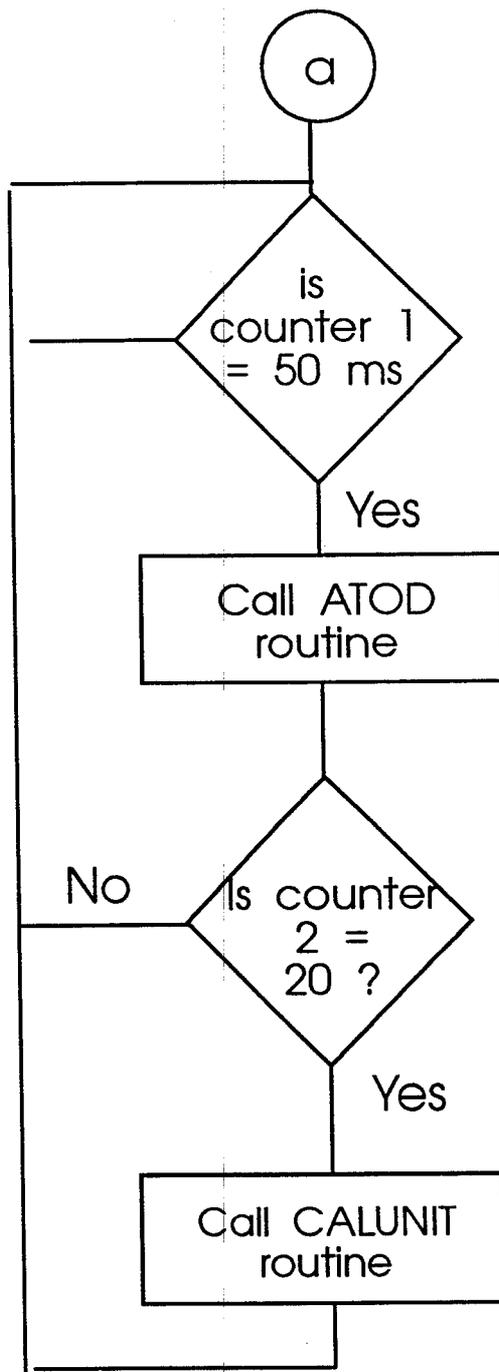
FIG - 7.2 FLOWCHART FOR TIMER
                 INTERRUPT ROUTINE

```
                    ┌─────────────┐
                    │    START    │
                    └──────┬──────┘
                           │
                           ▼
                ┌─────────────────────┐
                │     Read Port 2     │
                │  status to select   │
                │    the digit for    │
                │    display and      │
                │      save it        │
                └──────────┬──────────┘
                           │
                           ▼
                ┌─────────────────────┐
                │    Re - intitialise │
                │    timer for 2 ms   │
                └──────────┬──────────┘
                           │
                           ▼
                ┌─────────────────────┐
                │    Disable BUS      │
                └──────────┬──────────┘
                           │
                           ▼
                ┌─────────────────────┐
                │  Move port2 status  │
                │        into         │
                │    accumulator      │
                └──────────┬──────────┘
                           │
                           ▼
                ┌─────────────────────┐
                │   Point data RAM    │
                │    for display      │
                └──────────┬──────────┘
                           │
                           ▼
                ┌─────────────────────┐
                │   Point Data RAM    │
                │      display        │
                └──────────┬──────────┘
                           │
                           ▼
                      ╱────────╲       Yes   ┌──────────────────┐      ╭──────────╮
                     ╱   HAS    ╲──────────→ │  REFRESH DIGIT1  │──────│  RETURN  │
                     ╲ BITO SET ╱            └──────────────────┘      ╰──────────╯
                      ╲────────╱
                           │ No
                           ▼
                      ╱────────╲       Yes   ┌──────────────────┐      ╭──────────╮
                     ╱   HAS    ╲──────────→ │  REFRESH DIGIT2  │──────│  RETURN  │
                     ╲ BIT1 SET ╱            └──────────────────┘      ╰──────────╯
                      ╲────────╱
                           │ No
                           ▼
                         ( W )
```
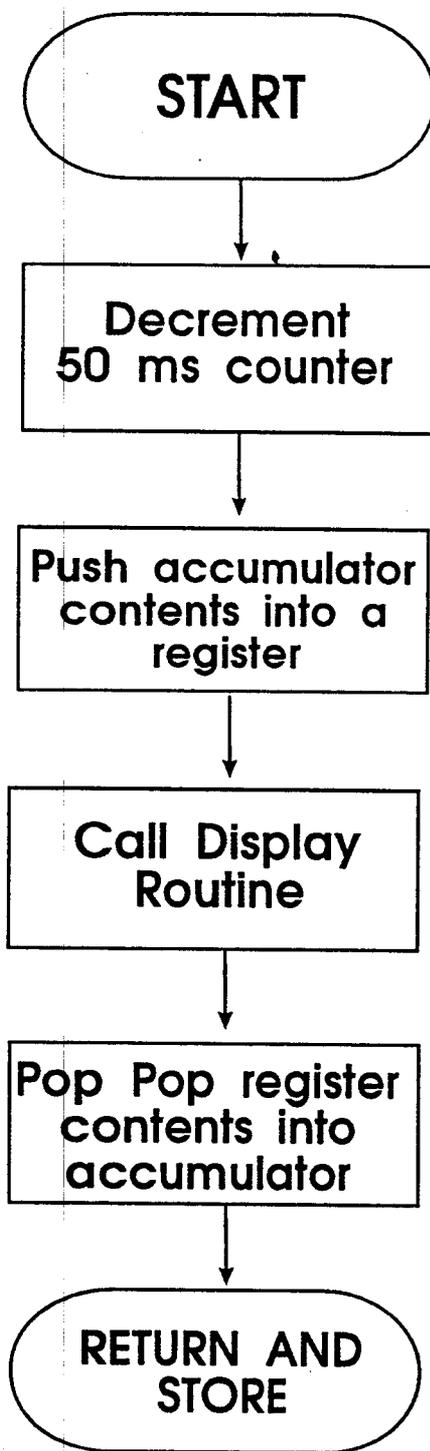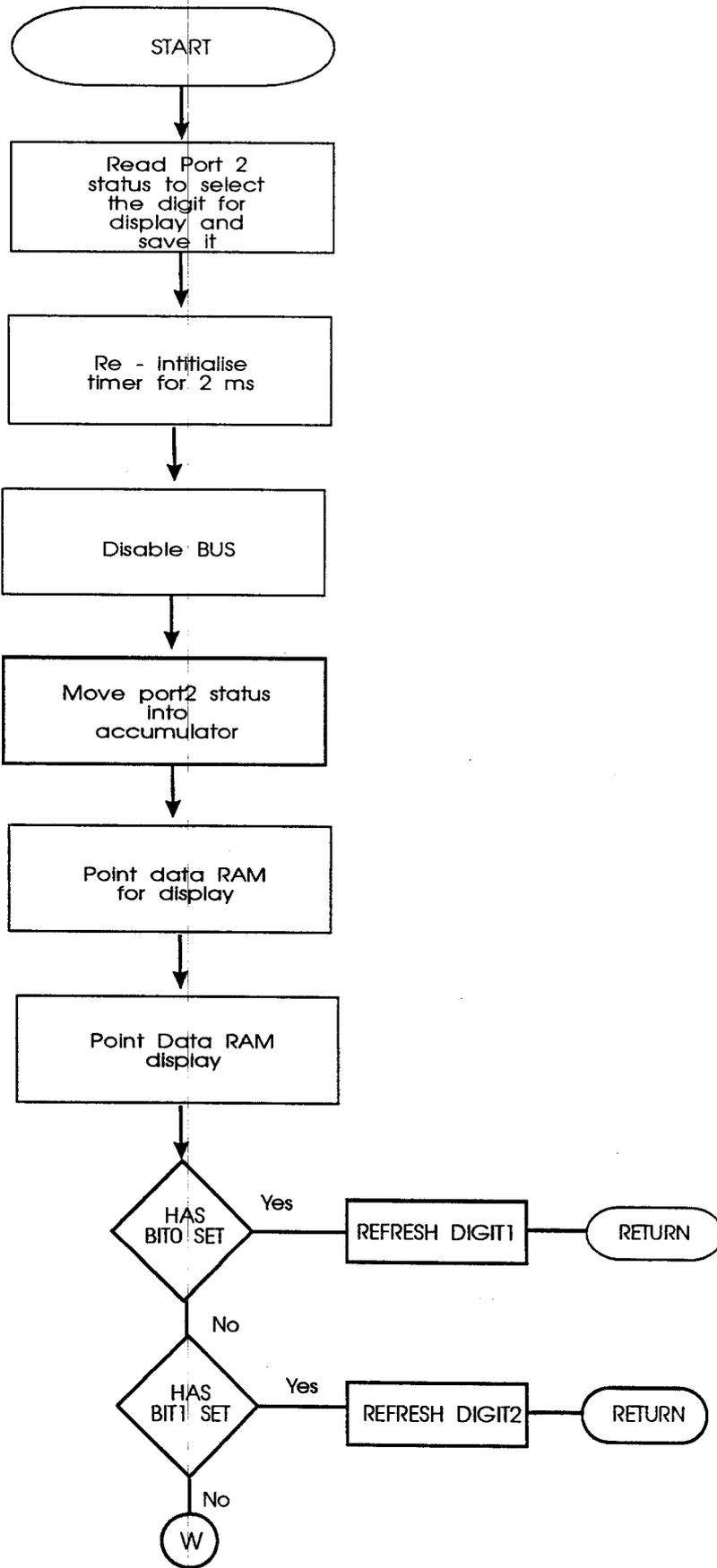
FIG - 7.3 FLOWCHART FOR DISPLAY ROUTINE

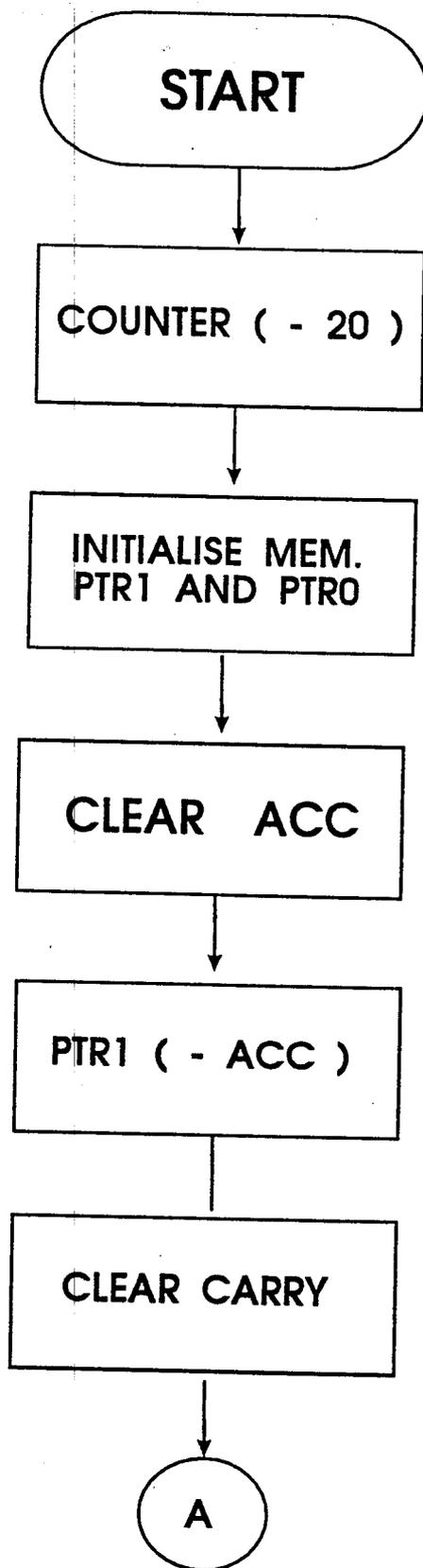FIG - 7.3 FLO.CHART FOR DISPLAY ROUTINE (Contd..)

```
                 ╭─────────────────╮
                 │      START       │
                 ╰─────────────────╯
                          │
                          ▼
            ┌───────────────────────────┐
            │   COUNTER ( - 20 )         │
            └───────────────────────────┘
                          │
                          ▼
            ┌───────────────────────────┐
            │   INITIALISE MEM.          │
            │   PTR1 AND PTR0            │
            └───────────────────────────┘
                          │
                          ▼
            ┌───────────────────────────┐
            │   CLEAR   ACC              │
            └───────────────────────────┘
                          │
                          ▼
            ┌───────────────────────────┐
            │   PTR1 ( - ACC )           │
            └───────────────────────────┘
                          │
                          ▼
            ┌───────────────────────────┐
            │   CLEAR CARRY              │
            └───────────────────────────┘
                          │
                          ▼
                       ╭─────╮
                       │  A   │
                       ╰─────╯
```

FIG — 7.4 FLOWCHART FOR ADDER ROUTINE

```
         ⓐ

  (ACC) < - (ACC) +
     (PTR1) + Carry


  (PTR 1) < - (ACC)


  Increment PTR.0
  Decrement PTR.1


      Dec
       IS
     Counter          No      ⓑ
     Zero ?

       Yes

      RETURN
```
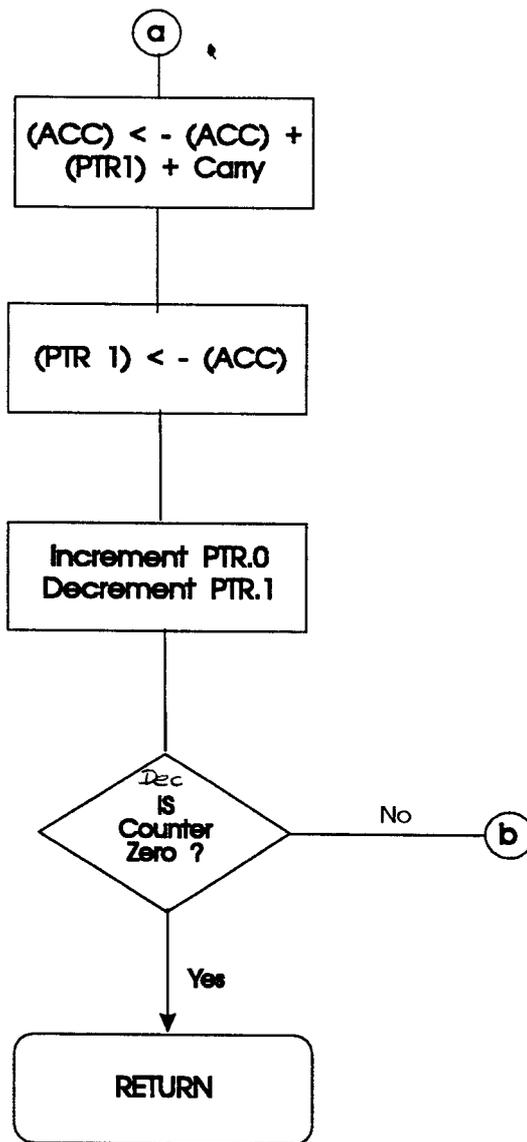
FIG − 7.4 FLOWCHART FOR ADDER ROUTINE (Contd..)
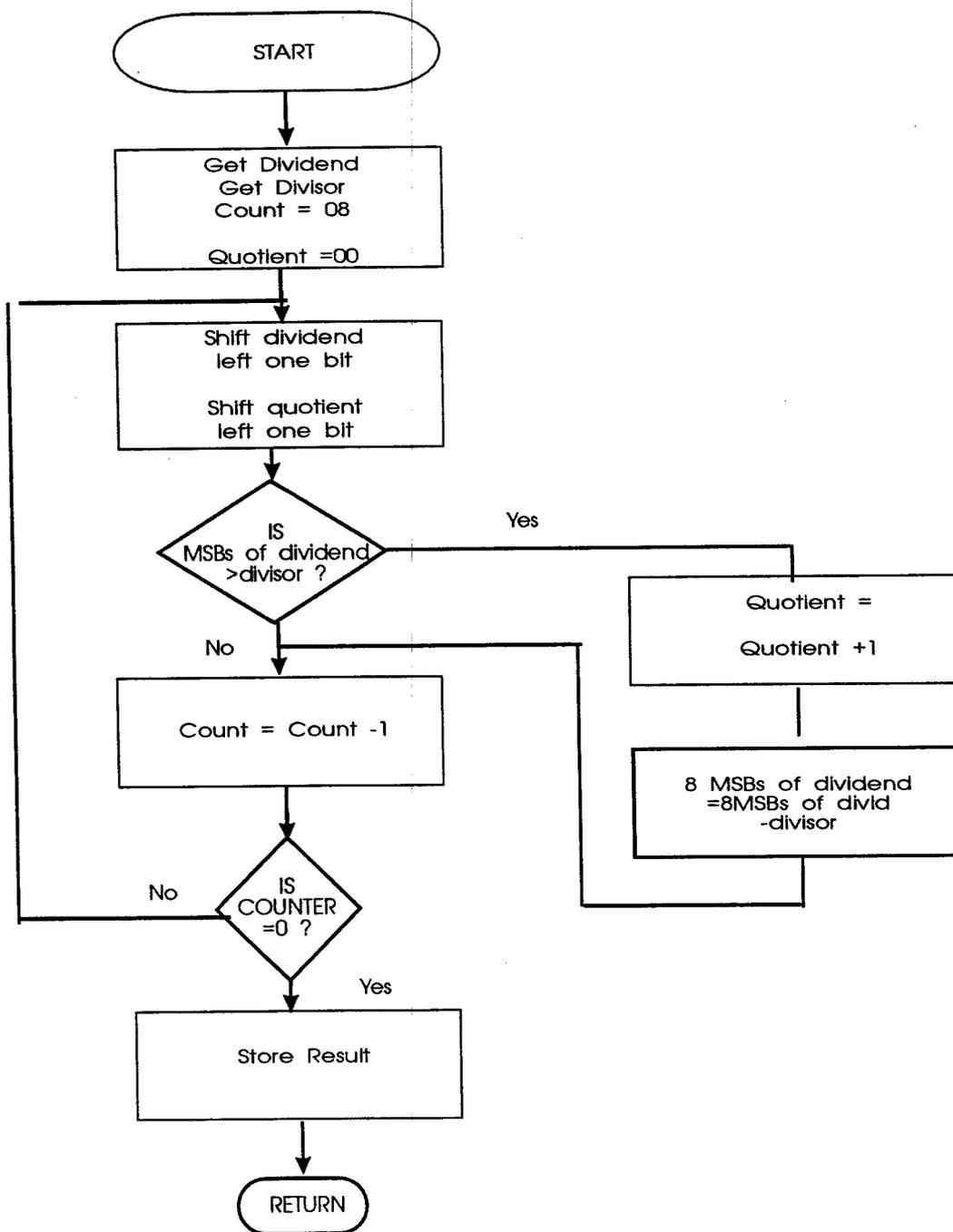
FIG - 7.5 FLOWCHART FOR DIVISION ROUTINE

```
        ┌─────────────┐
        │    START    │
        └──────┬──────┘
               │
               ▼
        ┌─────────────┐
        │ Call AVERAGE│
        │   routine   │
        └──────┬──────┘
               │
               ▼
        ┌─────────────┐
        │ Call COMPUTE│
        │   routine   │
        └──────┬──────┘
               │
               ▼
        ┌─────────────┐
        │ Call BIN BCD│
        │   Routine   │
        └──────┬──────┘
               │
               ▼
        ┌─────────────┐
        │ Call BCD ADD│
        │   Routine   │
        └──────┬──────┘
               │
               ▼
        ┌─────────────┐
        │   RETURN    │
        └─────────────┘
```
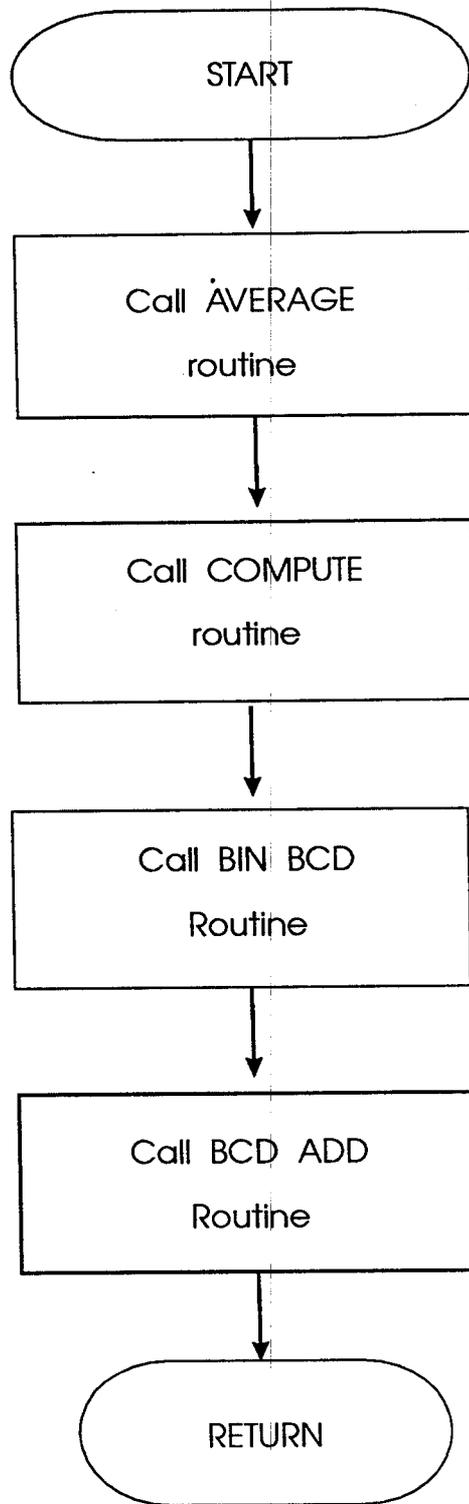
FIG - 7.6 FLOWCHART FOR UNITS CALCULATION

```
                    ┌─────────────┐
                    │    START    │
                    └─────────────┘
                           │
                           ▼
                  ┌──────────────────┐
                  │  Get multiplier  │
                  │ Get multiplicand │
                  └──────────────────┘
                           │
                           ▼
                  ┌──────────────────┐
                  │    Count = 9     │
                  └──────────────────┘
                           │
                           ▼
                  ┌──────────────────┐
                  │   Clear carry    │
                  │   clear Add      │
                  └──────────────────┘
                           │                    ┌─────┐
                           ▼                    │  y  │
                         ◇ IS ◇    Yes          └─────┘
                         ◇ t1 set◇ ───┐
                           │ No       │
                           ▼          │
                  ┌──────────────────┐│
                  │  Acc  < = Acc +  ││
                  │   multiplicand   ││
                  └──────────────────┘│
                           │ ◄────────┘
                           ▼
                  ┌──────────────────┐
                  │     Rotate       │
                  │   accumulator    │
                  │  through carry   │
                  └──────────────────┘
                           │
                           ▼
                  ┌──────────────────┐
                  │     Rotate       │
                  │   accumulator    │
                  │  through carry   │
                  └──────────────────┘
                           │
                           ▼
                  ┌──────────────────┐
                  │    Decrement     │
                  │     Count        │
                  └──────────────────┘
                           │
                           ▼
                       ┌───────┐
                       │   2   │
                       └───────┘
```

FIG - 7.7 FLOWCHART FOR COMPUTE ROUTINE

FIG - 7.7 FLOWCHART FOR COMPUTE ROUTINE (Contd..)

```
                    ┌─────────────┐
                    │    START    │
                    └─────────────┘
                           │
                           ▼
                ┌──────────────────────┐
                │  SET  MEMORY PTR.1   │
                │     TO  BINBCD        │
                │      LOCATION         │
                └──────────────────────┘
                           │
                           ▼
                ┌──────────────────────┐
                │  SET  MEMORY PTR.2   │
                │     TO  BCDADD        │
                │      LOCATION         │
                └──────────────────────┘
                           │
                           ▼
                ┌──────────────────────┐
                │     INITIALISE        │
                │    COUNTER.1=3        │
                │    COUNTER.2=4        │
                └──────────────────────┘
                           │
                           ▼
                ┌──────────────────────┐
                │ BINBCD + BINADD + CARRY│
                │   DEC ADJ. RESULT     │
                └──────────────────────┘
                           │
                           ▼
                ┌──────────────────────┐
                │     DECREMENT         │
                │     COUNTER 1         │
                └──────────────────────┘
                           │
                           ▼
                ┌──────────────────────┐
                │  INCREMENT  MEMORY    │
                │   PTR.1  &  PTR.2     │
                └──────────────────────┘
                           │
                           ▼
                        ╱────╲                          ( A )
                      ╱  IS    ╲        Yes      ┌──────────────────┐
                     ╱ COUNTER.1 ╲─────────────→ │ ADD BCDADD LOC   │
                     ╲   =0?     ╱               │   WITH CARRY     │
                      ╲        ╱                 │ DEC. ADJ RESULT  │
                        ╲────╱                   └──────────────────┘
                           │ No                           │
                           ▼                              │
              ( A )     ╱────╲                            │
              ┌───────╱  IS    ╲              ┌──────────────────┐
              │       ╲ COUNTER.2 ╲───────────│ DECR. COUNTER.2  │
                      ╲   =0 ?   ╱             │ INCR.MEM.PTR.2   │
                        ╲────╱                 └──────────────────┘
                           │ Yes
                           ▼
                    ┌─────────────┐
                    │   RETURN    │
                    └─────────────┘
```
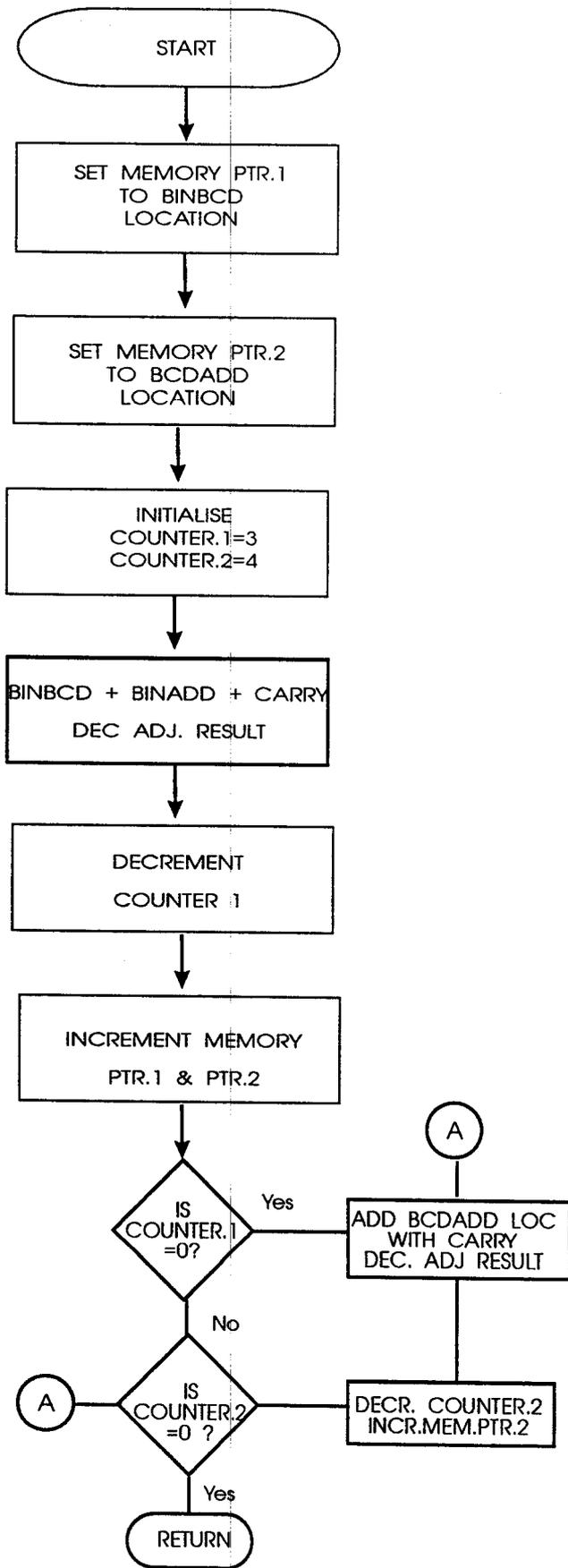
FIG − 7.8 FLOWCHART FOR BCD ADDITION ROUTINE

START

Reinitialise
counter1 to
count 50 ms

Counter3 <= 00

Result <= 00

(A) <= Result

Send (A)
through port 1

Increment
result

IS
t1 set

Yes

No

Decrement
counter 3

IS
COUNTER 3
=0

Yes

b

FIG - 7.9 FLOWCHART FOR ATOD

```
        ( b )
          │
   ┌──────┴──────┐
   │  Decrement  │
   │   result    │
   └──────┬──────┘
          │
   ┌──────┴──────┐
   │ Move result to │
   │   data RAM  │
   └──────┬──────┘
          │
          ▼
   ┌─────────────┐
   │  Increment  │
   │ memory pointer │
   └──────┬──────┘
          │
          ▼
   ╭─────────────╮
   │    RETURN   │
   ╰─────────────╯
```
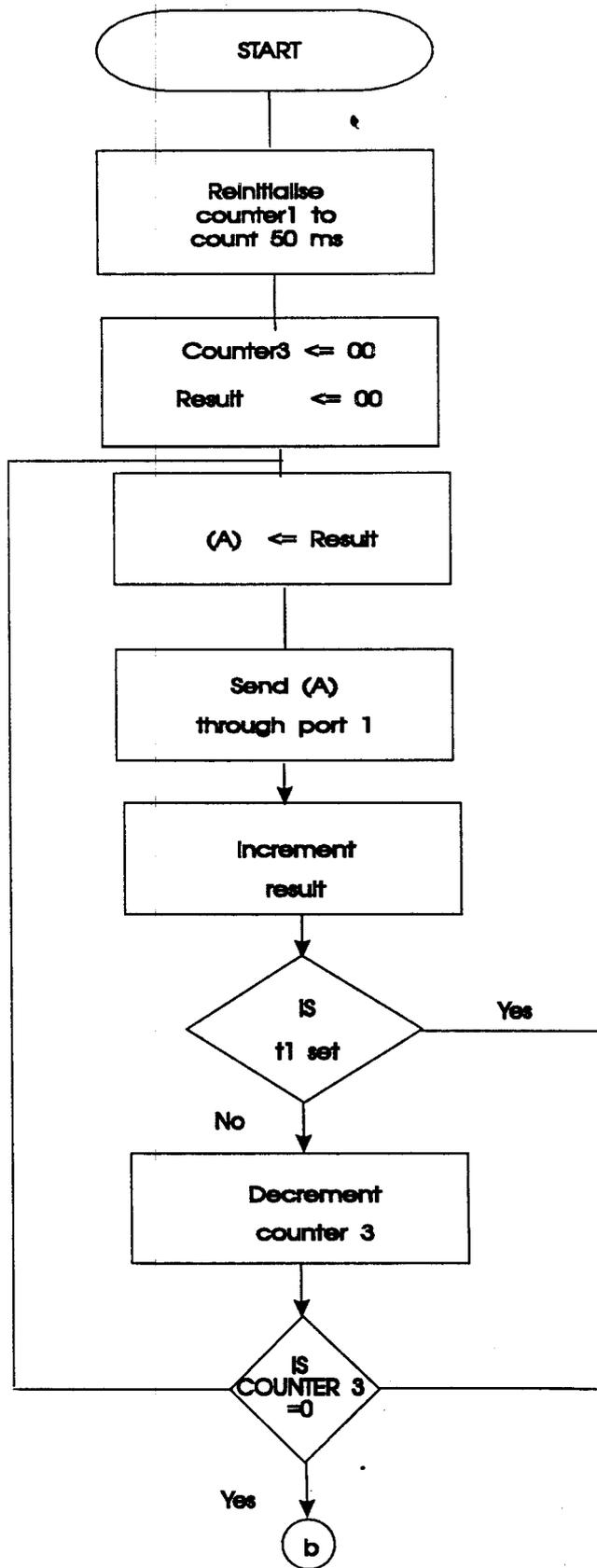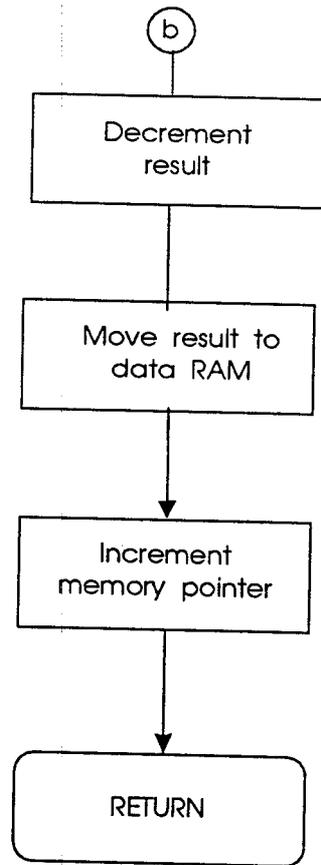
FIG - 7.9 FLOWCHART FOR ATOD (Contd..)

CONCLUSION

CONCLUSION

Our project has been designed in two printed circuit boards. The first board consists of power sensing and signal conditioning circuits which include voltage sensing, current sensing multiplier and averaging filter. The system controller and its associated hardware circuitry has been implemented in the second board.

The entire system has been properly interfaced and enclosed in a cabinet. Proper wire connections for the supply mains and load has been given. Our project records the energy consumed in steps of .1 units. The hence better accuracy and precision has been incorporated. The product has been found to work satisfactorily.

Our energy meter was tested for various loads under different conditions. All practical observations were found to coincide with the theoratical results satisfactorily. This product fails to work when the voltage drops below 200 V. The meter readings are accurate upto a maximum load current of 15A. Thus the range has been fixed in our design but this can be extended by hardware and software modifications. The power consumed by design is very less when compared to the conventional model by this can be further reduced a great deal using LCD's.

CONCLUSION

Suggested future expansions for existing model :

i)   Fibre optic interface for distributed data.

ii) RS-232C interface for MODEM connections.

iii) Optional PC interface.

   Our project is a single phase meter and it can be easily
upgraded to three phase systems by modifications in hardware and
software.

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BIBLIOGRAPHY

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APPENDICES

APPENDIX   A

FUNCTIONAL BLOCK DIAGRAM – XR-2208

XR-2208

MULTIPLIER OUTPUTS
1
2

X INPUT 3
COMMON 4
Y INPUT 5
Y-GAIN
6
7
X GAIN 8

FOUR QUADRANT MULTIPLIER

BUFFER AMP
+1

OP AMP

16 V+
15 HIGH FREQ. OUTPUT
14 OP AMP INPUTS
13
12 COMP.
11 OP AMP OUTPUT
10 V-
9 X GAIN

⊕ EXAR

Operational Multiplier

GENERAL DESCRIPTION

The XR-2208 operational multiplier combines a four-quadrant analog multiplier (or modulator), a high frequency analog multiplier (or modulator), and an operational amplifier in a monolithic circuit that is ideally suited for both analog computation and communications signal processing applications. As shown in the functional block diagram, the four sections are not internally connected. They are interconnected with a minimum number of external components, to perform arithmetic computation, such as multiplication, division, square-root extraction.

The operational amplifier can also function as a pre- or post-detection amplifier for synchronous demodulator applications. For signal processing, the high frequency buffer amplifier output is available at pin 15. This multiplier/amplifier combination extends the small signal bandwidth to 8 MHz and the transconductance bandwidth to 100 MHz.

The XR-2208 operates over a wide range of supply voltages, ±4.5V to ±16V. Current and voltage levels are internally regulated to provide excellent power supply and temperature stability. The XR-2208 operates over a 0°C to 70°C temperature range. The XR-2208M is specified for operation over the military temperature range of −55°C to +125°C.

FEATURES

Maximum Versatility, Op Amp, and Buffer
Excellent Linearity (0.3% typ.)
Wide Bandwidth
  3 dB BW — 8 MHz typ
  Phase Shift BW — 1.2 MHz typ
  Transconductance B W — 100 MHz
Built-in Offset Adjustments
Wide Supply Voltage Range (±4.5V to ±16V)

APPLICATIONS

Signal Computation   Triangle-to-Sinewave Converter
Voltage Dependent Multiplier, Op Amp and Buffer
Modulation   AGC Amplifier
Division   Phase Detector
Squaring   Phase-Locked Loop (PLL) Applications
Signal Processing   Motor Speed Control
AM Generation   Precision
Frequency Doubling   Carrier Detection
Frequency Translation   Phase-Locked AM Detection
Synchronous AM Detection   Demodulation

FUNCTIONAL BLOCK DIAGRAM
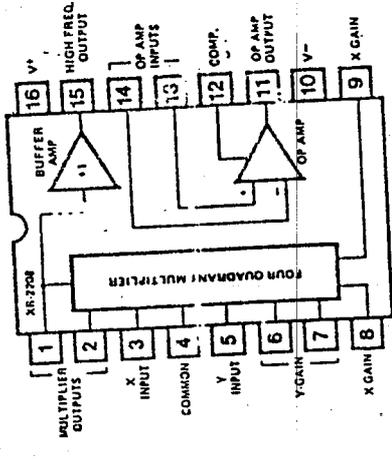
ABSOLUTE MAXIMUM RATINGS

Power Supply V+	+18 Volts
V−	−18 Volts
Power Dissipation	
Ceramic Package	750mW
Derate above +25°C	6mW/°C
Plastic Package	625 mV
Derate above +25°C	5 mW/°C
Storage Temperature Range	−65°C to +150°C

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2208M	Ceramic	−55°C to +125°C
XR-2208N	Ceramic	0°C to +70°C
XR-2208P	Plastic	0°C to +70°C
XR-2208CN	Ceramic	0°C to +70°C
XR-2208CP	Plastic	0°C to +70°C

SYSTEM DESCRIPTION

The XR-2208 multiplier/detector contains a four quadrant multiplier and a fully independent operational amplifier. The four quadrant multiplier has fully differential X and Y inputs and outputs. Both inputs have 3 MHz dynamic response and 100 MHz transconductance bandwidth. The operational amplifier features high gain and wide common mode range. The device is powered by a large common mode range. The device is powered by ±4.5V to ±16V split supplies.

For higher frequency applications, consider the XR-2208.

ELECTRICAL CHARACTERISTICS

Test Conditions: Supply Voltage = ±15V, TA = 25°C, unless otherwise specified.

PARAMETERS	XR-2208/XR-2208M MIN	TYP	MAX	XR-2208C MIN	TYP	MAX	UNITS	FIGURES	CONDITIONS
I. GENERAL									
Supply Voltage	±4.5		±16	±4.5		±16	Vdc		See Figure 11
Supply Current			7			8	mA	2	Measured at Pin 16
II. MULTIPLIER SECTION									
Non-linearity (Output Error in % of Full Scale)		0.3	0.5		0.5	1.0	%	3	No external offset trim
		0.3	0.5		0.5	1.0	%		$V_y = \pm10V$, $-10V < V_x < +10$
		0.7	1.0		0.8		%		$V_x = \pm10V$, $-10V < V_y < +10$ / $T_{LOW} \leq T_A \leq T_{HIGH}$ (Note 1) / f = 50 Hz
Feedthrough									
a) No Offset Adj X-input		45	80		70	120	mVpp		$V_x = 20$ Vpp, $V_y = 0$
Y-input		60	100		90	150	mVpp		$V_y = 20$ Vpp, $V_x = 0$
b) No Offset Adj X-input		120			200		mVp-p		$V_x = 20$ Vpp, $V_y = 0$
Y-input		120			200		mVp-p		$V_y = 20$ Vpp, $V_x = 0$
Temperature Coefficient of Scale Factor	0.5	±0.07			±0.07		%/°C		$T_{LOW} \leq T_A \leq T_{HIGH}$ See Definition Section
Input Bias Current X, Y Input	6	2	6	6	3	8	μA	2	l3, l5 of Figure 2
Common input	3	4	12	3	6	16	μA	2	l4 of Figure 2 / Measured looking into Pin 3 or Pin 5
Input Resistance		1.0			1.0		MΩ	2	Measured across Pins 1 and 2
Output Offset Voltage		50	80		80	140	mV	5	$T_{LOW} \leq T_A \leq T_{HIGH}$ See Definition Section
Avg. Temp. Drift		0.5			0.5		mV/°C		
Dynamic Response									
3-dB Bandwidth X-input	6	8		6	8		MHz		
Y-input	3	4		3	4		MHz		
3° Phase-Shift Bandwidth		1.2			1.2		MHz		
1% Absolute Error Bandwidth		30			30		kHz		
Transconductance Bandwidth		100			100		MHz		
Output Impedance		6			6		kΩ		Measured looking into Pin 15
III. BUFFER AMPLIFIER									
Output Impedance		200			200		Ω	5	Measured looking into Pin 15
Gain		1.0			1.0				
IV. OPERATIONAL AMPLIFIER									
Voltage Gain	70	70			70		dB	6	$R_S < 500$ / $T_{LOW} \leq T_A \leq T_{HIGH}$
Input Offset Voltage		1	3		2	6	mV	6	l91 − l92
Temperature Coefficient of Input Offset Voltage		6	20		9	30	μV/°C		l91 − l92
Input Offset Current		4	75		10	100	nA	6	$R_L \geq 2K$, $V_O = \pm10V$, f = 20
Input Bias Current		30	200		50	300	nA	6	$R_L \geq 2K$, $T_{LOW} \leq T_A \leq THIGH$
Differential Input Resistance		75			75		kΩ		
Output Voltage Sw'g		3			3		V		
Input Common Mode Range		±10	±12		±10	±12	V	6	
		±12	±14		±12	±14			
		−10	−12		−10	−12			
Common Mode Rejection	70	70	90		70	90	dB	6	
Output Resistance		2			2		kΩ	6	
Slew Rate		0.5			0.5		V/μs	7	Gain = 1, $R_L = 2K$, $C_L \leq 100$, $C_C = 20$ pF
Power Supply Sensitivity		30			30		μV/V	6	$R_S \leq 10K$

Note 1: $T_{LOW} = -55°C$, $T_{HIGH} = +125°C$ for XR-2208M; $T_{LOW} = 0°C$, $T_{HIGH} = +70°C$ for XR-2208/XR-2208C

CAUTION: When using only the op amp or only the multiplier section of the XR-2208, the input terminals to the unused section must be grounded. Thus, when using the multiplier section alone, ground pins 13 and 14, when using the op amp section alone, ground pins 3, 4 and 5.

# XR-2208

ELECTRICAL CHARACTERISTICS

Test Conditions: Supply Voltage ± 15V, T_A = 25°C, unless otherwise specified

PARAMETERS	XR-2208/XR-2208M MIN	TYP	MAX	XR-2208C MIN	TYP	MAX	UNITS	FIGURES	CONDITIONS
I. GENERAL									
Supply Voltage	±4.5		±16	±4.5		±16	Vdc	2	See Figure 11
Supply Current		4	7		5	8	mA	2	Measured at Pin 16
II. MULTIPLIER SECTION									No external offset trim
Non-linearity (Output Error in % of Full Scale)		0.3	0.5		0.5	1.0	%	3	$V_y = ±10V, -10V < V_x < +$
		0.3	0.5		0.5	1.0	%		$V_x = ±10V, -10V < V_y < +$
		0.7	1.0		0.8		%		$T_{LOW} \le T_A \le T_{HIGH}$ (Note) f = 50 Hz
Feedthrough									
a) With Offset Adj									
X-input		45	80		70	120	mVp-p		$V_x = 20$ Vp-p $V_y = 0$
Y-input		60	100		90	150	mVp-p		$V_y = 20$ Vp-p $V_x = 0$
b) No Offset Adj									
X-input		120			200		mVp-p		$V_x = 20$ Vp-p, $V_x = 0$
Y-input		120			200		mVp-p		$V_y = 20$ Vp-p, $V_x = 0$
Temperature Coefficient of Scale Factor		±0.07			±0.07		%/°C		$T_{LOW} \le T_A \le T_{HIGH}$ (Note)
Input Bias Current									
X, Y input		2	6		3	8	μA	2	I_3, I_5 of Figure 2
Common input		4	12		6	16	μA	2	I_4 of Figure 2
Input Resistance	0.5	1.0			1.0		MΩ	2	Measured looking into Pin 3 or Pin 5
Output Offset Voltage		50	80		80	140	mV	2	Measured across Pins 1 and 2
Avg Temp Drift		0.5			0.5		mV/°C		$T_{LOW} \le T_A \le T_{HIGH}$
Dynamic Response								5	See Definition Section
3-dB Bandwidth									
X-input	6	8		6	8		MHz		
Y-input	3	4		3	4		MHz		
3° Phase-Shift Bandwidth		1.2			1.2		MHz		
1% Absolute Error Bandwidth		30			30		kHz		
Transconductance Bandwidth		100			100		MHz		
Output Impedance		6			6		kΩ		Measured looking into Pins 1
III. BUFFER AMPLIFIER									
Output Impedance		200			200		Ω	5	Measured looking into Pin 16
Gain		1.0			1.0				
IV. OPERATIONAL AMPLIFIER									
Input Offset Voltage		1	3		2	6	mV	6	$R_S < 50Ω$
Temperature Coefficient of Input Offset Voltage		6	20		9	30	μV/°C		$T_{LOW} \le T_A \le T_{HIGH}$
Input Offset Current		4	75		10	100	nA	6	$I_{B1} - I_{B2}$
Input Bias Current		30	200		50	300	nA	6	$\frac{I_{B1} + I_{B2}}{2}$
Voltage Gain	70	75		70	75		dB	6	$R_L \ge 2K, V_0 = ±10V, f$
Differential Input Resistance	0.5	3			3		MΩ	6	
Output Voltage Swing	±10	±12		±10	±12		V		$R_L \ge 2K, T_{LOW} \le T_A \le$
Input Common	+12	+14		+12	+14				
Mode Range	-10	-12		-10	-12		V	6	
Common Mode Rejection	70	90		70	90		dB	6	f = 20 Hz
Output Resistance		2			2		kΩ	6	
Slew Rate		0.5			0.5		V/μs	7	Gain = 1, $R_L \ge 2K$ C_L $C_C = 20$ pF
Power Supply Sensitivity		30			30		μV/V	6	$R_S \le 10K$

Note 1: T_{LOW} = -55°C, T_{HIGH} = +125°C for XR-2208M T_{LOW} = 0°C, T_{HIGH} = +70°C for XR-2208/XR-2208C

CAUTION: When using only the op amp or only the multiplier section of the XR-2208, the input terminals to the unused section must be grounded. Thus, when using the multiplier section alone, ground pins 13 and 14; when using the op amp section alone, ground pins 3, 4 and 5

XR-2208

TYPICAL CHARACTERISTIC CURVES
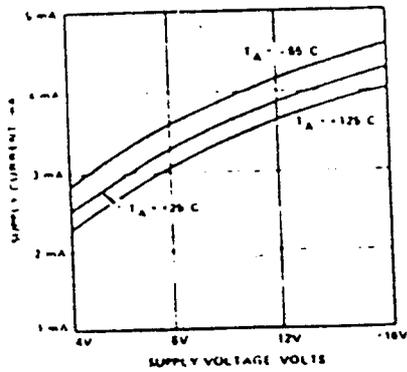
Figure 7. Supply Current vs Supply Voltage
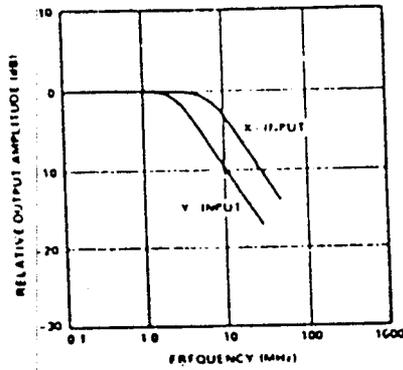
Figure 8. Small-Signal Frequency Response for the Multiplier Section. (Output Measured at Pin 15—See Fig. 4).
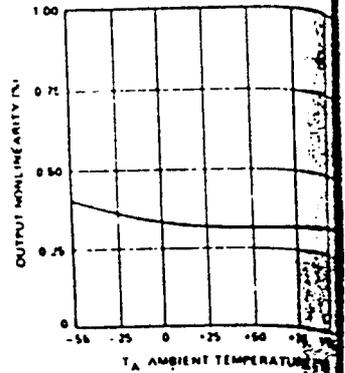
Figure 9. Temperature Dependence Output Nonlinearity for X or Y (See Figure 2).
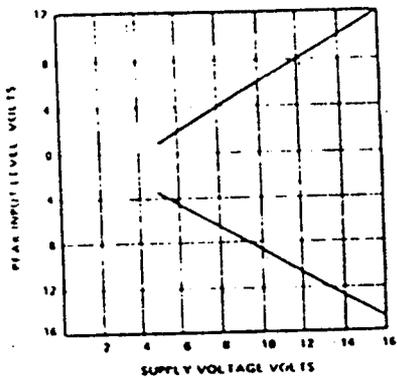
Figure 10. Multiplier Input Dynamic Range vs Power Supply
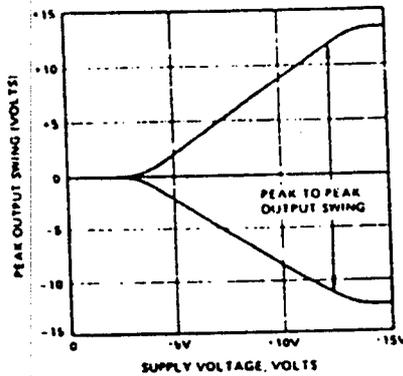
Figure 11. Op Amp Output Swing vs Power Supply
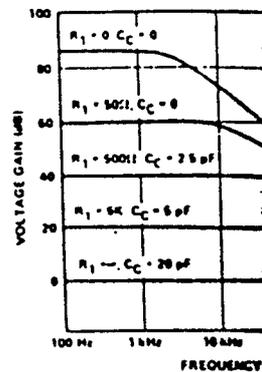
Figure 12. Op Amp Frequency Response
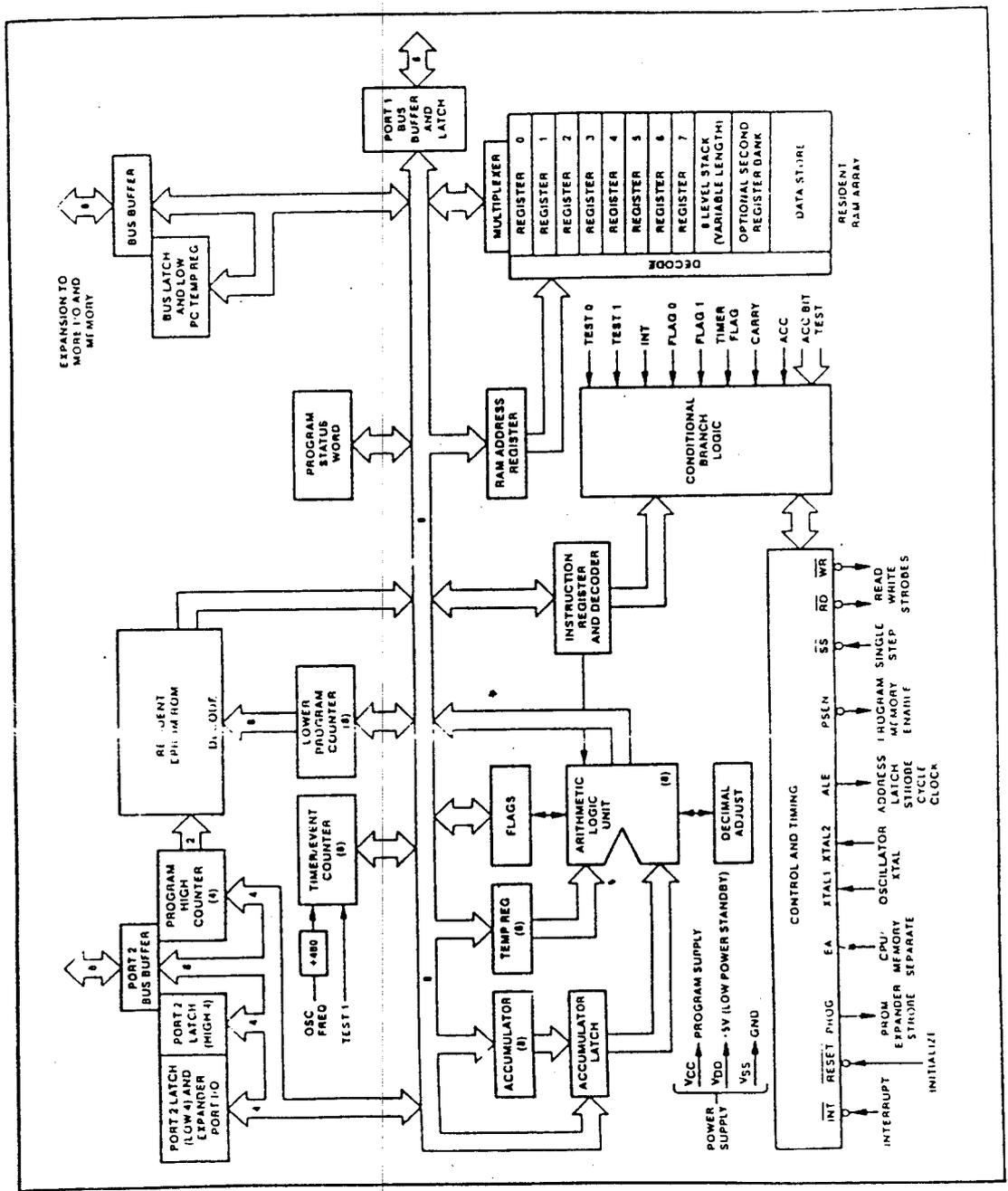
Figure 2-1. 8748H/8048AH/8749H/8049AH/8050AH Block Diagram
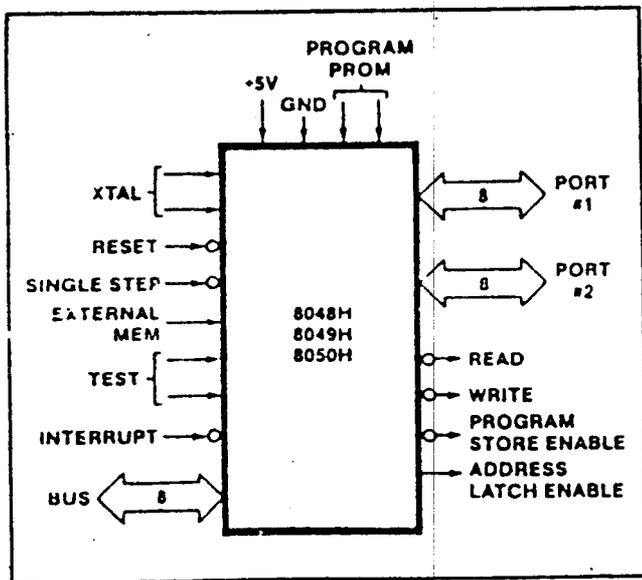
Figure 2-16. 8048AH and 8049AH Logic Symbol
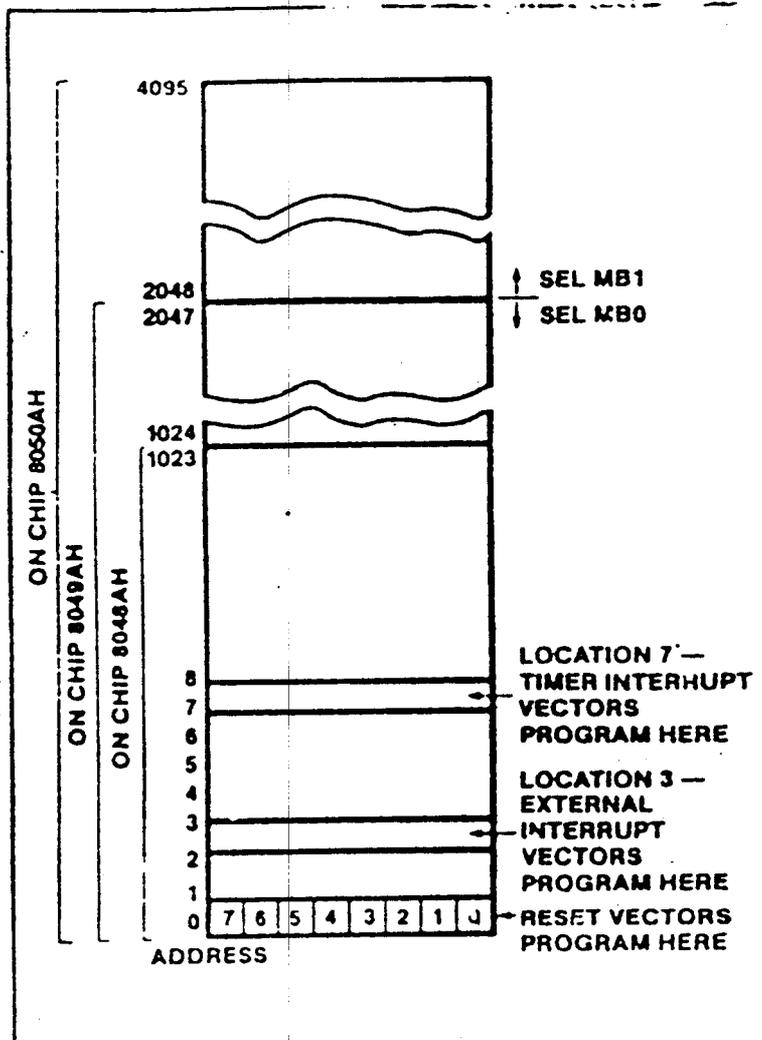
Figure 2-2. Program Memory Map
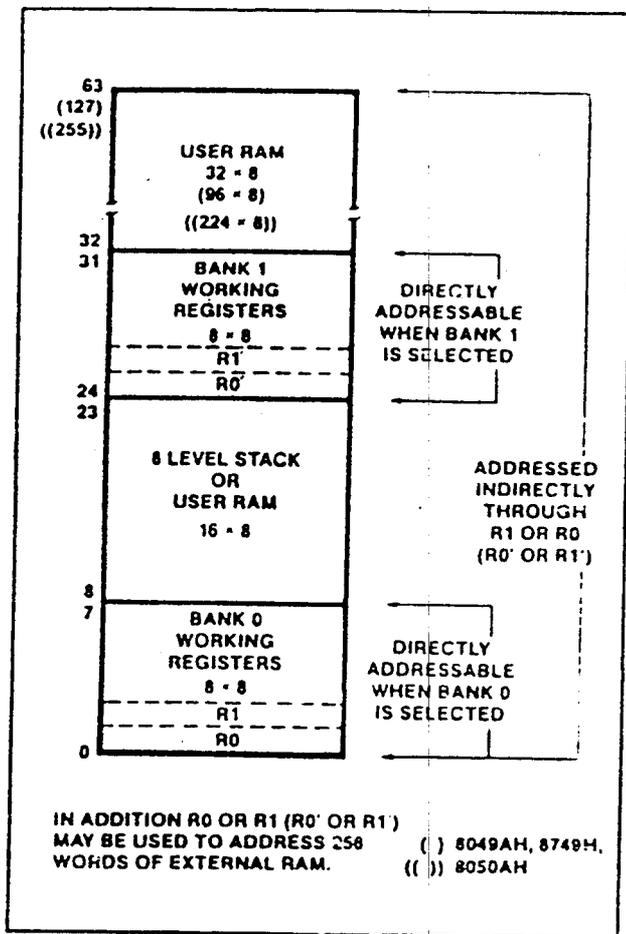
Figure 2-3. Data Memory Map

8048AH/8748H/8049AH/8749H
Instruction Set Summary

Mnemonic	Description	Bytes	Cycle
Accumulator			
ADD A, R	Add register to A	1	1
ADD A, @R	Add data memory to A	1	1
ADD A, # data	Add immediate to A	2	2
ADDC A, R	Add register with carry	1	1
ADDC A, @R	Add data memory with carry	1	1
ADDC A, # data	Add immediate with carry	2	2
ANL A, R	And register to A	1	1
ANL A, @R	And data memory to A	1	1
ANL A, # data	And immediate to A	2	2
ORL A, R	Or register to A	1	1
ORL A @R	Or data memory to A	1	1
ORL A, # data	Or immediate to A	2	2
XRL A, R	Exclusive Or register to A	1	1
XRL A, @R	Exclusive or data memory to A	1	1
XRL A, # data	Exclusive or immediate to A	2	2
INC A	Increment A	1	1
DEC A	Decrement A	1	1
CLR A	Clear A	1	1
CPL A	Complement A	1	1
DA A	Decimal adjust A	1	1
SWAP A	Swap nibbles of A	1	1
RL A	Rotate A left	1	1
RLC A	Rotate A left through carry	1	1
RR A	Rotate A right	1	1
RRC A	Rotate A right through carry	1	1
Input/Output			
IN A, P	Input port to A	1	2
OUTL P, A	Output A to port	1	2
ANL P, # data	And immediate to port	2	2
ORL P, # data	Or immediate to port	2	2
*INS A, BUS	Input BUS to A	1	2
*OUTL BUS, A	Output A to BUS	1	2
*ANL BUS, # data	And immediate to BUS	2	2
*ORL BUS, # data	Or immediate to BUS	2	2
MOVD A, P	Input Expander port to A	1	2
MOVD P, A	Output A to Expander port	1	2
ANLD P, A	And A to Expander port	1	2
ORLD P, A	Or A to Expander port	1	2

Mnemonics copyright Intel Corporation 1983
*For use with internal memory only.

Mnemonic	Description	Bytes	Cycles
Registers			
INC R	Increment register	1	1
INC @R	Increment data memory	1	1
DEC R	Decrement register	1	1
Branch			
JMP addr	Jump unconditional	2	2
JMPP @A	Jump indirect	1	2
DJNZ R, addr	Decrement register and jump	2	2
JC addr	Jump on carry = 1	2	2
JNC addr	Jump on carry = 0	2	2
JZ addr	Jump on A Zero	2	2
JNZ addr	Jump on A not Zero	2	2
JT0 addr	Jump on T0 = 1	2	2
JNT0 addr	Jump on T0 = 0	2	2
JT1 addr	Jump on T1 = 1	2	2
JNT1 addr	Jump on T1 = 0	2	2
JF0 addr	Jump on F0 = 1	2	2
JF1 addr	Jump on F1 = 1	2	2
JTF addr	Jump on timer flag = 1	2	2
JNI addr	Jump on INT = 0	2	2
JBb addr	Jump on Accumulator Bit	2	2
Subroutine			
CALL addr	Jump to subroutine	2	2
RET	Return	1	2
RETR	Return and restore status	1	2
Flags			
CLR C	Clear Carry	1	1
CPL C	Complement Carry	1	1
CLR F0	Clear Flag 0	1	1
CPL F0	Complement Flag 0	1	1
CLR F1	Clear Flag 1	1	1
CPL F1	Complement Flag 1	1	1
Data Moves			
MOV A, R	Move register to A	1	1
MOV A, @R	Move data memory to A	1	1
MOV A, # data	Move immediate to A	2	2
MOV R, A	Move A to register	1	1
MOV @R, A	Move A to data memory	1	1
MOV R, # data	Move immediate to register	2	2
MOV @R, # data	Move immediate to data memory	2	2
MOV A, PSW	Move PSW to A	1	1
MOV PSW, A	Move A to PSW	1	1

8048AH/8748H/8049AH/8749H
Instruction Set Summary (Con't)

Mnemonic	Description	Bytes	Cycle
Data Moves			
(Cont'd)			
XCH A, R	Exchange A and register	1	1
XCH A, @R	Exchange A and data memory	1	1
XCHD A,@R	Exchange nibble of A and register	1	1
MOVX A. @R	Move external data memory to A	1	2
MOVX @R, A	Move A to external data memory	1	2
MOVP A @A	Move to A from current page	1	2
MOVP3 A. @	Move to A from Page 3	1	2
Timer/Counter			
MOV A T	Read Timer/Counter	1	1
MOV T A	Load Timer/Counter	1	1
STRT T	Start Timer	1	1
STRT CNT	Start Counter	1	1
STOP TCNT	Stop Timer/Counter	1	1
EN TCNTI	Enable Timer/Counter Interrupt	1	1
DIS TCNTI	Disable Timer/Counter Interrupt	1	1

Mnemonic	Description	Bytes	Cycle
Control			
EN I	Enable external Interrupt	1	1
DIS I	Disable external Interrupt	1	1
SEL RB0	Select register bank 0	1	1
SEL RB1	Select register bank 1	1	1
SEL MB0	Select memory bank 0	1	1
SEL MB1	Select memory bank 1	1	1
ENT0 CLK	Enable clock output on T0	1	1
NOP	No Operation	1	1