

Electronic Graphic Display Unit

PROJECT REPORT

Submitted in partial fulfilment of the requirements for the award of the degree of Bachelor of Engineering in Electrical & Electronics Engineering of the Bharathiar University. Coimbatore-641 046

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We also extend our sincere thanks to Electronics and communication department faculty members for their kind co-operation by providing instruments for testing purpose of this project.

SYNOPSIS

This project comprises the fabrication of an electronic circuit which displays the frequency response of any two port network on the cathode ray oscilloscope. The system based on the 8038 voltage controlled oscillator operates in the frequency range of 100 Hz to 100 KHz, separate amplitude and phase response outputs are available. A variable amplitude swept frequency oscillator has been designed for the amplitude Vs frequency plot. The project is a low cost and efficient device that obviates the necessity of making tedious measurements in industrial and research laboratories. The designed circuit is compatible with any modern oscilloscope and can also be used with an x.t plotter with minor modifications. The frequency response of several two port networks such as filters (active and passive) have been obtained by using the proposed circuit. These responses of the circuit have been found to agree with the theoretical response obtained by computer simulation.

CHAPTER - I
INTRODUCTION

1.1 AIM OF THIS PROJECT :

The fundamental objective of the project "ELECTRONIC GRAPHIC DISPLAY UNIT" comprises the design and fabrication of a circuit that is capable of displaying the frequency response of any low power two port network.

The frequency response has two basic parts.

1. The Amplitude response.
2. The phase response.

These can be displayed on two channels of the oscilloscope or can be taken on x-t plotter with minor modifications. Only oscilloscope display part is made available here in this project.

Frequency response of networks help in providing vital information about the nature of the network. Circuit parameters such as gain, cutoff and resonant frequencies, band width, gain and phase margins etc., can be easily determined. The effect of changes in circuit components on the characteristics can be studied while the circuit is in operation. This can give a good insight to us while explanation of the network is going

on. In Industrial laboratories this facility could be very helpful in trimming component values to obtain optimum performance. For example the effect of variation of capacitance or inductance on resonant frequency and Q factor of the resonant circuit can be seen clearly.

1.2 HISTORICAL DEVELOPMENT :

Earlier circuits used transistorized voltage controlled oscillation or VCO's based on basic linear IC's such as the 741. These circuits were based on concepts such as the use of JFET's as voltage variable resistor (VVRs) etc., such devices had inherent disadvantages of low frequency range (less than 2KHz), poor FM linearity and high total harmonic distortion. These were essentially due to non linear V_{gs} - R_d characteristics of the JFET.

Better components improved the linearity but the low frequency range, distortion and high sensitivity remained. The phase response within our knowledge is an absolutely original idea. The earlier circuits could only give the phase at a fixed frequency and repetitive measurements had to be made to obtain the graph.

The proposed EGDU circuit is based on the monolithic integrated circuit 8038. This chip is capable

of producing stable sine frequencies from 0.001Hz to 300KHz. Facility for frequency sweeping is available and good FM linearity of 0.5% can be achieved. The total harmonic distortion is also greatly reduced.

A variable amplitude output is available from the EGDU. There are three frequency ranges for the circuit (100Hz - 1KHz, 1KHz - 10KHz, 10KHz to 100KHz). Any Audio frequency to lower intermediate frequency circuit response can be obtained. The response is obtained on both sides of the zero axis of the CRO and the positive side response above can be obtained by merely connected a small signal diode at the output of the test circuit.

The phase plot is based on the central concept of using timing pulses from the VCO inputs and two port network output in order to give a voltage proportional to the phase angle difference between the two signals. The basic components are the LM339 based zero crossing detector and a 555 based bistable MV. Lag and lead can be easily distinguished because of operation in all four quadrants.

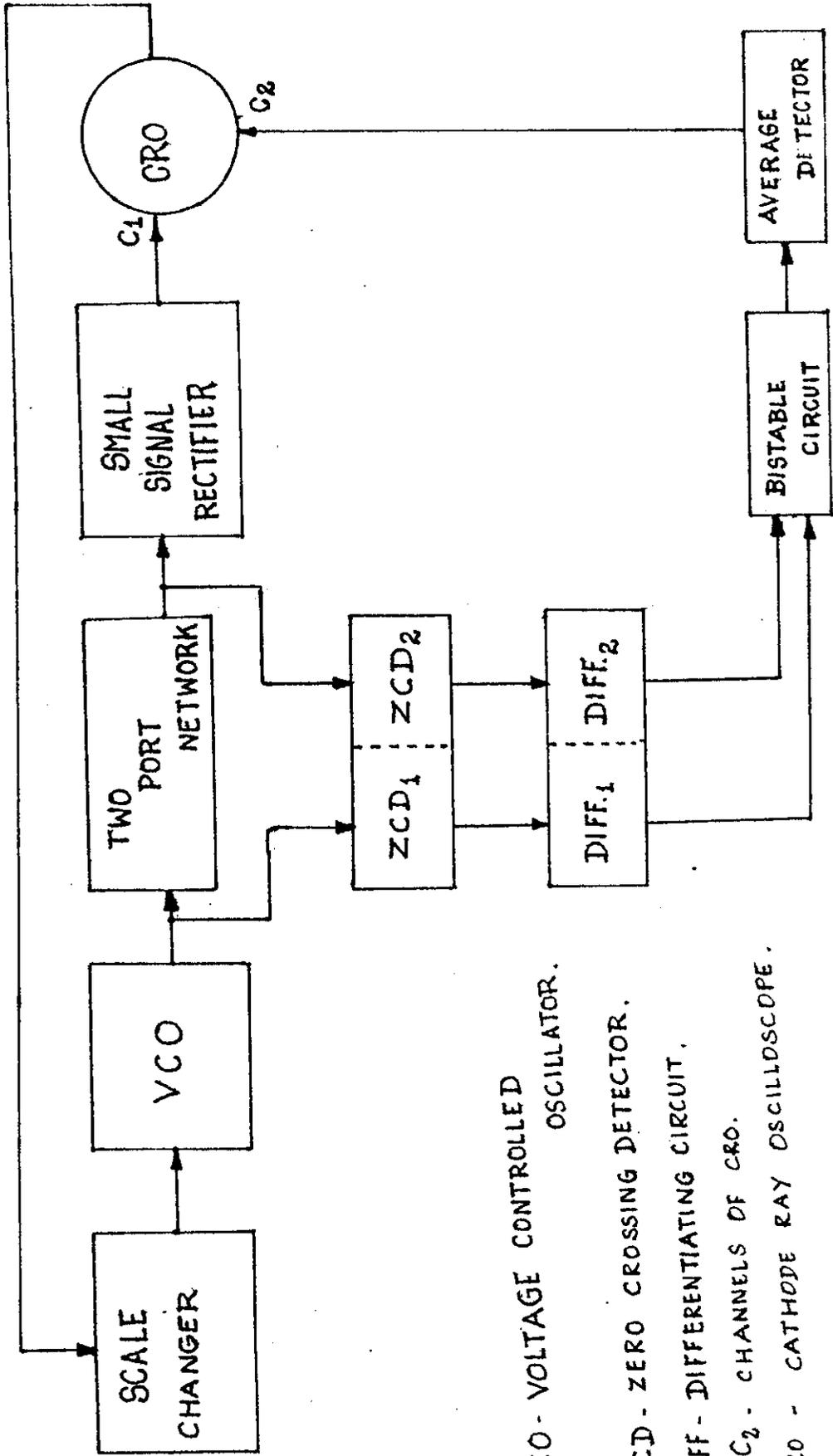


FIG.1.1 BLOCK DIAGRAM OF ELECTRONIC GRAPHIC DISPLAY UNIT

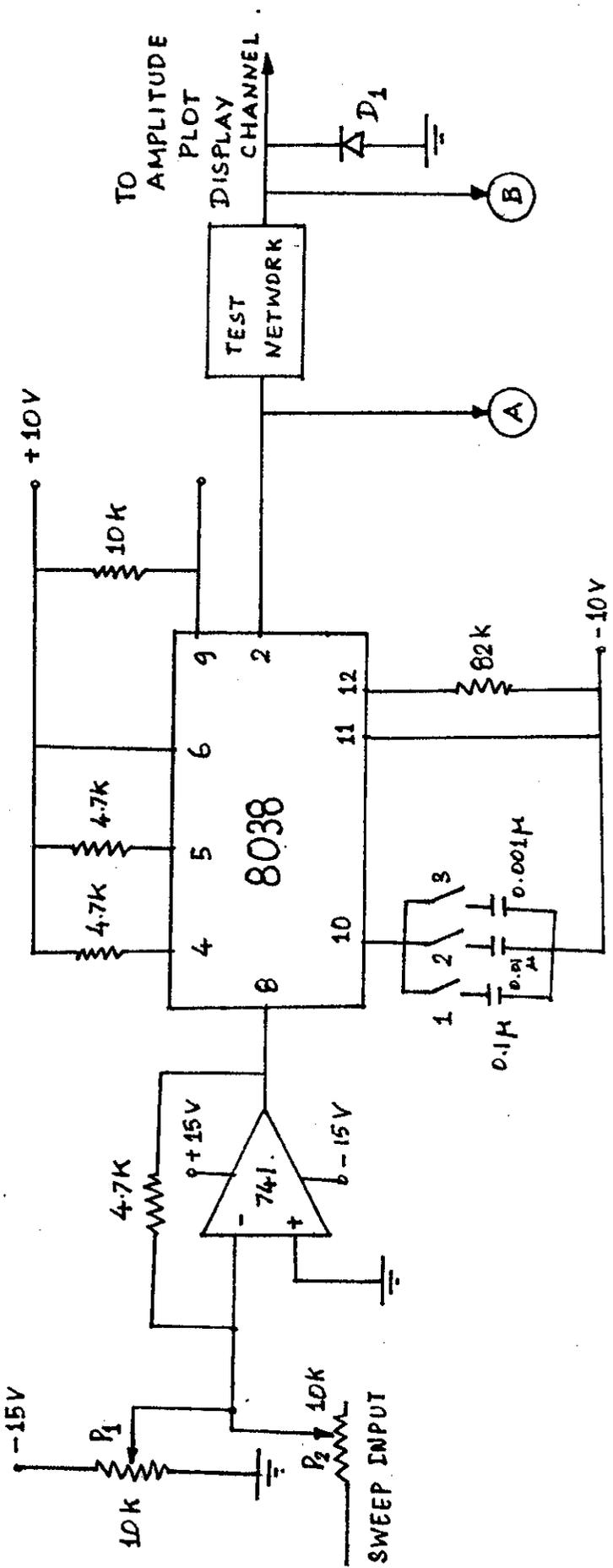


FIG.1.2 CIRCUIT DIAGRAM FOR AMPLITUDE PLOT DISPLAY.

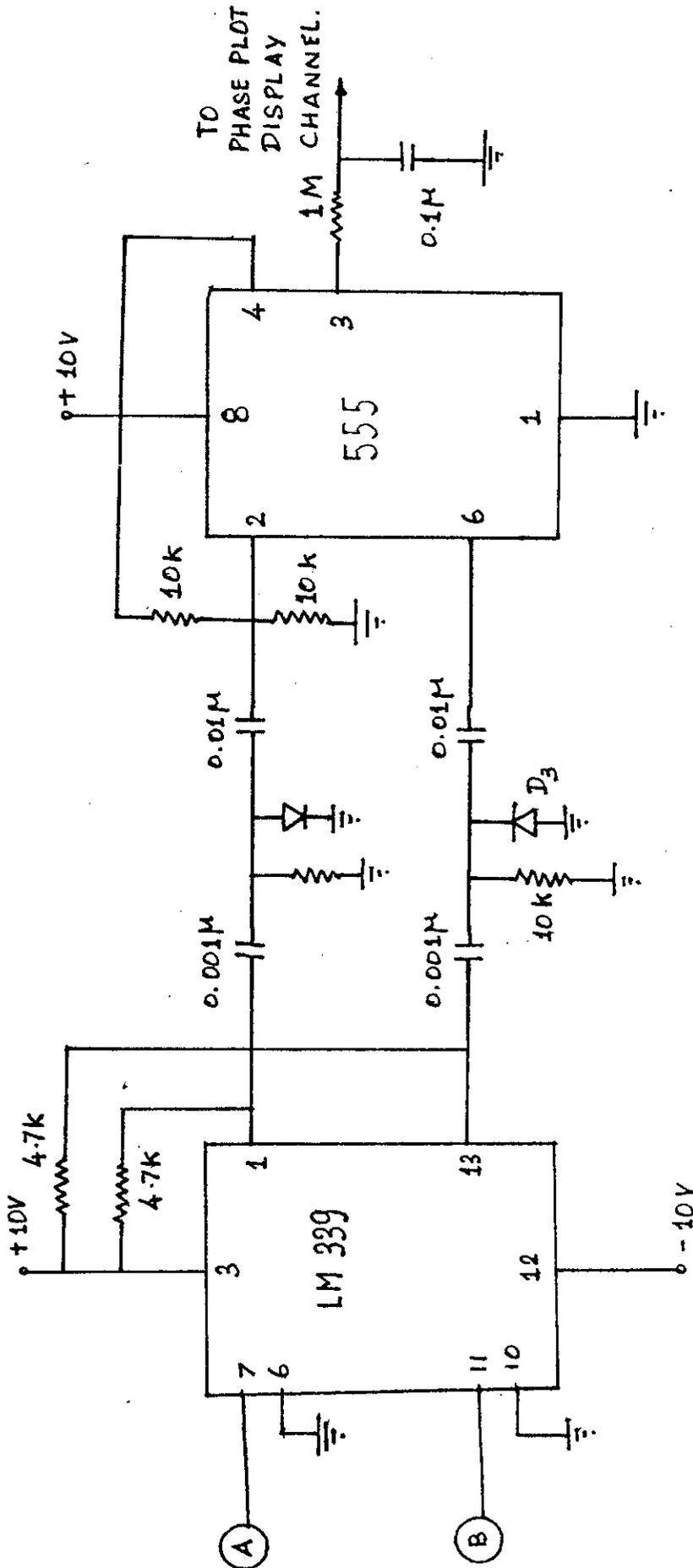


FIG. 1.3 CIRCUIT DIAGRAM FOR PHASE PLOT DISPLAY.

1.3 ORGANIZATION OF THE REPORT

CHAPTER 2 deals with design and working of the amplitude response circuitary. This is the first part of the project.

CHAPTER 3 gives with the design of the EGDU circuit. The designing of the circuit is well explained in this chapter.

CHAPTER 4 describes the second part of the project namely the phase response circuit features and design. Grapphs are used to illustrate the idea on which it is based.

CHAPTER 5 gives the design details of the quad comparator namely LM 339, differentiator circuit as well as details about blistable multivibrator.

CHAPTER 6. gives the procedure of how to use the EGDU.

CHAPTER 7. gives the result Analysis and test waveforms.

CHAPTER 8. conclusion is given in this chapter.

CHAPTER 2

AMPLITUDE RESPONSE DISPLAY SYSTEM

2.1 As mentioned in the first chapter, the amplitude response display system is used to display the amplitude Vs. frequency plot on a cathode Ray Oscilloscope (CRO). The block display is shown in fig.2.1. The explanation of each building block along with the necessary design is describe in this chapter.

2.2 SWEEP GENERATOR

The sweep generator is used to give a negative going ramp whose voltage can be swept from $V+$ by $1/3V$ supply- $2V$ to be fed to voltage controlled oscillator. The sweep output terminal provided in any modern CRO and operational Amplifier summer constitute the sweep generator. Sweep voltage of any cathode ray oscilloscope is highly linear in nature and has zero fly back time. The swept voltage of the CRO which is a positive going ramp is fed to an opAmp. Summer as shown in fig.2.2 preset 1 is provided for the purpose of adjusting the magnitude of the sweep and preset 2 is used for controlling sweep position. The potentiometers have to be adjusted so that the sweep voltage varies from $V+$ down by $1/3 V$ supply - 2 volts (i.e) from 10 volts down

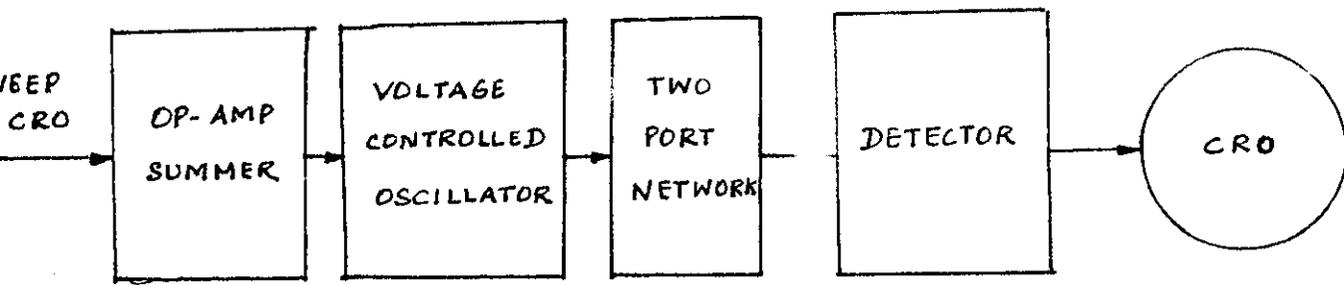


FIG. 2.1 BLOCK DIAGRAM OF AMPLITUDE RESPONSE DISPLAY SYSTEM.

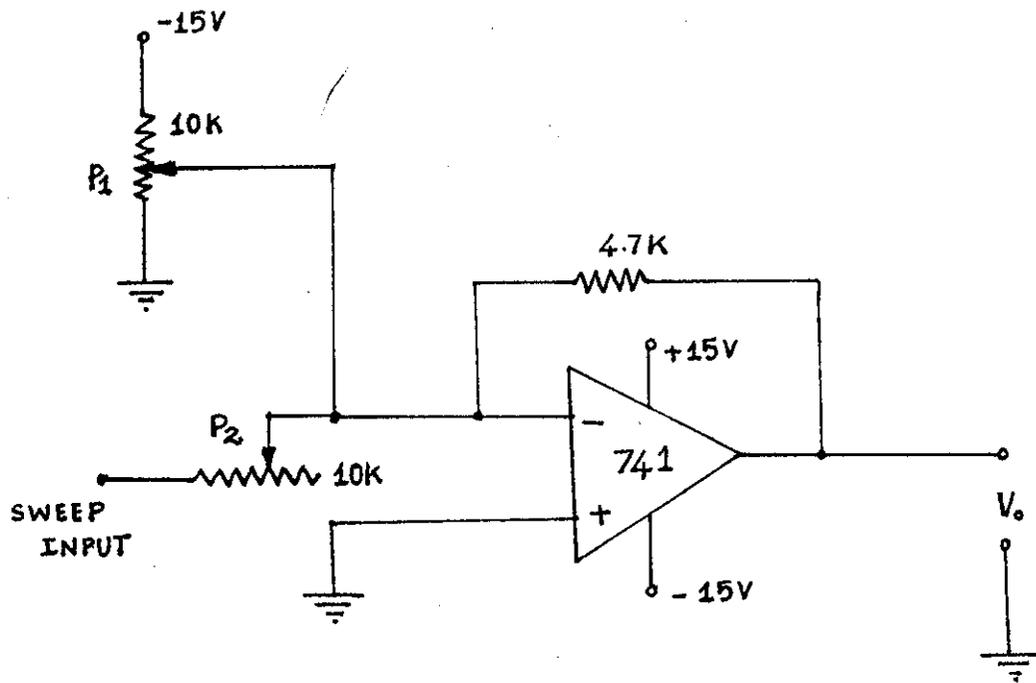


FIG. 2.2 OPAMP SUMMER.

to 4.66v where V_+ refers to the positive supply voltage of the VOLTAGE CONTROLLED OSCILLATOR and V supply refers to V_+ to V_- which is equal to 20v since a dual supply of + or - 10v has been used for the voltage controlled oscillator. The output of the opAmp summer will be a negative going ramp as indicated in the figure.2.2

2.3 VOLTAGE CONTROLLED OSCILLATOR (VCO)

Voltage controlled oscillator (VCO) is obtained by using 8038 IC. The description of the chip is given below and the chip specification are given in appendix 1.

The 8038 waveforms generator is a monolithic integrated circuit capable of producing high accuracy sine, square, triangular, sawtooth and pulse waveforms with a minimum of external components. The frequency can be selected externally from 0.001Hz to more than 300 KHz using either resistors or capacitors. 8038 IC is fabricated with advanced monolithic technology using schottky-barrier diodes and thin-film resistors, and the output is stable over a wide range to temperature and supply variations. The operation of 8038 function generator is based mainly on the linear charging and discharging of a capacitor. This produces triangular

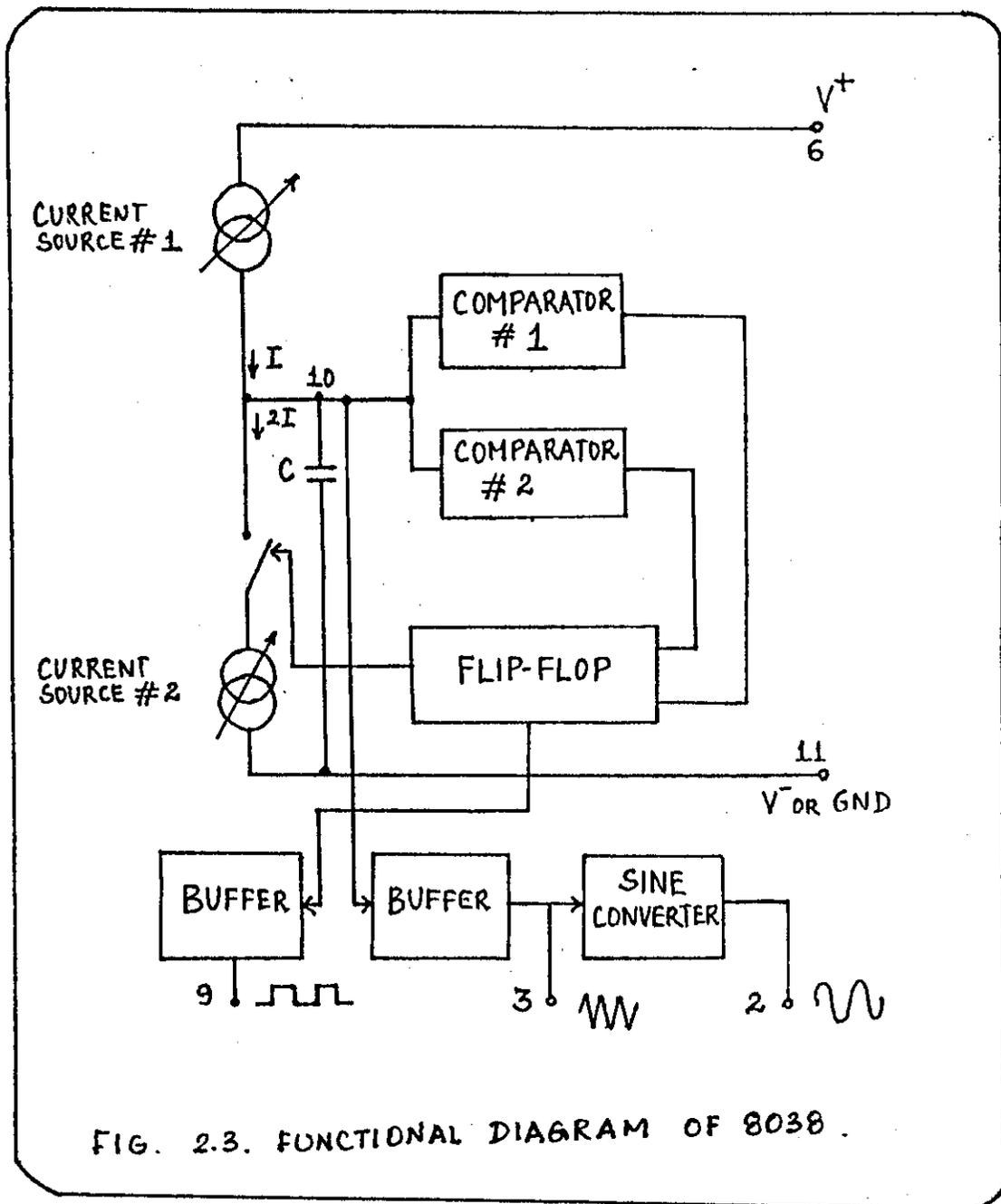


FIG. 2.3. FUNCTIONAL DIAGRAM OF 8038 .

waveform from which the square and sine waves are obtained. Fig. 2.3 shows the functional diagram of the IC and the Appendix 2 shows the pin configuration.

An external capacitor C is charged and discharged by two current sources. Current source 2 is switched On and OFF by a flip-flop, which current source 1 is ON continuously. Assuring that the the flip-flop is in a state such that current source 2 is OFF, and the capacitor C is charged with a current I, the voltage across the capacitor rises linearly with time. When this this voltage reaches the level of comparator 1 (set at $2/3$ of the supply voltage), the flip flop is triggered, changes state and releases current source 2. This current source normally carries a current "2I" thus the capacitor is discharged with a net current I and the voltage across it drops linearly with time. When it has reached the level of comparator 2 (set at $1/3$ of the supply voltage) the flip-flop is triggered into its original state and the cycle starts again. With the current sources set at I and 2 I respectively, the charge and discharge times are equal. Thus a triangle waveform is created across the capacitor and the flip flop produces a square-wave. Both waveforms are fed to buffer stages and are available at pins 3 and 9.

The levels of the current sources can, however, be selected over a wide range with two external resistors. Therefore, with the two currents set at values different from I and 2I, an assymmetrical sawtooth appears at terminal 3 and pulses with a duty cycle from less than 1% to greater than 99% are available at terminal 9.

The sine wave is created by feeding the triangle wave into a non-linear network (sine converter). This network provides a decreasing shunt impedance as the potential of the triangle moves towards the two extremes.

2.4 WAVEFORM TIMING :

The symmetry of all wave forms can be adjusted with the external timing resistor Ra and Rb. Ra controls the rising portion of the triangle and sine wave and the 1 state of the square wave.

The magnitude of the triangular waveform is set at 1/3 supply, therefore the rising portion of the triangle is

$$\begin{aligned}
 t_1 &= \frac{C \times V}{I} \\
 &= \frac{C \times (1/3) \times V_{\text{supply}} \times R_a}{(1/5) \times V_{\text{supply}}}
 \end{aligned}$$



$$= (5/3) \times R_a \times C$$

The falling portion of the triangle and sinewave and 0 state of the square wave is

$$\begin{aligned}
 t_2 &= \frac{C \times V}{I} \\
 &= \frac{C \times (1/3) \times V_{\text{supply}}}{(2/5) \times (V_{\text{supply}}/R_b) - (1/5) \times (V_{\text{supply}}/R_a)} \\
 &= (5/3) \times R_a \times R_b \times C / (2 \times R_a - R_b)
 \end{aligned}$$

Thus a 50% duty cycle is achieved when $R_a = R_b$ with two separate timing resistors, the frequency is given by

$$\begin{aligned}
 f &= 1 / (t_1 + t_2) \\
 &= \frac{1}{(5/3) \times R_a \times C \times (1 + (R_b / (2 \times R_a - R_b)))}
 \end{aligned}$$

if $R_a = R_b = R$, $f = (0.3) / (R \times C)$

Neither time nor frequency is dependent on supply voltage, even though none of the voltage are regulated inside the integrated circuit. This is due to the fact that both current and thresholds are direct, linear function of the supply voltage and thus their effects cancel.

It minimize sine wave distortion 82 K resistor between pnts 11 & 12 is connected with this arrangement distortion of less than 1% is achievable.

CHAPTER 3

CHOICE OF ELEMENTS

3.1 SELECTING Ra, Rb & C.

For any given output frequency, there is a wide range of RC combinations that will work, however certain constraints are placed upon the magnitude of the charging current for optimum performance. At the low end, currents of less than 1 uA are undesirable because circuit leakages will contribute significant errors at high temperatures. At higher currents (I less than 5 mA), transistor betas and saturation voltages will contribute increasingly larger errors. Optimum performance will, therefore, be obtained with charging currents of 10uA and 1 mA. The magnitude of charging current for Ra =4.7 K, Rb =4.7 K is given by

$$I = \frac{R_1 (V - V)}{(R_1 + R_2)} \times \frac{1}{R_a} = \frac{(V - V)}{5 R_a}$$
$$= 0.851 \text{ mA}$$

3.2 WAVEFORM CONTROL AND POWER SUPPLIES:

The waveform generator can be operated either from a single power supply (10 to 30 volts) or a

dual power supply (+ or - 5 to + or - 15v). With a single power supply the average levels of the triangle and sine-wave are at exactly one-half of the supply voltage, while the square wave alternates between $V+$ and ground. A split power supply has the advantage that all waveforms move symmetrically about ground.

The output of the buffer, the square wave output, is of open collector type. In the open collector type, there is a short (0.2v) between the output and negative supply (pin 11) during negative half cycle but the output is open during next half cycle. A pull-up resistor (10-15 K ohms) should be connected between pin 9 and positive supply to obtain output voltage. Although this may appear to be inconvenient, one can pull-up the output to some voltage other than that from which the device is operated. Thus the square wave can be made compatible with any digital logic family. With a pull-up resistor the peak to peak amplitude of the square-wave is 90% of the difference in potential between the pull up supply and $-V_{cc}$. The output pull-up resistor, $R_{pull-up}$, should be high enough to avoid excessive power dissipation yet low enough to supply enough drive to switch whatever circuitry is used on the output.

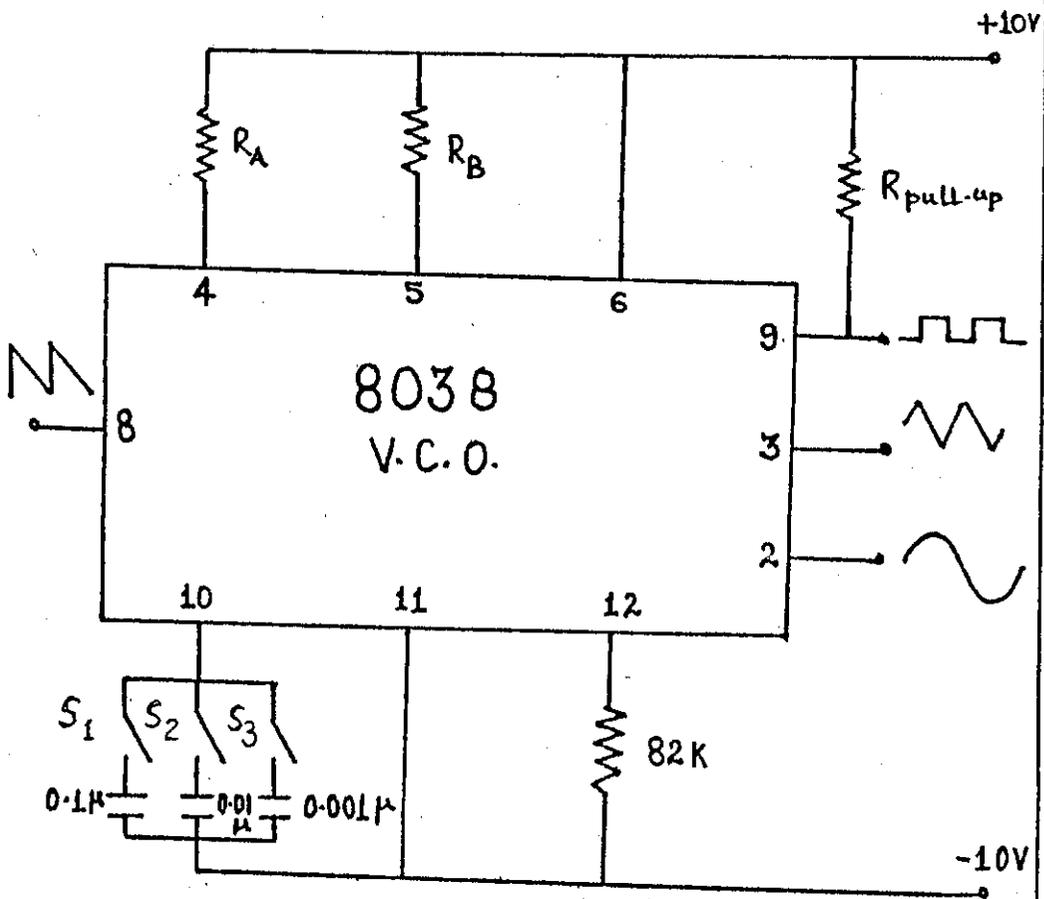


FIG. 3.1 VOLTAGE CONTROLLED
OSCILLATOR

3.3 FREQUENCY MODULATION AND SWEEPING:

The frequency of the waveform generator is a

direct function of the DC voltage at terminal 8. By

altering this voltage, frequency modulation is performed.

For frequency sweeping, the entire bias for the current

sources is created. Care must be taken, to regulate the

supply voltage; in this configuration the charging

current is no longer a function of the supply voltage and

thus the frequency becomes dependent on the supply

voltage. The potential on pin 8 may be swept down from

V+ by (1/3 v supply - 2volts) with a + or - 10 volts

supply, voltage of pin 8 is swept down from + 10 volts by

4.66 volts. This is obtained from the Opamp summer and

sweep output of CRO and is fed at pin 8. Since the sweep

is provided from external source, equation (2.4) becomes

$$f = \frac{2 \times R \times C \times V_{\text{supply}}}{3 \times (V - V_{\text{pin8}})}$$

The frequency is lowest at the highest sweep

voltage (+ or - 10v) and highest at 4.66v. The sine-wave

output at 2 pin has an output impedance of 1 Kohm. The

magnitude of the sine-wave output is 0.2v supply.

3.4 FREQUENCY RANGE AVAILABLE:

By charging the timing capacitor, we obtain different frequency ranges. A three way switch provided for changing the frequency range of the VCO so that any network can be tested for the frequency ranging for 100Hz to 100KHz. The three ranges that are available by varying the switch positions are shown in table 1. The use of 8038 as VCO with Ra, Rb and C is given in fig 3.1

CAPACITOR VALUE	SWITCH POSITION	FREQUENCY RANGE AVAILABLE
0.1 uF	1	100 Hz - 1 KHz
0.01 uF	2	1 KHz - 10 KHz
0.001 uF	3	10 KHz - 100 KHz

Table 1 SWITCH POSITION AND FREQUENCY RANGES AVAILABLE

3.5 TWO PORT NETWORK:

Any two port network can be tested for its frequency response. The only requirement of two port network is that it should not load the VCO stage. Variation of any parameter with respect to frequency can also be visualised.

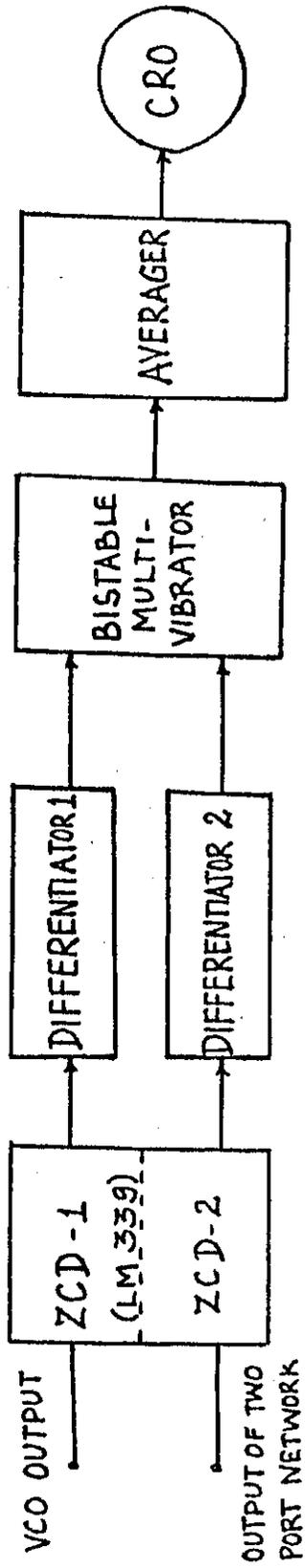


FIG. 3.2 BLOCK DIAGRAM OF PHASE RESPONSE

3.6 DETECTOR AND CRO:

The range of frequencies that are obtained from VCO is fed into the two port network under test. The response of the network is symmetrical with respect to X-axis. A small signal diode clips off the negative portion of the response and this is fed to the CRO. The response on the CRO will be a plot of Amplitude (Y-axis) Vs. frequency (X-axis).

In this chapter, the scheme for displaying the amplitude plot has been described. The 8038 waveform generator chip and its use as VCO has been dealt with elaborately. The next chapter explains the method of obtaining phase plot.

CHAPTER 4

PHASE RESPONSE DISPLAY SYSTEM

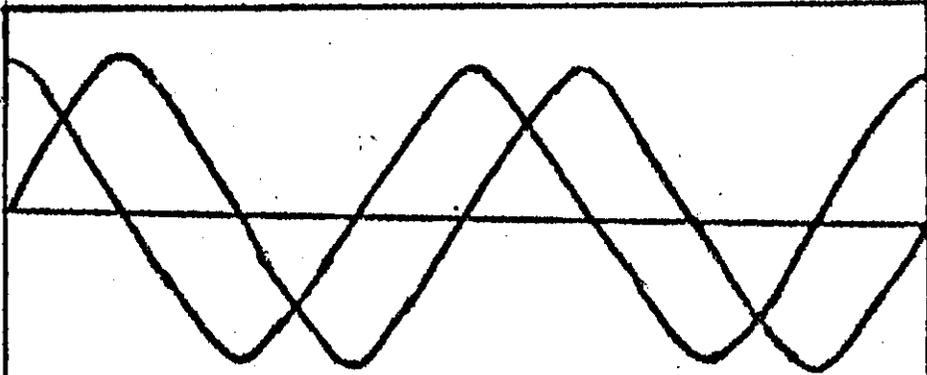
4.1 This chapter describes the second part of the project in detail, i.e., the method of obtaining phase plot. First the basic block diagram is shown in fig.3.2 and the individual blocks are explained later in detail.

4.2 PRINCIPLE OF OPERATION

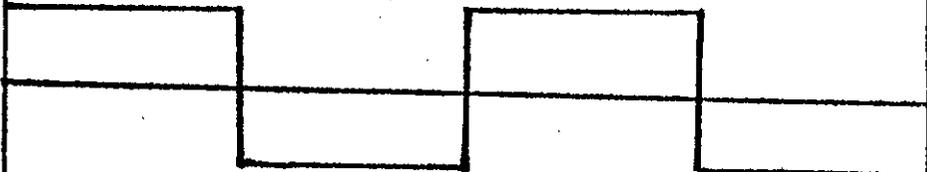
Zero crossing detectors are made use of to produce output, pulse at the zero crossing of the VCO and two port network output sinusoidal waveforms. The polarity of the pulse is positive or negative depending on whether the voltage goes from positive to negative or negative to positive. If the pulse goes from positive to negative, a negative pulse is produced and vice-versa. Negative pulse from the VCO and positive pulses from the test network are given to the set and reset terminals of the bistable multivibrator. The output of the bistable is a square wave whose duty cycle depends on the phase difference between the two voltages.

This can be understood by studying first the waveforms for a constant frequency setting for different phase differences. The waveforms are shown in

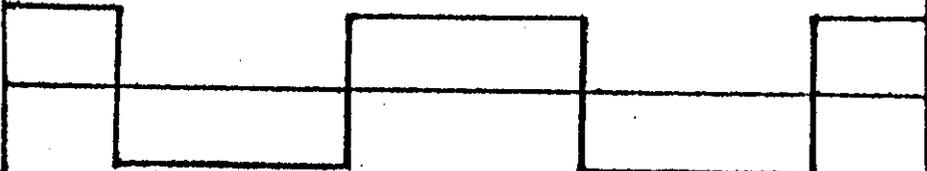
VCO AND
TEST CIRCUIT
OUTPUTS



COMPARATOR
2 OUTPUT



OUTPUT OF
COMPARATOR 4



ZCD₁ OUTPUT



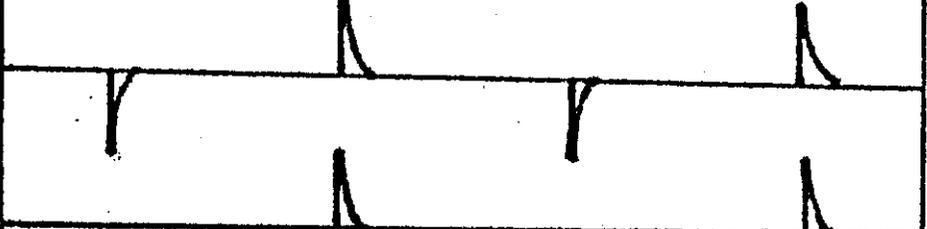
TRIGGER INPUT
OF 555



ZCD₂ OUTPUT



THRESHOLD
INPUT OF 555



555 OUTPUT



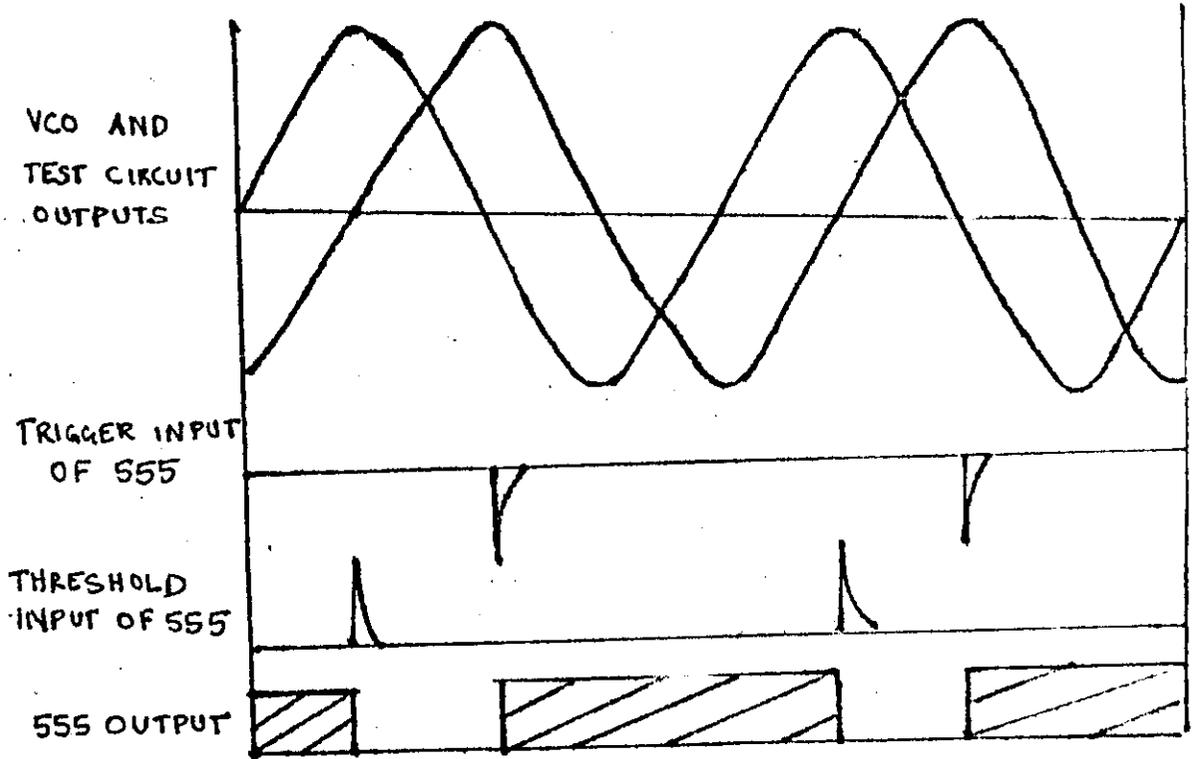
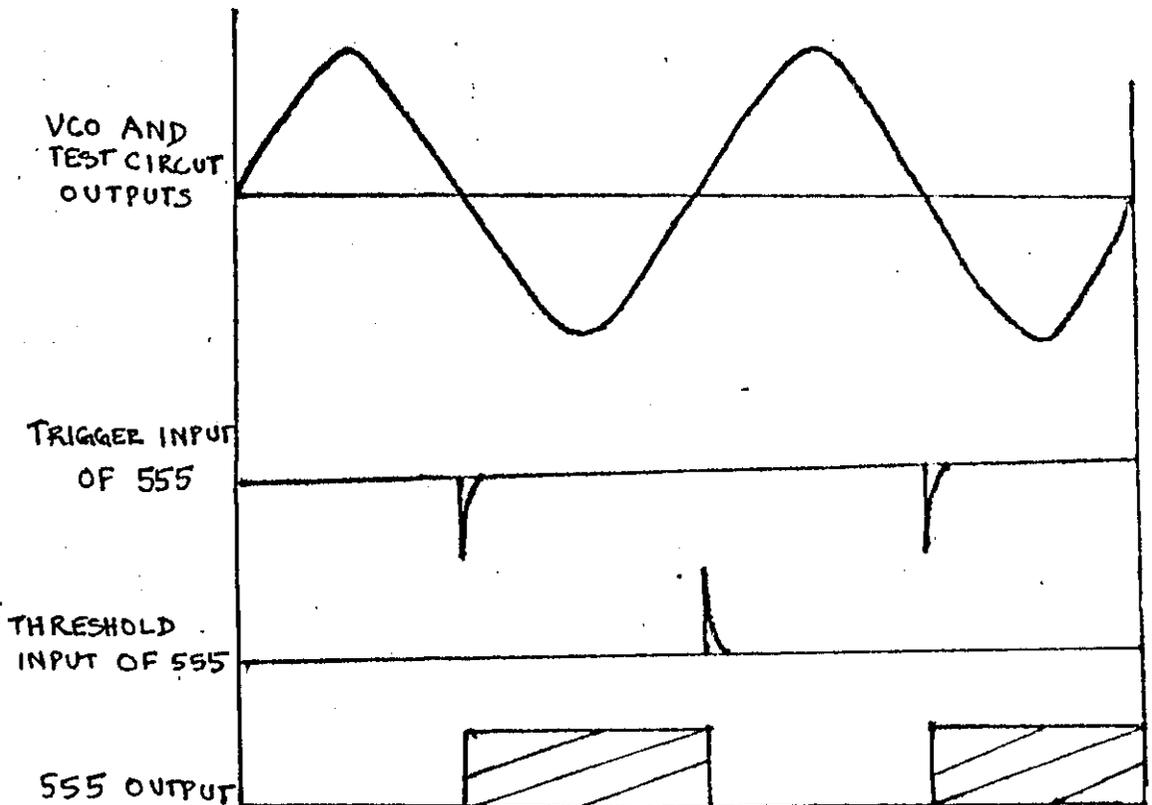


FIG. 4-3(a) WAVE FORMS FOR 90° LAG.



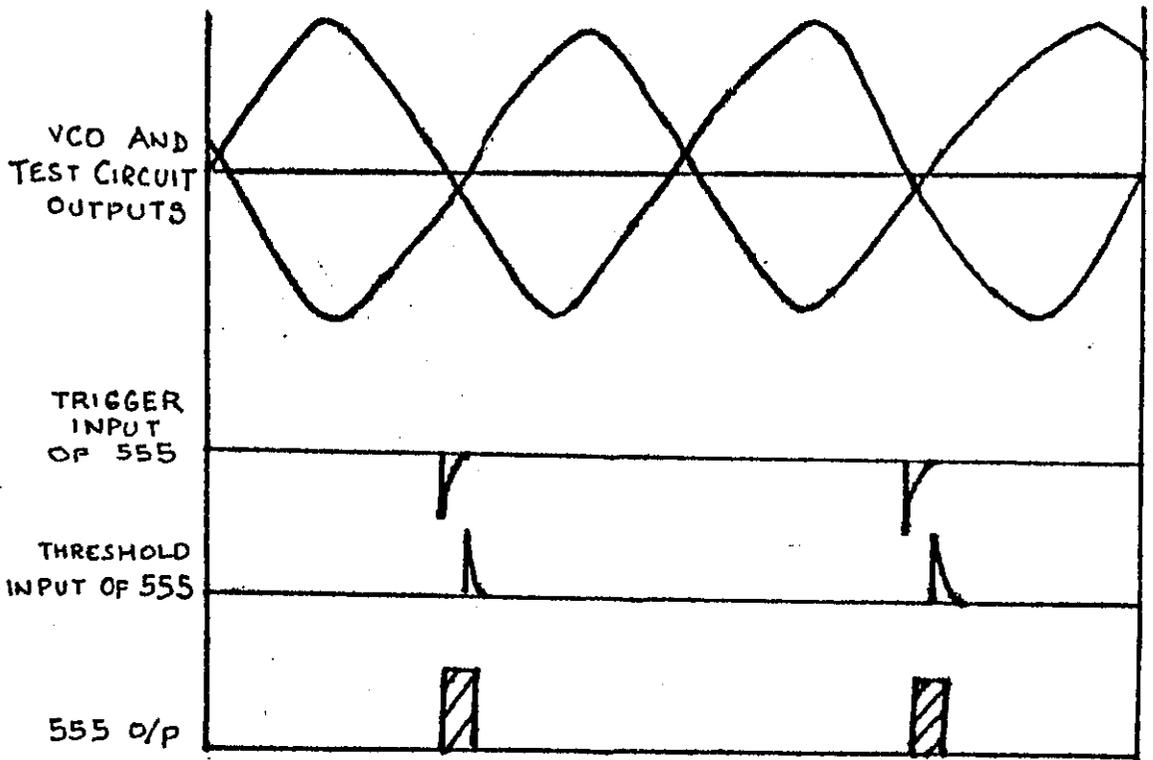
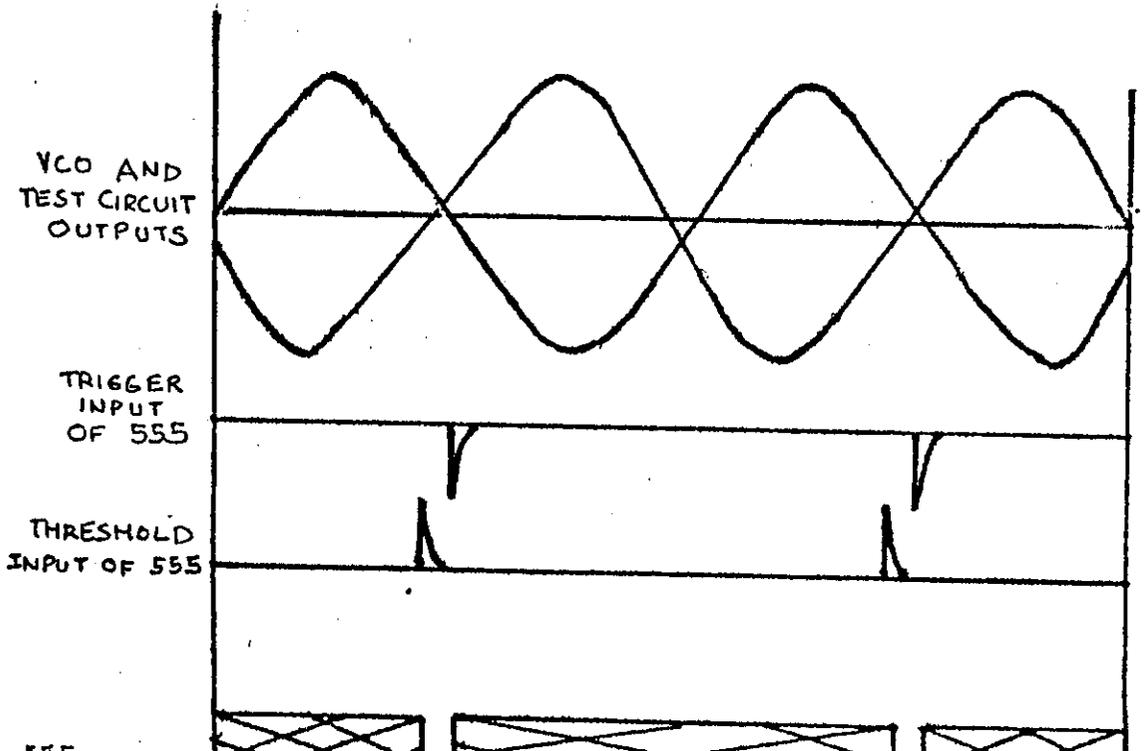


FIG 4.4 WAVEFORMS FOR 180° LEAD.



figs. 4.2 & 4.5

From the waveform it is seen that the output of the bistable is maximum for phase differences very nearly equal to 180 Degrees lag and minimum for 180 Degrees lead. For exact 180 degrees phase difference (lag or lead) the set and reset pulses occur at the same instant and hence racing condition occurs in the bistable which is nothing but an R-S flip-flop whose truth table is shown in table 2. The racing condition causes the output of the flip-flop to become indeterminate and hence an erroneous phase value may appear on the CRO screen after averaging (explained below).

However in actual circumstances, the phase difference is constantly changing and hence race condition exists only for a short duration. So there is no damage to the flip-flop.

For phase angles between 180 Degrees lag and 180 Degrees lead, the output waveform duty cycle reduces linearly from one to zero. Thus the basis for phase plot can be obtained. The variation of duty cycle with phase is shown in fig. 4.7

To obtain the actual plot, the square wave output of the bistable has to be averaged and this is

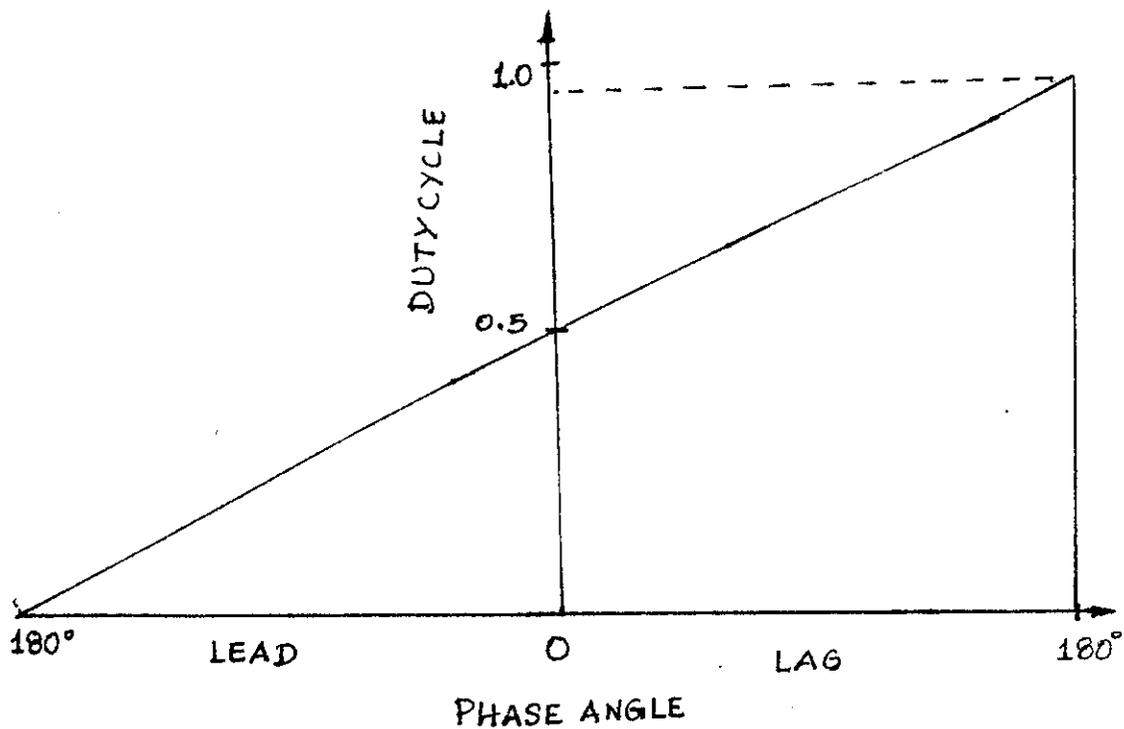


FIG. 4.7 VARIATION OF DUTY CYCLE WITH PHASE ANGLE.

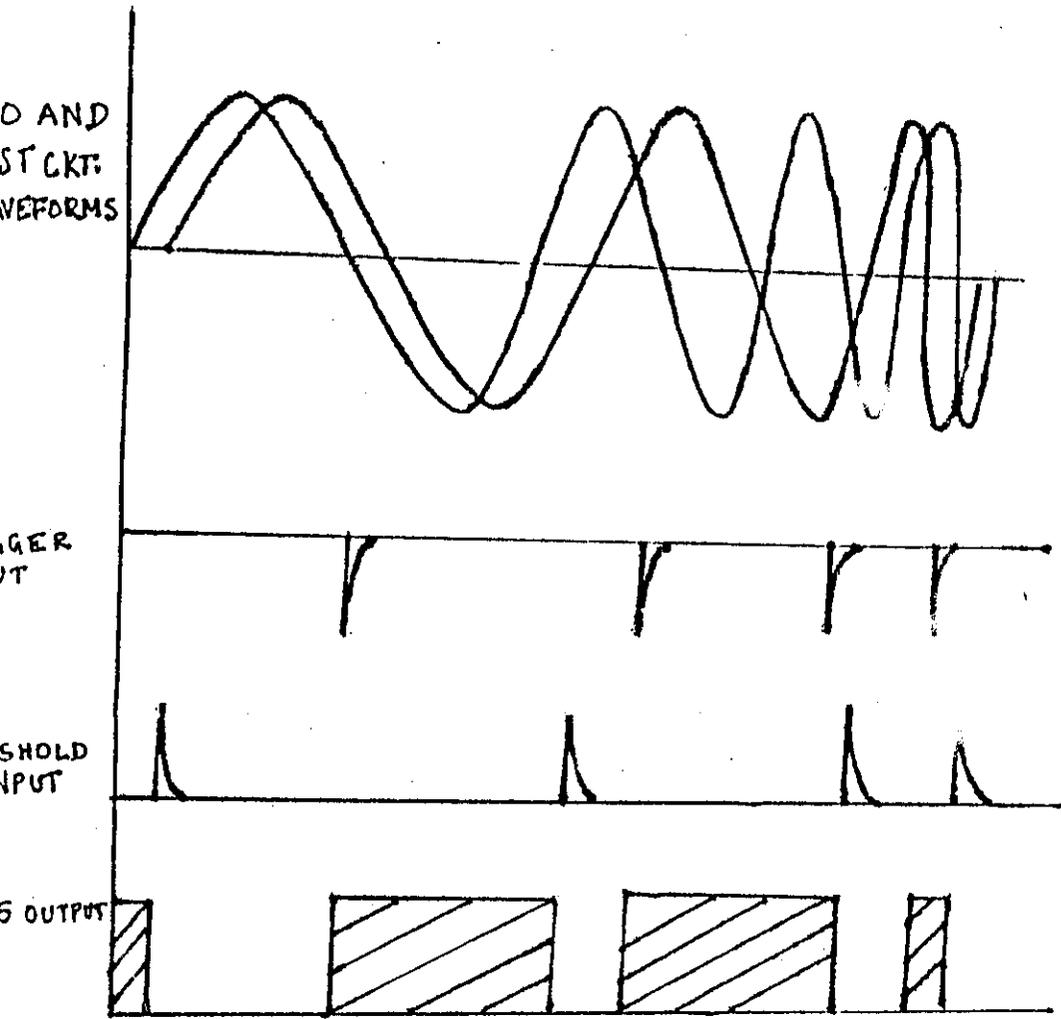
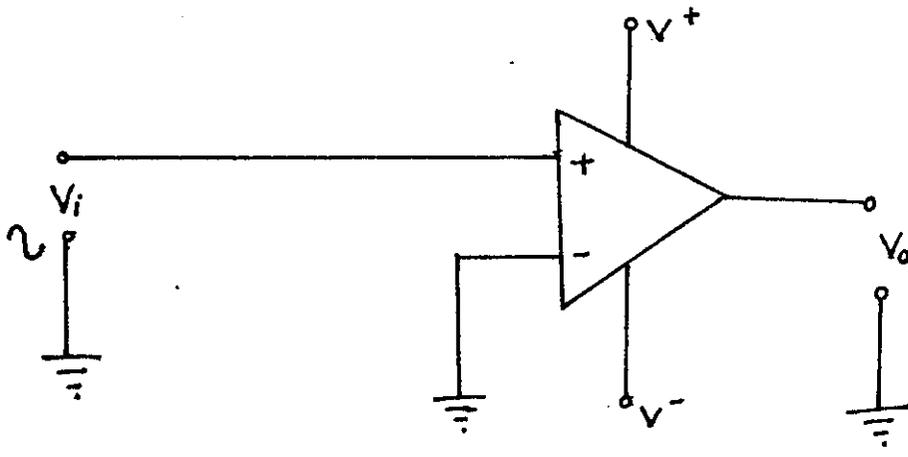
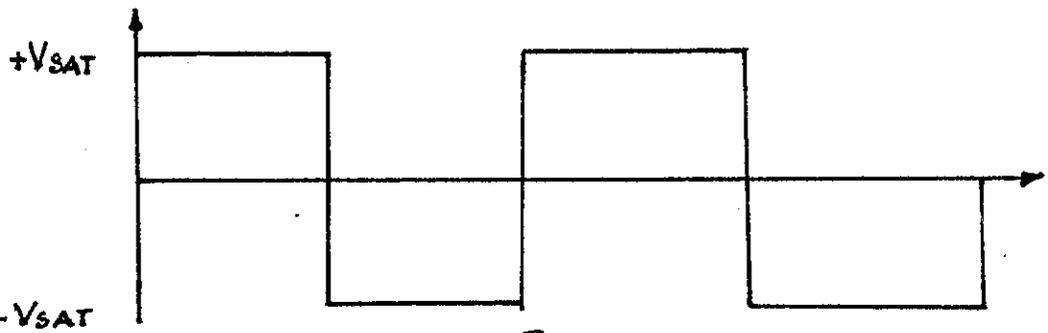
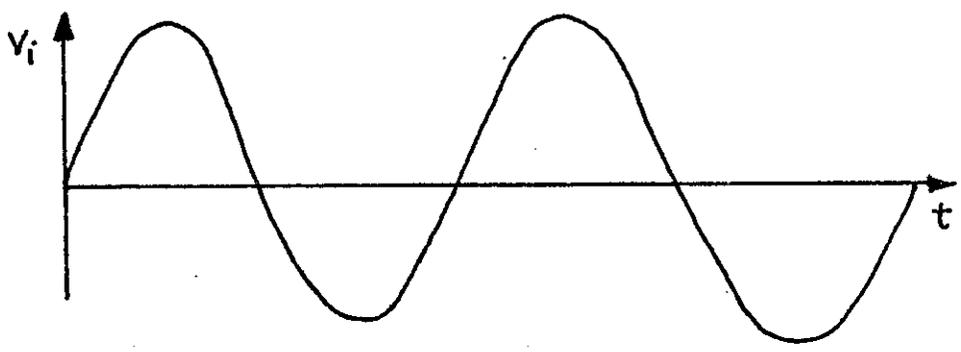


FIG. 4.8 WAVEFORMS FOR CONTINUOUSLY VARYING FREQUENCY.



(A)

FIG. 4.9 ZERO CROSSING DETECTOR.
(USING SIMPLE VOLTAGE COMPARATOR).



(B)

FIG. 4.9 INPUT-OUTPUT WAVEFORMS OF ZCD.

n_0	S_n	R_n	Q_{n+1}
1	0	0	Q_n
2	1	0	1
3	0	1	0
4	1	1	UNDEFINED

TABLE . 2 TRUTH TABLE OF R.S. FLIP FLOP.

done with a simple R-C circuit (integrator).

In fig. 4.8 is shown the actual VCO output with continuously varying frequency and all the other corresponding waveforms. The output of the test network is assumed to have an arbitrarily varying phase with respect to the VCO output, i.e., the input to the network.

4.3 ZERO - CROSS DETECTOR

Each time the input signal V_{in} crosses the zero value, the output changes state. When V_{in} is positive, the output is positive and vice-versa. This function is achieved using a simple voltage comparator as shown in fig 4.9. The function of a comparator is to compare the time varying voltage at one input with a fixed reference voltage on the other input (zero volts in this case).

The output of the comparator is given by

$$V_{out} = A \times (V_2 - V_3) = A \times V_{in} \quad (\text{Because } V_3=0)$$

where A is the gain of the comparator.

When V_{in} positive, the comparator goes to 1 state, i.e., the positive saturation level of the comparator. When V_{in} is negative, the output of the comparator goes into negative saturation, i.e., the zero state.

CHAPTER 5
CIRCUIT DESIGN

5.1 LM 339 (DUAL IN LINE AND FLAT PACKAGE)

The LM 339 is a quad voltage comparator. i.e., there are four voltage comparators. The chip layout and pin function diagram are shown in appendix 3.

The phase response circuit requires two comparators one to detect zero crossing of the VCO output and the other to detect zero crossing of the output from the test circuit. The LM 339 was chosen because of its low cost and fast response time (1.3 u sec.) which makes it suitable for high frequency operations. The important features of LM 339 are listed in appendix 4.

The comparators are designed as a high gain difference input single ended output amplifier. The input impedance, voltage gain and output voltage are somewhat lower compared to an Opamp. The comparator does not reproduce any part of the original input waveform but operates a non-linear device in the open loop mode.

The circuit connections of the LM 339 are shown in fig. 5.1. The chip is operated from a dual supply of 10V. This voltage was chosen to obtain a square

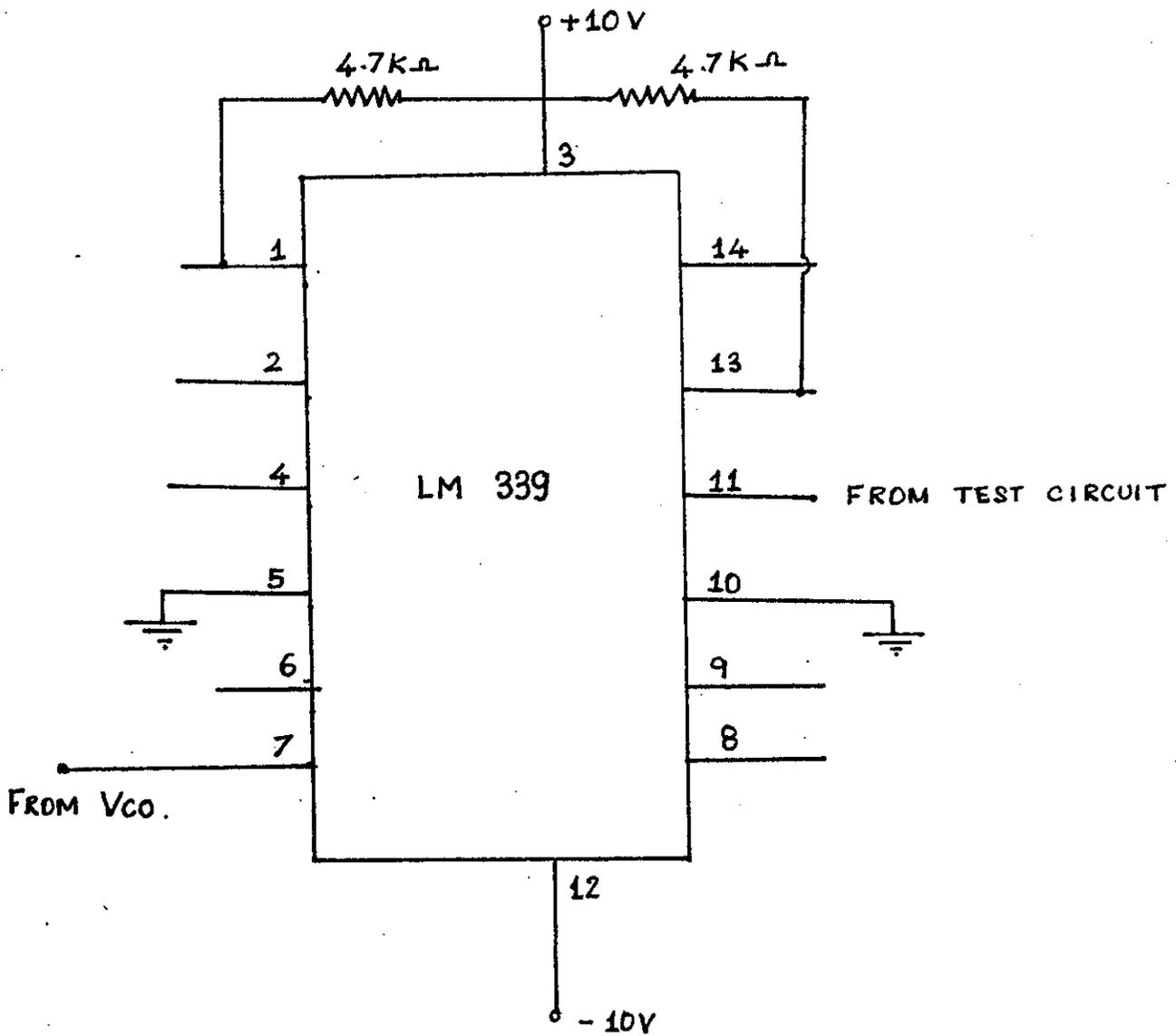


FIG. 5.1 CIRCUIT CONNECTIONS OF LM 339.

wave of 10V amplitude. The pulse to be obtained from this square wave must have a voltage (maximum) of $\frac{2}{3} \times V$ supply where V supply is the supply voltage of the bistable multivibrator (10 V).

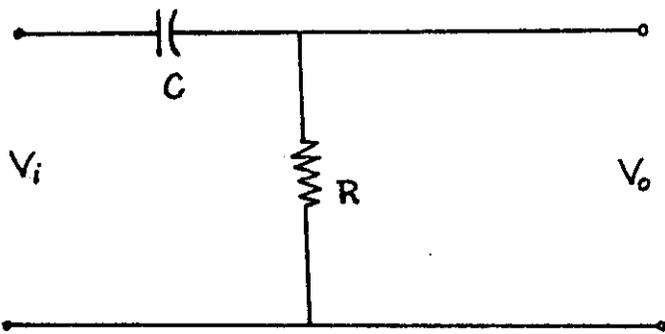
The outputs of the comparators which are used (2 and 4) are connected through a pull-up resistor to positive supply. The design value specified for LM 339 is 4.7 ohms. The pull-up resistor is used to pull the output quickly to positive saturation from negative saturation. The value of the resistor used must not be very small since it will draw larger current from the supply and it should also not be very large since it has to drive the circuits connected to the output.

5.2 DIFFERENTIATOR

This is a simple C-R high pass filter network (see fig. 5.2). The differentiator is used to get a pulse at the zero crossings of the input square signal from the LM 339.

The output of this circuit will appear as shown in fig. 5.3. The waveform is that of a capacitor discharging. The working of the differentiator can also be explained as follows :

When the step voltage is first applied, the



$C = 0.001 \mu F$
 $R = 10 k\Omega$

FIG.5.2 DIFFERENTIATOR .

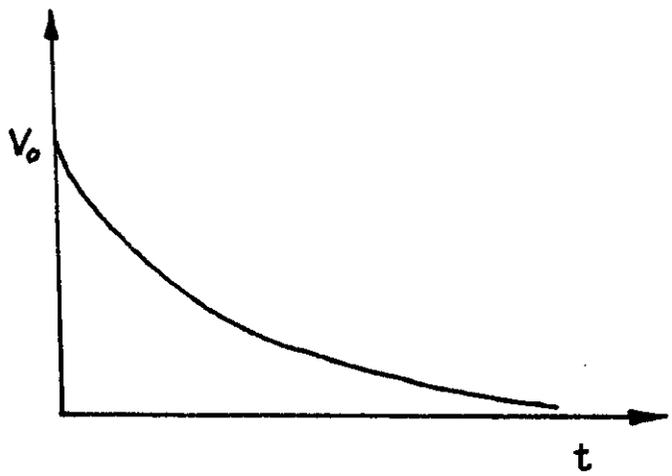
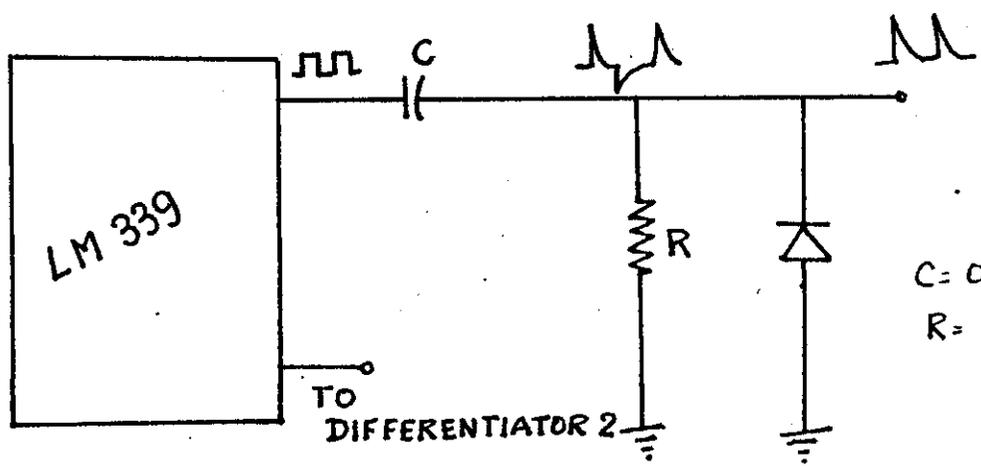


FIG.5.3 DISCHARGING OF C .



$C = 0.001 \mu F$
 $R = 10 k\Omega$

FIG 5.4 USE OF DIODE TO REMOVE NEGATIVE PULSES.

capacitor acts as a short circuit and hence all the input voltage appears across the resistor R. Then the capacitor gradually starts charging up to 10 V and hence the voltage across R decreases.

5.3 DESIGN OF R AND C

The differentiator must have a small time constant to get a narrow pulse width. This time constant must be less than or equal that of the time period of the largest frequency signal at the input. The largest frequency for which the EGDU is designed is 100 KHz. Therefore the smallest time period in the input signal is $1 / (10^2 \times 10^3) = 10^{-5}$ secs.

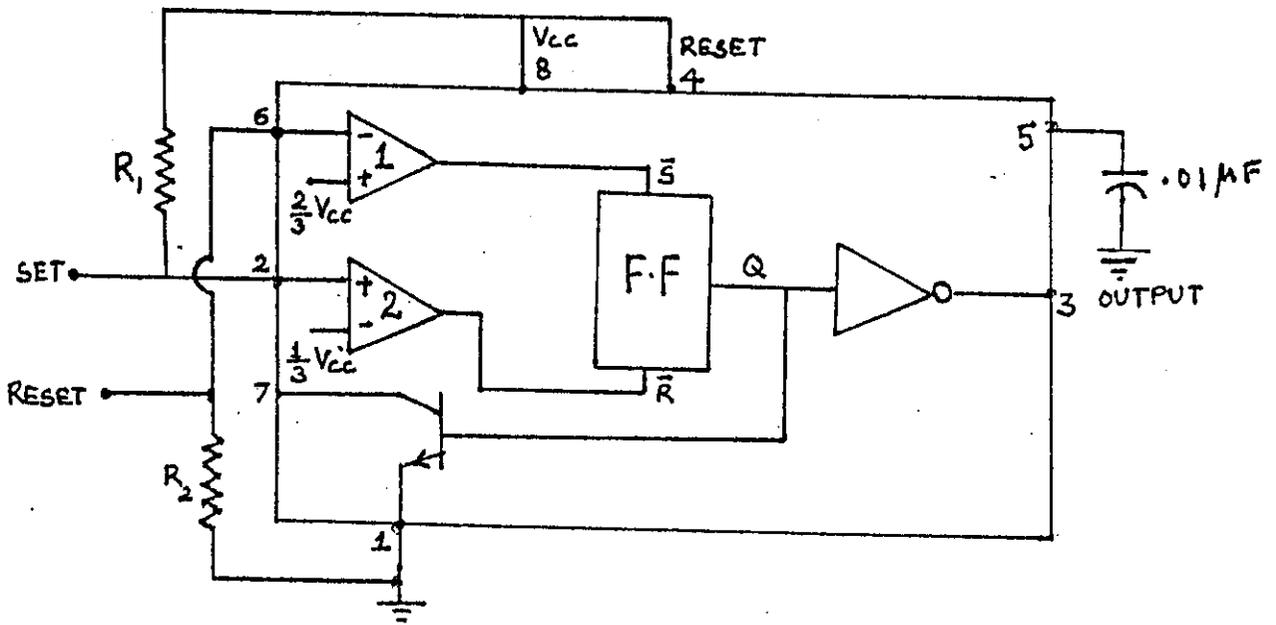
$$c = \text{Time constant} = 10^{-5} \text{ sec (Assume)}$$

$$\text{Let } R = 10 \text{ K ohms}$$

$$\therefore C = \frac{10^{-5}}{10 \times 10^3} = 10^{-9} \text{ Farads} \\ = 1000 \text{ pf}$$

The same values of R and C can be used for both the differentiators.

The sign of the pulse depends on the LM 339 output. The polarity of the pulse is same as that of the input. A diode can be connected after the zero crossing detector to remove pulses of one polarity. Consider a diode connected as shown in Fig.5.4.



- 1 - EARTH
- 2 - TRIGGER
- 6 - THRESHOLD

FIG. 5.5 555 BISTABLE MULTIVIBRATOR.

5.4 555 AS BISTABLE MULTIVIBRATOR

The 555 is used here to convert the time period between the pulses from the VCO and test network to a square wave which can be averaged to give a phase plot. The circuit diagram for use of 555 as bistable is given in fig 5.5 . The reset terminal (pin 4) is connected to V_{cc} so that the input to the base of the transistor T2 is permanently high. This turn off T1 since the control terminal is also not used, it is by passed to ground by a small filter capacitor , usually 0.01 μ F.

This is to avoid stray pick up at pin 5. The set input should be greater than $V_{cc}/3$ in magnitude and the reset pulse should be greater than $2V_{cc}/3$ in magnitude. The value of V_{cc} used here is +10V. This is to operate the 555 at the same voltage as that of the 8038 waveform generator chip and hence avoid need for another supply. Since the LM 339 quad voltage comparator is also operated at 10V the value of the pulse voltage is greater than $2/3V_{cc}$.

The working can be explained by referring to the waveforms of fig 5.6.

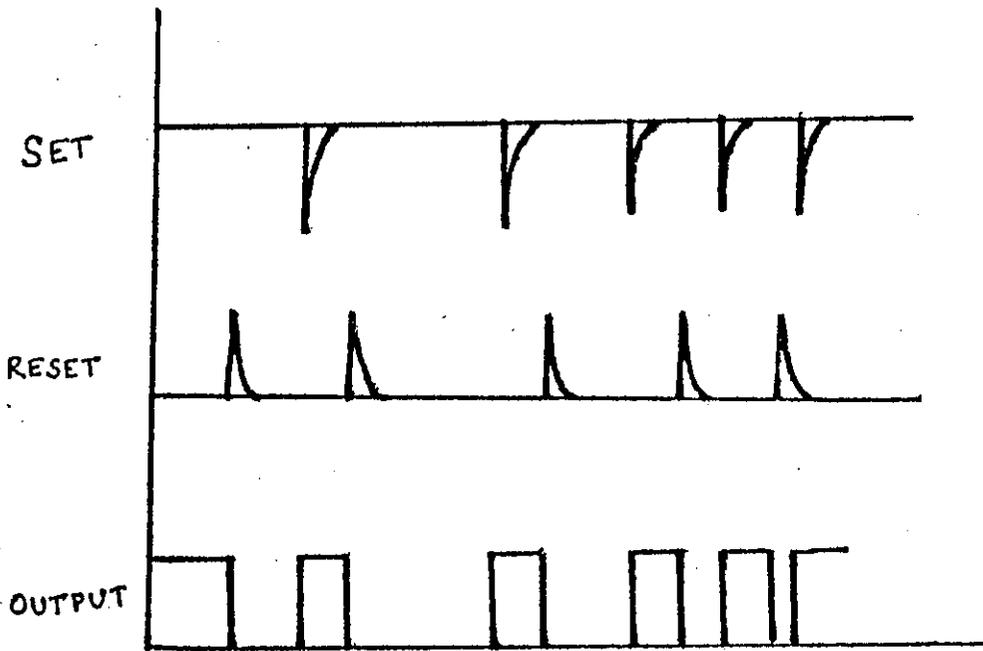


FIG 5.6 INPUT AND OUTPUT WAVEFORMS
OF 555.

When set input is given to the positive input of comparator 2, the difference of the input voltages of C2 will be negative and hence output will be negative. This is because the output voltage V_o is proportional to the difference of V_2 and V_1 where V_2 is the input to the positive terminal of the comparator, V_1 is the input to the inverting terminal of the comparator. The negative output of C2 resets the flip-flop making as zero, is the output of the flip-flop. However due to the inverter, the output at pin 3 is positive. This is the first stable state of the bistable multivibrator.

When the reset signal which is greater than $\frac{2}{3} V_{cc}$ is given to the inverting terminal of C1, the difference of the two input voltage is negative, and hence C1 output is negative. This sets the flip-flop and hence output is one. Due to inverting buffer, output at pin 3 is zero. This is the second stage of the bistable multivibrator.

As shown in overall circuit diagram the input to the trigger terminal is given through a coupling capacitor. As shown in fig, the voltage at the junction of R1 & R2 is 5V since R1 & R2 are equal and R1 is connected to the +10 V supply. So the effective pulse voltage to pin 2 is the difference of the pulse voltage and 5V .

This arrangement prevents spurious signals from setting the flip-flop.

CHAPTER 6

PROCEDURE TO USE THE KIT

6.1 HOW TO USE THE ELECTRONIC GRAPHIC DISPLAY UNIT:

In this chapter a simple procedure of how to use EGDU is given. With this a person who is not familiar with the internal circuitry can also use the EGDU. A few precautions are given to enable correct working of the circuit without damage to any of the components.

6.2 REQUIREMENTS:

10 V Dual Supply (100 mA)
15 V Dual Supply (100 mA)
CRO with sweep out facility.

6.3 PRECAUTIONS:

(a) Do not overload the VCO output. The minimum input impedance must be limited to 1 K.

(b) Set supply current limit to minimum.

(c) Once the supply voltages are set, do not touch the voltage adjust terminal. Any small changes in supply voltage will cause drastic changes in frequency of output.

(d) See that all ground terminals have a continuity (inclusive of CRO, EGDU, Supply and Test

network grounds).

6.4 AVERAGER:

This is a simple R.C. circuit as shown in fig 6.1. The Voltage Waveform across the capacitor will appear as shown in Fig. 6.2.

6.5 DESIGN:

This time constant of the averager should be greater than the largest time constant of the input signal to the integrator. It should not be very large since the flyback time of the CRO sweep is negligible and capacitor charging or discharging waveform will be seen to the left of the CRO screen while displaying the phase plot.

Largest time period of the input signal $1/100 = 0.1$ sec. Let time constant of integrator be 0.1 sec. Let $R = 1M\Omega$.

Therefore, $C = 0.1/10^6 = 0.1 \mu F$.

In this chapter we have seen how all the components required for the phase response display are designed. In the next chapter, the printed circuit board layout and instruction on how to use the Electronic Graphic display unit are described.

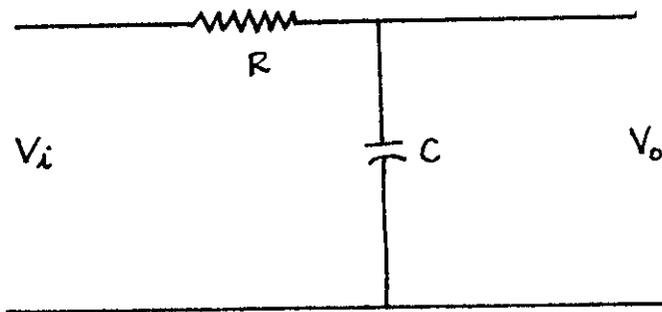


FIG. 6.1 AVERAGER.

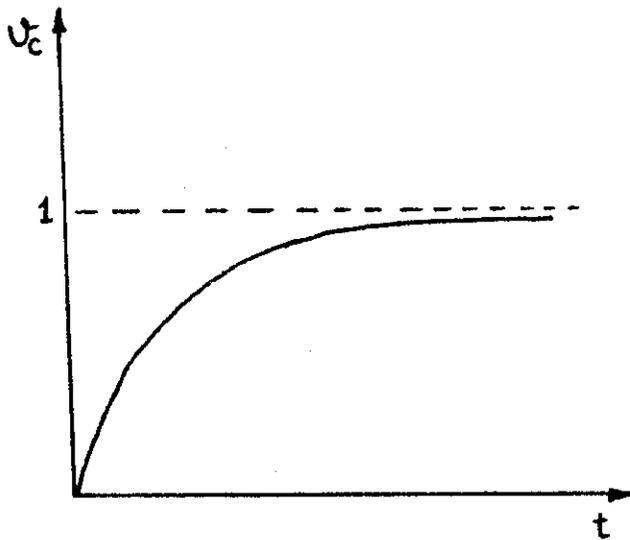


FIG. 6.2 CAPACITOR WAVEFORM.



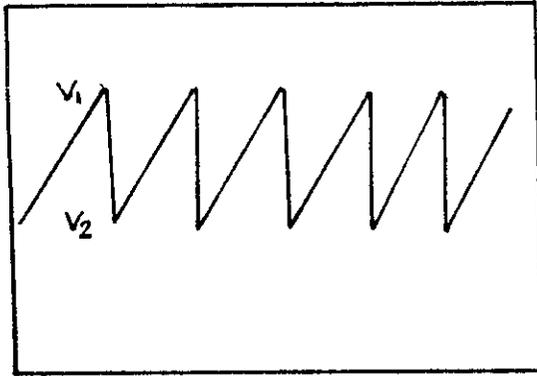
6.6 PROCEDURE:

(i) Connect the CRO sweep output to the input channel of the same CRO and change the INT/EXT button to EXT position. Note the magnitude of sweep (see fig 6.3) and then disconnect sweep out.

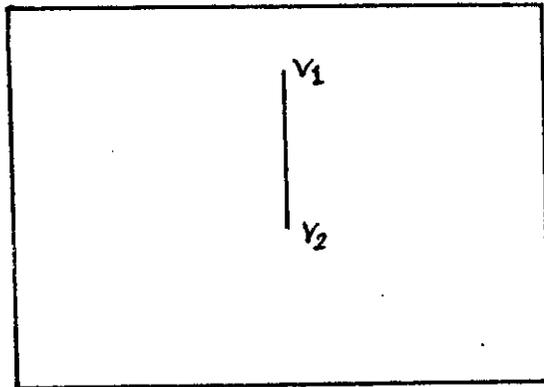
(ii) Connect the supplies and ground of the circuit switch on the supplies and check if the corresponding LEDs glow (Red LED for 15v supply and yellow LED for 10v supply).

(iii) Connect the sweep output of the CRO to other SWEEP IN terminal of the EGDU. Set CRO on DC see fig.6.4. Check the voltage output at sweep out of the EGDU circuit. Adjust presets 1 and 2 in order to get a sweepout voltage of 10 v to 5.33 v from the EGDU. (Preset 1 controls sweep magnitude while Preset 2 controls sweep position. See figs. 6.5 and 6.6.

(iv) Check the VCO Out terminal of the EGDU. The output must appear as shown in fig.6.7. If the frequencies at the extreme ends of the CRO screen are not as indicated in table 1, adjust the presets (make only very fine adjustments). Make sure the proper frequency range has been attained for all three switch positions.



CRO
ON
INT
MODE.



CRO
ON
EXT
MODE.

FIG. 6.3 CRO SWEEP WAVEFORM.

(v) Connect the VCO OUT to the input of test network. Connect the output of the test network to the SINE IN of the EGDU circuit. If variable magnitude is desired use VAR terminal and adjust the potentiometer.

(vi) Observe the amplitude response at the output of the twoport network. (Note that here the output will be swinging on both sides of the zero axis. If a single sided output is desired, use a small signal diode at the output). The phase response can be seen at the PHASE OUT terminal of the EGDU at CRO time setting greater than 50ms/div. The phase response may give a very slow movement of a dot across the screen and a low amplitude. Adjustments can be made for the same.

6.7 TROUBLE SHOOTING:

(i) If the LEDs do not glow, check up the corresponding fuses.

(ii) If the SINE OUT does not produce any wave but only a shift, check the SWEEP OUT for proper voltage magnitudes. If the 8038 is on the chip holder, then with the 15 v supply on and the 10 V supply OFF, the +10 v voltmeter must show about 3-4 V

(iii) Most distortions are caused by improper grounding. So check all ground terminals.

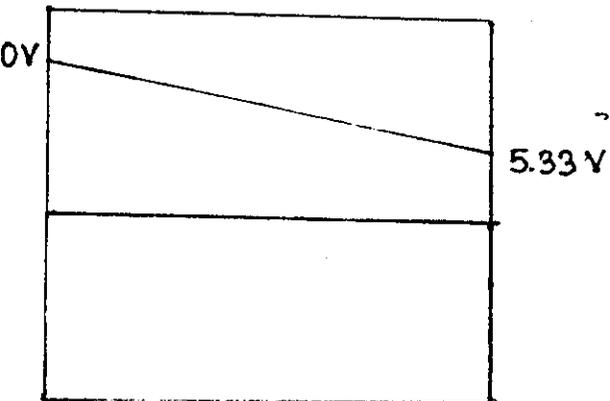


Fig. 6.4 CRO SCREEN SHOWING OPTIMUM SWEEP VOLTAGE.

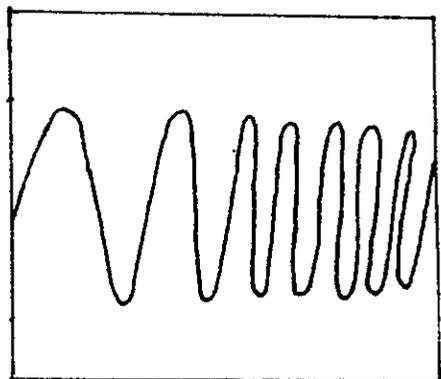


Fig. 6.7 SHOWING NORMAL VCO OUTPUT.

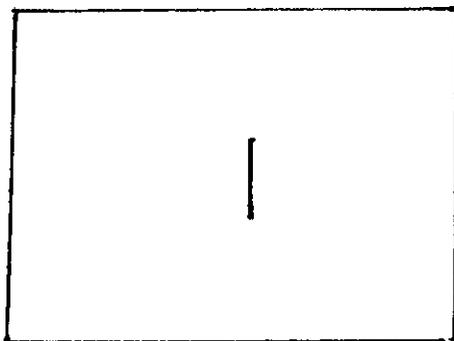
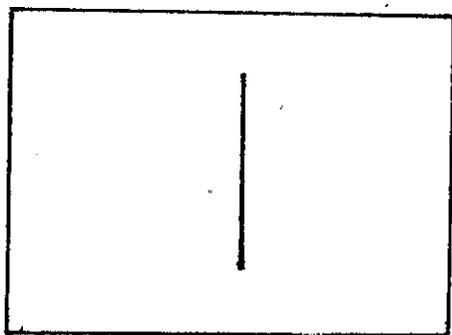


Fig. 6.5 ADJUSTMENT OF SWEEP MAGNITUDE USING P_1 (CRO ON EXT. MODE)

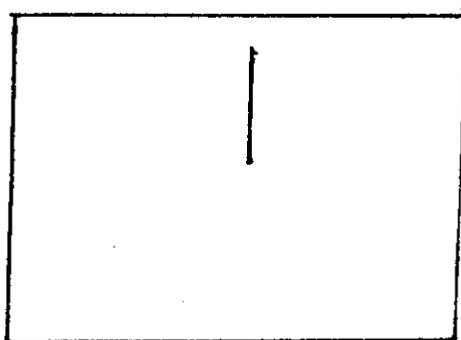
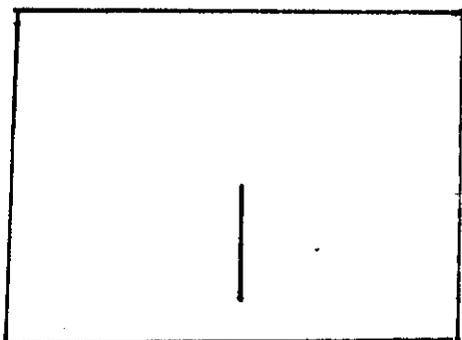


Fig. 6.6 ADJUSTMENT OF SWEEP POSITION USING P_2 . (CRO ON EXT. MODE)

(iv) If the SINE OUT works and the SINE IN has proper waveform but the phase plot does not appear, check for negative spikes at pin 2 and positive spikes at pin6.

(v) For the testing of the 8038 chip, a test circuit has been provided, probe square, triangular and sinewave terminals.

Appendix 7 gives the computer program to obtain theoretical amplitude and phase plots.

CHAPTER 7
RESULT ANALYSIS

The results that were obtained conform to those obtained theoretically. The waveforms in the CRO were photographed and they are attached here for ready reference graphs are also attached as they provide accurate reproduction of the results.

Cross checking were made by simulating the actual tests using the computers. The complete program is given in Appendix I.

1. Passive single stage low pass filter cutoff frequency 482.28 Hz

Transfer function

$$\frac{E_o}{E_i} (s) = \frac{1}{1 + 3.3 \times 10^4 (-4)s}$$

2. Passive single stage high pass filter cutoff frequency 4.822 KHz.

Transfer function

$$\frac{E_o}{E_i} (s) = \frac{3.3 \times 10^4 (-5)s}{1 + 3.3 \times 10^4 (-5)s}$$

3. Active resonant bandpass filter cutoff frequency 5 KHz.

Gain $A_o = 50$ (34 db), Q

Transfer Function

$$\frac{E_o}{E_i} (s) = \frac{-2 \times 10^8 s}{s^2 + 4255.3s + 9.88 \times 10^{10}}$$

4. Active Twin T band reject (notch) filter Notch frequency 15.392 KHz.

A quick glance at the experimental results and theoretical responses by computer software would show that the correlation is very close.

As a final note it can be said that the planned objective of fabricating the circuit of the EGDU was achieved. The performance of the device was very good and reasonable methods of overcoming the limitations of the circuit are suggested in the next chapter.

CHAPTER 8

CONCLUSION

The chapters so far have discussed in detail the design principles of the amplitude and phase response circuits, their construction and operations. The working procedure with the EGDU has been outlined and hints and kinks have been discussed. In the previous chapter, the test results, summing up, the limitations and scope for improvement were discussed.

The highlights of this kit can be given as follows:

The EGDU is a compact device, operating with a minimum of external requirements (supplies and CRO), which is capable of giving a vast amount of knowledge about any two port network through the two responses. The design principles are simple and the net cost is extremely low (Rs. 750/-) making it easy to fabricate and commercially viable. It offers several special features that are :

1. Wide frequency range (100 Hz to 100 KHz).
2. Seperate amplitude and phase outputs.
3. Variable amplitude VCO outputs.
4. Good FM linearity (0.5 %).
5. Low total Harmonic Distortion (2.0 %).
6. Compatible with any modern CRO.

Despite the above positive features the circuit is not without its limitations and offers ample scope for improvements and refinements. The basic points in this respect could once again be listed as below :

1. Frequency variations with supply voltage. As was seen in Chapter 2, the VCO frequency is a very sensitive function of the supply voltage, which must remain absolutely fixed.

2. Two dual supplies are needed. A single on board regulated DC supply using 10V and 15V IC could solve this problem.

3. Erroneous operation at angles nearing 180 degrees. This is due to the racing conditions in the bistable due to overlapping of set and reset pulses as explained in chapter 3.

4. Ripple in phase plot - caused due to the inadequacy of the averager. It could be resolved by use of better active averaging circuits such as high speed low pass active filters.

We shall now proceed to see the circuits tested. For brevity sake only four circuits were explained and plots shown.

REFERENCES

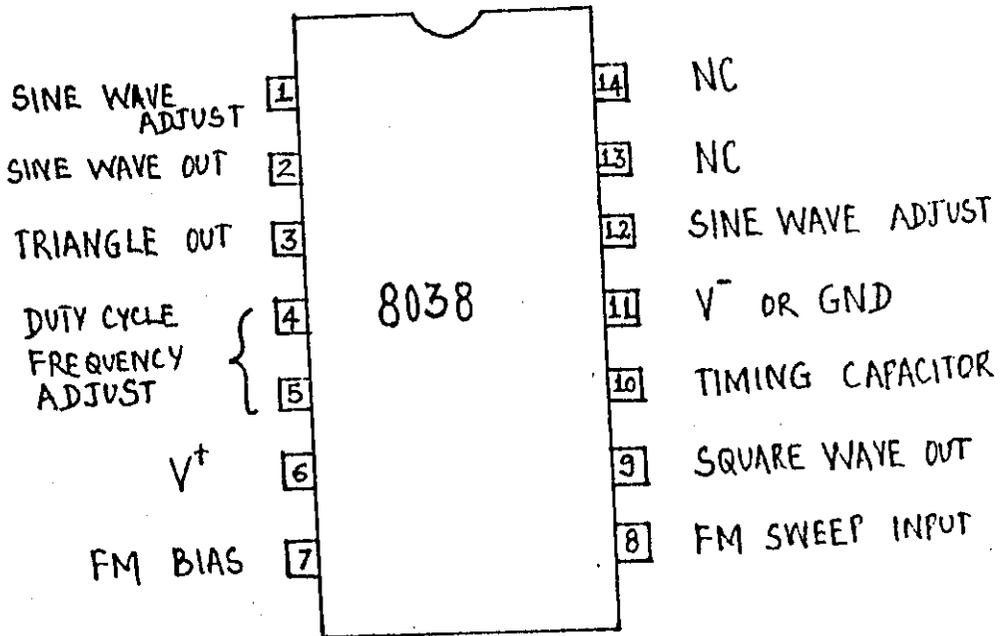
1. Millman and Halkias, Integrated Electronics, McGraw Hill, 1971.
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3. S M Usmani, IEEE Transactions on Education, Vol. E-26, No. 1, PP 40-43, Feb 1983.
4. K R Botkar, Integrated Circuits, Khanna Publishers, 1985.
5. Wai-Kai Chen, Passive and Active Filters, John Wiley and Sons, 1986.
6. Arpa D Barna and Dan I Porat, Operational Amplifiers, John Wiley and Sons, 1987.
7. ICL 8038 Data Sheet.
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APPENDIX 1

8038 CHIP SPECIFICATIONS

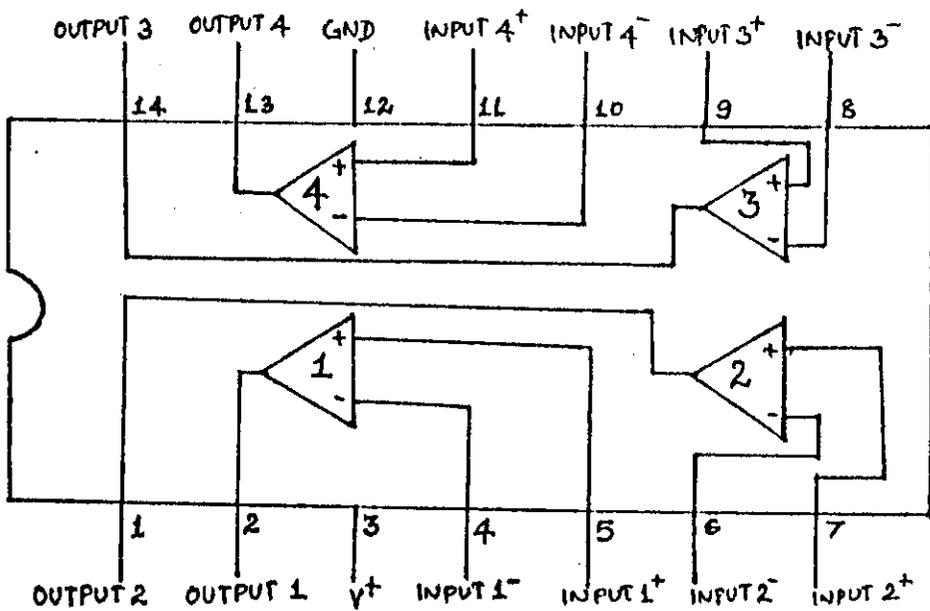
Power Dissipation	:	750Nw
Dual Supply	:	+/-10 v
Supply Current	:	37.5 mA
Rise Time	:	180 ns
Fall Time	:	40 ns
Sine wave amplitude	:	0.2 Vsupply
Total harmonic distortion (THD)	:	2%

APPENDIX 2



APPENDIX 3

LM 339 QUAD COMPARATOR TOP VIEW



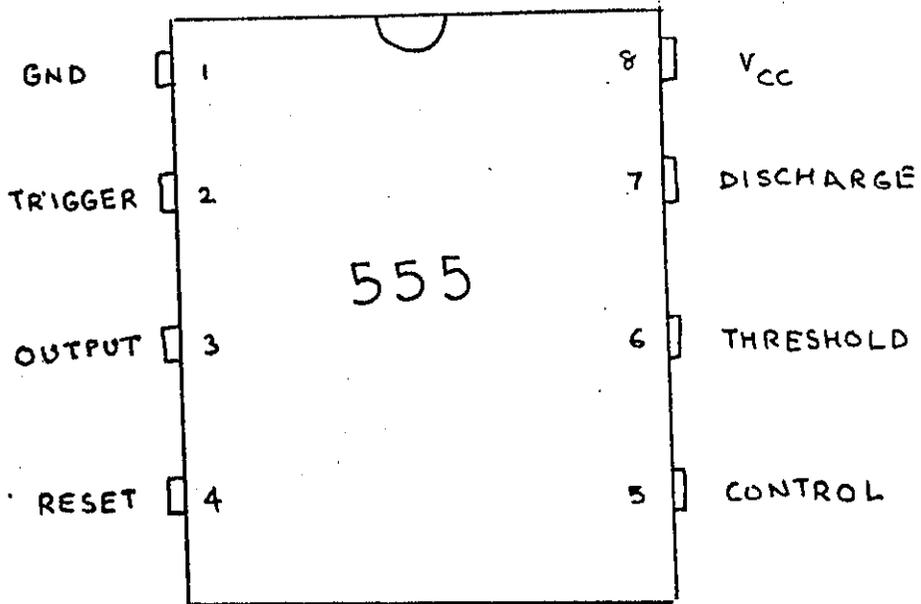
APPENDIX 4

ABSOLUTE MAXIMUM RATINGS OF LM 339

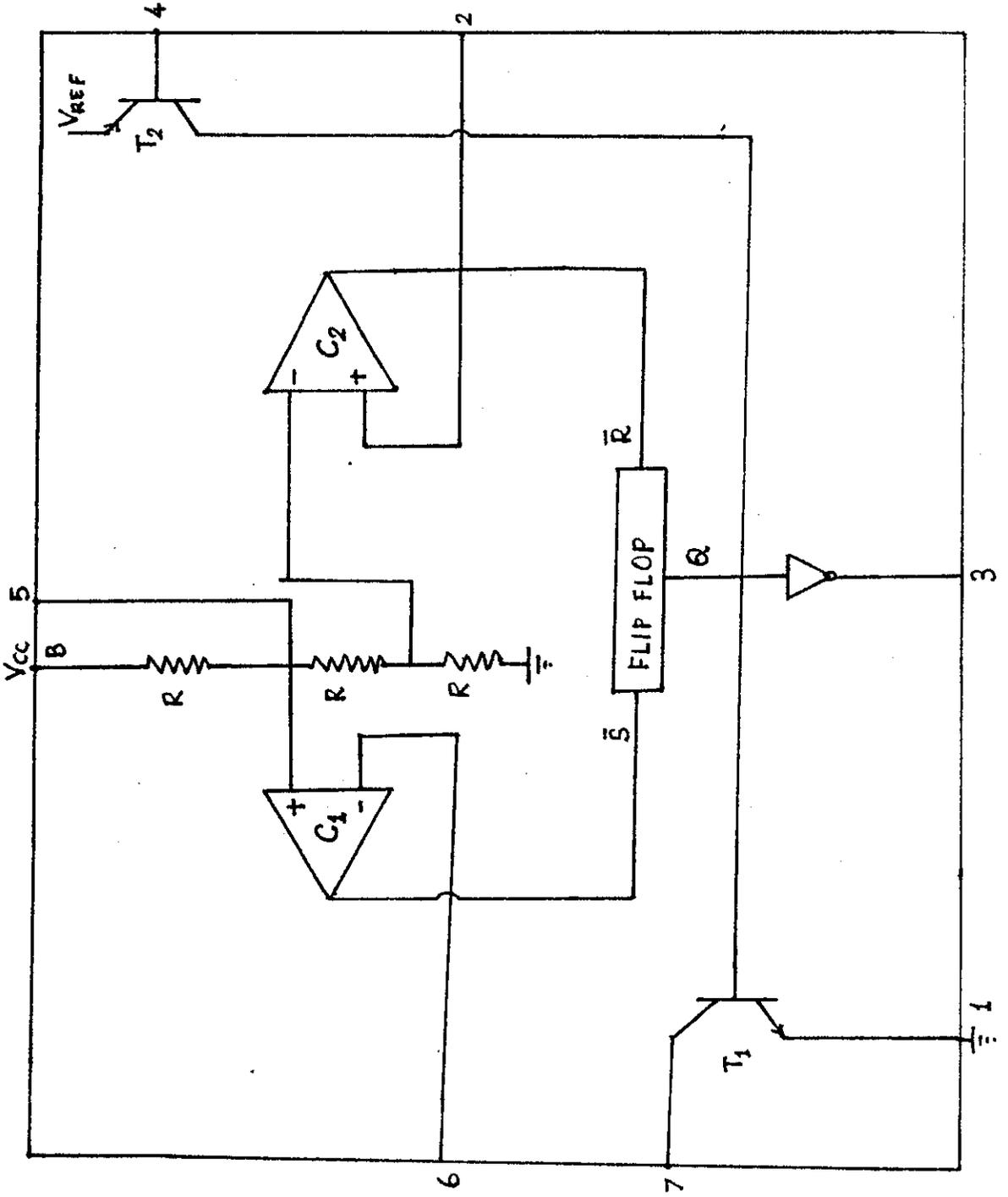
Supply Voltage V+	:	36V DC or +/-18V DC
Differential input voltage	:	36V DC
Input voltage	:	0.3V DC to 36V DC
Input offset Current	:	+/- 50 nA DC
Input offset Voltage (at Ta = 25 deg C)	:	+/- 5.0 mV DC
Input bias Current (at Ta = 25 deg C)	:	250 nA DC
Input Common mode voltage range	:	V+ - 1.5V DC
Supply current (RL= , Ta = 25 deg C)	:	2 mA DC
Voltage gain	:	200 V/mV
Large signal response time (RL = 5.1 K)	:	300 ns
Output sink current	:	16 mA DC
Saturation Voltage	:	400 mV DC

APPENDIX 5

PIN CONFIGURATION OF THE 555 TIMER



- 1 - GND
- 2 - TRIGGER
- 3 - OUTPUT
- 4 - RESET
- 5 - CONTROL
- 6 - THRESHOLD
- 7 - DISCHARGE
- 8 - V_{CC}



PIN CONFIGURATION OF 555.

APPENDIX 6

555 CHIP SPECIFICATION

Supply voltage	:	4.5 to 18 v
Supply Current	:	3 mA (for $V_{cc}=5v, R_L = \infty$)
	:	10 mA (for $V_{cc}=15v, R_L=\infty$)
Trigger current	:	0.5 uA
Reset voltage	:	0.7 v
Reset current	:	0.1 mA
Rise and fall time of output	:	100 ns

```

140     FORMAT (10X, '** ACTIVE CIRCUIT **@/, 10X,
'NUMBER OF STAGES..@, 18, /110X, 'ORDER.., 16, //)
145     XA1 = XA / (2.0 * 3.14159)
146     XB1 = XB / (2.0 * 3.14159)
147     PRINT 150, XA1, XB1
150     FORMAT (10X, 'FREQUENCY RANGE ...@, F10.2, 'HZ
TO @ , F10.2, 'FZ@, //)
155     GO TO (160, 175), NTYP
160     PRINT 165
165     FORMAT(//, 120('-@), ///, 40X, 'AMPLITUDE
RESPONSE@, /, 40X, 18('-@')
170     GO TO 180
175     PRINT 176
176     FORMAT (//, 120('-@), ///, 40X, 'PHASE
RESPONSE@, /, 40X, 14('-@)
180     CONTINUE
C
C
C     PROGRAM FOR GRAPH PLOTTING BEGINS NOW
C
C
190     N=(XB-XA)/H+1
236     IF((BTYP.EQ.2).AND.(YMIN.LT.0.0)) GOTO 238
237     GOTO 243
238     YMINI=YMIN
239     YMIN=YMIN+3.14159
240     YMAX=YMAX+3.14159
241     PRINT 242
242     FORMAT (//, 5X, 'LAG CIRCUIT @, //)
C
C
C
243     Y4=(YMAX-YMIN)/4.0
245     Y14=YMIN+(1.0*Y4)
250     Y12=YMIN+(2.0*Y4)
255     Y34=YMIN+(3.0*Y4)
260     PRINT 265, YMIN, Y14, Y12, Y34, YMAX
265     FORMAT(////, T24, F6.2, T44, F6.2, T64, F6.2, T84,
F6.2, T104, F6.2)
270     PRINT 275
275     FORMAT (T27, 'I@, T47, 'I@, T67, 'I@, T87, 'I@,
T107, 'I@)
280     PRINT
285     FORMAT (' ', T27, 81('-'))
290     PRINT 295
295     FORMAT ('&@, 5X, 'Z%HZ @, 5X, 'Y@, ', 5X, 7('-@),
5X, '-@, T27, 'I@)

```

```

C
C
C   INTERVAL FOR DEPENDENT VARIABLE IS
C   CALCULATED
C   SEPARATE SUBROUTINES FOR AMPLITUDE AND PHASE
C   PLOTS ARE CALLED
C
C
310  YDEL=NPRINT/(YMAX-YMIN)
315  X=XA
320  GO TO (325,335),NTYP
325  CALL AMP (X,YMIN,YMINI,YDEL,STAR,XLINE,
        NPRINT,N,BLANK,H)
340  PRINT 345
345  FORMAT (1H2)
350  PRINT 355
355  FORMAT (5X,'***END OF PROGRAM**@)
360  PRINT 365
365  FORMAT (1X,120('-@))
370  PRINT
375  FORMAT(//,5X,'SHANKAR@,/, 'KALAI@/,5X,'SAKTHI@,
        ///,5X,'PROJECT-EGDU@,/)
380  STOP
385  END

```