SECRECY IN PARALLEL TELEPHONES

PROJECT REPORT P-1312

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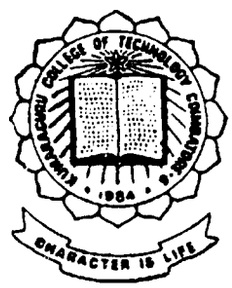
Submitted in partial fulfilment of the requirements
for the award of the Degree of

Bachelor of Engineering

in ***Electronics and Communication Engineering*** *of the*
Bharathiar University, *Coimbatore.*



Department of Electronics and Communication Engineering

Kumaraguru College of Technology

Coimbatore - 641 006

1995-96.

Kumaraguru College of Technology

Coimbatore -641 006.

Department of Electronics and Communication Engineering

Certificate

This is to Certify that the Report entitled

"SECRECY IN PARALLEL TELEPHONES"

has been submitted by

Ms .....

in partial fulfilment of the requirements for the award of Degree of Bachelor of Engineering in the Electronics and Communication Engineering Branch of the Bharathiar University, Coimbatore – 641 006 during the academic year 1995 -'96.

(Guide)

(Head of Department)

Certified that the Candidate was Examined by us in the Project Work Viva-Voce Examination held on _____ *and the University Register Number is* _____

(Internal Examiner)

(External Examiner)

TATAFONE

1.4.96

TO WHOMSOEVER IT MAY CONCERN

This is to certify that the following students of Kumaraguru college of Technology, Chinnavedampatty, Coimbatore - 6, have successfully completed the project titled "Secrecy in Parallel Telephones" at our factory, as a part of their curriculam for their B.E. Degree in Electronics and Communication Engineering.

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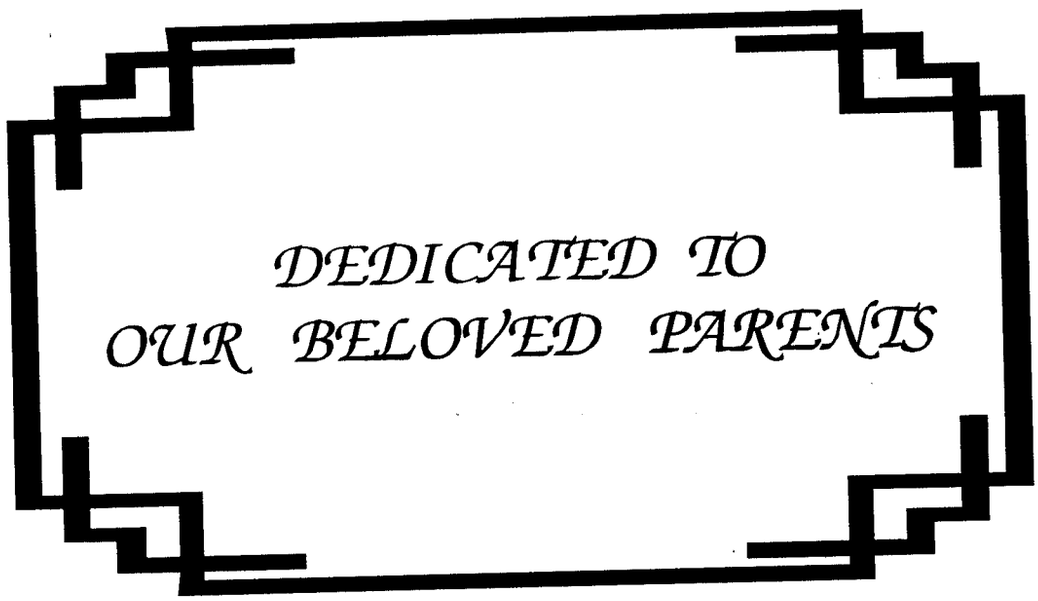
DEDICATED TO
OUR BELOVED PARENTS

ACKNOWLEDGEMENT

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"Ungrateful" will be the word if we do not thank all the faculty members and our friends for being there when we needed them most.

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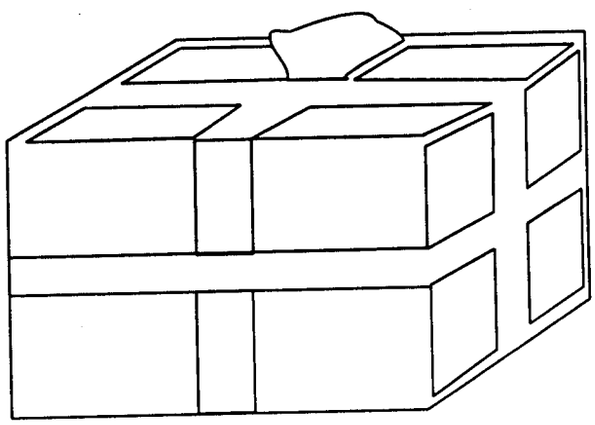
SYNOPSIS

SYNOPSIS

Our system presented in this project allows upto 4 telephone sets to be connected at its output. The exchange line is given as the input to our system. The facility provided by our system is the most desired feature in parallel telephones - "SECRECY". The added advantage of this system is its circuit flexibility.

A slight modification allows up to any number of telephone sets to be connected . The system works for both tone and pulse dialling. Since this system uses only discrete components, it is relatively easy to add or change certain features. Since the use of microprocessor / microcontroller is avoided the cost is drastically reduced.

Our project comprises of some extra features such as call transfer which only adds on to the existing advantage. The circuit is completely designed, fabricated and tested.



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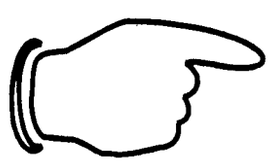


INTRODUCTION

CHAPTER-1

INTRODUCTION

Speech is the most natural means of human expressions and that explains why telephones have become an indispensable part in our day to day life.

Advancements in telecommunication is at its zenith with the prospect of a slew of wireless communication, mobile satellite systems etc. It only goes on to prove that there are still many areas in telecommunication left open to the reseacher and even slight modifications performed on existing system would result in a customer endurable product. One such is providing the most desired feature to an array of parallelly connected telephones (i.e,)'SECRECY'.

Especially in a busy environment, as it exists in every other industry, educational institutions and household, today parallel telephones are a common affair. Providing secrecy in this case will undoubtedly be an added asset.

For any commercial entity cost is the major factor that determines its success and that is why our project aims at providing a cost effective system too.

With the drastic changes taking place in the field of telecommunication, we have contributed our mite to the ever changing facets of technology. Our project " SECRECY for Parellel Telephones"

TELEPHONE
IT'S BASICS

CHAPTER-2

TELEPHONE - IT'S BASICS

The availability of rapid and reliable means of communication is now vital to the conduct of human affairs and of utmost importance in the day-to-day activities of government, commerce and industry. The scientific discoveries concerning electricity and electromagnetism in the early 19th century led to the invention of some communication systems such as the telegraph and forty years later to the telephone. This was because with the limited technical resources of the time it was not readily possible to form any true assessment of the problem involved : to cause the minute forces produced by the vibrations of air in the neighbourhood of a source of sound to actuate an electrical device in such a way as to produce usable electric signals, and then to cause these electric signals to reproduce similar vibrations of the air at some distant point. This was the basic principle behind the working of a telephone.

Understanding Telephony :-

Telephony deals with the transmission of speech at a distance. In line telephony, information is sent in the form of electric current through the medium of line conductors between them. When any subscriber speaks into the transmitter of his telephone set, his speech is converted into oscillatory electrical current and this current is sent through the lines to the receiving end of the called subscriber. Two seperate line conductors are necessary for transmission of telephone signals for every subscriber and hence there are as many pairs of line conductors as the total number of subscribers. All these line conductors from different subscribers premesis are connected at the telephone exchange.

Telephone Exchanges :-

All the early telephone exchanges were operated on a manual basis, the connection between subscribers being completed by an operator. In course of time reliable automatic switching systems were developed and automatic exchanges were installed. Because of the greater costs of installing and maintaining automatic exchanges as compared with manual equipment the use of automatic switching is economically justified only if counterbalancing savings can be achieved by reduction in operating costs and

in the more efficient use of line plant. The functions of operators are performed by switching or selector stages. There are principally two types of automatic exchanges operating in various parts of the world. They are:-

1. Cross bar system.

2. Step by step strowger system.

A type of exchange known as electronic exchange is the latest and it utilizes transistors and other solid state devices and will soon replace the existing electromechanical system.

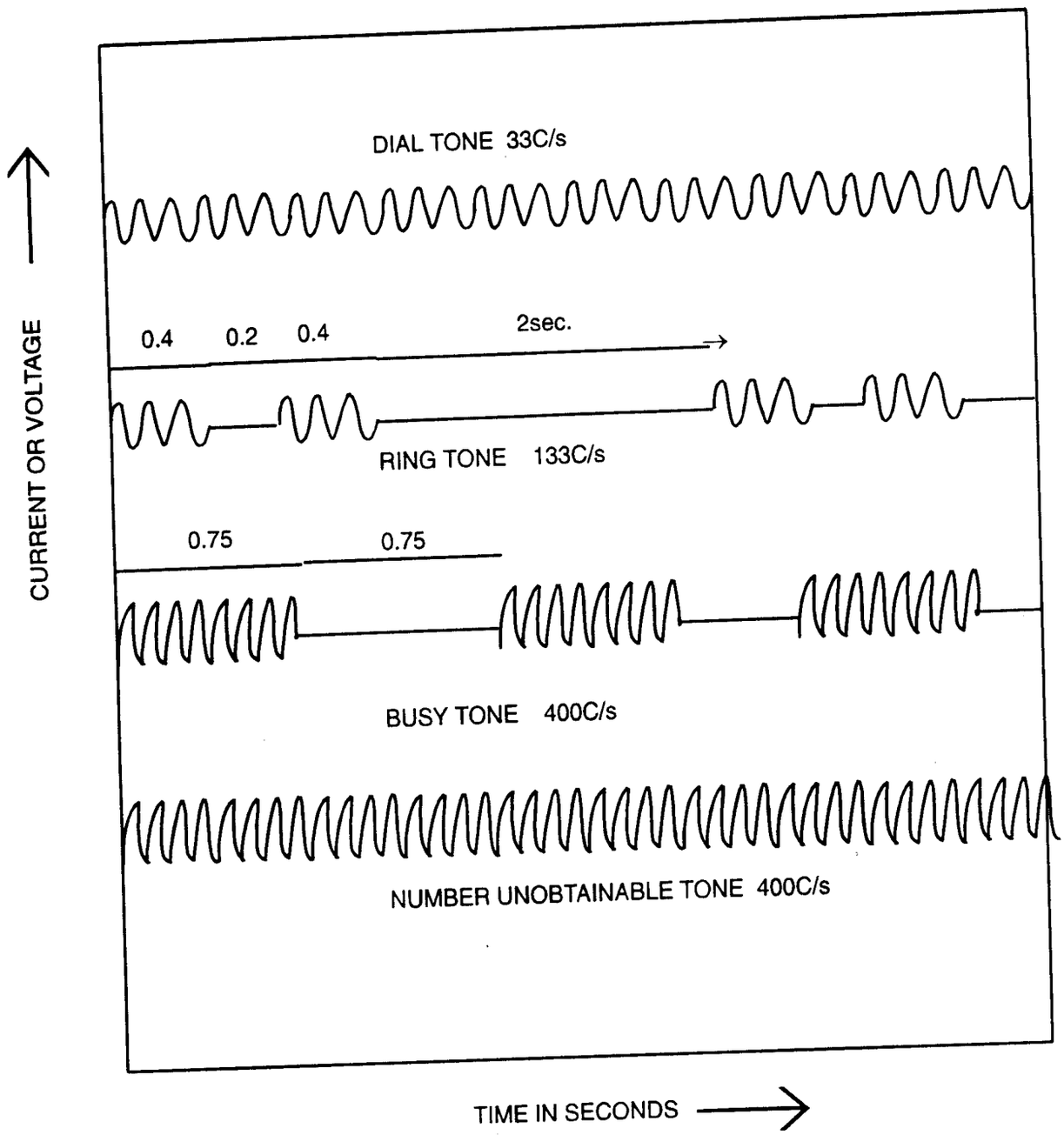
Tones used in automatic exchange:-

A) DIAL TONE:-

This tone is returned to the calling subscriber from the first group selector and indicates that the exchange is ready to accept dialling from the subscribers. The dial tone is sent by the exchange as soon as the subscriber lifts his handset. The dial tone stops as soon as the first digit is dialled. It is a continuous tone of 33c/s.

(B). RING TONE :-

This tone is returned to the calling subscriber from the final selector when the bell of the called party's bell is ringing. It stops as soon as the called party answers by lifting his handset.



It is an interrupted tone of 133c/s with interruption as follows :

0.4sec on, 0.2sec off, 0.4sec on, 0.2sec off and so on.

(C) BUSY TONE :-

This tone is returned to the calling subscriber from the final selector when the called party is engaged. The tone stops only when the calling subscriber replaces his handset. It is an interrupted tone of 400c/s with interruptions as follows :-

0.75 sec on, 0.75 sec off and so on.

(D) NUMBER UNOBTAINABLE TONE :-

This tone is returned to the calling subscriber from the final selector when the called party's line is out of order or disconnected, or not available for some reason. It is continuous tone of 400c/s.

THE PUBLIC TELEPHONE SERVICE :-

As mentioned earlier the first exchanges were manually operated; however, it was not very long before experiments were started with automatic switching equipment. Subsequently the design of automatic exchange have been so extended and improved that systems are now available to cover the whole range from rural communities needing small exchanges up to large densely populated areas requiring closely spaced and inter linked exchanges to serve large numbers of subscribers having a community of interests.

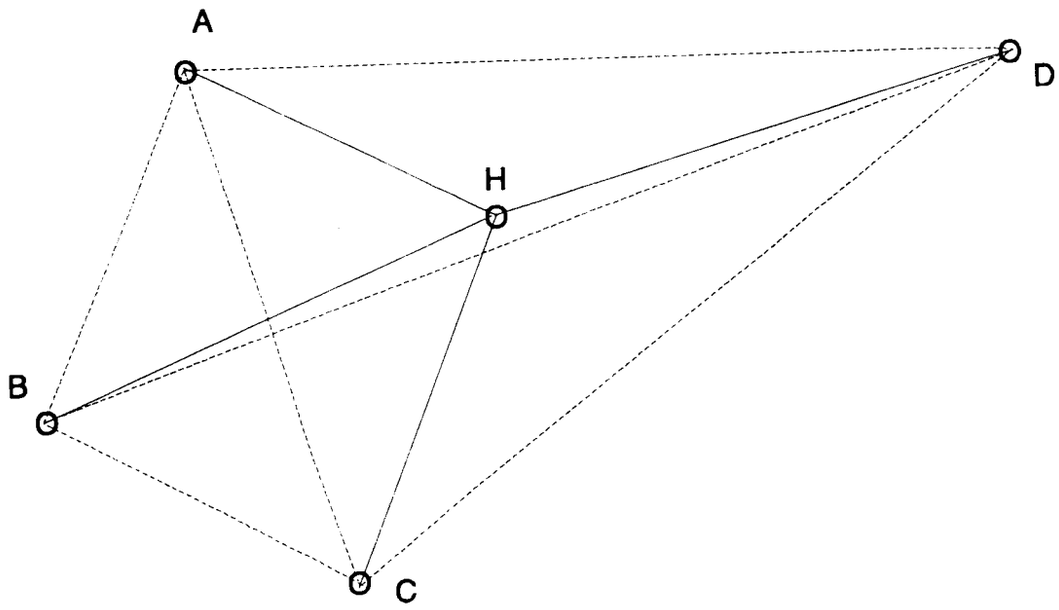
In parallel with these switching developments, the improvements

in long distance transmission techniques have not only reduced circuit cost to a fraction of their former value but also greatly improved the quality of transmitted speech. This led to considerable development of the trunk services, which are now also reaping the benefit of automatic switching.

MULTI - EXCHANGE AREA SCHEME:-

When the number to be dialled is very large, naturally a very large number of subscribers will be situated at an appreciable distance from the exchange and inorder that there may not be appreciable voltage drop, these long lines should also be of thicker guage. This makes cost of external line abnormally high. So the different portions of the exchange are detached from the main exchange and placed at suitable places at large distances from it and at centres of groups of subscribers who are served by the respective units.The interconnections are done by trunk and junction lines, thus reducing the external lines and hence its cost. This detached unit of the main exchange is called as the satellite exchange. Such an exchange system consisting of one main exchange and several satellite exchanges scattered over the area is known as the multiexchange area system.

Generally the main exchange is connected with all the satellite exchanges so that main exchange is tandem position for connections between any two satellite exchanges as in figure below.



If any subscriber of any satellite exchange say B, wants a connection with any subscriber of any other satellite exchange say D, he has to go through the main exchange for getting connection and this main exchange is connected in tandem.

If there is some interest of community between two satellite exchanges, there may be direct junction line connections between them as shown by dotted lines and the subscribers may get connection direct with others in such cases.

DIRECTOR SYSTEM :-

When the subscribers in the exchanges is large, then a complicated trunking arrangement has to be used. This can be avoided if routing of a call is made independant of the actual trunking arrangement. In the director system this principle is utilised. The director portion

of the system absorbs the digits dialled and translates them into required trains of impulses which are generated according to the arrangement. These generated trains of impulses are then sent to the lines and they are followed by the numerical portion of numbering.

The principle of working of a director system will be clear from fig(b). The director portion after receiving definite number of impulses, translates them into the required trains of impulses and stores the numerical portions which are sent later. These impulses are generated by means of an oscillator or vibrator.

When the subsriber takes up his receiver, his uniselector goes on hunting for a free trunk line and it stops as soon as one such is seized.

The director hunter then begins to hunt and it stops when a free director is seized and then only the dial tone is sent. When the subscriber dials the code portion, the director is operated accordingly and when the numerical portion follows the digits are stored in director.

SIGNALLING :-

When comprehensive signalling facilities are provided the principle signalling conditions usually catered for are as follows;

Forward direction :-

1. A calling or seizure signal when a circuit is taken into use.
2. Transmission of dial pulses (automatic working)

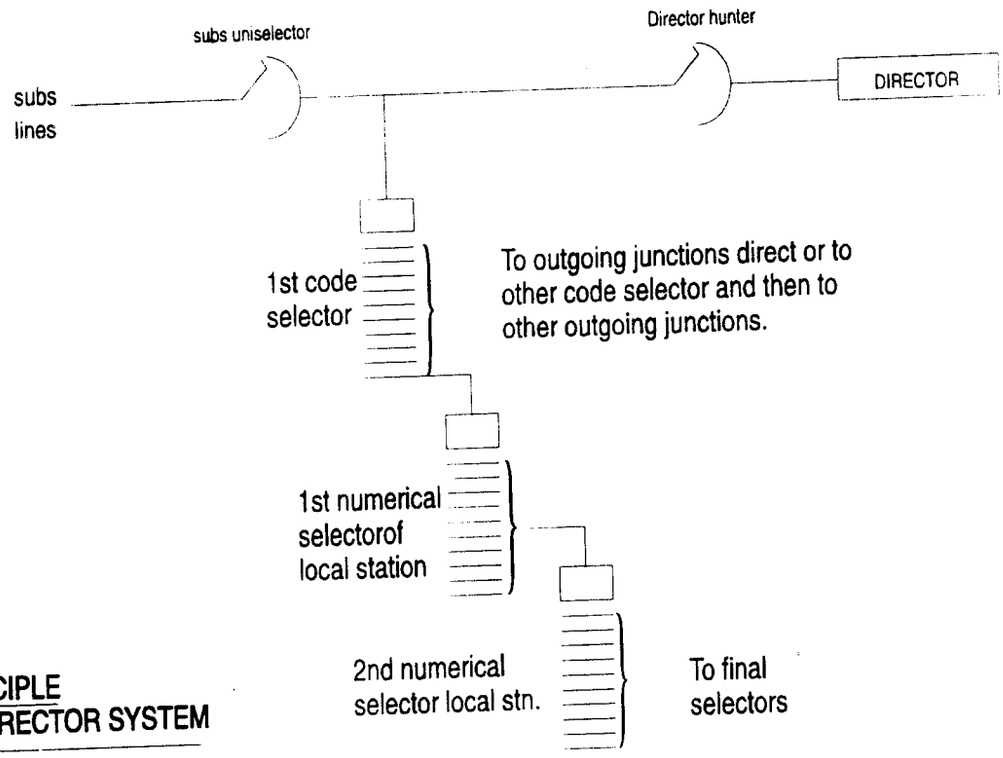


Fig.(b)

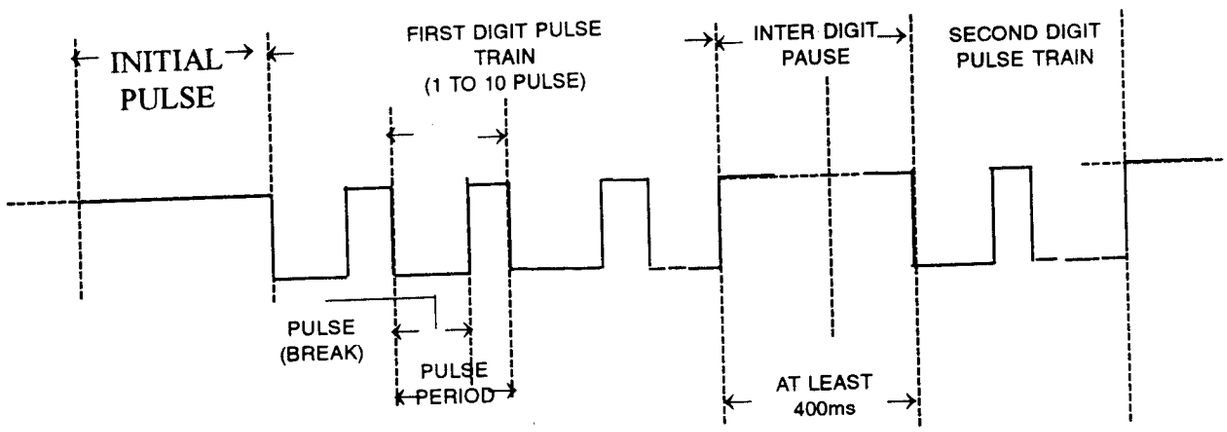
3. Forward holding condition (when appropriate).
4. Forward clearing signal.

Backward detection :-

1. An answering signal returned from the incoming end of circuit (when appropriate).
2. A call answered signal when the called subscriber answers.
3. A clearing signal when the called subscriber clears.
4. When appropriate, return of metering pulses from the group switching centre on STD calls.
5. Where appropriate, return of an engaged condition (backward busy signal) if the incoming circuit is not free to accept a call.

DC. SIGNALLING

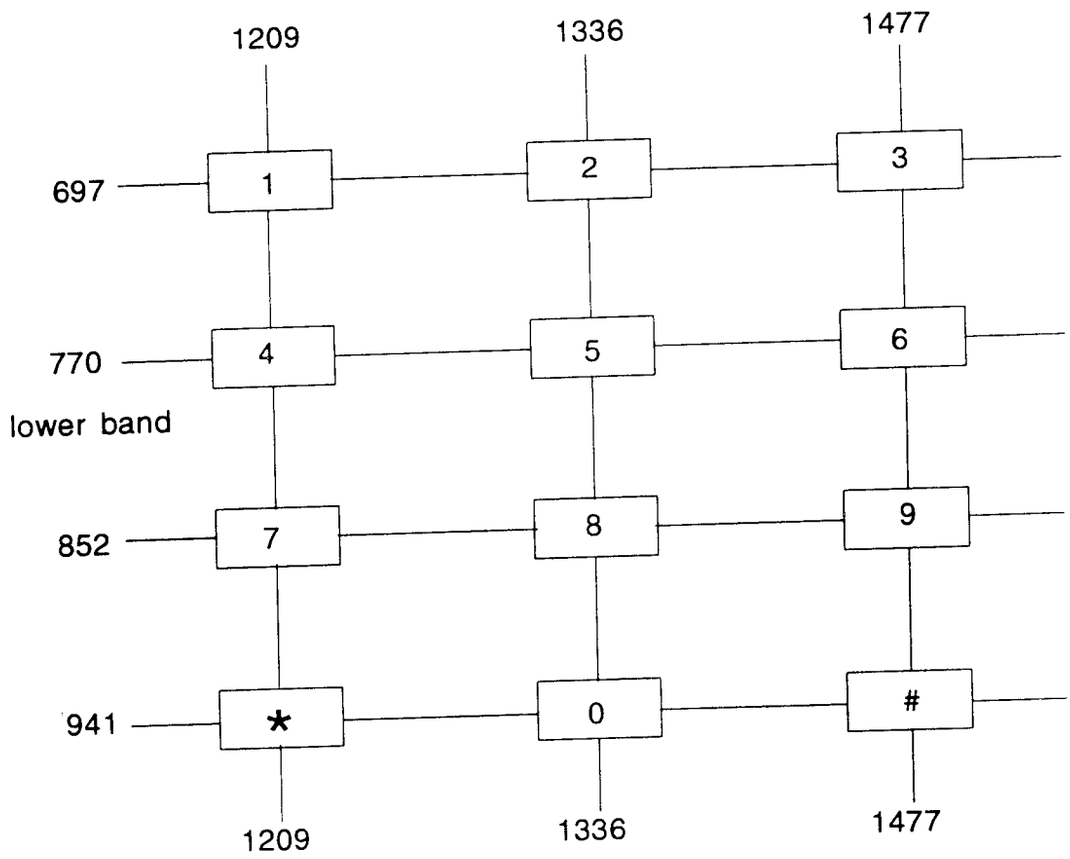
Whenever a junction or trunk circuit is of a type suitable to carry direct-current signals, and the resistance is not too high to permit dc signalling currents of adequate strength to be transmitted, a comprehensive range of calling and automatic supervisory signals can be obtained. Dial pulses may also be transmitted unless the length and characteristics of the circuits are such as to cause excessive pulse distortion.



STANDARD PULSE TRAINS IN AUTOMATIC SWITCHING SYSTEMS

DIALLING:-

In case of pulse dialling each digit (0 to 9) is represented by different train of pulses and hence a two digit will be represented by two trains of impulses. The shortcomings of this method is the time taken was longer for the higher numbers compared to others and hence most of the systems today



Upper band frequency (Hz) - 12 combinations

encourage tone dialling. The concept of combination of freq is made use in tone dialing. Each number dialled is represented as a combination of frequencies depending on the row and column frequencies. This is explained as per the table given above.

POWERSUPPLY FOR TELEPHONE EXCHANGE:-

All the switches and relays require electric current for their operations and the switches of automatic exchanges consume appreciable amount of power. This power can be easily supplied from electric mains supply, but incase of its failure there will be complete breakdown of telephone service. Telephony, however, is a very important service and its importance increases at times of emergency like failure of the mains supply. So powersupply from sources other than the mains is essential for telephone exchanges. So batteries with charging arrangement from the mains can be used as they will provide uninterrupted supply. Secondary batteries or accumulators are invariably used as large amount of current is required. The accumulators of lead-acid type have sulphuric acid as the electrolyte, red lead oxide as the positive plate and spongy lead as the negative plate and they work on the principle of reversible actions. When current is drawn from the batteries, sulphuric acid reacts with red lead and spongy lead converting them into leadsulphates and the electrolyte becomes dilute in strength. When the conversions are complete the batteries cannot be used to supply any further current and they are required to be charged up. This is done by sending current into them in reverse directions from some external dc supply as source.

Charging and discharging can be done in different ways such as

1 Charge-discharge working.

2 Floating working.

3 Booster cells.

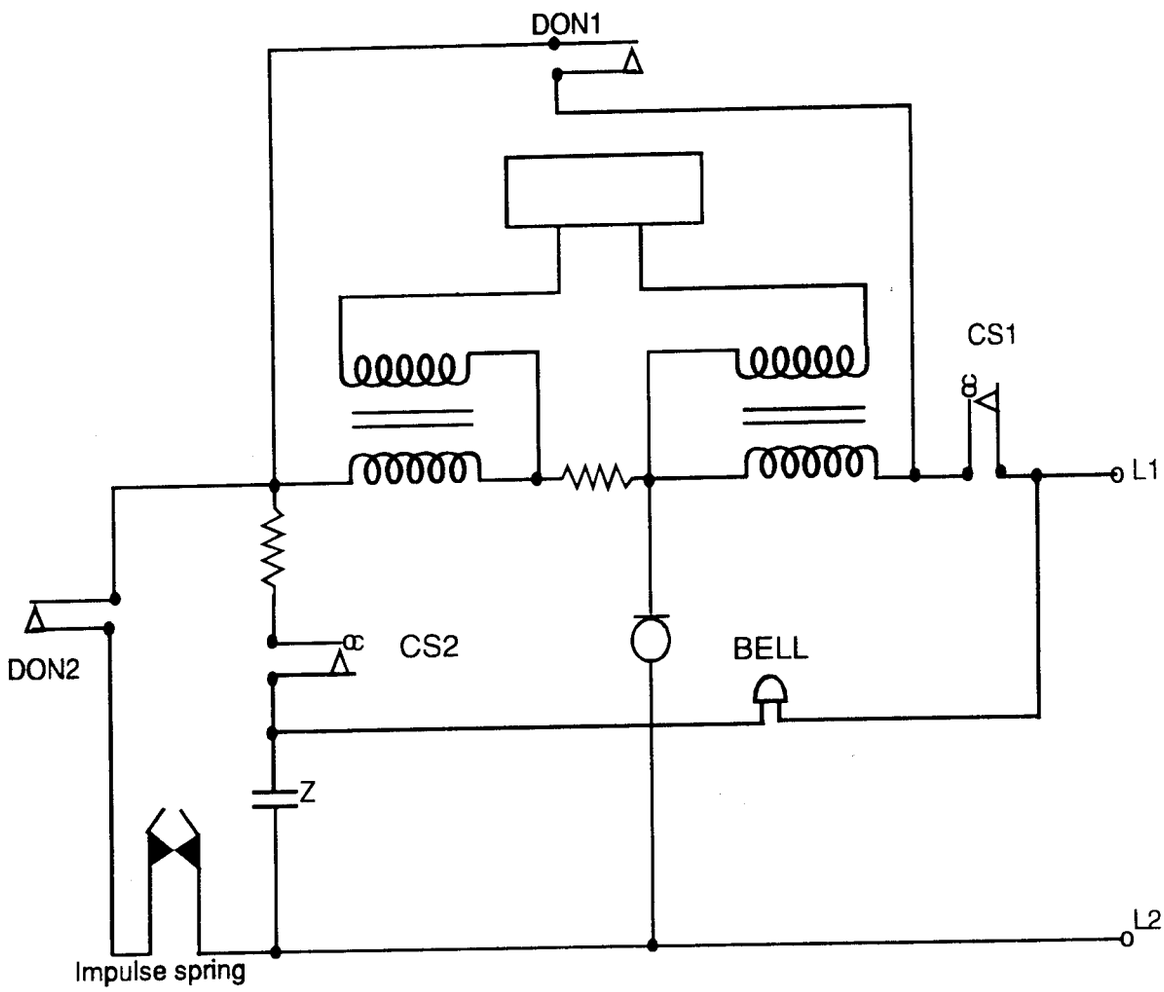
4 C.E.M.F. cells.

GENERAL WORKING OF AN EXCHANGE

The telephone handset has both the receiver and transmitter in it. If subscriber 'A' wants to make a call he lifts up his handset. Initially in the on-hook position there was no connection with the external exchange line as there is open circuit. When 'A' lifts the handset the system goes off-hook, immediately a resistance is provided across the external line and a closed circuit is formed and thus the subscriber gets access to the external line. Depending on the tone available, if a dialtone is present then he proceeds to dial the required number. With the help of group selectors and final selectors required connections are established in the exchange. For each number dialed a train of pulses are sent and depending on these impulses the required connections are established. This is indicated to the called subscriber by providing the ringing tone. Whenever a ring is present at the lines a 75V ac is made available and a 17 c/s ringing current is sent. This is detected and a ring is sounded. As the called subscriber `B` lifts the handset, he too is connected to the external line when his system goes off-hook . Thus the communication between the two subscribers are established until on-hook occurs again or make contact condition prevails.

SUBSCRIBER TELEPHONE SET:

The ringing bell is generally connected in seires with a condensor in the subscribers telephone set so that the bell circuit may not produce



SUBSCRIBER'S TELEPHONE SET

a short circuit but at the same time low frequency ac ringing current may flow through it.

INTRODUCTION TO PUSH BUTTON DIGITAL CODE:

In place of a dial, nowadays a telephone is operated by pressing push button. Ten buttons are provided each for one digit . The speed of operation is increased compared to the dial arrangement. With the advent of electronic exchanges, a corresponding high speed of call completion will be possible and the full benefit of push button signalling will be obtained. Apart from this however the rhythm enforced by the nature of dial operation in case of large numbers is avoided.

Here each digit is signalled as a pulse consisting of two frequencies, one from a group of four and one from another group of three, giving a possible of 4 x 3 = 12 seperate signals.

The four frequencies in one group, called as the low group are all in the lower part of the frequency range, and those in the other group, called high group, are in the upper part of the range. The design of the receiver is such that it fails to operate unless both a low and a high frequency are received. This is especially necessary because the circuit arrangements are such that the telephone microphone is live during part of the time the signal receiver is connected to the line.

A typical code arrangement is shown in figure. The low and high range frequencies are as follows:-

Low group (Hz) : 895 989 1094 1209

High group(Hz) : 1554 1717 1897 2097

The 2097 Hz frequency is not used in the one out of four plus one out of three code.

The multi frequency receiver employed at the exchange to receive and decode the v.f. signals will normally operate reliably on signals of only 25ms duration. This gives a considerable advantage in terms of signalling speed over the ordinary dial, and there is no sensible restraint placed on the rate at which the user may signal a series of digits.

SHORT COMINGS OF EXISTING SYSTEMS:-

The strowger step by step system and some other telephone system depend for their working on electro mechanical switches of one or other type. In such sytems inter connections of different transmission circuits are made by metal contacts which are operated by mechanical movement produced by the attraction of an iron armature of an electro magnet or by the operation of an electric motor. There are some disadvantages of such systems. They are :-

1. Such contacts are subject to wear due to use.
2. Such contacts require adjustments from time to time.
3. Such contacts require constant cleaning as deposits of thin films of dust or oil on them produces high resistance at the contacts.

4. Such contacts are subject to corrosion due to sparking at the contacts both at the time of making and breaking circuits.
5. Such mechanical contacts are subject to bouncing and there may not be proper connections between them.
6. Mechanical movements in the electro mechanical switches take appreciable time during operation. As a result, an appreciable amount of time elapses before a connection is established and very quick operation is not possible.
7. Sizes of switches with mechanical contacts become unmanageably big when they are provided with a large number of contacts.

ELECTRONIC EXCHANGES:-

In electronic telephone exchanges, the inter connection between different transmission circuit are effected by electronic devices and electro mechanical relays and switches are dispersed with. Such electronic devices remove difficulties associated with mechanical contacts mentioned above.

The greatest advantage of using the electronic devices in place of electro mechanical devices is that no time is lost in making a connection and a very high speed of operation is possible which is so much important nowadays.

Some of the electronic devices which can be used for establishing electrical connections and can be used as switching devices are :-

1. Vaccum tubes.
2. Gas tubes .
3. Semi conductor diode.
4. Transistors.

50 LINE ELECTRONIC EXCHANGE:-

50 line EPAX is the second generation electronic exchange in which the program control logic is used and this is used as a private exchange.The switching matrix is worked with PNPN cross-points.There are seven links each of which is provided with a separate register. The progress of the call is under the control of a program available in a ROM in the control circuit. All the operation in the exchange are synchronised and the timing pulse generator gives out all the signals required for this purpose. The scanner devotes 160 micro-seconds to each line every 8 milli-seconds.Each time slot of 160 micro-seconds is further devided into sub-divisions and in these sub-divisions the controlgets information regarding the condition of the line,gives out information regarding the condition of the line,gives out information or analyses the available information.The states of different lines and links are stored in RAMs by a central control.The call processing sequence is on the form of a flowchart and different steps are stored in the ROM. They have stages and branches.The stages indicate different steps of call processing and the branches indicate the next course of action.The signals that are obtained from the output of the ROM operate the different gates, Mux's, decoders etc. to accomplish the different actions in the process.

The earlier type of electronic 50 Line PABX is of the wired logic type.There are 9 local links and 12 junctions in it.The speech circuit is completed through a 3 stage matrix with reed cross-points.The later type of electronic 50 Line PABX is of the Stored Program Control (SPC) type using a Central Processing Unit (CPU). Principles

PROJECT INTRODUCTION

CHAPTER 3

PROJECT INTRODUCTION

The same exchange lines can be used by a number of people from different telephone sets placed at different places. The ways in which this is possible are given below:-

1. Party line working.
2. Extension from the main subsrcibers station.
3. Connection to the main exchange through private branch exchanges.

PARTY LINE WORKING:-

In party line working a number of subscribers are connected across the same pair of lines and all of them share the same lines for getting connections with exchange. There can not be any secrecy however, between the subscribers of a party but from economic point of view it is very suitable specially in rural areas where traffic is not heavy and where secrecy is not so essential. Here the disturbances due to code ringing is reduced by sending ringing current through one line and using earth as the return path.

EXTENSION WORKING:-

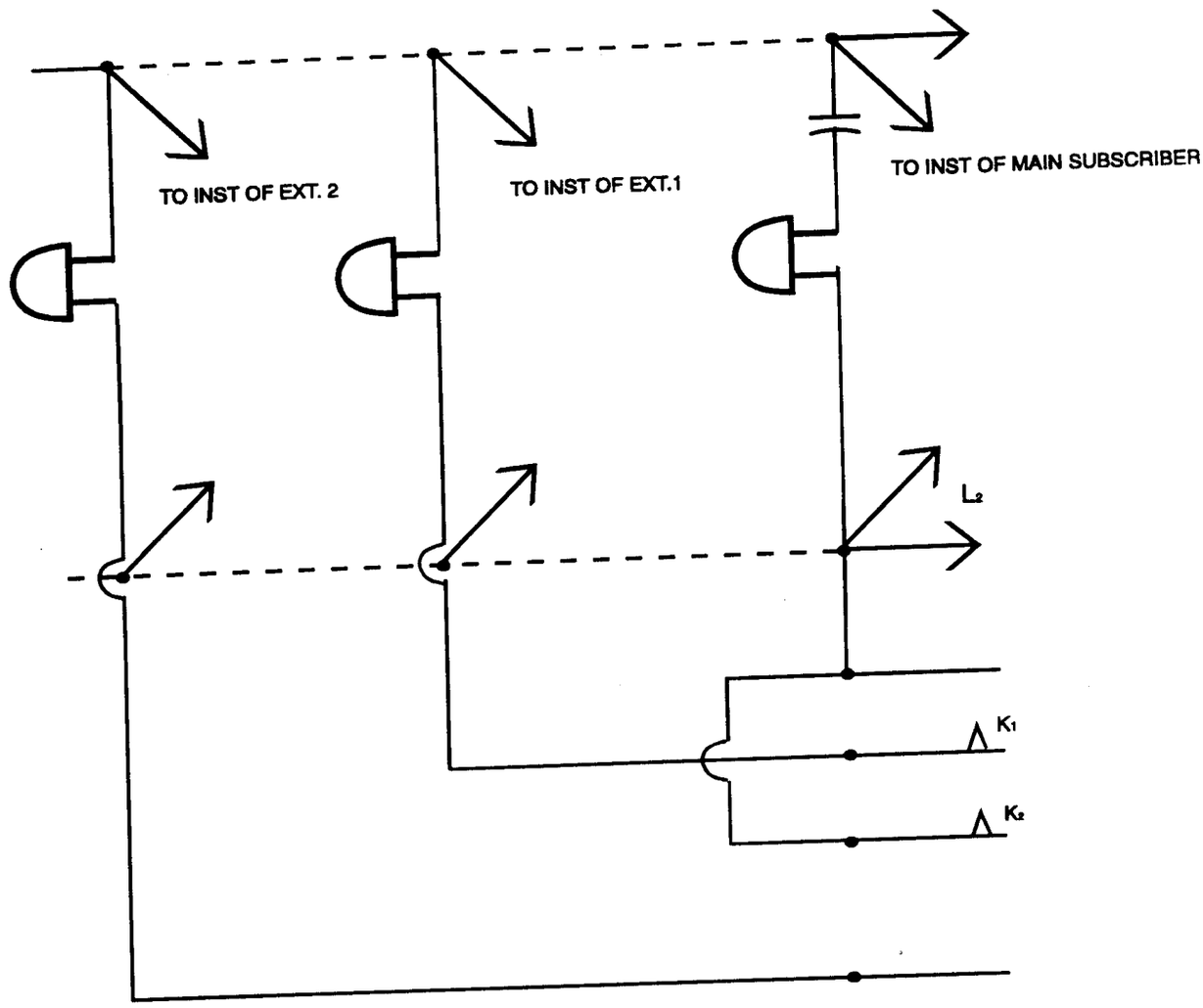
In extension working the lines from the exchange are terminated on the main subscribers apparatus and a number of extensions are connected from the main subscriber's apparatus. When a call is originated from the exchange, the bell of the main subscriber's apparatus rings at first and knowing which extension is called, the main subscriber calls the appropriate subscriber of the extensions who is then connected with the exchange. A telephone set meant for using extension in local battery working is shown in figure(C).

As the telephone instrument of the the extensions are connected across the same line, subscribers from any extension can easily talk by simply taking the handset out of the cradle. When any extension wants to originate a call, he simply takes up the telephone set and the loop produced gives the calling signal to the operator.

PRIVATE MANUAL BRANCH EXCHANGE:-

When the number of extensions is large and when it becomes necessary for the extensions to have usual facility for having connections amongst themselves as well as to have connections with the main exchange, it is usual to have extension through a small exchange which is placed in the position of the main subscriber. Such an exchange is called a private branch exchange. Number of extension lines and exchange lines provided in the exchange are designated as

$$\frac{\text{No. of extension lines + No. of exchange lines}}{\text{Total capacity of the exchange}}$$



PARALLEL CONNECTION OF TELEPHONES

WORKING PRINCIPLE

CHAPTER 4

WORKING PRINCIPLE

The calling subscriber on dialing the required number gets access to the exchange line, be it a DOT or an EPBAX as per availability of free lines. The calling subscriber is immediately connected to our system which simulates a telephone. The calling subscriber then passes the unique code say within five seconds. Now he gets access to the required telephone which is one among an array of parallely connected network. In case the code is not pressed within five seconds the default phone rings. When the called subscriber's telephone goes off-hook the rest of the telephones in the line are cut off thereby maintaining SECRECY. An additional feature available is the call transfer facility . The call can be transferred by pressing the # button followed by the required code. There is facility to make an external call provided the line is free. Our system incorporates the following;-

RING DETECTOR.
OFF HOOK SIMULATOR.
HOLD ON MUSIC.
DTMF DECODER.
TIMERS.
RELAY SWITCHING NETWORK .
OFF- HOOK DECISION .
INTERNAL RING SUPPLY.
FEED BRIDGE ARRANGEMENT.

RING DETECTOR:-

Our system incorporates the ring detector so that it senses the ringing signal sent when the line is found free. This indicates an incoming call. The ring detector is activated whenever there is a 25Hz, 75Vrms present in the external line along with the 24Vdc that is normally present. The capacitor at the input path of the ring detector is the blocking capacitor which allows only the 75V ac to pass to the ring detector i/p. The ring detector processes the 75V ac and provides a 5V dc at its output. The ring detector IC used is 1240.

OFF HOOK SIMULATOR:-

Since our system has all the features of a telephone to detect a call except the handset, the off- hook condition normally detected by lifting of the handset has to be simulated; i.e. generally when the handset of the intercom is lifted that is in off-hook condition, the exchange should stop feeding the ringer signal. This event is called ring trip. This subscriber off-hook status is signalled by completion of the dc loop resulting in a dc current of 20 to 35 mA. Thus the off-hook simulator provides a 600 ohm impedance across the external lines to form an enclosed dc loop. Normally in the on-hook condition there is only an ac path through the loop. There is no dc path i.e. there is no dc current in the loop. The inputs to the off-hook simulator are from the ring detector and the on-hook decision.

Whenever anyone of these inputs are high the 600 ohm impedance is connected across the line.

LATCH:-

As soon as our system detects the ring and off-hook simulator connects the load across the lines the ring trip condition occurs and the exchange stops providing the ring voltage. But still the ring has to be provided to the respective telephones. So this output of the ring detector is latched so that it is used even after the exchange has stopped the ring signal. A 4013 latch is used.

HOLD ON MUSIC:-

A UM 66 IC is specially used to provide this feature. Since there is a small time delay before the unique code pressed reaches the destination telephone, this hold on music is provided during that time interval indicating the calling subscriber that the line is active. After the connection between the subscribers are established the hold on music is stopped.

DTMF DECODER:-

The dialling can either be a tone dialling or pulse dialling. In case of tone dialling any number dialled appears as a combination

of frequencies. There are standard values usually ranging from 600Hz - 1500Hz. For each number the frequency at the row and column are different and thus the numbers are distinguished. For the purpose of further processing these frequencies ought to be converted into the binary form of the particular number dialled. This dual tone multiple frequency decoder thus decodes the unique code pressed and provides at the output a binary equivalent. In case the calling subscriber fails to press the unique code the output is 0000. This is the default condition.

DEMULTIPLEXER:-

The binary output of the DTMF decoder through an arrangement of gates is given to a 74LS154 (4:16) demux so that based on the binary input the particular output line goes low i.e.if the unique code pressed is 2, the binary output of 8870 is 0010 and the second pin goes low at the output of the demux. During the default condition the 0th pin goes low to which the default phone is connected.

TIMERS:-

There are two timers incorporated in our circuit. The 5 sec. timer is provided so that it starts as soon as the ring appears and it signifies that the unique code be pressed within this time. The one minute timer also starts with the appearance of the ring voltage.

If the ring goes on for one minute and no off-hook condition has occured the external connection is cut off. If the called subscriber has lifted the handset within one minute then connection is established and one minute timer goes off.

RELAY SWITCHING NETWORK:-

When an external call comes:-

1. The telephone whose code was pressed should be provided with the ring supply.
2. When the called subscriber lifts his handset, he should be connected to the external line.

To make an external call step 2 has to be repeated. The output of the multiplexer controls the above mentioned operations depending on its inputs which are off-hook detections and decoder output. Since the output of the multiplexer is not enough to drive the relays directly, we introduce a relay driving circuit which provides the amplified current for the relay operation.

OFF-HOOK DECISION:-

Whenever there is an incoming call, ie. a ring is detected and hence initially a load is connected across the external lines. This load has to be removed under the following conditions:

1. When the called subscriber lifts his handset at the parallel

end the load has to be removed in order to avoid excess current drawn by the circuit.

2. The load has to be disconnected when nobody has lifted any of the telephones at the called end even after one minute.

These two decisions are made by the off-hook decision circuit.

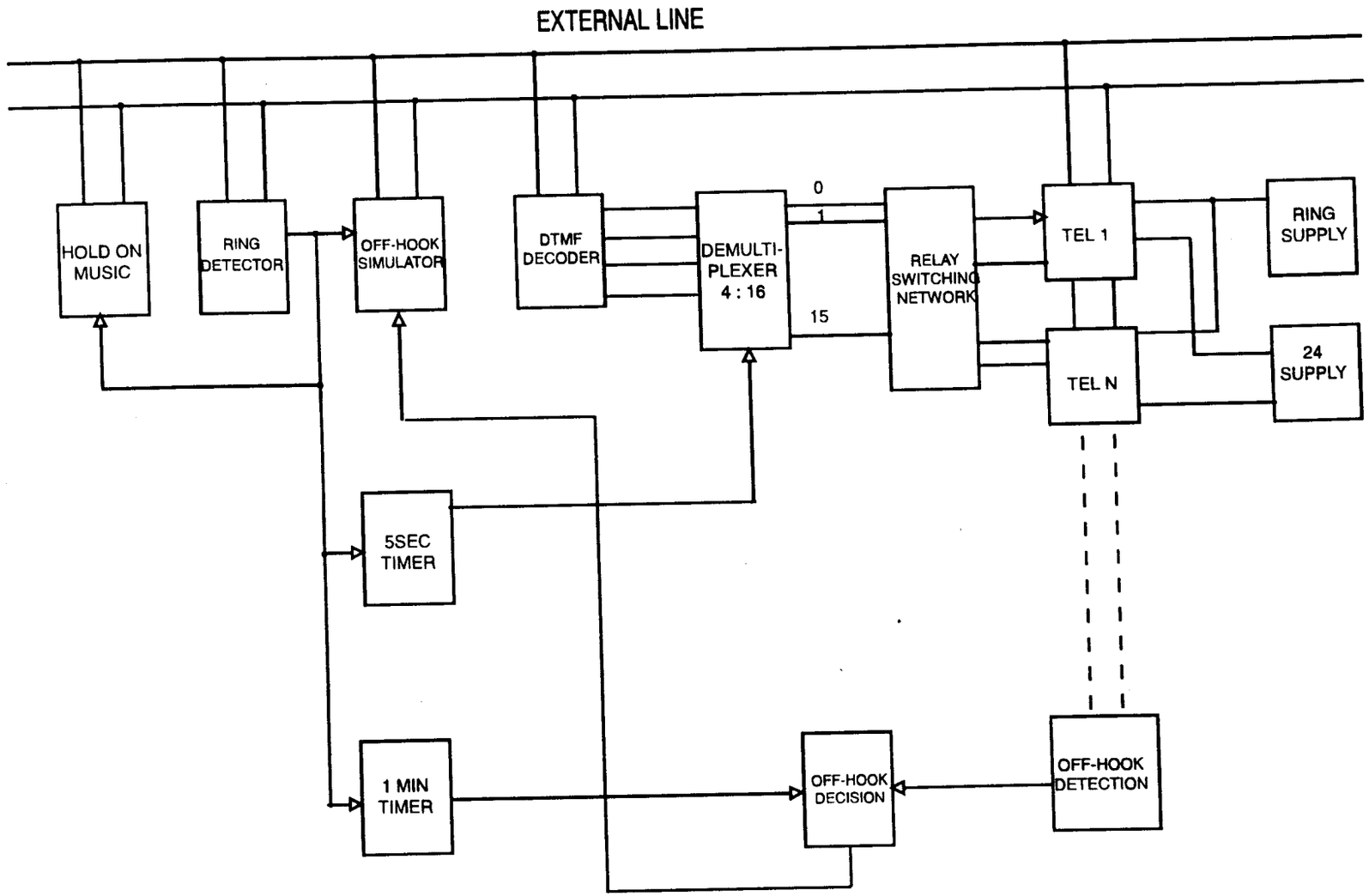
POWER SUPPLY FOR THE SYSTEM:-

The required voltage for our system are :-

1. 75V ac to provide ring voltage to the telephones.
2. 5 V dc for all the components.
3. 24 V dc which has to be to available for off-hook decision.

These voltages are acquired from the secondary of a step down transformer, to the primary of which the line voltage of 220V is given. The 24V dc and 5V dc are obtained from the ac output by using a bridge rectifier.

If a common 24V power supply is used then when a person is speaking then the ac signal will flow into the other telephone circuits thereby preventing secrecy. In order to avoid this a voice coil is provided in the feed bridge arm. The feed bridge arrangement consists of this coil, resistors and diodes which are connected back to back inorder to prevent current flowing from the internal supply to the exchange and vice versa.



BASIC BLOCK DIAGRAM

HARDWARE DESCRIPTION

CHAPTER 5
HARDWARE DESCRIPTION

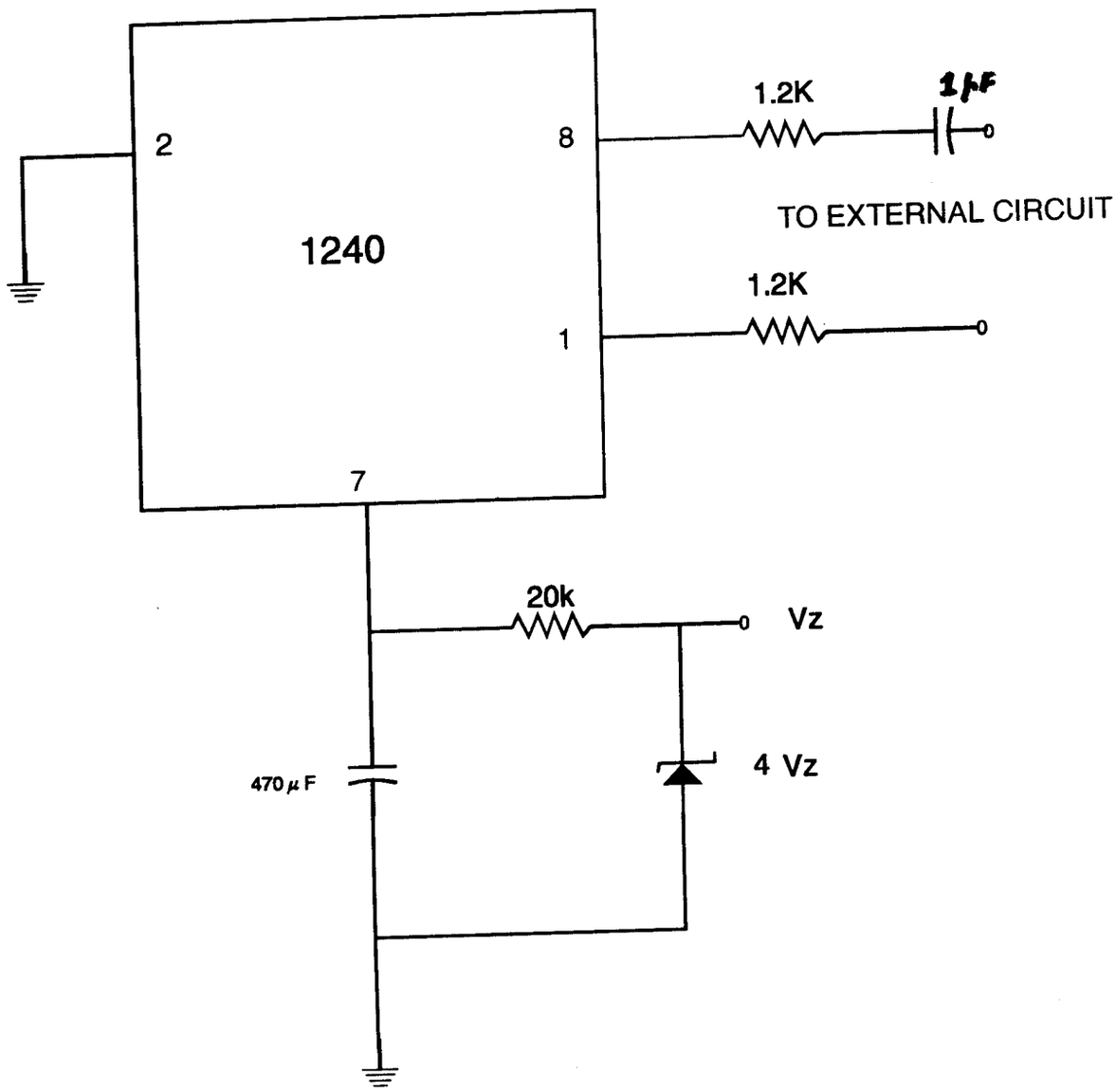
RING DETECTOR:-

The ring detector used here is the 1240 IC which is a replacement for the mechanical bell used in the earlier telephone sets. This integrated circuit is preferred because of its compactness and flexibility. The output of 1240 can drive a piezoceramic convertor (buzzer) .

Initially the telephone line has 24V dc across it. Whenever there is an external call i.e. 75V ac is also available along with the 24Vdc already present in the line. The purpose of the ring detector is to detect this 75V ac whenever it is available across the line. This 1240 acts as a rectifier providing at the output a dc voltage. The supply voltage is obtained from the ac ring signal and the circuit is designed so that noise on the line or variation of the ringing signal cannot affect correct operation of the device.

The internal configuration consists of a rectifier bridge connected between pin 1 & 8 across which the telephone line is connected. In the external circuit the pin 8 is connected to the telephone line through a resistor and a capacitor . The capacitor acts as a blocking capacitor as it allows the 75V ac to pass through it and blocks the 24V dc in the line.This ac signal is rectified by the rectifier bridge and the output is available across the rectifier capacitor connected

RING DETECTOR.



between pin 7 and ground. The rectified output is then brought to the required value of nearly 5V with the help of a 4V7 zener diode.A sweep rate control capacitor can be connected at pin 3 and output control resistor at pin 4 but in our circuit these two pins are not used as we are not directly connecting a buzzer or loudspeaker at the output pin 5 but only making use of the rectified output to drive other circuits like the off-hook simulator.

In case of tone dialling the two frequencies generated are switched by an internal oscillator in a fast sequence and made audible across output amplifier in the loudspeaker if one such is connected across the output.

The advantages or some features of 1240 are

1. Low current consumption in order to allow the parallel operation of 4 devices.
2. Integrated rectifier bridge with zener diode to protect against over voltage.
3. Little external circuitary.
4. Tone and switching frequencies are adjustable by external components.
5. Integrated voltage and current hysteresis.

As soon as the ring signal given by the exchange is detected by our system the exchange stops the ring once a load is connected by the off-hook simulator across the lines. But since we need this rectified ring voltage for later stages to provide actual ringing of the

required telephone at the output , it is required to store this voltage in a latch for use at later stage.

LATCH:-

The latch we choose to use here is the CD4013A which is a COS / MOS Dual D- type flip - flop. The CD4013A has the following features.

a) Set - Reset capability.

b) Static flip - flop operation - retains state indefinitely with clock level either 'high' or 'low'.

c) Medium speed operation - 10 MHz clock toggle rate at 10V.

d) Quiescent current specified at 15 V.

e) Maximum input leakage current of 1 micro ampere at 15V (full package - temperature range).

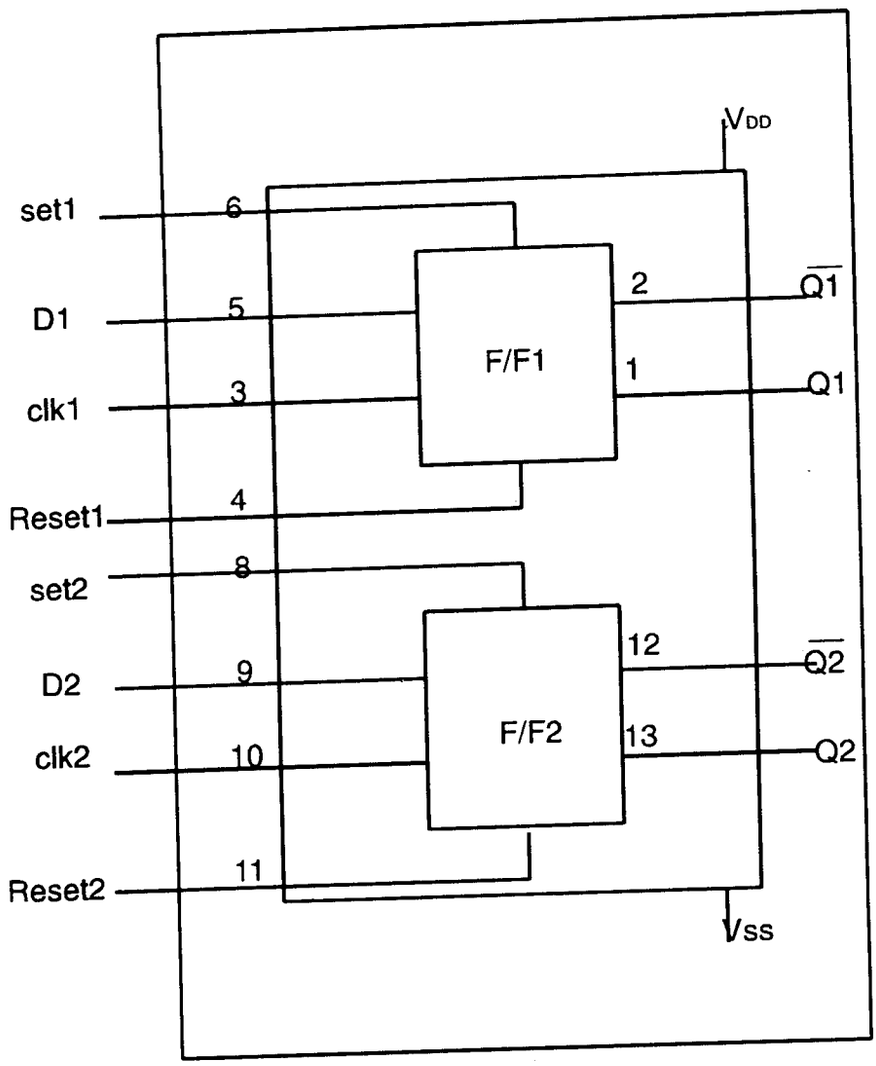
f) I-V noise margin.

WORKING:-

The CD4013A consists of two identical, independent data - type, flip - flops. Each flip - flop has independent data, set, reset and clock input and Q and $\overline{Q}$ outputs. These devices can be used for shift register applications and by connecting $\overline{Q}$ output to the data input, counters and toggle applications.The logic level present at the D input is transferred to the Q output during the positive going transition

of the clock pulse. Setting or resetting is independent of the clock and is accomplished by a high level on the set or reset line, respectively.

FUNCTIONAL DIAGRAM

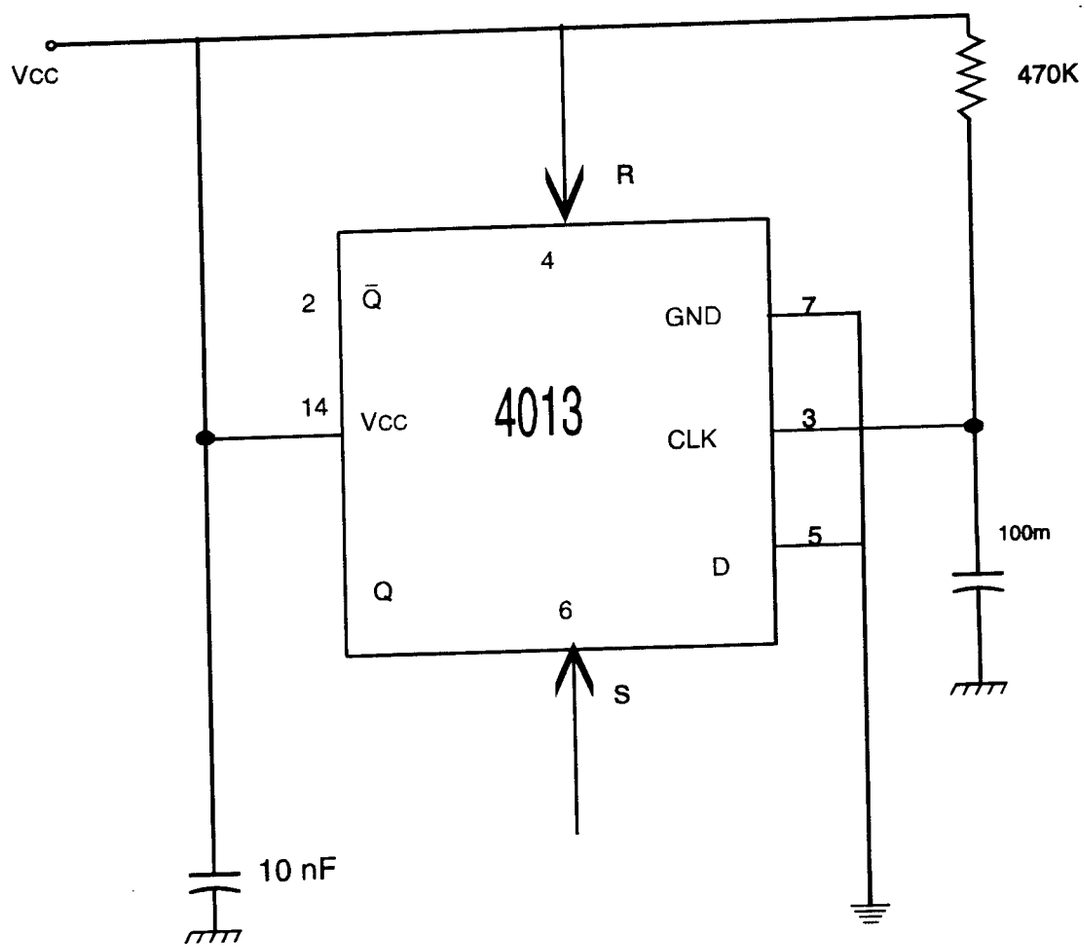


The set input to pin 6 is from the output of the ring detector. D, input is connected to pin 7 which is grounded. The clock input at pin 3 is from the supply Vcc, which is usually +5V. The reset input is given at pin 4. This input depends on the output of the one minute timer and the OR-ed output of all the off-hook decisions. Through a set of logic gates like invertor and 4081 AND gate, 74LS32 OR gate etc, this pin is reset. The truth table is as follows.

TRUTH TABLE

CLK	D	R	S	Q	$\overline{Q}$
⎍	0	0	0	0	1
⎍	1	0	0	1	0
⎎	X	0	0	Q	$\overline{Q}$
X	X	1	0	0	1
X	X	0	1	1	0
X	X	1	1	1	1

CIRCUIT DIAGRAM



Whenever the set input is high the Q output is high and the 5V is available at Q. When it is reset then Q is high. Thus the set input is high whenever a ring is detected and the ring detector output is high. The 4013 is reset whenever any one of the telephone goes off-hook.

The output Q is given as input to off - hook simulator thereby being one of the inputs to determine whether the load be connected across the line or not.The Q output is given to the 18,19 pins of the 4:16 demultiplexer.

During operation near the maximum supply voltage limits, care should be taken to avoid or suppress power supply turn - on and turn - off transients, power supply ripples or ground noise. Any of these conditions must not cause Vcc - Vss to exceed the absolute maximum rating.

To prevent damage to the input protection circuit, input signals should never be greater than Vcc nor less than Vss. Input current must not exceed 10mA even when the power supply is off.

A connection must be provided at every input terminals. All unused input terminals must be connected to either Vcc or Vss, wherever is appropriate.

Shorting of outputs to Vdd or Vss may damage COS / MOS devices by exceeding the maximum device dissipation.

OFF- HOOK SIMULATOR:-

The main function of the off - hook simulator is to present a load of 600 ohm across the exchange lines whenever an external

call is received. This depends on the off - hook decision output and the ring detector output.

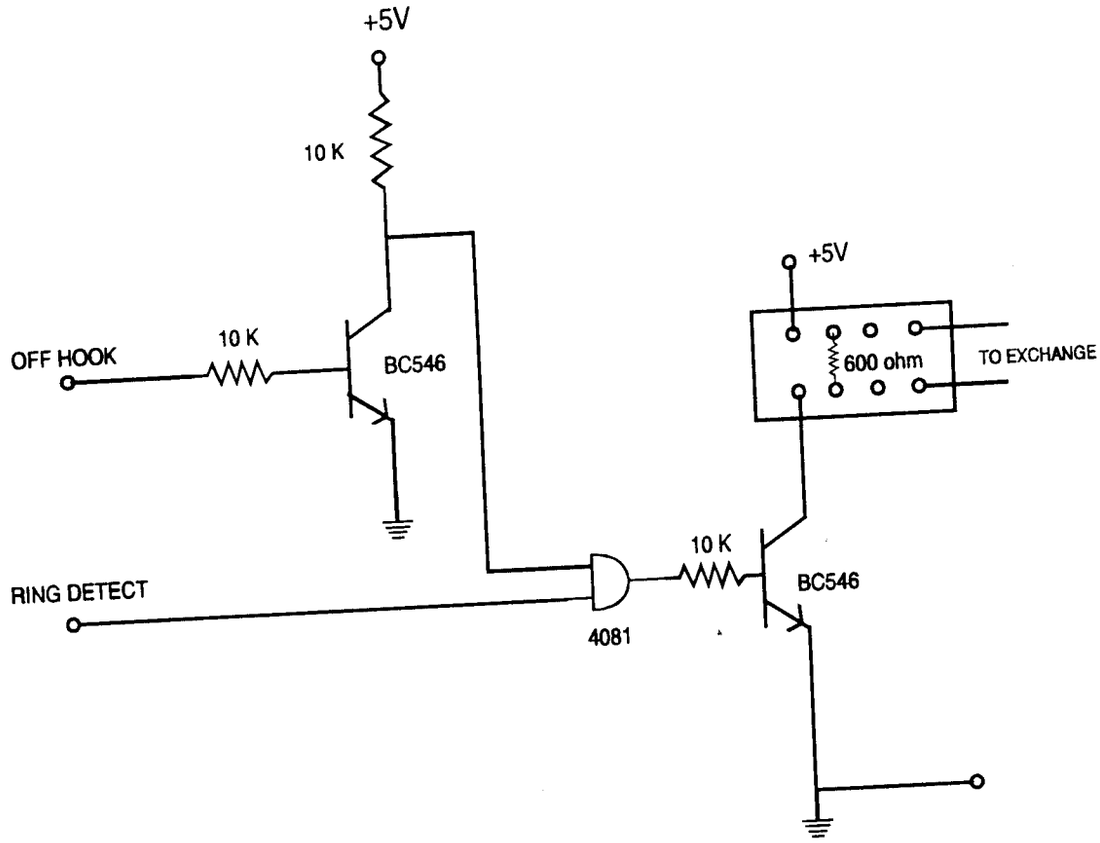
TRUTH TABLE

When the Off - hook output is logic '0' and the ring is present i.e, logic 1, the inputs of the AND - gate are both 1 and hence at the output of the AND gate is logic 1. This logic 1 is then given to a transistor invertor circuit which gives 0V at the collector output. The 600 ohm impedance is connected to the exchange through a relay to avoid loading. The collector output is given as a control input to the relay coil. The 600 ohm impedance is connected across the CN pin of the relay.In the normal condition when no ring is present, the CN and NC are connected, but when a ring is received the output of the collector goes low and hence the relay coil is energised and hence current flows through the coil. This activates the relay switching and hence the CN is now connected to NO and the 600 ohm impedance is connected across the exchange lines. During all the other conditions the collector output is '1' and hence the coil is not energised and hence current flows. Therefore the relay remains in the CN and NC position and the 600 ohm impedance is disconnected from the exchange.

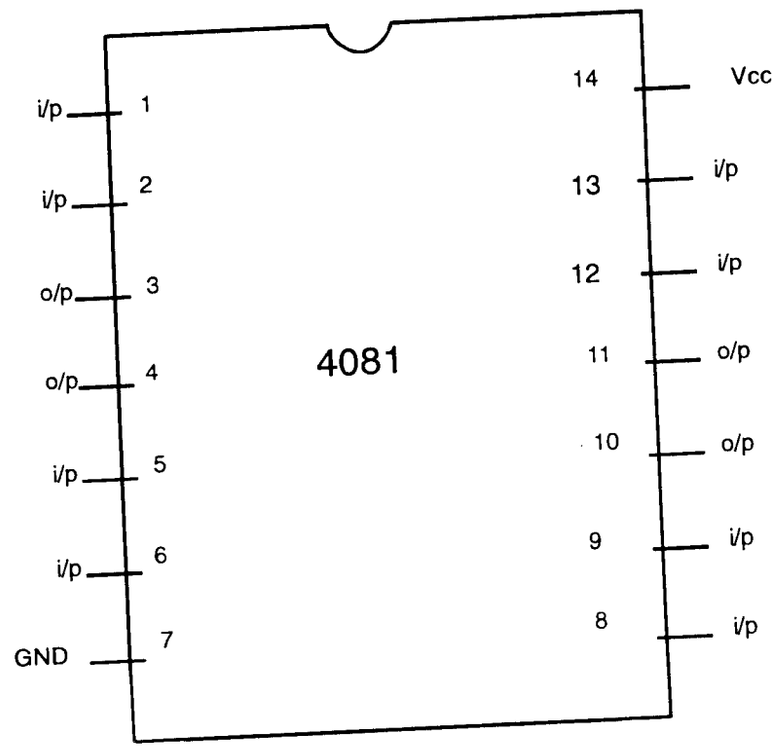
CN - Common
NC - Normally Closed
NO - Normally Open

OFF HOOK	RING DETECT	OUTPUT
0	0	0
0	1	1
1	0	0
1	1	0

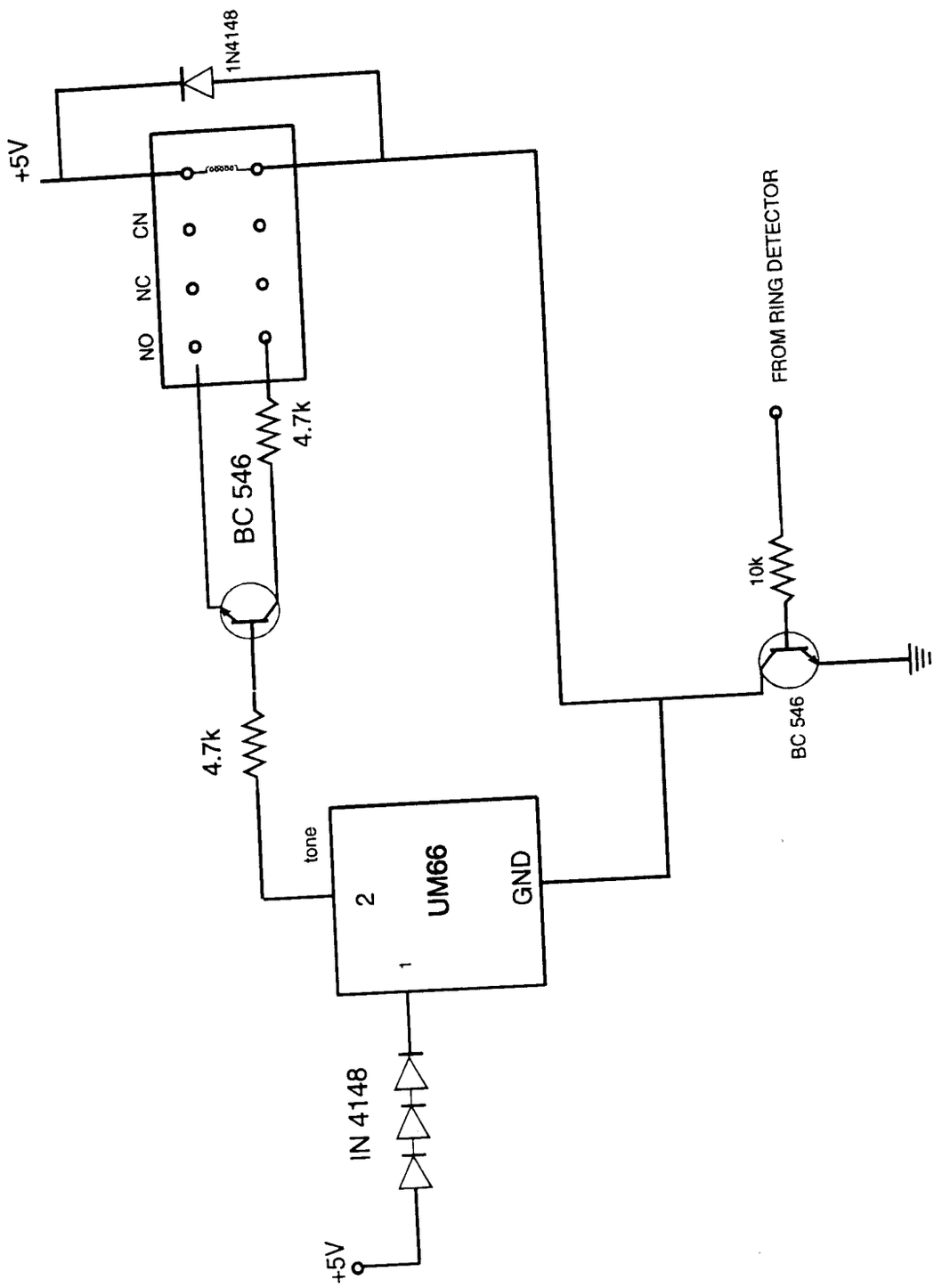
OFF HOOK - SIMULATOR :-



IC 4081 PIN DETAILS



HOLD ON MUSIC:-



Hold on music is provided to inform the caller that the selection of particular telephone is going on internally. As soon as the particular phone is lifted or if nobody lifts the handset after 1 minute the hold on music stops.

UM66 is a three pin IC. Its maximum supply voltage is 3V. There is a music at the output pin 2 when pin 3 is grounded. When a call comes, the call is immediately accepted and FFI is set, 5V is applied to the base of the transistor BC546. Thus pin 3 is grounded and the music is applied to the external line through transistor MPSA44. The external line is connected to the transistor through a relay to avoid loading of the transistor when there is no hold on music.

FF1 - FLIP FLOP 1

The flip - flop is a bistable device, a circuit with only two stable states, 0 and 1. If an input causes it to go to its 1 state it will remain there and remember a 1 untill some signal causes it to go to the 0 state. The flip - flop can be level triggered or edge triggered. In the level triggered the flip flop responds to the input during the level of the clock signal (+ve or -ve). In an edge triggered flip flop the flip flop responds to the input when there is a transition, positive edge triggered [logic 0 to 1] negative edge triggered [logic 1 to 0].

4013 is a positive edge triggered flip flop. The flip flop is set whenever a ring signal arrives. Whenever there is a ring, the ring detector output is 5V, this is applied to the set input of the

flip flop. Due to the positive transition, the flip flop is set. The reset input is from the off-hook decision. The truth table of the flip flop is

S	R	Q	$\bar{Q}$
1	0	1	0
0	1	0	1
0	0	Previous State	
1	1	x	x

The $\bar{Q}$ output which is given as select input to the demultiplexer. The demultiplexer is selected till somebody lifts the telephone or after 1 minute. When nobody lift the telephone the reset input is 1 thus FF is reset $\bar{Q}$ = 1 and the demultiplexer is deselected, making all output high.

TIMER :-

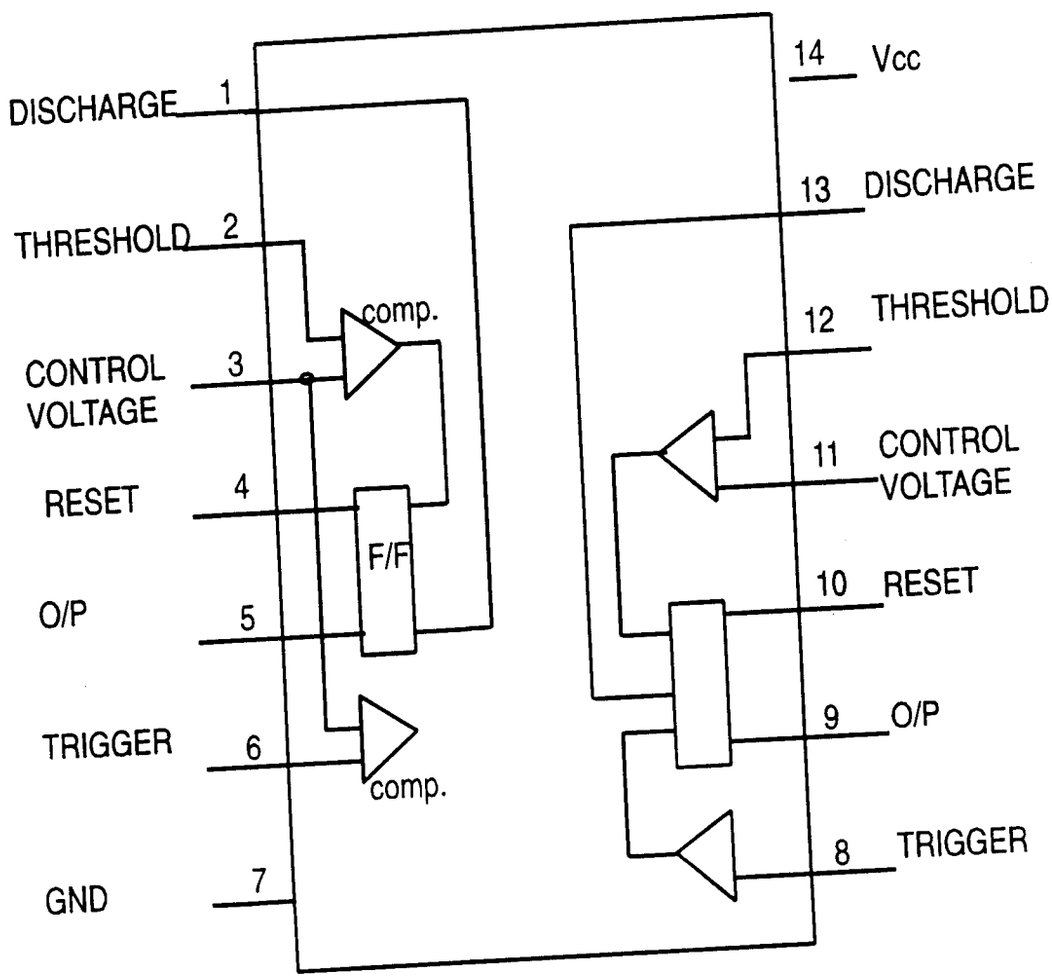
A timer is required for two purposes in our system.

1) A 5 sec. Timer :- A time limit of 5 sec is given for the caller to dial the DTMF code he desires.
2) A 1 minute Timer :- If there is nobody on the called side to receive the call then after 1 minute the system on the called side is automatically disconnected from the exchange.

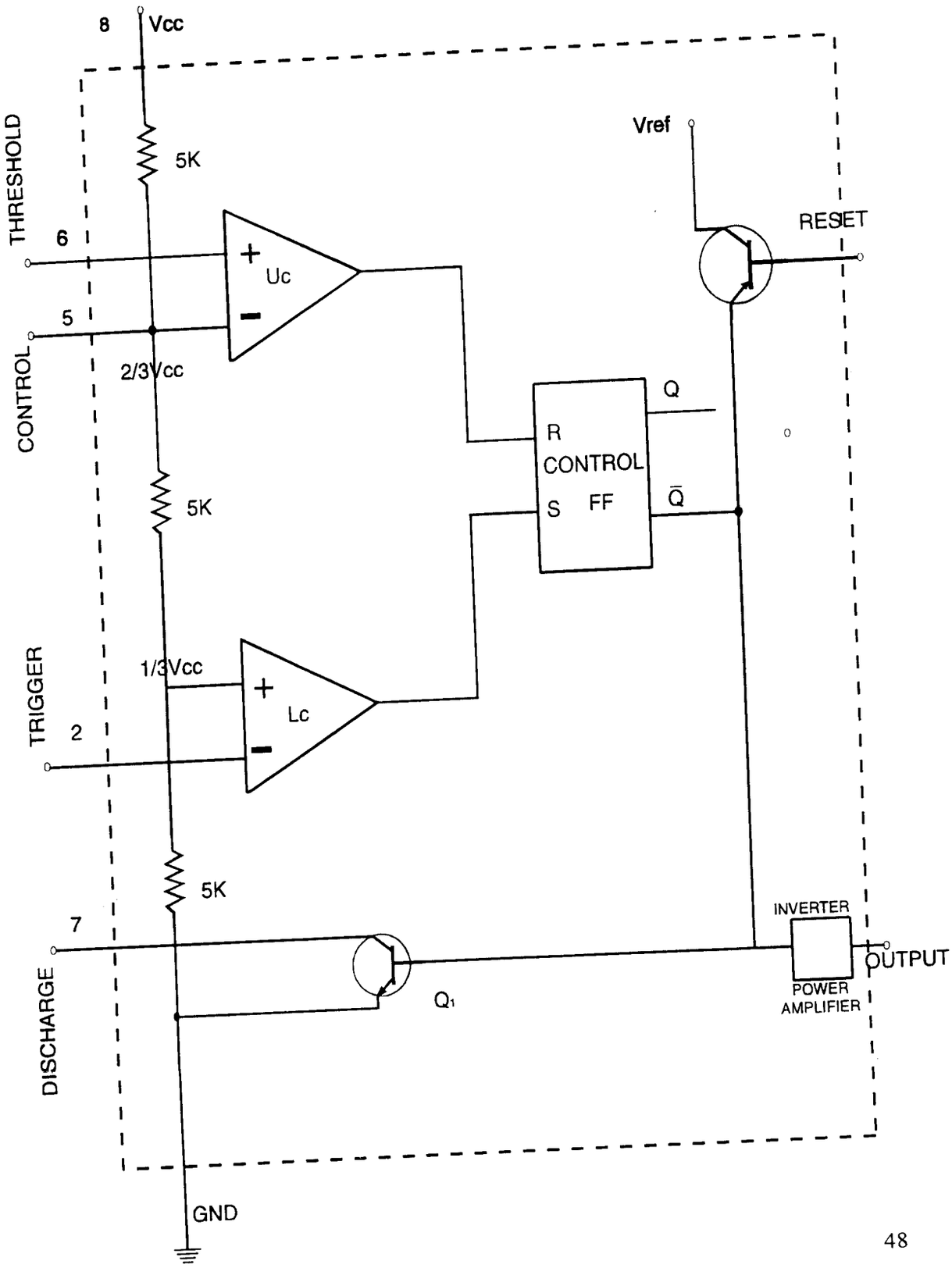
To implement the two timers we have used 556 which has two 555 timers in it. The 555 timer is a highly stable device for generating

accurate time delay. The 555 timer can be used with supply voltage in the range of +5V to +18V and can drive load upto 200mA. It is compatible with both TTL and CMOS logic circuits. Because of the wide range of supply voltage, the 555 timer is versatile and easy to use in various applications.

PIN DETAILS OF 556



FUNCTIONAL DESCRIPTION OF 555



The three 5 kohm internal resistors act as voltage divider, providing bias voltage of 2/3 Vcc to the upper comparator (UC) and 1/3 Vcc to the lower comparator (LC) where Vcc is the supply voltage. Since these two voltages fix the necessary comparator threshold voltage, they also aid in determining the timing interval. A capacitor (0.01 μfarad) is usually connected between control voltage (pin 5) and ground to by-pass noise or ripple from the supply.

In the standby (stable) state, the output $\bar{Q}$ of the control flip flop (FF) is HIGH. This makes the output low because of power amplifier which is basically an invertor. A negative going trigger pulse is applied to the pin 2 and should have its dc level greater than the threshold level of the lower comparator (i.e, Vcc / 3). At the negative going edge of the trigger, as the trigger passes through Vcc / 3, the output of the lower comparator goes HIGH and sets the FF (Q = 1, $\bar{Q}$ = 0). During the positive excursion, when the threshold voltage at pin 6 passes through 2 /3 Vcc the output of the upper comparator goes HIGH and resets the FF (Q = 0 , $\bar{Q}$ = 1).

The reset input provides a mechanism to reset the FF in a manner which overrides the effect of any instruction coming to FF from lower comparator. This overriding reset is effective when the reset is less than about 0.4V. When this reset is not used, it is returned to Vcc. The transistor Q2 is driven by an internal reference voltage Vref obtained from supply voltage Vcc.

In the standby (stable) state, FF holds transistor Q1 on, thus clamping the external timing capacitor C to ground. The output remains at ground potential i.e, LOW. The trigger input is from the output of ring detector. Whenever a ring comes from the exchange i.e, somebody is calling the output of the ring detector is 5V. Since the timer is negative edge triggered, the output of ring detector is inverted and given as trigger to the timer input.As the trigger passes through Vcc / 3 the FF is set i.e, $\bar{Q}$ = 0. This makes the transistor Q1 off and the short circuit across the timing capacitor C is released. As $\bar{Q}$ is LOW, output goes high (= Vcc). The timing cycle now begins. Since C is also unclamped, voltage across it rises exponentially through R toward Vcc with a time constant RC.

After a time period T the capacitor voltage is just greater than 2 / 3 Vcc and the upper comparator resets the FF, that is R = 1, S = 0. (Assuming very small trigger pulse width) This makes $\bar{Q}$ = 1, transistor Q1 goes on (i.e, saturates), thereby discharging the capacitor C rapidly to ground potential. The output returns to the standby state or ground potential. The voltage across the capacitor is given by,

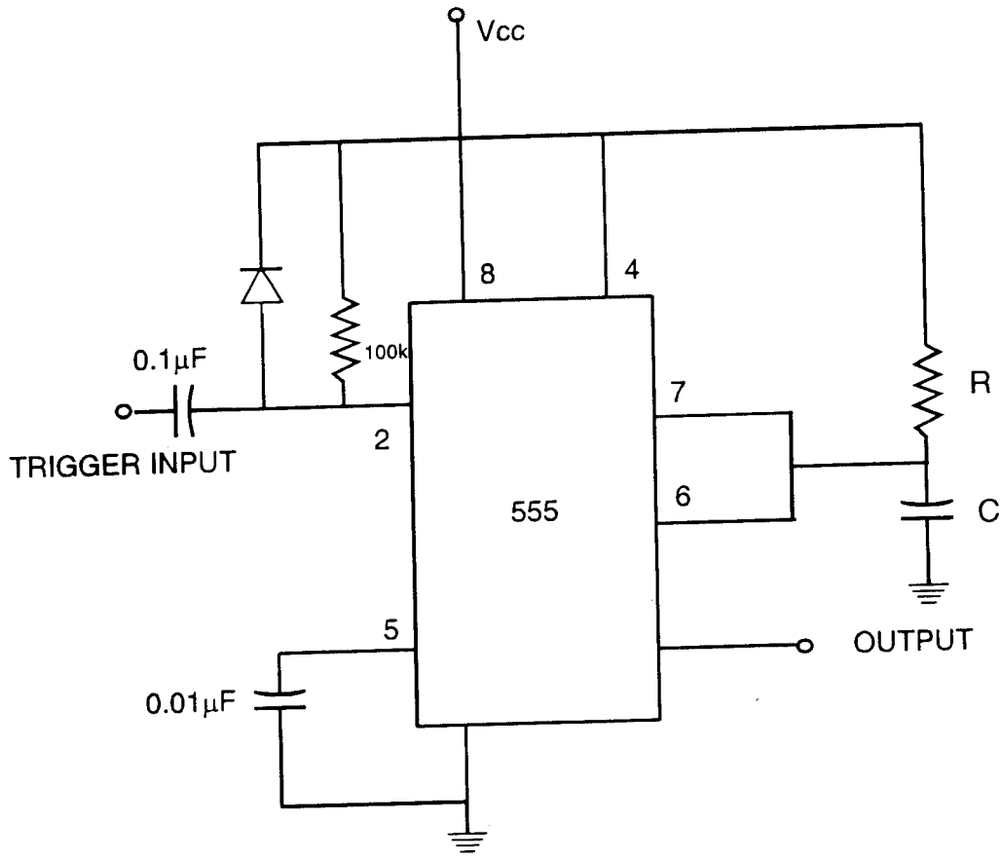
$$Vc = Vcc \left(1 - e^{-t/RC} \right)$$

At t = T, $Vc = (2/3)Vcc$

Therefore, $2/3\ Vcc = Vcc \left(1 - e^{-T/RC} \right)$

$$T = RC \ln (1/3)$$

$$T = 1.1\ RC \text{ (seconds)}$$



MONOSTABLE OPERATION

5SEC TIMER

Tp = 5 sec

Tp = 1.1 RC

R = 450 k

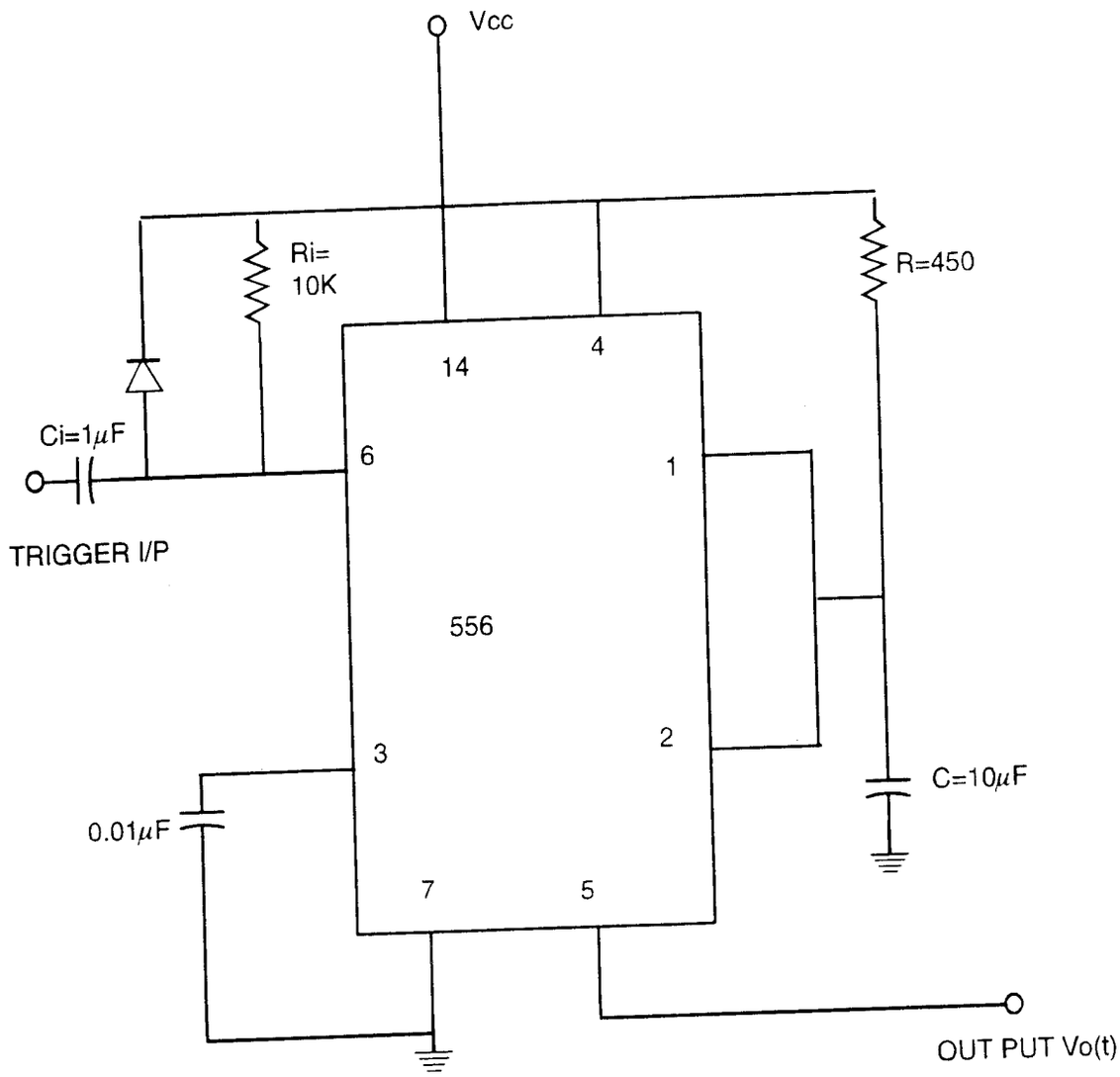
C = 10 micro farad

1-MINUTE TIMER

Tp = 60 sec.

C = 100μF

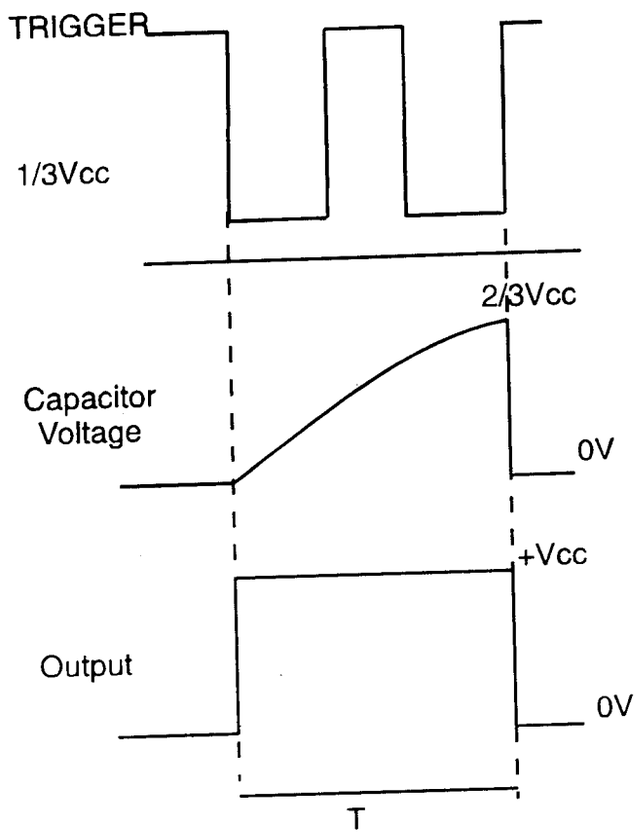
R = 545kohm



TIMER CIRCUIT

5 SEC TIMER

It is evident from equation T = 1.1 RC, that the timing interval is independent of the supply voltage. It may also be noted that once triggered the output remains in the HIGH state untill time T elapses, which depends only upon R and C. Any additional trigger pulse coming during this time will not change the output state. Sometimes the monostable circuit mistriggers on positive pulse edges, even with the control pin bypass capacitor. To prevent this a resistor and capacitor, 10k and .001micro farad is used at the input which forms a differentiator. During the positive going edge of the trigger, diode D becomes forward biased, thereby limiting the amplititude of positive spike to 0.7V.



DTMF DECODER:-

The unique code which is used to select a particular telephone is dialled in the Tone mode by the calling person. On the called side a DTMF receiver is used to receive this tone which is a combination of two frequencies and convert it to a Binary Coded Decimal. For this purpose the DTMF decoder UM92870 is used.

The UM92870 is a complete DTMF receiver designed to detect standard DTMF signals. It includes a differential input amplifier, filter section, decoder section and steering logic circuits. The differential input amplifier allows adjustments of gain and choice of input configuration. The filter section provides a dial tone filter for dial- tone rejection and separates the dual tone signals into low-group and high- group tones. The decoder decodes all 16 DTMF tone pairs into a four bit code.

FUNCTIONAL DESCRIPTION

The exchange line is applied to the inverting input through C1, R1 of the differential input operational amplifier and a bias source Vref is used to bias the input at midrail. Adjustment of gain is achieved by connecting a feedback resistor to the OP amp output (GS). For a single ended input configuration OP-amp is connected for unity gain and Vref = $V_{DD}/2$.

The differential amplifier is followed by the filter section. Dial tone at 350 Hz and 440 Hz is then rejected by a third order switched capacitor notch filter. The signal is split into individual high and low frequency components by two sixth order switched capacitor bandpass filter. Each component tone is then smoothed by an output filter and squared up by a hard limiting comparator. If the original DTMF input signals are valid tones, then the outputs of the comparators will be two rectangular waves.

The resulting rectangular waves are applied to a decoder where a counting algorithm measures and averages their periods. When the decoder recognizes the presence of a valid tone the Est signal goes high. Est indicates that two tones of proper frequency have been detected and initiates an RC timing circuit.If both tones are present for a minimum guard time, which is determined by the external RC network, the DTMF signal is decoded and the resulting data is latched in the output register. A logic high on Est causes Vc to reach the threshold of the steering logic. When the voltage on Vc rises above V_{TST} it causes the device to register the detected tone pair and update the output latch. At this point, the GT output is activated and drives Vc to VDD. GT continues to drive high as long as Est remains high. FInally, the delayed steering (StD) output is raised and indicates that new data is available. The contents of the output latch are made available on the four-bit output bus by raising the three-state control input (TOE) to a logic high.

The internal clock circuit is completed with the addition of an external 3.5795 MHz crystal.

5SEC TIMER:-

The 5 sec. timer is used to present the DTMF code at the input of the demultiplexer. If the code is not pressed within 5 sec of dialling the number then the default phone is selected.

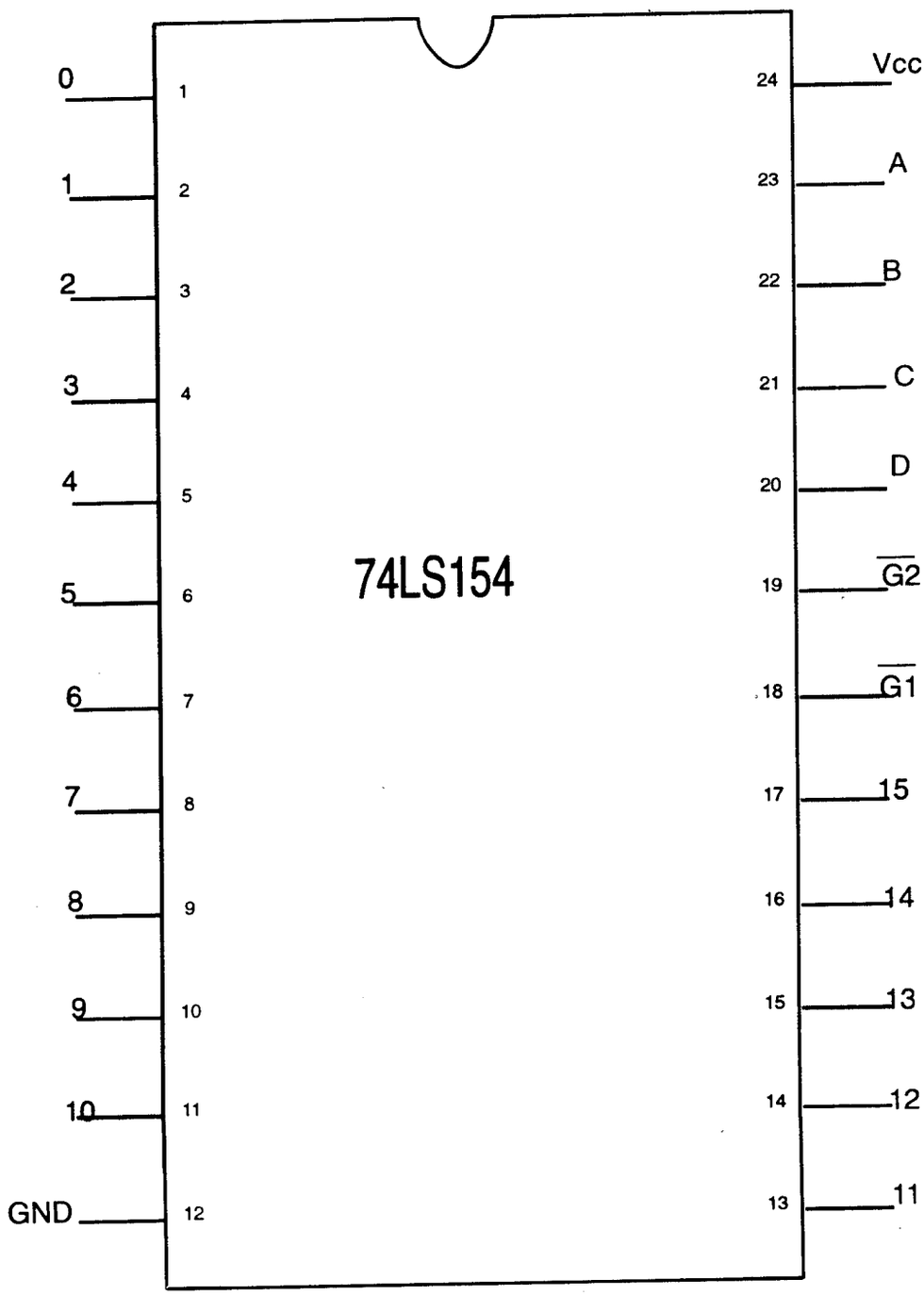
When a valid code is pressed, pin 15 of DTMF decoder goes high. When this happens within 5 sec, the flip flop is set. The Q output of the flip flop is given to the AND gate so that the code is given as input to the demultiplexer, to select the desired telephone. If the code is not pressed during 5sec then the flip flop is not set Q = 0 and the code pressed after 5 sec is not allowed to reach the input of the demultiplexer. Since one input of all AND gates are 0, the input to the demultiplexer is all 0's and the default phone is selected.

4 : 16 DECODER / DEMUX:-

An important feature of the system is the unique code for each of the telephone connected in parallel. Depending on the code dialled at the calling end, a DTMF signal is sent acrossthe external line which is received at the called end (our system) and using a

74 154

PIN DETAILS



DTMF decoder, a four - bit BCD code is obtained for each code (0,1,2,3.....) pressed at the calling end. The BCD code is used to activate that particular telephone alone, which is done using a 4:16 decoder/demux. For this purpose 74LS154 is used.

Depending on the code pressed the BCD input to the demultiplexer varies and the corresponding output of 74LS154 goes low since output signal is active low.

There are two select inputs pin 17 and 18. The demultiplexer is enabled only as long as pin 17 and 18 is low, otherwise all outputs are high irrespective of the inputs. These inputs are used to enable the demultiplexer only as long as that particular telephone whose code was pressed is ringing. As soon as the person lifts the telephone the off-hook detection circuit gives an output of +5V which resets the flip flop, hence $\bar{Q} = 1$ which given as select input to the demultiplexer disables it. Thus any code pressed at the calling end when the conversation is going on is prevented from reaching the telephone at the called end.

If nobody lifts the telephone then after 1 minute, the output of the 1 minute timer goes low. The flip flop is then reset $\bar{Q} = 1$ and the demultiplexer is disabled untill the next incoming call.

MULTIPLEXER

There are four different conditions to be satisfied.

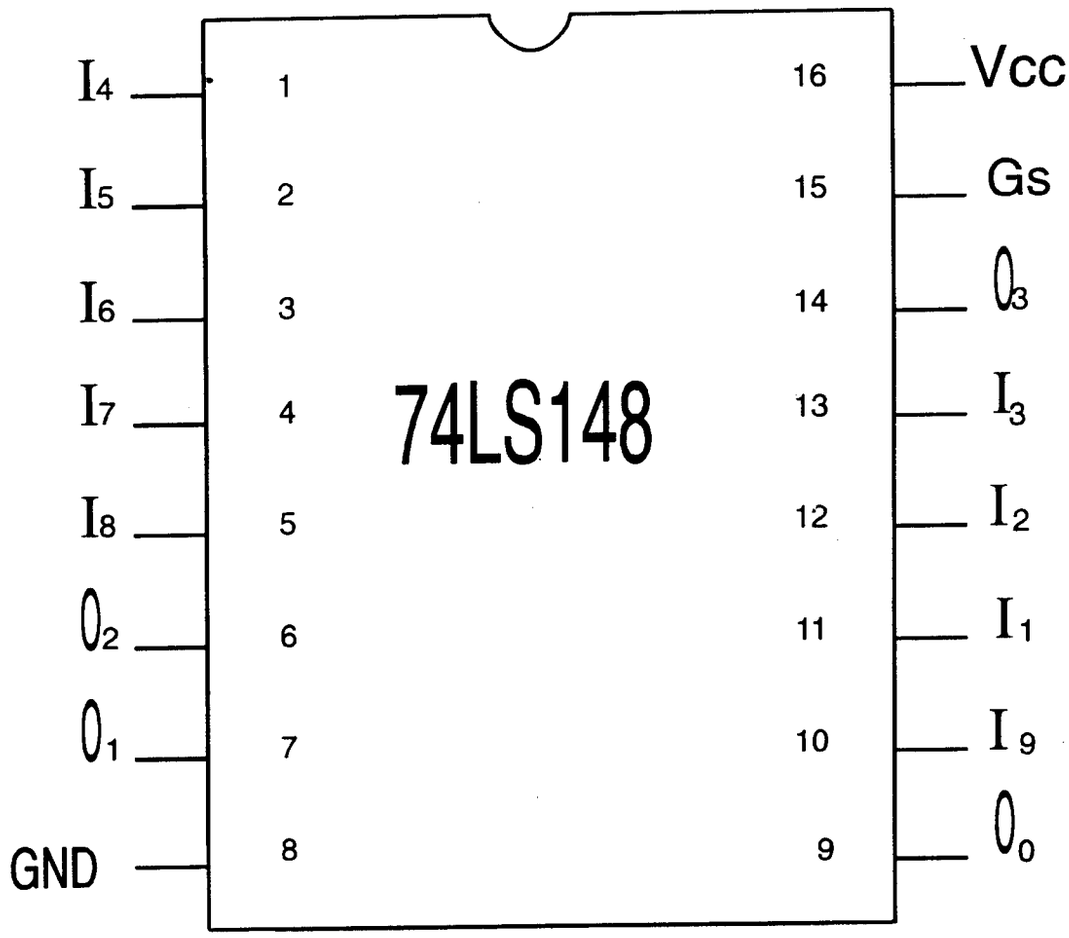
1. When there is an incomingcall the telephone whose code was pressed should ring.
2. When the person lifts the handset the ring signal is stopped and he should be connected to the exchange.
3. When the person places back the handset he should be disconnected from the exchange.
4. When anybody lifts the handset he should be connected to the exchange.

Demultiplexer O/P	Off - hook detection O/P
0	0
1	0
x	1

The relays used for each telephone are switched accordingly to satisfy the above conditions. The output of the multiplexer is given as control voltage to the relays.

74LS148

74LS148 is an 8 line to 3 line priority encoder. These priority Encoder encodes the inputs to ensure that only the highest order data line is encoded. All inputs and outputs are active low.The EI is used to provide secrecy.Whenever any one of the telephones go off-hook the output of 74LS148 goes low. This is inverted and given



to EI all other (z) telephones. Since the EI of the other 74LS148 is high it does not respond to the inputs, thus even if they lift the handset they are not connected to the exchange thus providing secrecy.

Inputs I_5,$I_6$are used and outputs A0, A1 are used.The output of off-hook detection is inverted and given to I5 (pin 2).The output of decoder 74LS154 is given to I_6 (pin 3). I_7 is permanently given to Vcc.

OFF - HOOK DETECTION:-

An off-hook decision circuit is needed in order to detect the ON/OFF hook states of the telephone, since that decides when the telephone should be connected to the exchange.

When an external call comes, the particular telephone whose code was sent at the calling end rings. The person then lifts the telephone which is sensed as off- hook by the detection circuit and then by controlling the relay switching, that particular telephone alone is connected to the exchange.

Similarly when a person wants to make an external call, he lifts the telephone handset, the detection circuit senses it as off-hook and then connection to the exchange is given, subsequently allowing him to make an external call.

When the telephone is in ON-hook the voltage across the pair of telephone wires is 24 V (for EPBAX) and when it goes to OFF-hook it drops to around 12V, a current of 40 mA is drawn.An internal supply of 24V is provided for this purpose of OFF-hook detection. A comparator is used to sense the changes 24V to 12V and similarly 12V to 24V.To reduce the voltage to TTL logic level (0 - 5V) a resistordivider network is introduced at the input to the negative terminal of LM324.

BASIC OPERATION OF COMPARATOR:-

A comparator is a circuit which compares a signal voltage applied at one input of an OP-amp with a known reference voltage at the other input. It is basically an open loop OP- amp with +Vsat (= Vcc).There are two types of comparators

1. Non- inverting Comparator.
2. Inverting Comparator.

CIRCUIT DIAGRAM:-

Here an inverting comparator is used.The reference input is 3.7V provided by thr zener diode 3V7 which is reverse biased by the 10k ohm resistor. The reference voltage is given at the non-inverting input of LM324. The input voltage to be compared is given to the inverting input which is the output of the resistor divider network.In ON-hook condition 24V is present across the telephone wires. The voltage at the inverting input is approximately,

$$I = \frac{24}{22K + 5.6K} = 0.869 \text{ mA}$$

$$V = IR$$

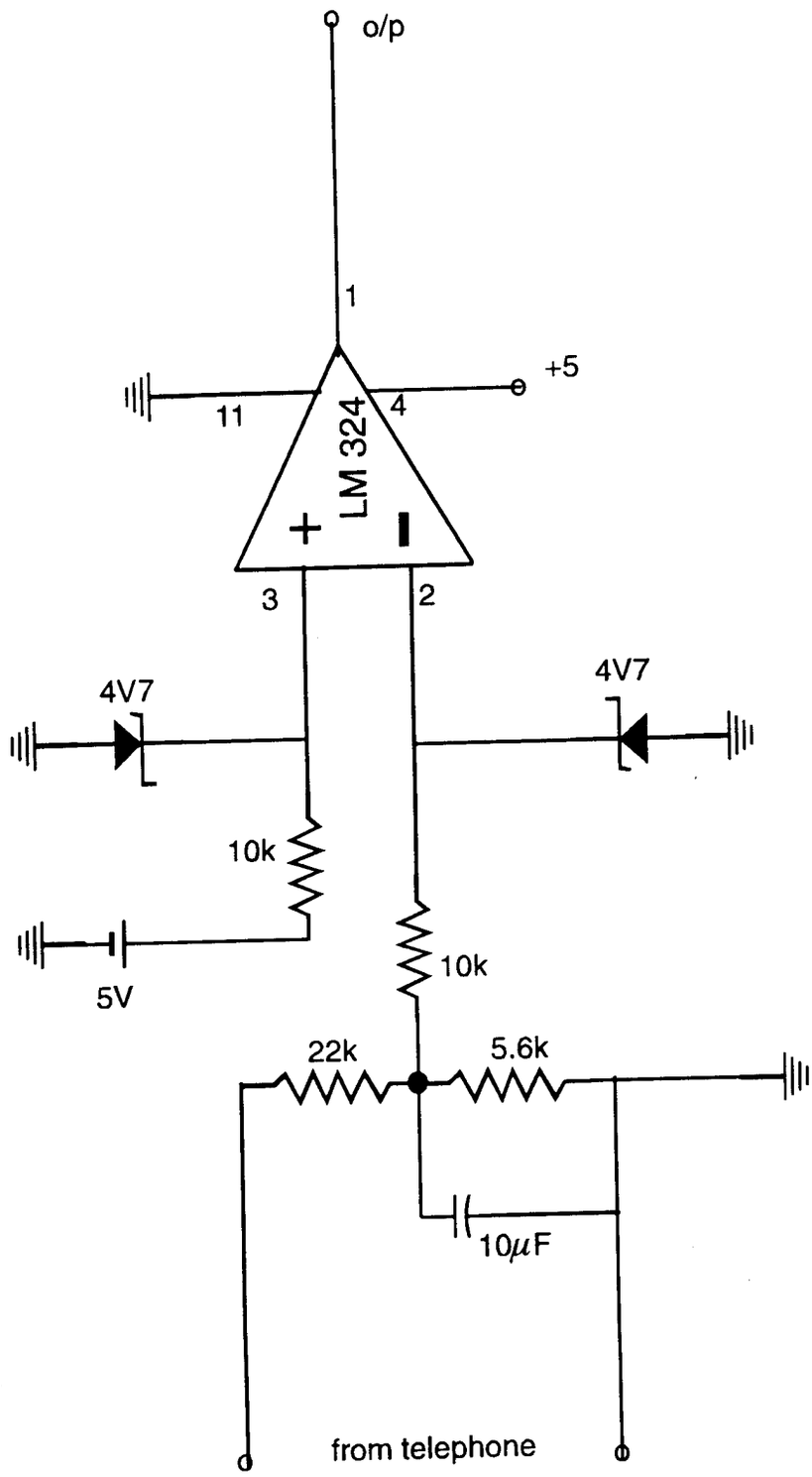
$$= 0.869 \times 10^{-3} \times 5.6 \times 10^{3}$$

$$Vin = 4.86V$$

$$Vref = 3.7V$$

Since the inverting input is greater than the non-inverting input the output is -Vcc which is 0V.

OFF - HOOK DETECTION



OFF-HOOK CONDITION:-

In Off-hook condition the telephone draws around 40 mA current and hence voltage drops to 12V.The voltage applied to the inverting input is

$$I = V/R = \frac{12}{22K + 5.6K} = 0.434mA$$

$$V = IR = 0.434 \times 10^{-3} \times 5.6k$$

Vin =2.43V

Vref =3.7V

Here Vref > Vin. Therefore the output of the comparator is +Vcc which is 5V.

A capacitor of value 10micro farad is connected at the input of the OP-amp to bypass the ac signal to ground which is coming from the ring supply;otherwise the ac signal are super-imposed on dc.

OFF-HOOK DECISION:-

Whenever a ring comes, the call is immediately accepted as the off-hook simulator presents a load of 600 ohm across the exchange lines,drawing a current of 40 mA. This load has to be removed from the exchange on two conditions,

1. Whenever any one of the telephone among the parallel array of telephones is off-hook.

2. If nobody is there to receive the call,then after 1minute the load is to be removed.

The first condition is tested by OR' -ing the output of off-hook decision of each of the telelphone. If any one telephone is off-hook then the output of the OR-gate is 1. This is given to an AND gate the output of AND gate is 1 during the1 minute, thus flip flop 1 is reset.The output of OR gate is also given to the invertor i.e, to the base of the transistor,thus 600 ohm is removed from the exchange, as the relay is de-energised.

For the second condition, if nobody has gone off-hook after 1minute,output of inverter is 1, thus reset input is 1 and the flip flop is reset and load 600 ohm is removed from the exchange.

RELAY DRIVING NETWORK:-

The maximum output current of the 74LS148 multiplexer is only 50 mA which is not enough to drive the relay. So this current has to be amplified before giving to the relay and this is done by the transistor MPSA44 which is a high voltage NPN transistor.The output of 74LS148 is therefore given to the base of this transistor through a 5.6.k resistor.

The transistor is driven into saturation when the input is 5V. Therefore maximum current flows in the collector arm which is 300 mA thus enough to drive the relay.

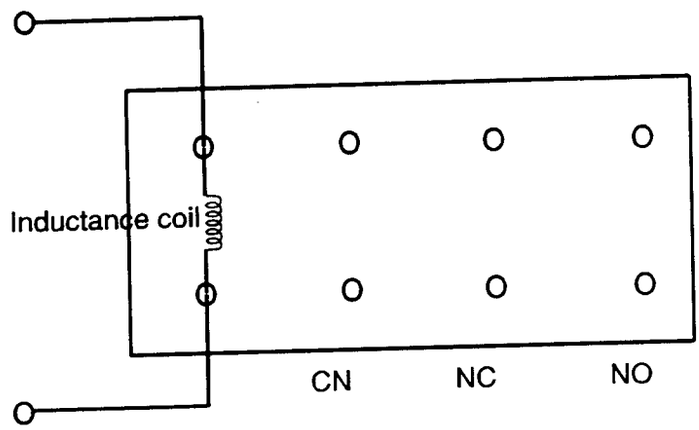
In designing the modern general purpose telephone relay, the main consideration has been the normal switching requirements met within automatic telephone exchanges. Thus neither a high degree of sensitivity nor very high speed of operation is required while high voltage and current have not to be catered for, and except in certain cases a high degree of precision in the timing of relay operation is not called for. What is principally needed is a robust relay of straight forward design capable of simple maintenance in sites and giving reliable operation over long periods of time. In addition, in view of the large numbers required in automatic exchanges the relay need to be compact and require little mounting space and to be relatively cheap to manufacture.

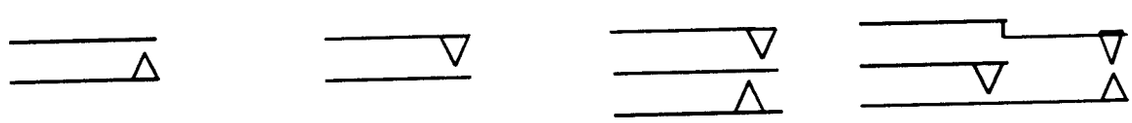
There are mainly four types of contacts in the relays. They are:-

1. Make contact :-In this the contacts which are normaly broken, are made when the relay is operated.
2. Break contact :- These are normally made contacts that are broken by the operation of the relay.
3. Change over contacts :- In this the movable contacts while changing over its position by the operation of the relay breaks with one contact and makes with the other.
4. Make before - Break contact :- When the relay is operated, one normally broken contact is first made and then only a second normally made contact is broken.

The relay we use in our system is of the latest fast operating type of relay and is much compact. It is represented as follows.

RELAY CONNECTIONS





(a) (b) (c) (d)

There are three contact points. They are common (CN), normally closed (NC) and normally open (NO). Initially there is contact between the common point and the normally closed. When the relay coil is energised the contact between common and the normally open is made. These relays are used here to establish connections and provide ring voltage whenever necessary depending on the output of the multiplexer. These relays are also used in the off-hook simulator and hold on music in order to prevent current drawn by the exchange.

POWER SUPPLY ARRANGEMENTS :-

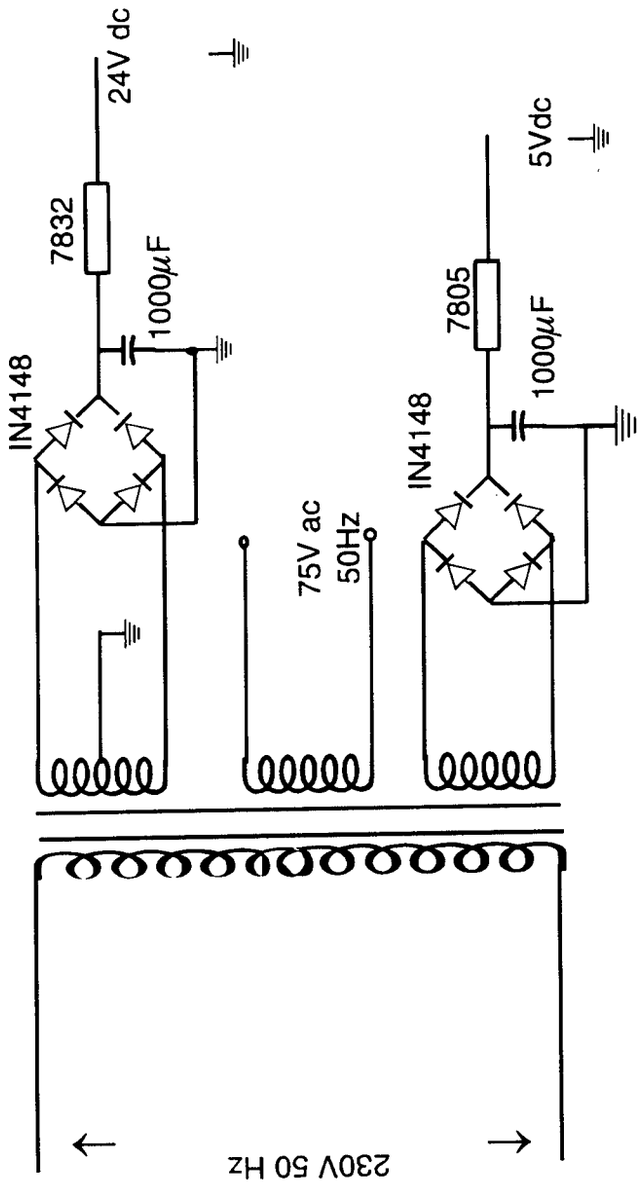
Since all the integrated circuits, transistors, relays etc. used in the circuits require power for its operation which is normally 5V, it has to be provided by an external supply, generally from the mains. A step down transformer is used, the primary of which is connected to the mains i.e, 220V.

A 75V ac supply is required to provide ring voltage to the parallelly connected telephones, whenever that particular telephone is called. This voltage is also obtained from the secondary of the same transformer.This 75V ac is cut off as soon as the system goes off-hook.

A 24 V dc supply is also provided across each telephone and the common point of the relay. This 24V dc supply is provided from the output of the transformer. Since the output of the transformer provides only ac, a bridge rectifier arrangement is used at the output

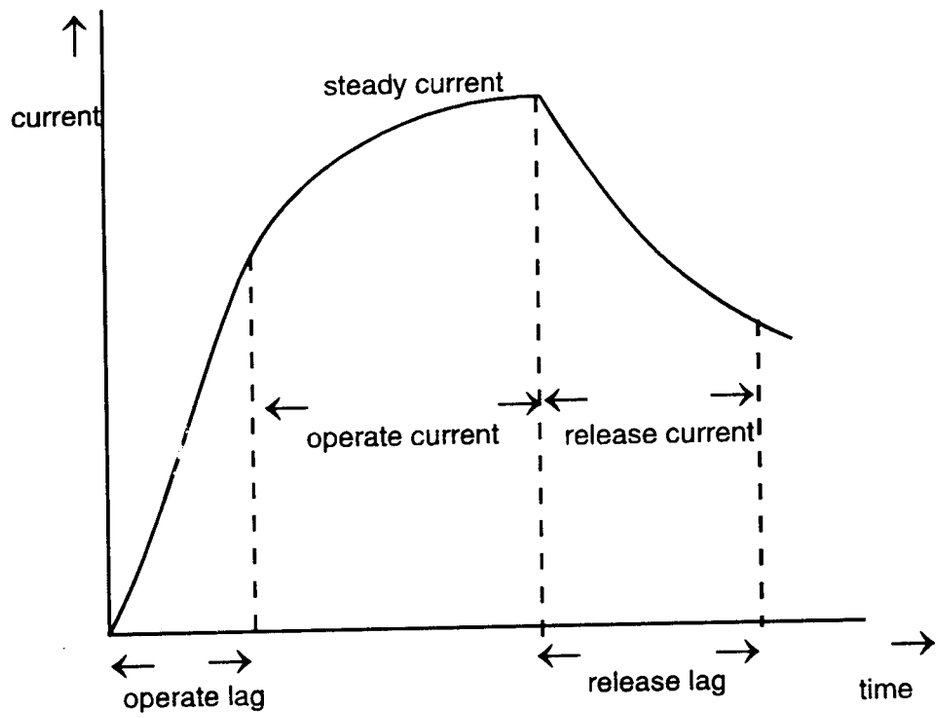
of which a dc is obtained.

The transformer providing the power supply is as shown below.



EFFECT OF COIL INDUCTANCE ON THE RELAY OPERATION:-

The minimum current at which the relay is just operated is known as the operate current and the maximum current at which the relay is just released is known as Release current.Two other currents in connection with the relay operation are known as non - operate current and hold current.



Owing to the appreciable inductance due to large number of turns of relay coil, the current in the relay coil takes some time to reach its maximum steady value and it varies exponentially as shown

may be too low to operate the transmitter efficiently and for very short lines it may have abnormally high value. The variation of current with line resistance is compensated to some extent by using resistors in series with the impedance coils of the bridges and thus working length of line is increased.

Apart from its effect on the dc line current, the transmission bridge along with the lines effects the frequency transmission characteristic to a large extent. It behaves like a band pass filter and both very low and very high frequencies are attenuated.

Here in our system the feed bridge arrangement consists of a coil, resistor and diode connected back to back to prevent the a.c speech current from reaching the other telephones while one telephone is off-hook thereby maintaing secrecy. This feed bridge arm prevents the current flowing fromthe internal supply to the exchange and vice versa in case of use of a common 24V power supply.

CONCLUSION

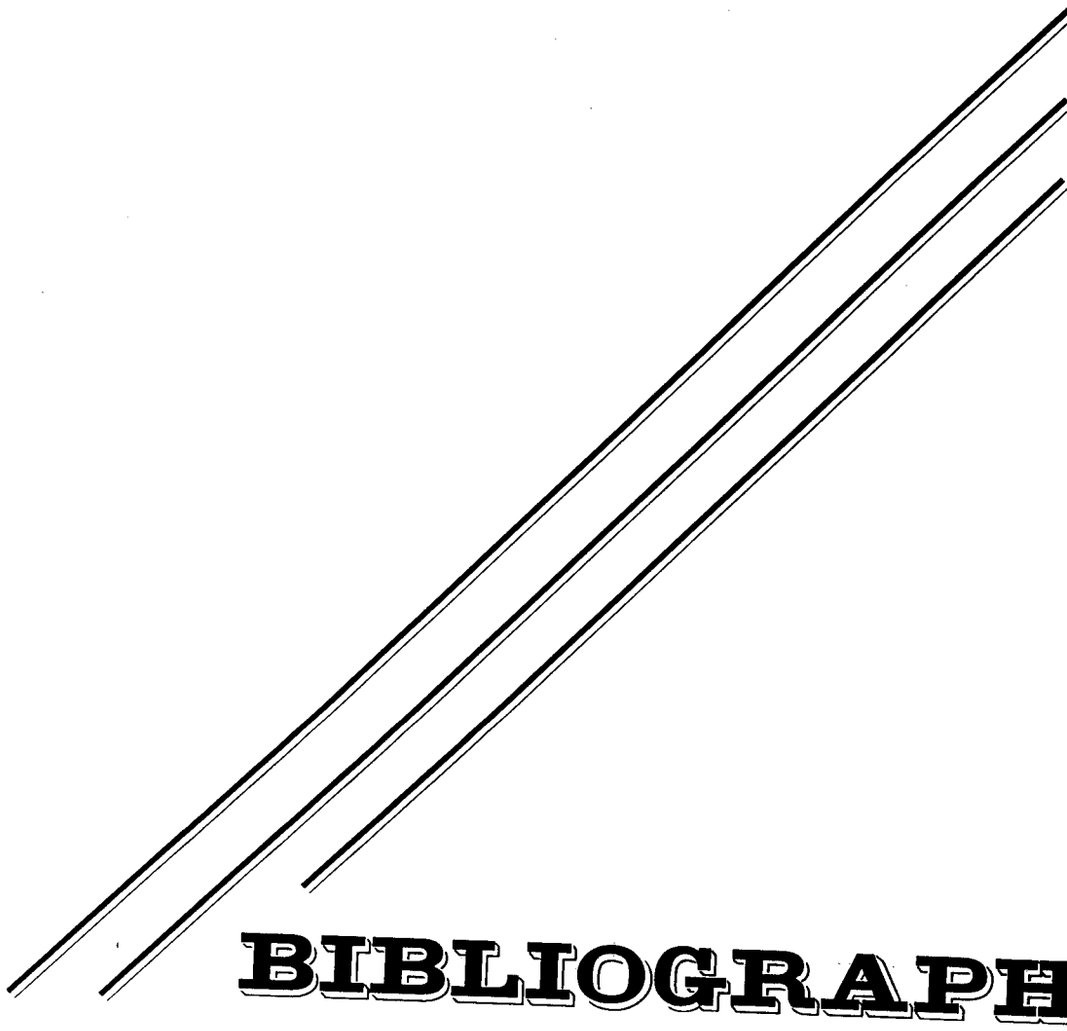
CONCLUSION

The project "SECRECY IN PARALLEL TELEPHONES"has been designed, fabricated and tested to confirm to the target specifications.

Details about the IC chips, the configurations,operational characteristics of all the chips used in implementing the hardware has also been explained.

There are also provisions for future developments such as call transfer facility. With some specifications in the circuit, the # button can be used for call transfer. At present there is manual call transfer.

This project can be used in large industries, educational institutions, stock markets and the unique feature of this project is that any number of telephones can be connected to our system as required by the user. What has been achieved through the project can at best be a techno-compromise to give an optimum performance.



BIBLIOGRAPHY

BIBLIOGRAPHY

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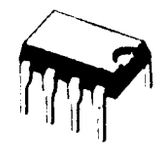
APPENDIX

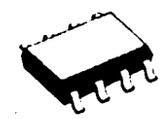
ELECTRONIC TWO - TONE RINGER

- LOW CURRENT CONSUMPTION, IN ORDER TO ALLOW THE PARALLEL OPERATION OF 4 DEVICES
- INTEGRATED RECTIFIER BRIDGE WITH ZENER DIODES TO PROTECT AGAINST OVERVOLTAGES
- LITTLE EXTERNAL CIRCUITRY
- TONE AND SWITCHING FREQUENCIES ADJUSTABLE BY EXTERNAL COMPONENTS
- INTEGRATED VOLTAGE AND CURRENT HYSTERESIS

MINIDIP



SO-8J



ORDER CODES :

Minidip	SO-8
LS1240 LS1240A	LS1240D1 LS1240AD1

DESCRIPTION

LS1240 and LS1240A are monolithic integrated circuits designed to replace the mechanical bell in telephone sets in connection with an electro-acoustical converter. Both devices can drive directly a piezoceramic converter (buzzer).

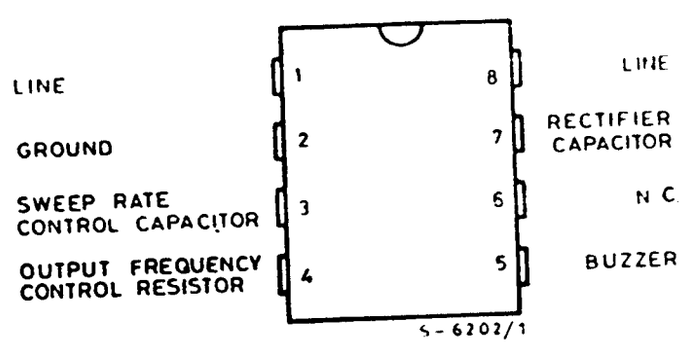
The output current capability of LS1240A is higher than LS1240. For driving a dynamic loudspeaker LS1240 needs a transformer, while LS1240A, needs a decoupling capacitor.

No current limitation is provided on the output stage of LS1240A, so a minimum load DC of 50 Ω is adviced.

The two tone frequencies generated are switched by an internal oscillator in a fast sequence and made audible across an output amplifier in the loudspeaker, both tone frequencies and the switching frequency can be externally adjusted.

The supply voltage is obtained from the AC ring signal and the circuit is designed so that noise on the line or variations of the ringing signal cannot affect correct operation of the device.

PIN CONNECTION (top view)



BLOCK DIAGRAM

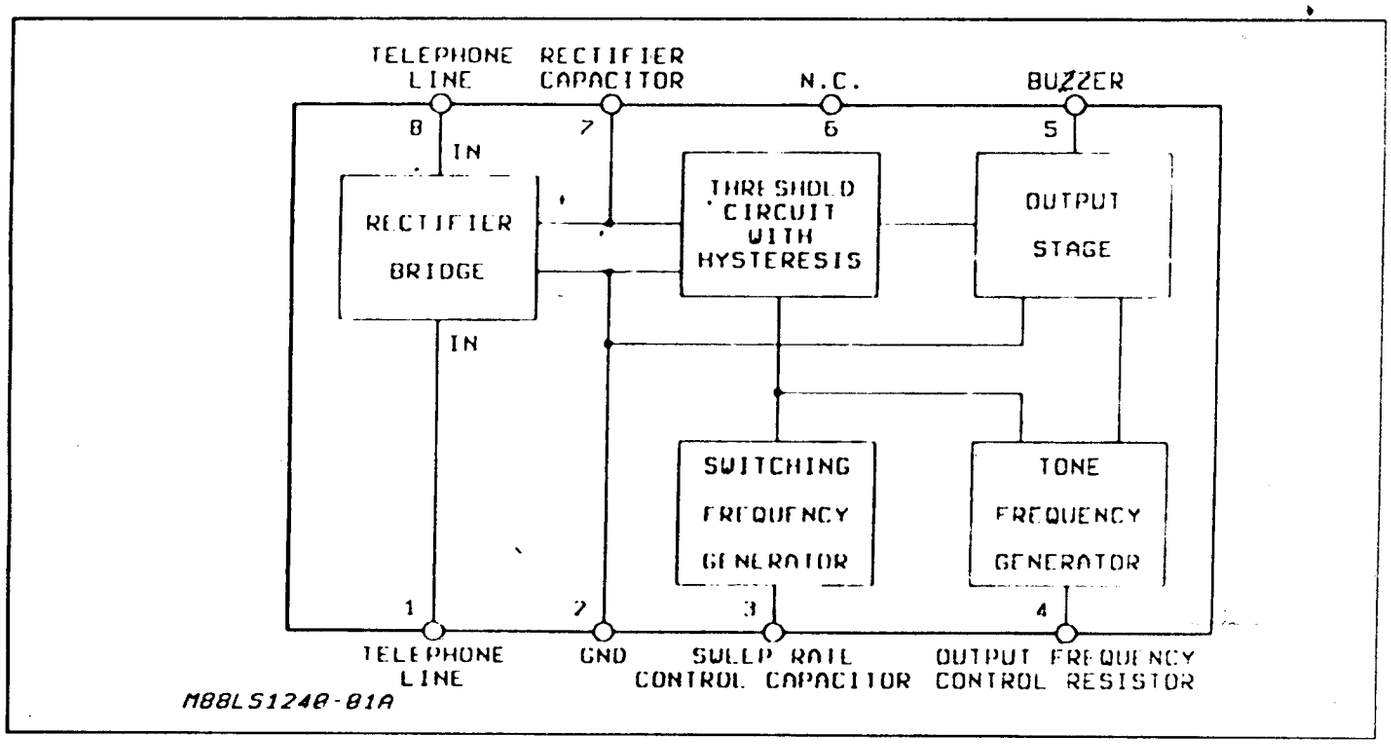
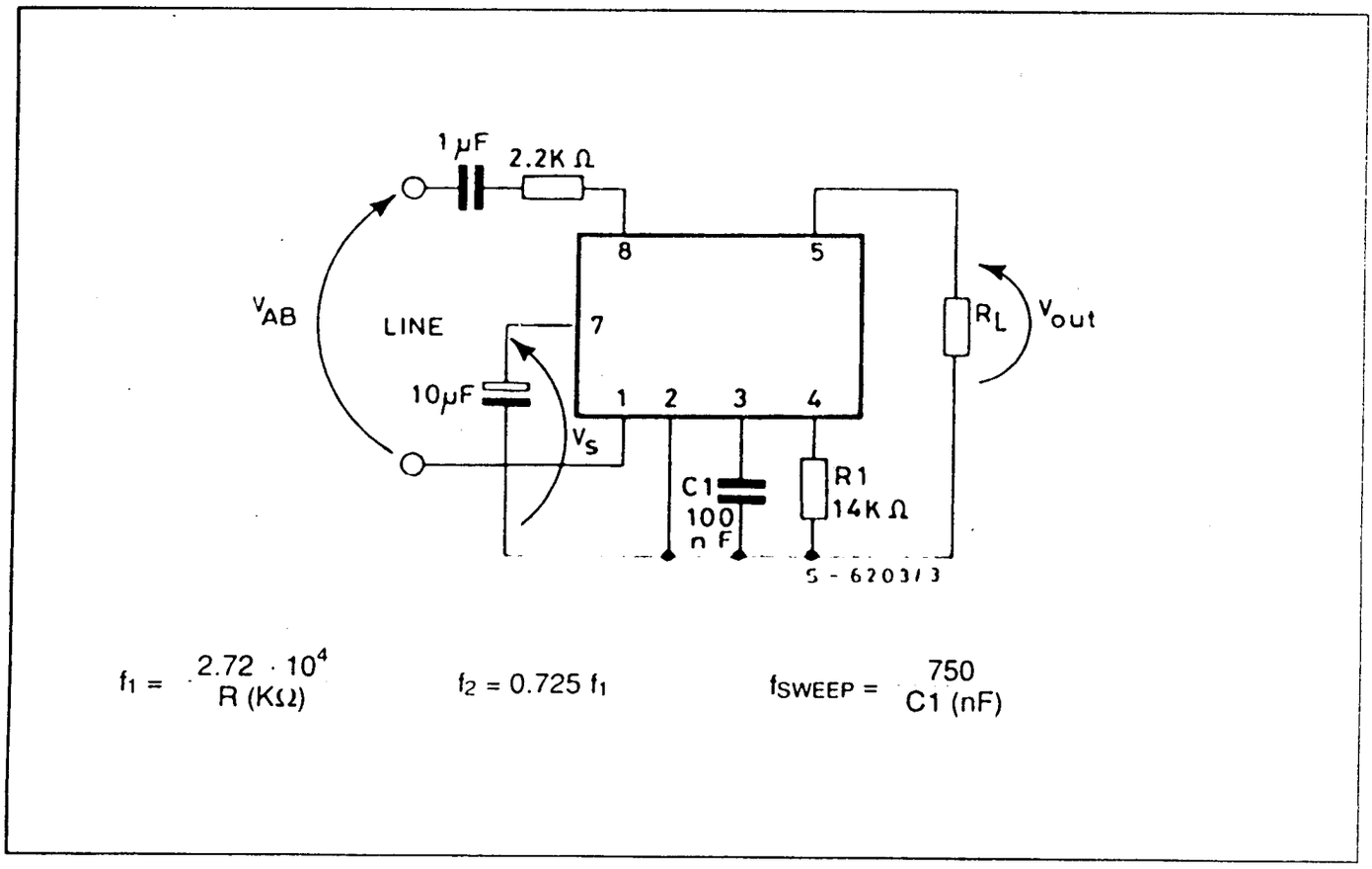


Figure 1 : Test Circuit.



$f_1 = \frac{2.72 \cdot 10^4}{R\ (K\Omega)}$ $\quad f_2 = 0.725\ f_1$ $\quad f_{SWEEP} = \frac{750}{C1\ (nF)}$

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{AB}	Calling Voltage (f = 50 Hz) Continuous	120	V_{rms}
V_{AB}	Calling Voltage (f = 50 Hz) 5s ON/10s OFF	200	V_{rms}
DC	Supply Current	30	mA
T_{op}	Operating Temperature	– 20 to + 70	°C
T_{stg}	Storage and Junction Temperature	– 65 to + 150	°C

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	100	°C/W

ELECTRICAL CHARACTERISTICS

(T_{amb} = 25 °C; V_s = applied between pins 7-2 unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply Voltage				26	V
I_B	Current Consumption without Load (pins 8-1)	V_s = 9.3 to 25 V		1.5	1.8	mA
V_{ON}	Activation Voltage **LS1240** **LS1240A**		12.2 12		13.2 13.5	V V
V_{OFF}	Sustaining Voltage **LS1240** **LS1240A**		8 7.8		9 9.3	V V
R_D	Differential Resistance in OFF Condition (pins 8-1)		6.4			KΩ
V_{OUT}	Output Voltage Swing			V_s – 5		V
I_{OUT}	Short Circuit Current (pins 5-2) **LS1240** **LS1240A**	V_s = 20 V R_L = 0 Ω R_L = 250 Ω		35 70		mA mA

AC OPERATION

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
f_1 f_2	Output Frequencies f_{out1} f_{out2}	V_s = 26 V R_1 = 14 KΩ V_s = 0 V V_s = 6 V	1.74 1.22		2.14 1.6	KHz
	$\frac{f_{out1}}{f_{out2}}$		1.33		1.43	
	Programming Resistor Range		8		56	KΩ
f_{SWEEP}	Sweep Frequency	R_1 = 14 KΩ C_1 = 100 nF	5.25	7.5	9.75	Hz

Figure 2 : Typical Application for LS1240.

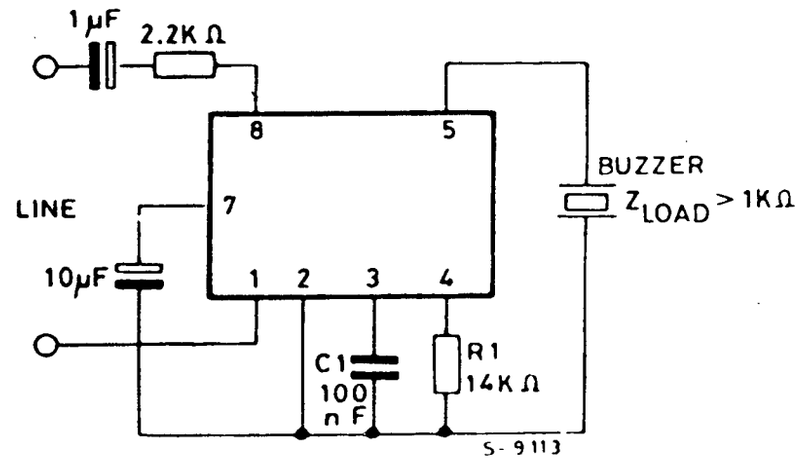
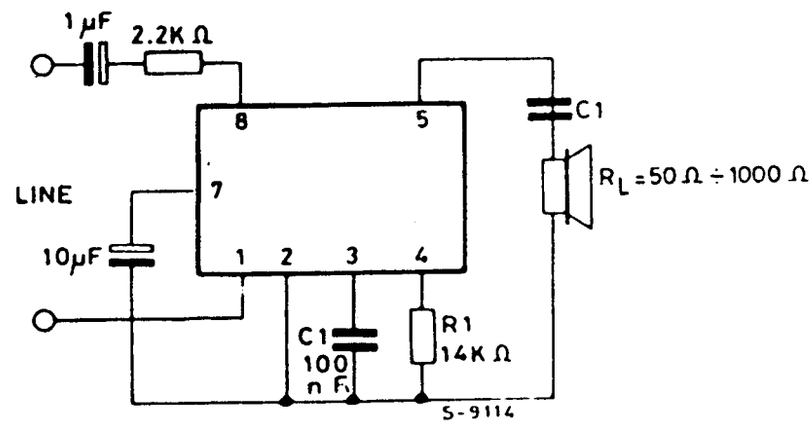


Figure 3 : Typical Application for LS1240A.



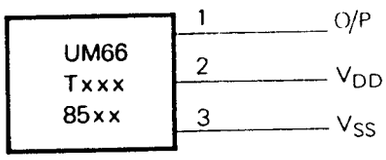
C_1 such that $|Z_{LOAD}| > 1\ K\Omega$

UM66T Series Simple Melody Generator

Features

- 64-note ROM memory
- 1.3V to 3.3V operating voltage and low power consumption
- Dynamic speaker can be driven with an external NPN transistor
- OSC. resistor is built-in
- One-shot mode or level-hold mode can be selected
- Power on reset; melody begins from the first note
- Direct piezo drive
- Packaged in inexpensive TO-92 package

Pin Configuration

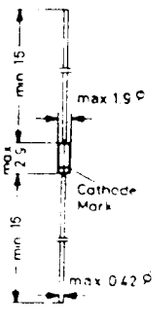


1N4148

Silicon Epitaxial Planar Diode
fast switching diode.

This type in case DO-35 is also available to specification **CECC 50.001.023**

This diode is also available in glass case DO-34



These diodes are delivered taped.
Details see "Taping".

Glass case JEDEC DO-35
54 A 2 according to DIN 41880

Weight approx. 0.13 g
Dimensions in mm

These diodes are available branded in clear text or in international color code

Glass case JEDEC DO-3[illegible]

Weight approx. 0.1 g
Dimensions in mm

branded on reel or AMMOPAK

Absolute Maximum Ratings

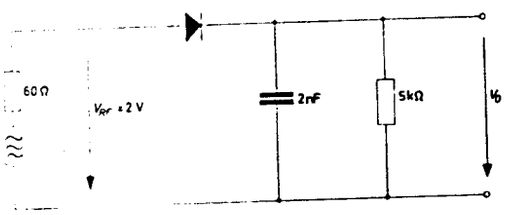
		Symbol	Value	Unit
Reverse Voltage		V_R	75	V
Peak Reverse Voltage		V_{RM}	100	V
Rectified Current (Average) Half Wave Rectification with Resist. Load at T_{amb} = 25 °C and f ≥ 50 Hz		I_0	150[1]	mA
Surge Forward Current at t < 1 s and T_j = 25 °C		I_{FSM}	500	mA
Power Dissipation at T_{amb} = 25 °C	case DO-35	P_{tot}	500[1]	mW
Power Dissipation at T_{amb} = 25 °C	case DO-34	P_{tot}	300[1]	mW
Junction Temperature	case DO-35	T_j	200	°C
Junction Temperature	case DO-34	T_j	175	°C
Storage Temperature Range	case DO-35	T_S	−65 to +200	°C
Storage Temperature Range	case DO-34	T_S	−65 to +175	°C

[1] Valid provided that leads at a distance of 8 mm from case are kept at ambient temperature.

Characteristics at $T_j = 25$ °C

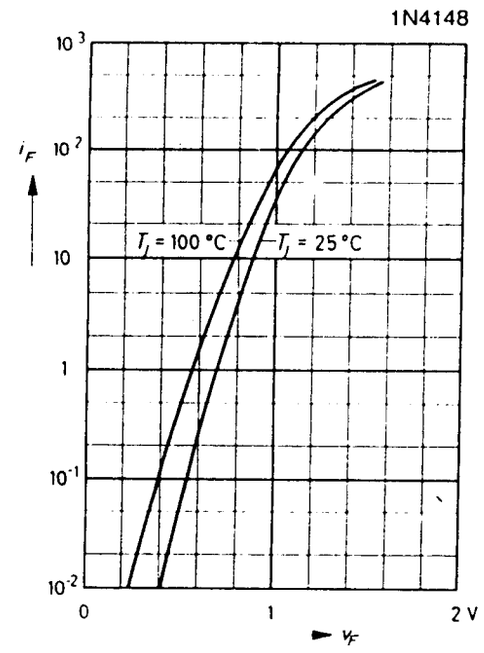
	Symbol	Min.	Typ.	Max.	Unit
Forward Voltage at $I_F = 10$ mA	V_F	–	–	1	V
Leakage Current at $V_R = 20$ V at $V_R = 75$ V at $V_R = 20$ V, $T_j = 150$ °C	I_R I_R I_R	– – –	– – –	25 5 50	nA µA µA
Reverse Breakdown Voltage tested with 100 µA Pulses	$V_{(BR)R}$	100	–	–	V
Capacitance at $V_F = V_R = 0$	C_{tot}	–	–	4	pF
Voltage Rise when Switching ON tested with 50 mA Forward Pulses $t_p = 0.1$ µs, Rise Time < 30 ns, $f_p = 5$ to 100 kHz	V_{fr}	–	–	2.5	V
Reverse Recovery Time from $I_F = 10$ mA to $I_R = 1$ mA, $V_R = 6$ V, $R_L = 100\ \Omega$	t_{rr}	–	–	4	ns
Thermal Resistance Junction to Ambient Air case DO-35	R_{thA}	–	–	0.35[1]	K/mW
Thermal Resistance Junction to Ambient Air case DO-34	R_{thA}	–	–	0.4[1]	K/mW
Rectification Efficiency at f = 100 MHz, $V_{RF} = 2$ V	η_V	0.45	–	–	–

[1] Valid provided that leads at a distance of 8 mm from case are kept at ambient temperature.

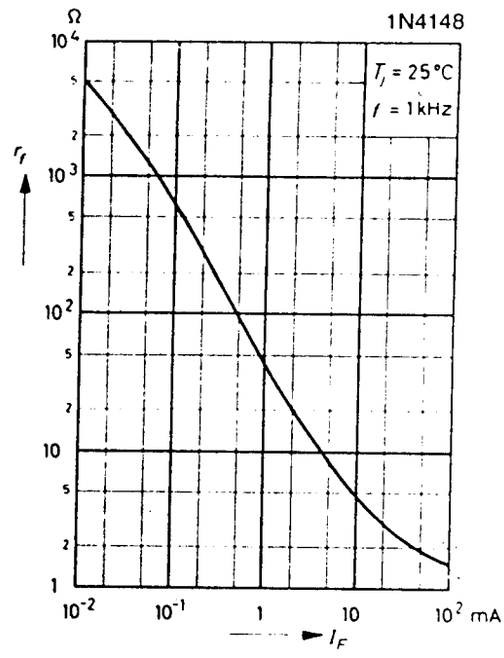


Rectification Efficiency Measurement Circuit

Forward characteristics

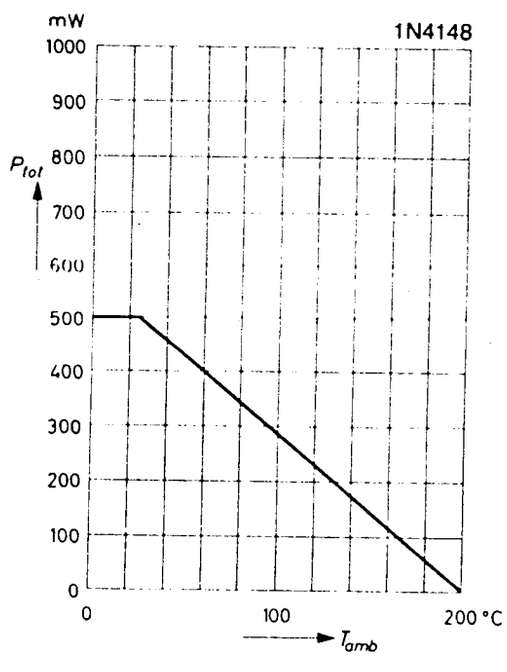


Dynamic forward resistance versus forward current

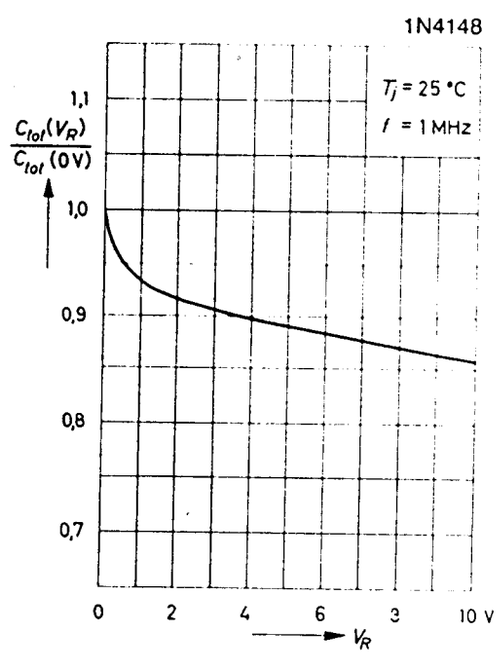


Admissible power dissipation versus ambient temperature (case DO-35)

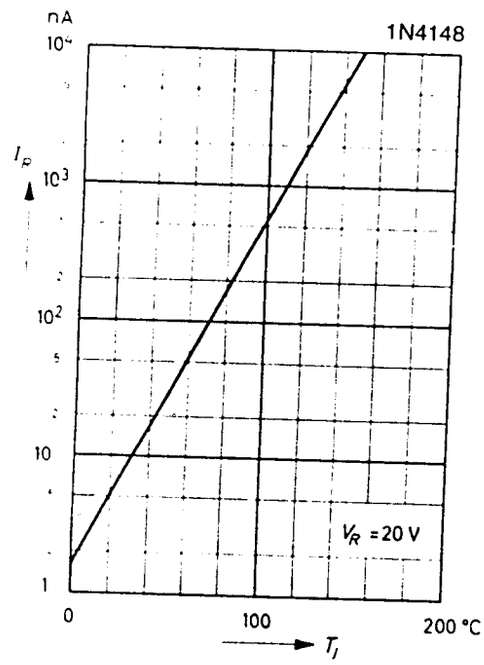
Valid provided that leads at a distance of 8 mm from case are kept at ambient temperature



Relative capacitance versus reverse voltage

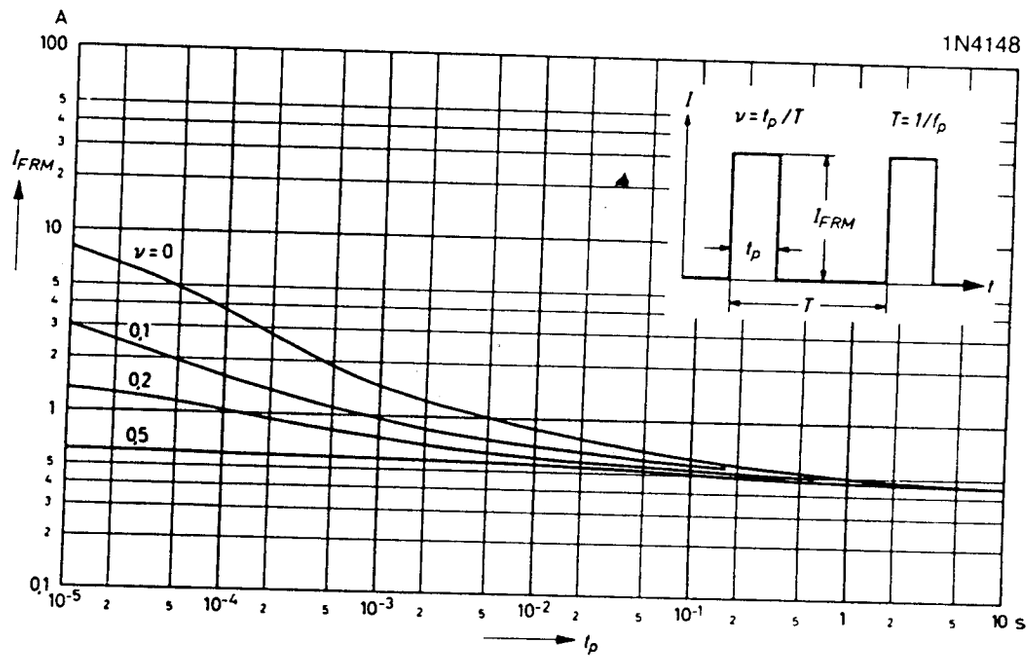


Leakage current versus junction temperature



Admissible repetitive peak forward current versus pulse duration (case DO-35)

Valid provided that leads at a distance of 8 mm from case are kept at ambient temperature

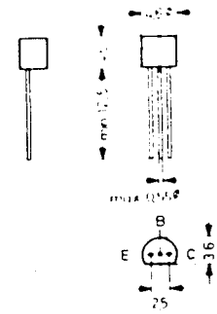


BC546 ... BC550

NPN Silicon Epitaxial Planar Transistors
for switching and AF amplifier applications.

These transistors are subdivided into three groups A, B and C according to their current gain. The type BC546 is available in groups A and B, however, the types BC547 and BC548 can be supplied in all three groups. The BC549 and BC550 are low noise types and available in groups B and C. As complementary types the PNP transistors BC556 ... BC560 are recommended.

On special request these transistors are also manufactured in the pinconfiguration TO-18.



Plastic package 10D3
according to DIN 41870 (≈ TO-92)
The case is impervious to light

Weight approximately 0.18 g
Dimensions in mm

Absolute Maximum Ratings

		Symbol	Value	Unit
Collector Base Voltage	**BC546**	V_{CBO}	80	V
	BC547, BC550	V_{CBO}	50	V
	BC548, BC549	V_{CBO}	30	V
Collector Emitter Voltage	**BC546**	V_{CES}	80	V
	BC547, BC550	V_{CES}	50	V
	BC548, BC549	V_{CES}	30	V
Collector Emitter Voltage	**BC546**	V_{CEO}	65	V
	BC547, BC550	V_{CEO}	45	V
	BC548, BC549	V_{CEO}	30	V
Emitter Base Voltage	**BC546, BC547**	V_{EBO}	6	V
	BC548, BC549	V_{EBO}	5	V
	BC550			
Collector Current		I_C	100	mA
Peak Collector Current		I_{CM}	200	mA
Peak Base Current		I_{BM}	200	mA
Peak Emitter Current		$-I_{EM}$	200	mA
Power Dissipation at T_{amb} = 25 °C		P_{tot}	500[1]	mW
Junction Temperature		T_j	150	°C
Storage Temperature Range		T_S	−65 ... +150	°C

[1] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case

Characteristics at T_{amb} = 25 °C

		Symbol	Min.	Typ.	Max.	Unit
h-Parameters at V_{CE} = 5 V, I_C = 2 mA, f = 1 kHz						
Small Signal Current Gain	**Current Gain Group A**	h_{fe}	–	220	–	–
	B	h_{fe}	–	330	–	–
	C	h_{fe}	–	600	–	–
Input Impedance	**Current Gain Group A**	h_{ie}	1.6	2.7	4.5	kΩ
	B	h_{ie}	3.2	4.5	8.5	kΩ
	C	h_{ie}	6	8.7	15	kΩ
Output Admittance	**Current Gain Group A**	h_{oe}	–	18	30	μS
	B	h_{oe}	–	30	60	μS
	C	h_{oe}	–	60	110	μS
Reverse Voltage Transfer Ratio						
	Current Gain Group A	h_{re}	–	$1.5 \cdot 10^{-4}$	–	–
	B	h_{re}	–	$2 \cdot 10^{-4}$	–	–
	C	h_{re}	–	$3 \cdot 10^{-4}$	–	–
DC Current Gain						
at V_{CE} = 5 V, I_C = 10 μA	**Current Gain Group A**	h_{FE}	–	90	–	–
	B	h_{FE}	–	150	–	–
	C	h_{FE}	–	270	–	–
at V_{CE} = 5 V, I_C = 2 mA	**Current Gain Group A**	h_{FE}	110	180	220	–
	B	h_{FE}	200	290	450	–
	C	h_{FE}	420	500	800	–
at V_{CE} = 5 V, I_C = 100 mA	**Current Gain Group A**	h_{FE}	–	120	–	–
	B	h_{FE}	–	200	–	–
	C	h_{FE}	–	400	–	–
Thermal Resistance Junction to Ambient		R_{thJA}			250 [1]	K/W
Collector Saturation Voltage						
at I_C = 10 mA, I_B = 0.5 mA		V_{CEsat}	–	80	200	mV
at I_C = 100 mA, I_B = 5 mA		V_{CEsat}	–	200	600	mV
Base Saturation Voltage						
at I_C = 10 mA, I_B = 0.5 mA		V_{BEsat}	–	700	–	mV
at I_C = 100 mA, I_B = 5 mA		V_{BEsat}	–	900	–	mV
Base Emitter Voltage						
at V_{CE} = 5 V, I_C = 2 mA		V_{BE}	580	660	700	mV
at V_{CE} = 5 V, I_C = 10 mA		V_{BE}	–	–	720	mV
Collector Cutoff Current						
at V_{CE} = 80 V	**BC546**	I_{CES}	–	0.2	15	nA
at V_{CE} = 50 V	**BC547, BC550**	I_{CES}	–	0.2	15	nA
at V_{CE} = 30 V	**BC548, BC549**	I_{CES}	–	0.2	15	nA
at V_{CE} = 80 V, T_j = 125 °C	**BC546**	I_{CES}	–	–	4	μA
at V_{CE} = 50 V, T_j = 125 °C	**BC547, BC550**	I_{CES}	–	–	4	μA
at V_{CE} = 30 V, T_j = 125 °C	**BC548, BC549**	I_{CES}	–	–	4	μA
at V_{CB} = 30 V		I_{CBO}	–	–	15	nA
at V_{CB} = 30 V, T_j = 150 °C		I_{CBO}	–	–	5	μA
Gain Bandwidth Product at V_{CE} = 5 V, I_C = 10 mA, f = 100 MHz		f_T	–	300	–	MHz
Collector Base Capacitance at V_{CB} = 10 V, f = 1 MHz		C_{CBO}	–	3.5	6	pF

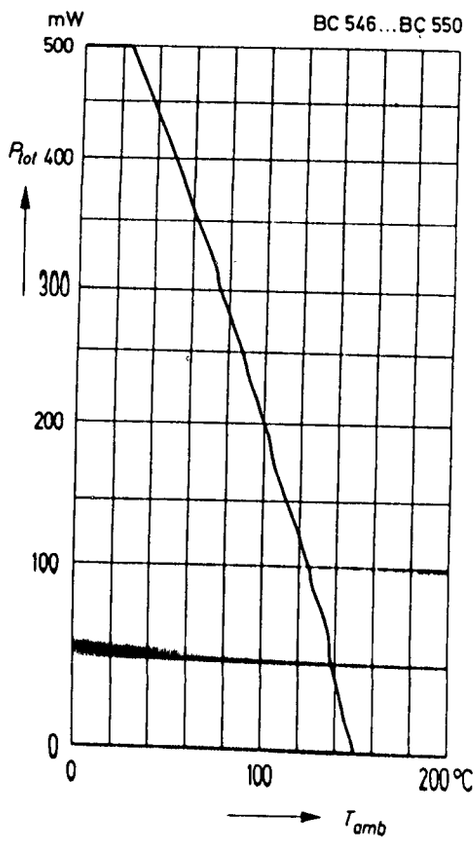
[1] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case

Characteristics, continuation

	Symbol	Min.	Typ.	Max.	Unit
Emitter Base Capacitance at V_{EB} = 0.5 V, f = 1 MHz	C_{EBO}	–	9	–	pF
Noise Figure at V_{CE} = 5 V, I_C = 200 μA, R_G = 2 kΩ, f = 1 kHz, Δf = 200 Hz **BC546, BC547, BC548** **BC549, BC550** at V_{CE} = 5 V, I_C = 200 μA, R_G = 2 kΩ, f = 30 . . . 15000 Hz **BC549** **BC550**	 F F F F	 – – – –	 2 1.2 1.4 1.4	 10 4 4 3	 dB dB dB dB
Equivalent Noise EMF at V_{CE} = 5 V, I_C = 200 μA, R_G = 2 kΩ, f = 10 . . . 50 Hz **BC550**	v_r	–	–	0.135	μV

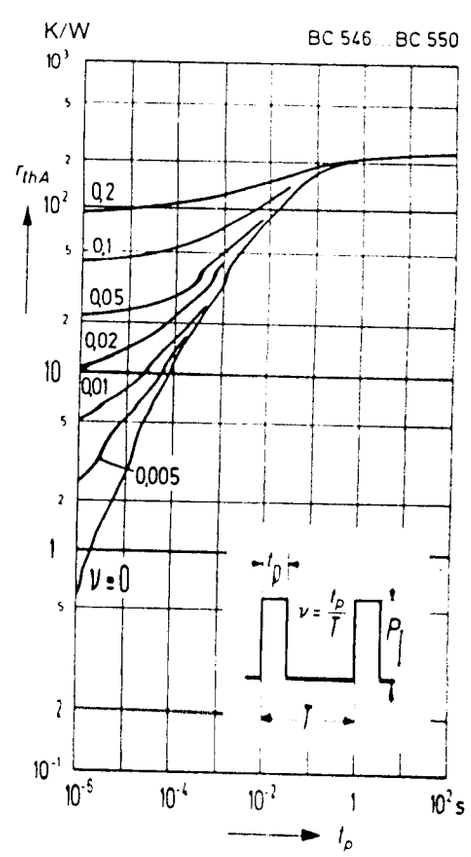
Admissible power dissipation versus temperature

Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case

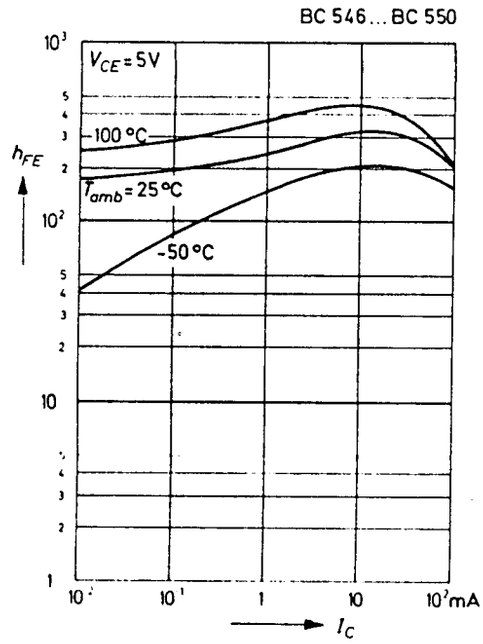


Pulse thermal resistance versus pulse duration

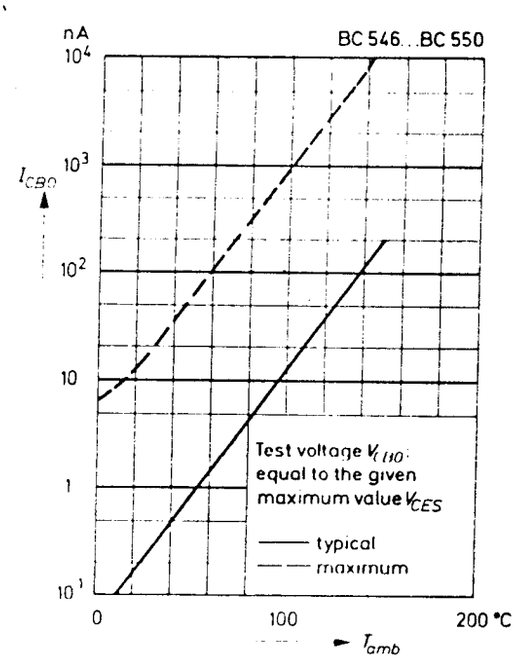
Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case



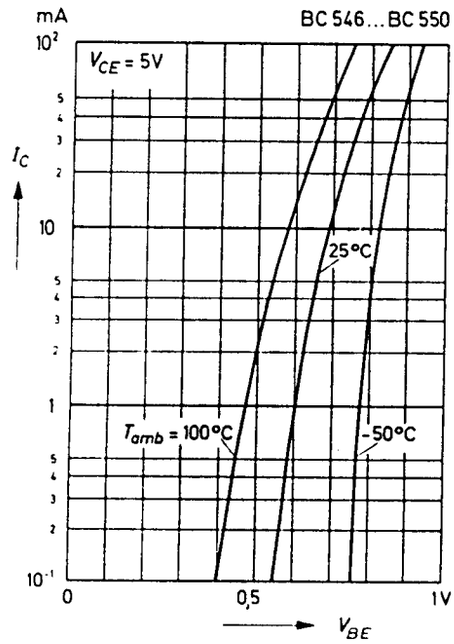
DC current gain versus collector current



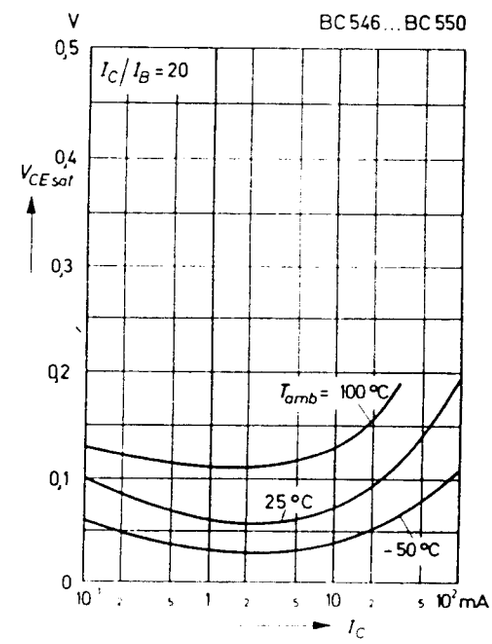
Collector cutoff current versus ambient temperature



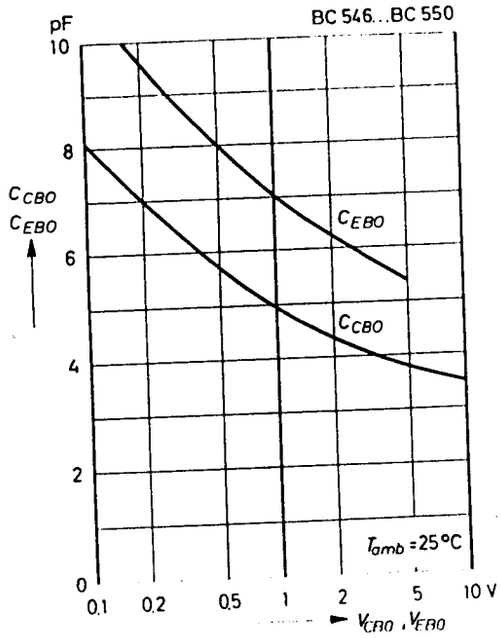
Collector current versus base emitter voltage



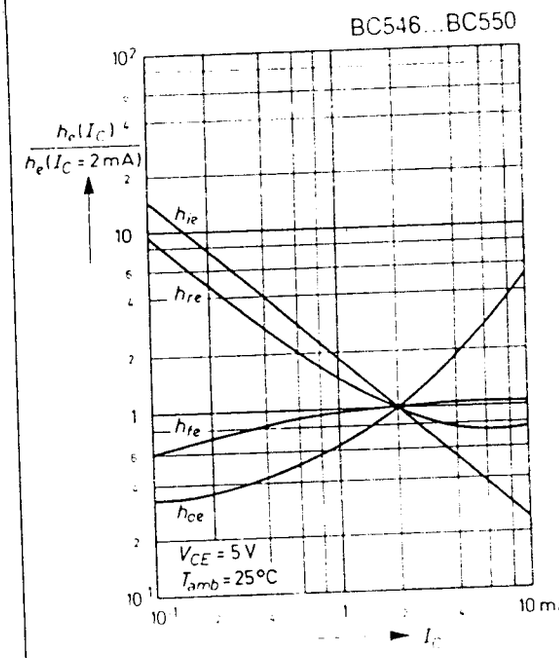
Collector saturation voltage versus collector current



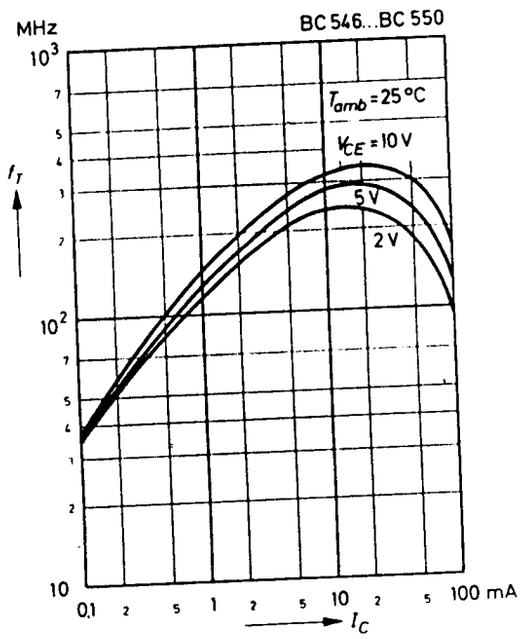
Collector base capacitance, Emitter base capacitance versus reverse bias voltage



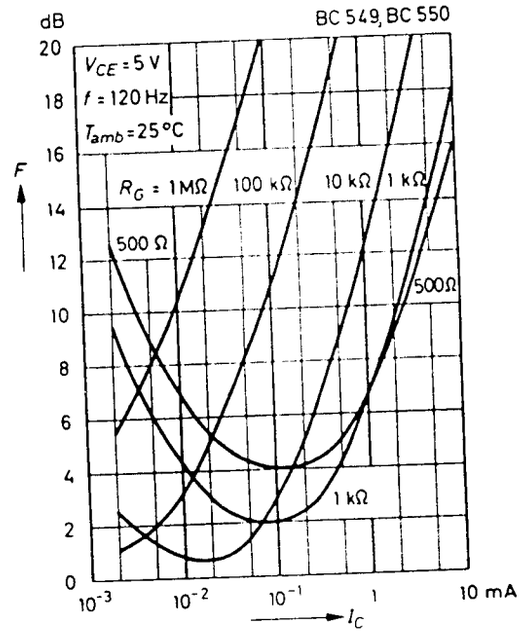
Relative h-parameters versus collector current



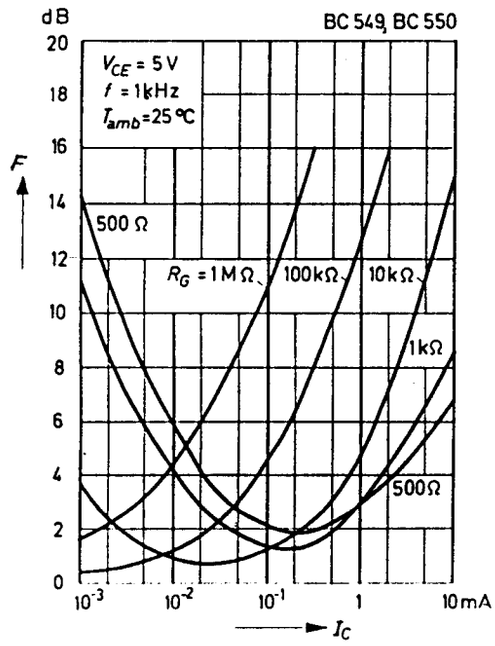
Gain bandwidth product versus collector current



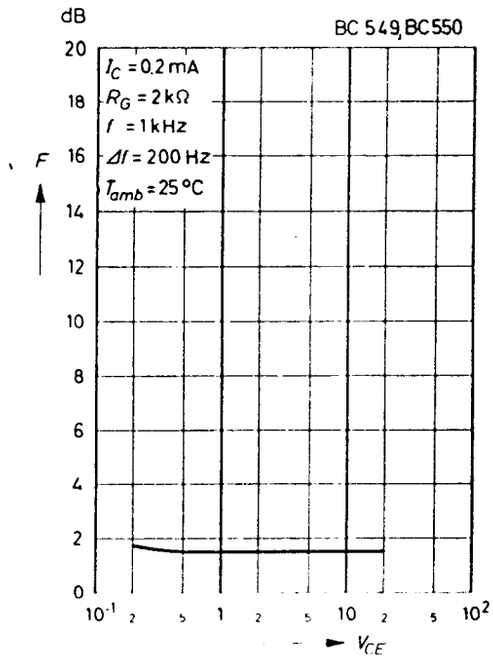
Noise figure versus collector current



Noise figure
versus collector current

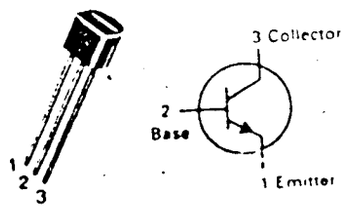


Noise figure
versus collector emitter voltage



MPSA44
MPSA45

CASE 29-04, STYLE 1
TO-92 (TO-226AA)



HIGH VOLTAGE TRANSISTOR

NPN SILICON

MAXIMUM RATINGS

Rating	Symbol	MPSA44	MPSA45	Unit
Collector-Emitter Voltage	V_{CEO}	400	350	Vdc
Collector-Base Voltage	V_{CBO}	500	400	Vdc
Emitter-Base Voltage	V_{EBO}	6.0	6.0	Vdc
Collector Current — Continuous	I_C	300		mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	625 5.0		mW mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	1.5 12		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	83.3	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	200	°C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Breakdown Voltage(1) (I_C = 1.0 mAdc, I_B = 0)	MPSA44 MPSA45	$V_{(BR)CEO}$	400 350	— —	Vdc
Collector-Emitter Breakdown Voltage (I_C = 100 μAdc, V_{BE} = 0)	MPSA44 MPSA45	$V_{(BR)CES}$	500 400	— —	Vdc
Collector-Base Breakdown Voltage (I_C = 100 μAdc, I_E = 0)	MPSA44 MPSA45	$V_{(BR)CBO}$	500 400	— —	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)		$V_{(BR)EBO}$	6.0	—	Vdc
Collector Cutoff Current (V_{CB} = 400 Vdc, I_E = 0) (V_{CB} = 320 Vdc, I_E = 0)	MPSA44 MPSA45	I_{CBO}	— —	0.1 0.1	μAdc
Collector Cutoff Current (V_{CE} = 400 Vdc, V_{BE} = 0) (V_{CE} = 320 Vdc, V_{BE} = 0)	MPSA44 MPSA45	I_{CES}	— —	500 500	nAdc
Emitter Cutoff Current (V_{BE} = 4.0 Vdc, I_C = 0)		I_{EBO}	—	0.1	μAdc
ON CHARACTERISTICS(1)					
DC Current Gain(1)	(I_C = 1.0 mAdc, V_{CE} = 10 Vdc) (I_C = 10 mAdc, V_{CE} = 10 Vdc) (I_C = 50 mAdc, V_{CE} = 10 Vdc) (I_C = 100 mAdc, V_{CE} = 10 Vdc)	h_{FE}	40 50 45 40	— 200 — —	—
Collector-Emitter Saturation Voltage(1)	(I_C = 1.0 mAdc, I_B = 0.1 mAdc) (I_C = 10 mAdc, I_B = 1.0 mAdc) (I_C = 50 mAdc, I_B = 5.0 mAdc)	$V_{CE(sat)}$	— — —	0.4 0.5 0.75	Vdc
Base-Emitter Saturation Voltage (I_C = 10 mAdc, I_B = 1.0 mAdc)		$V_{BE(sat)}$	—	0.75	Vdc
SMALL-SIGNAL CHARACTERISTICS					
Output Capacitance (V_{CB} = 20 Vdc, I_E = 0, f = 1.0 MHz)		C_{obo}	—	7.0	pF
Input Capacitance (V_{EB} = 0.5 Vdc, I_C = 0, f = 1.0 MHz)		C_{ibo}	—	13	pF
Small-Signal Current Gain (I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 10 MHz)		h_{fe}	2.0	—	—

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

FIGURE 1 — DC CURRENT GAIN

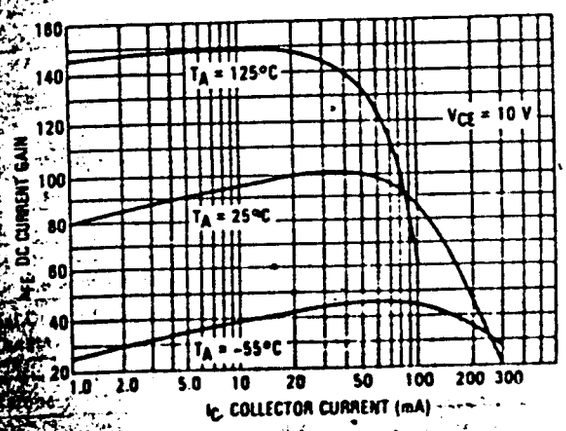


FIGURE 2 — COLLECTOR SATURATION REGION

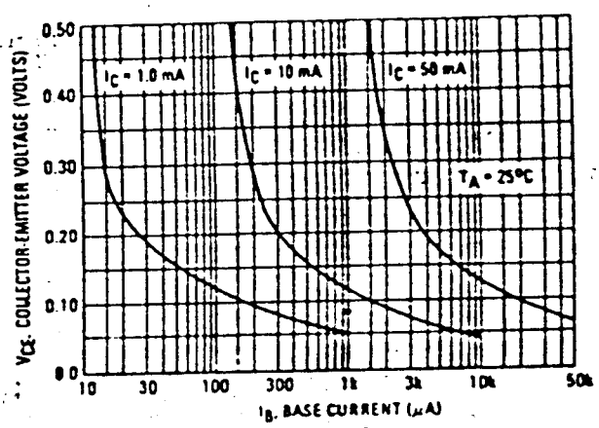


FIGURE 3 — ON VOLTAGES

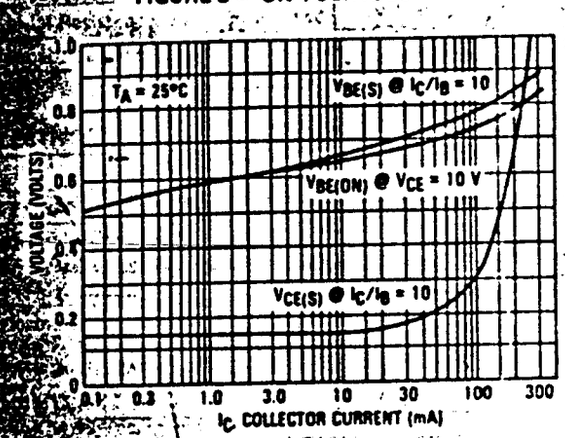


FIGURE 4 — ACTIVE REGION — SAFE OPERATING AREA

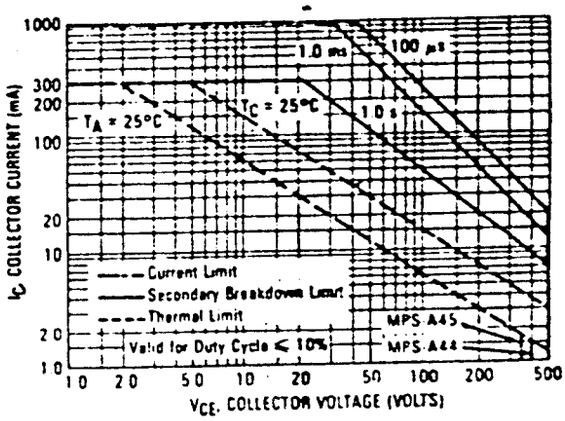


FIGURE 5 — CAPACITANCE

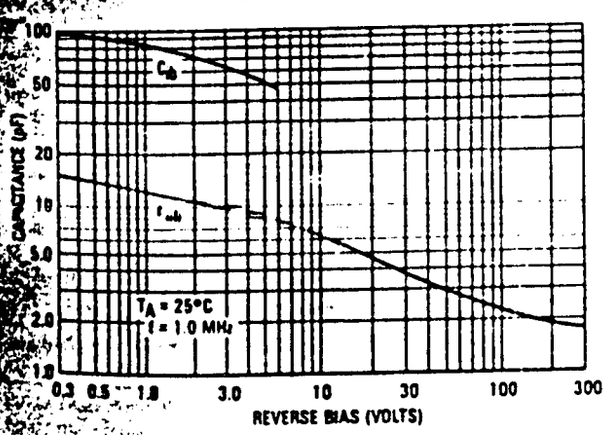
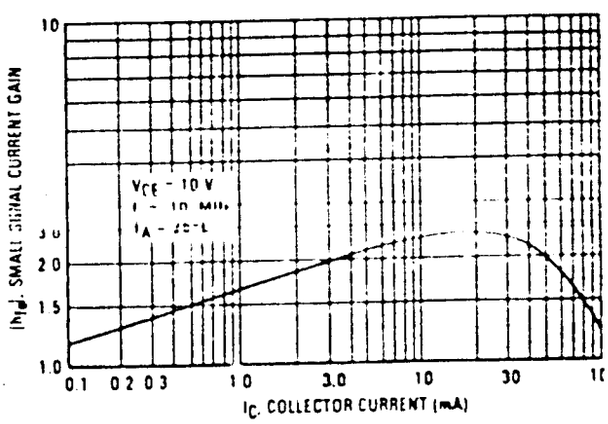


FIGURE 6 — HIGH FREQUENCY CURRENT GAIN

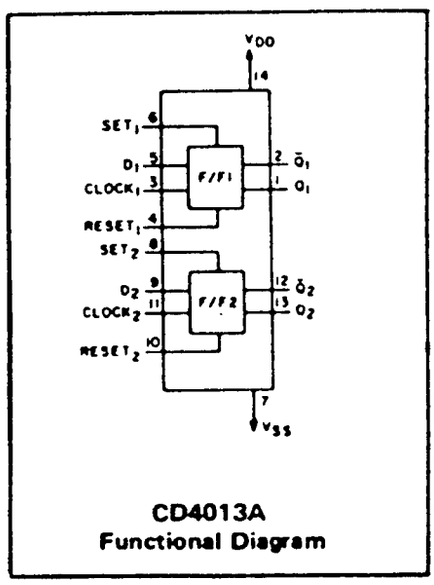


Digital Integrated Circuits

Monolithic Silicon

CD4013A

COS/MOS Dual 'D'-Type Flip-Flop



CD4013A
Functional Diagram

Features

- Set-Reset capability
- Static flip-flop operation - retains state indefinitely with clock level either "high" or "low"
- Medium-speed operation - 10 MHz (typ.) clock toggle rate at 10 V
- Quiescent current specified to 15 V
- Maximum input leakage current of 1 μA at 15 V (full package-temperature range)
- 1-V noise margin (Full package-temperature range)

Applications

- Registers, counters, control circuits

The BEL CD4013A consists of two identical, independent data-type, flip-flops. Each flip-flop has independent data, set, reset and clock inputs and Q and $\overline{Q}$ outputs. These devices can be used for shift register applications and by connecting $\overline{Q}$ output to the data input, for counter and toggle applications. The logic level present at the D input is transferred to the Q output during the positive-going transition of the clock pulse. Setting or resetting is independent of the clock and is accomplished by a high level on the set or reset line, respectively.

The CD4013A Series types are supplied in 14-lead hermetic dual-in-line ceramic package(F suffix)and 14-lead dual-in-line plastic package (E suffix).

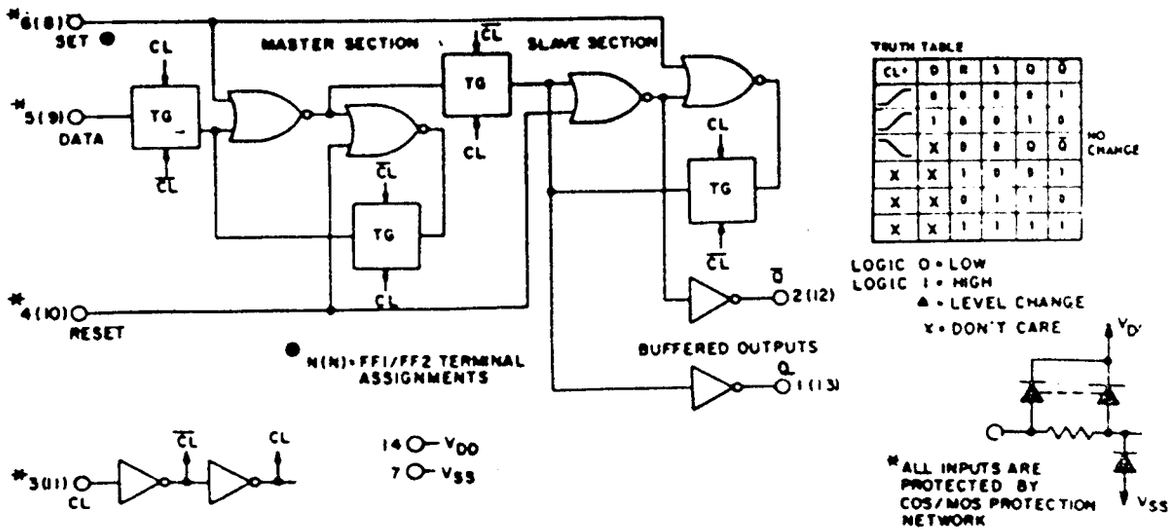


Fig. 1 – Logic diagram and truth table for CD4013A (one of two identical flip flops)

MAXIMUM RATINGS, Absolute-Maximum Values

Storage-Temperature Range	... (T_{stg})	−65 to +150	°C
Operating-Temperature Range	... (T_A)		
F Package	...	−55 to +125	°C
E Package	...	−40 to +85	°C
DC Supply-Voltage Range (Voltages referenced to V_{SS} Terminal)	... (V_{DD})	−0.5 to +15	V
Power Dissipation per Package:	... (P_D)		
For T_A = −40 to +60°C (E Package)	...	500	mW
For T_A = +60 to +85°C (E Package)	...	Derate linearly 12 mW/°C to 200	mW
For T_A = −55 to +100°C (F Package)	...	500	mW
For T_A = +100 to +125°C (F Package)	...	Derate linearly 12 mW/°C to 200	mW
Device Dissipation per Output Transistor: For T_A = Full Package-Temperature Range (All Package Types)	...	100	mW
Input Voltage Range, All Inputs	...	−0.5 to V_{DD} +0.5	V
Lead Temperature (During Soldering): At distance 1/16 ±1/32 in. (1.59 ±0.79 mm) from case for 10 s max.	...	+265	°C

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, except as noted

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTICS	V_{DD} (V)	LIMITS				UNITS
		F PACKAGE		E PACKAGE		
		Min.	Max.	Min.	Max.	
Supply Voltage Range (For T_A = Full Package Temperature Range)	-	3	12	3	12	V
Data Setup Time, t_S	5	40	-	50	-	ns
	10	20	-	25	-	
Clock Pulse Width, t_W	5	200	-	500	-	ns
	10	80	-	100	-	
Clock Input Frequency, f_{CL}	5		2.5		1	MHz
	10	dc	7	dc	5	
Clock Rise or Fall Time, t_rCL*, t_fCL	5	-	15	-	15	µs
	10	-	5		5	
Set or Reset Pulse Width	5	250	-	500	-	ns
	10	100	-	125	-	

* If more than one unit is cascaded in a parallel clocked operation, t_rCL should be made less than or equal to the sum of the fixed propagation delay time at 15 pF and the transition time of the output driving stage for the estimated capacitive load.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)								UNITS
				F PACKAGE				E PACKAGE				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	-55	+25 Typ.	+25 Limit	+125	-40	+25 Typ.	+25 Limit	+85	
Quiescent Device Current, I_L Max.	-	-	5	1	0.005	1	60	10	0.01	10	140	µA
	-	-	10	2	0.005	2	120	20	0.02	20	280	
	-	-	15	25	0.5	25	1000	250	2.5	250	2500	
Output Voltage: Low Level, V_{OL}	-	0.5	5	0 Typ.; 0.05 Max.								V
	-	0.10	10	0 Typ.; 0.05 Max.								
High Level, V_{OH}	-	0.5	5	4.95 Min.; 5 Typ.								
	-	0.10	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	4.2	-	5	1.5 Min.; 2.25 Typ.								V
	9	-	10	3 Min.; 4.5 Typ.								
Inputs High, V_{NH}	0.8	-	5	1.5 Min.; 2.25 Typ.								
	1	-	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	-	5	1 Min.								V
	9	-	10	1 Min.								
Inputs High, V_{NMH}	0.5	-	5	1 Min.								
	1	-	10	1 Min.								
Output Drive Current: N-Channel (Sink) I_DN Min.	0.5	-	5	0.65	1	0.5	0.35	0.35	1	0.3	0.24	mA
	0.5	-	10	1.25	2.5	1	0.75	0.72	2.5	0.6	0.5	
P-Channel (Source) I_DP Min.	4.5	-	5	-0.31	-0.5	-0.25	-0.175	-0.17	-0.5	-0.14	-0.12	
	9.5	-	10	-0.8	-1.3	-0.65	-0.45	-0.4	-1.3	-0.33	-0.27	
Input Leakage Current I_{IL}, I_{IH}	Any Input		15	$\pm 10^{-5}$ Typ.; ±1 Max.								µA

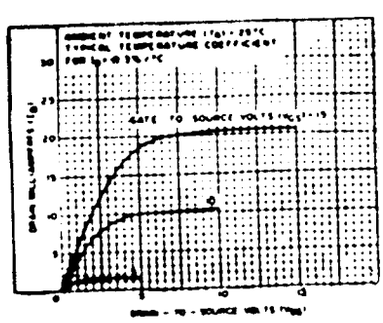


Fig 2 – Typical n channel drain characteristics

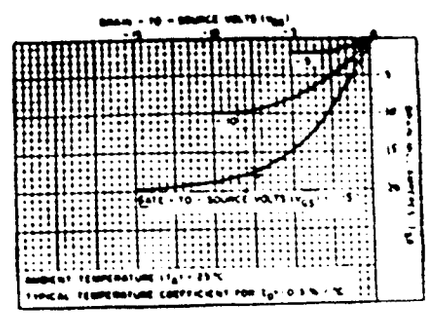


Fig 3 – Typical p-channel drain characteristics

DYNAMIC ELECTRICAL CHARACTERISTICS

At $T_A = 25°C$, Input t_r, $t_f = 20$ ns, $C_L = 15$ pF, $R_L = 200$ kΩ

CHARACTERISTICS	V_{DD} (V)	LIMITS						UNITS
		F PACKAGE			E PACKAGE			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Propagation Delay Time: Clock to Q or $\overline{Q}$ outputs t_{PHL}, t_{PLH}	5	–	150	300	–	150	350	ns
	10	–	75	110	–	75	125	
Set to Q or Reset to $\overline{Q}$, t_{PLH}	5	–	175	300	–	175	350	
	10	–	75	110	–	75	125	
Set to $\overline{Q}$ or Reset to Q, t_{PHL}	5	–	175	300	–	175	350	
	10	–	75	110	–	75	125	
Transition Time, t_{THL}, t_{TLH}	5	–	75	125	–	75	150	ns
	10	–	50	70	–	50	75	
Maximum Clock Input Frequency, f_{CL}	5	2.5	4	–	1	4	–	MHz
	10	7	10	–	5	10	–	
Minimum Clock Pulse Width, t_W	5	–	125	200	–	125	500	ns
	10	–	50	80	–	50	100	
Minimum Set or Reset Pulse Width, t_W	5	–	125	250	–	125	500	ns
	10	–	50	100	–	50	125	
Minimum Data Setup Time, t_S	5	–	20	40	–	20	50	ns
	10	–	10	20	–	10	25	
Clock Rise or Fall Time: t_rCL, t_fCL	5	–	–	15	–	–	15	μs
	10	–	–	5	–	–	5	
Average Input Capacitance, C_I	Any Input	–	5	–	–	5	–	pF

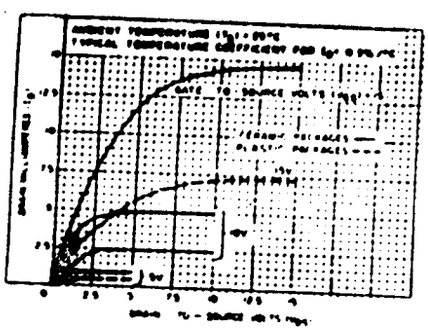


Fig 4 – Minimum n-channel drain characteristics

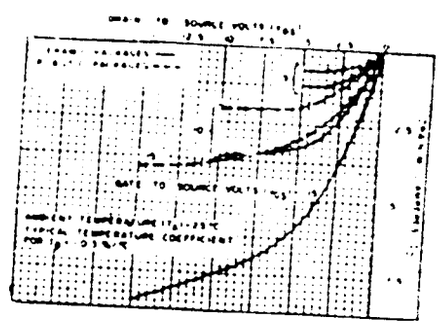


Fig 5 Minimum p-channel drain characteristics

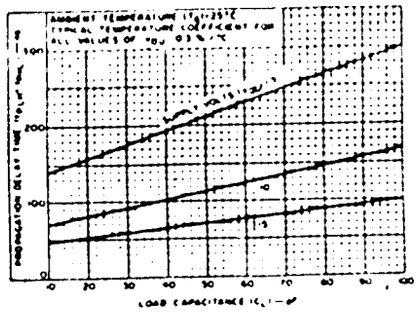


Fig.6 – Typical propagation delay time vs. C_L.

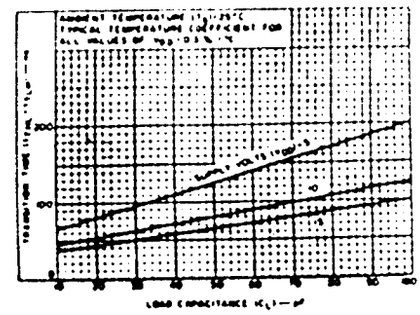


Fig.7 – Typical transition time vs. C_L.

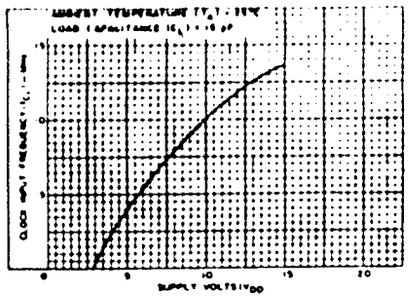


Fig.8 – Typical maximum clock input frequency vs. V_{DD}

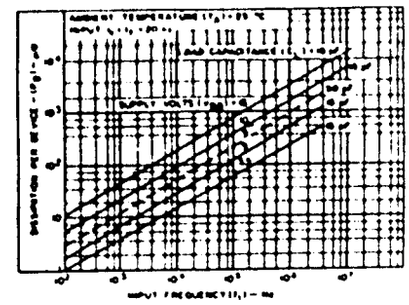


Fig.9 – Typical dissipation characteristics.

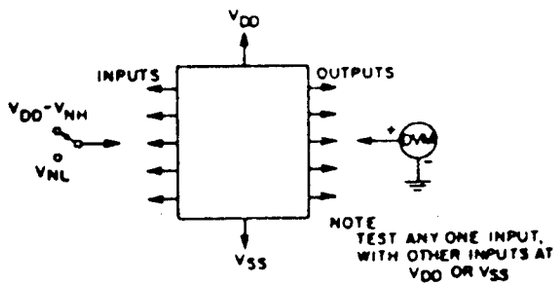


Fig.10 – Noise immunity test circuit.

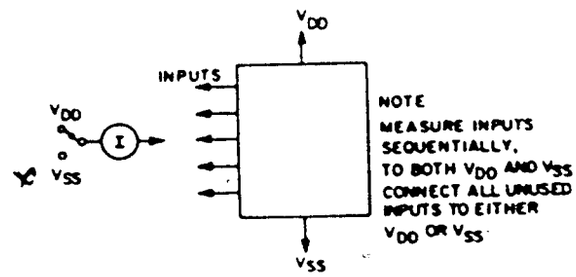


Fig.11 – Input leakage test circuit.

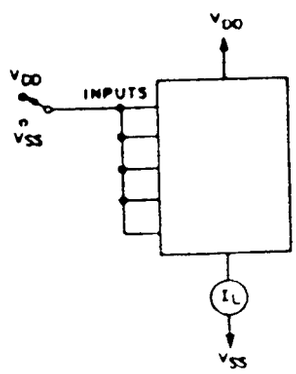
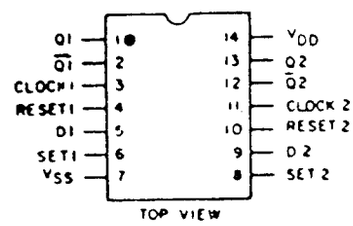


Fig.12 – Quiescent device-current test circuit.

TERMINAL ASSIGNMENT



CD4013A

OPERATING & HANDLING CONSIDERATIONS

Handling

All inputs and outputs of this device have a network for electrostatic protection during handling. Recommended handling practices for BEL COS/MOS devices are described in Application Information AI/DIC-3 "Handling and Operation of MOS Integrated Circuits"

Operating

OPERATING VOLTAGE

During operation near the maximum supply voltage limits, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause V_{DD}-V_{SS} to exceed the absolute maximum rating.

INPUT SIGNALS

To prevent damage to the input protection circuit, input signals should never be greater than V_{DD} nor less than V_{SS}. Input currents must not exceed 10 mA even when the power supply is off

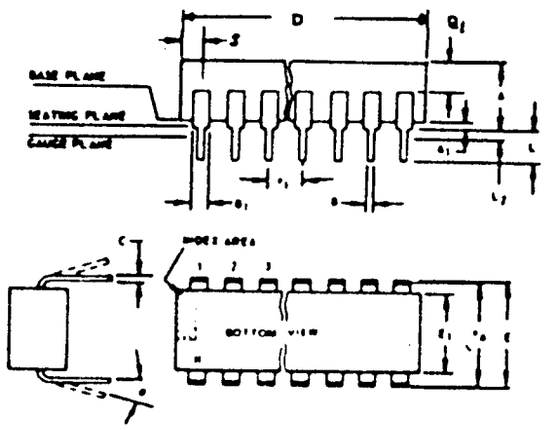
UNUSED INPUTS

A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{DD} or V_{SS}, whichever is appropriate.

OUTPUT SHORT CIRCUITS

Shorting of outputs to V_{DD} or V_{SS} may damage COS/MOS devices by exceeding the maximum device dissipation.

DIMENSIONAL OUTLINES



JEDEC MO-001-AB
14-Lead Dual-in-Line
Plastic or Frit-Seal Ceramic Package

SYMBOL	INCHES		NOTE	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.155	0.200		3.94	5.08
A_1	0.020	0.050		0.51	1.27
B	0.014	0.020		0.356	0.508
B_1	0.050	0.065		1.27	1.65
C	0.008	0.012	1	0.204	0.304
D	0.745	0.770		18.93	19.55
E	0.300	0.325		7.62	8.25
E_1	0.240	0.260		6.10	6.60
e_1	0.100 TP		2	2.54 TP	
e_A	0.300 TP		2, 3	7.62 TP	
L	0.125	0.150		3.18	3.81
L_2	0.000	0.030		0.000	0.76
α	0°	15°	4	0°	15°
N	14		5	14	
N_1	0		6	0	
Q_1	0.040	0.075		1.02	1.90
S	0.065	0.090		1.66	2.28

NOTES

Refer to Rules for Dimensioning (JEDEC Publication No. 13) for Axial Lead Product Outlines

1. When this device is supplied solder dipped the maximum lead thickness (narrow portion) will not exceed 0.013"
2. Leads within 0.005" (0.12 mm) radius of True Position (TP) at gauge plane with maximum material condition and unit installed
3. e_A applies in zone L_2 when unit installed
4. α applies to spread leads prior to installation
5. N is the maximum quantity of lead positions
6. N_1 is the quantity of allowable missing leads

BHARAT ELECTRONICS LTD.,
Jalahalli P.O., BANGALORE - 560 013. INDIA

SILICON PLANAR EPITAXIAL TRANSISTORS

General purpose n p n transistors in a plastic TO 92 variant, especially suitable for use in driver stages of audio amplifiers.

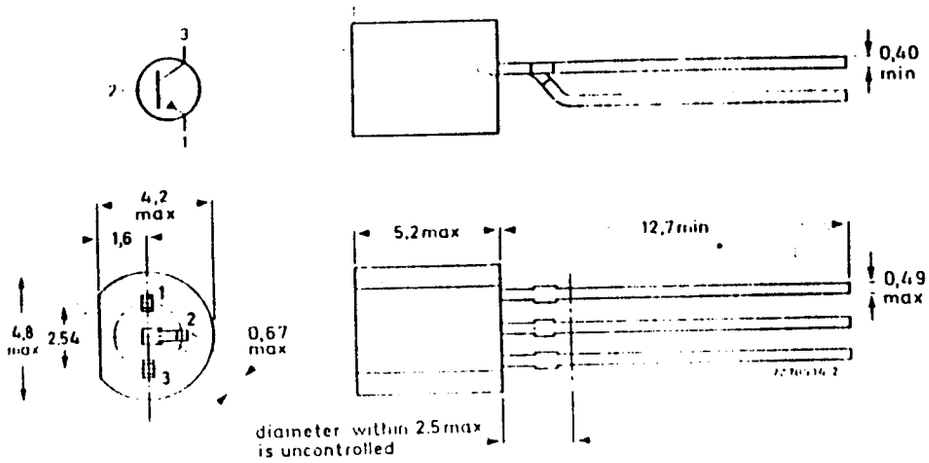
QUICK REFERENCE DATA

		BC546	BC547	BC548	
Collector emitter voltage (V_{BE} 0)	V_{CES} max.	80	50	30	V
Collector emitter voltage (open base)	V_{CEO} max.	65	45	30	V
Collector current (peak value)	I_{CM} max.	200	200	200	mA
Total power dissipation up to T_{amb} 25 °C	P_{tot} max.	500	500	500	mW
Junction temperature	T_j max.	150	150	150	°C
D.C. current gain I_C = 2 mA; V_{CE} = 5 V	h_{FE}	110 450	110 800	110 800	
Transition frequency I_C 10 mA; V_{CE} 5 V	f_T typ.	300	300	300	MHz
Noise figure at R_S 2 kΩ I_C 200 μA; V_{CE} 5 V f 1 kHz; B 200 Hz	F typ.	2	2	2	dB

MECHANICAL DATA

Dimensions in mm

Fig. 1 TO-92 variant.



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

			BC546	BC547	BC548
Collector base voltage (open emitter)	V_{CBO}	max.	80	50	30 V
Collector emitter voltage (V_{BE} = 0)	V_{CES}	max.	80	50	30 V
Collector emitter voltage (open base)	V_{CEO}	max.	65	45	30 V
Emitter-base voltage (open collector)	V_{EBO}	max.	6	6	5 V
Collector current (d.c.)	I_C	max.	100 mA		
Collector current (peak value)	I_{CM}	max.	200 mA		
Emitter current (peak value)	$-I_{EM}$	max.	200 mA		
Base current (peak value)	I_{BM}	max.	200 mA		
Total power dissipation up to T_{amb} = 25 °C	P_{tot}	max.	500 mW		
Storage temperature	T_{stg}		−65 to + 150 °C		
Junction temperature	T_j	max.	150 °C		

THERMAL RESISTANCE

From junction to ambient in free air	$R_{th\,j\,a}$	=	0,25 K/mW
From junction to case	$R_{th\,j\,c}$	=	0,15 K/mW

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Collector cut off current			
I_E = 0; V_{CB} = 30 V	I_{CBO}	<	15 nA
I_E = 0; V_{CB} = 30 V; T_j = 150 °C	I_{CBO}	<	5 μA
Base emitter voltage*			
I_C = 2 mA; V_{CE} = 5 V	V_{BE}	typ.	660 mV
			580 to 700 mV
I_C = 10 mA; V_{CE} = 5 V	V_{BE}		770 mV

* V_{BE} decreases by about 2 mV/K with increasing temperature.

Saturation voltage* I_C = 10 mA; I_B = 0,5 mA	V_{CEsat}	typ	90	mV
			250	mV
I_C = 100 mA; I_B = 5 mA	V_{BEsat}	typ	700	mV
	V_{CEsat}	typ	200	mV
			600	mV
	V_{BEsat}	typ.	900	mV
Collector capacitance at f = 1 MHz $I_E = I_e$ = 0; V_{CB} = 10 V	C_c	typ.	2,5	pF
Emitter capacitance at f = 1 MHz $I_C = I_c$ = 0; V_{EB} = 0,5 V	C_e	typ.	9	pF
Transition frequency at f = 35 MHz I_C = 10 mA; V_{CE} = 5 V	f_T	typ	300	MHz
Small signal current gain at f = 1 kHz I_C = 2 mA; V_{CE} = 5 V	h_{fe}		125 to 900	

		BC546	BC547	BC548	
Noise figure at R_S = 2 kΩ I_C = 200 μA; V_{CE} = 5 V f = 1 kHz; B = 200 Hz	F	typ.	2	2	2 dB
		<	10	10	10 dB

		BC546A BC547A BC548A	BC546B BC547B BC548B	BC547C BC548C
DC current gain I_C = 10 μA; V_{CE} = 5 V	h_{FE}	typ 90	150	270
		> 110	200	420
I_C = 2 mA; V_{CE} = 5 V	h_{FE}	typ. 180	290	520
		> 220	450	800

* V_{BEsat} decreases by about 1,7 mV/K with increasing temperature.

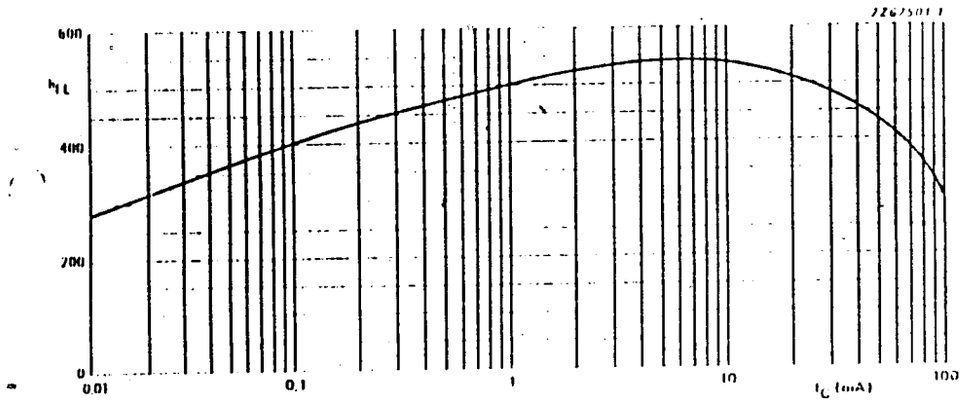


Fig. 4 BC547C and BC548C
V_{CE} = 5 V; T_j = 25 °C; typical values.

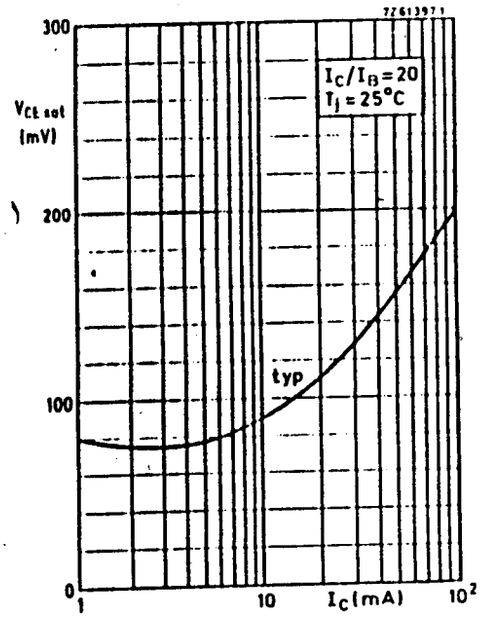


Fig. 5.

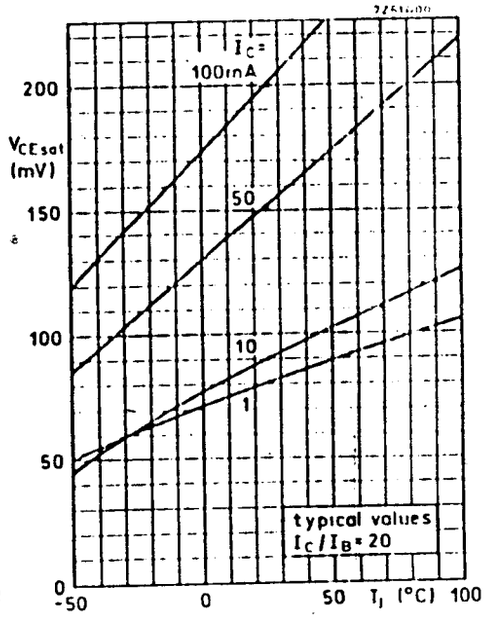


Fig. 6.

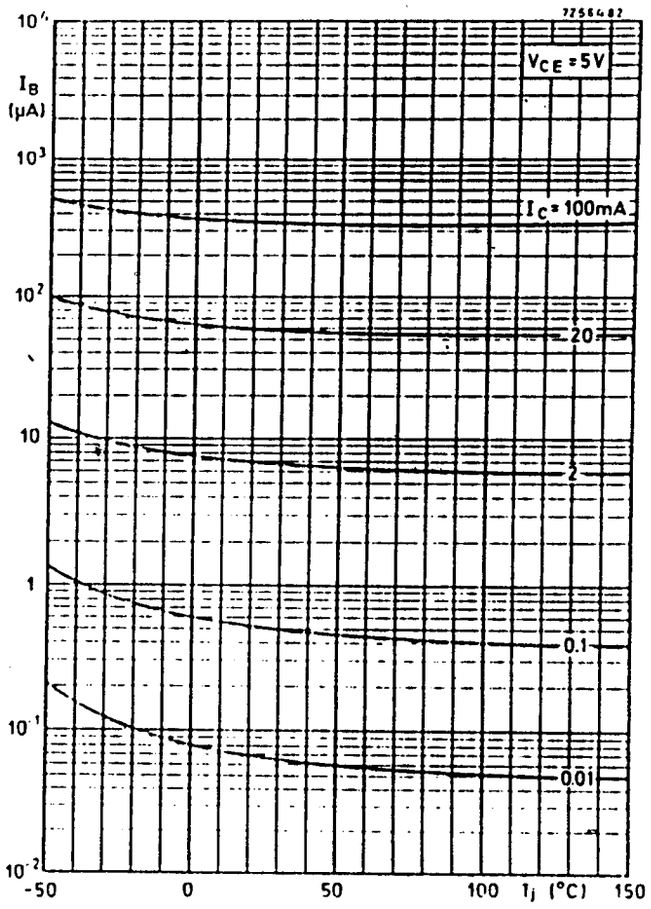

7256482
10^4
I_B (μA)
10^3
10^2
10
1
10^{-1}
10^{-2}
V_{CE} = 5V
I_C = 100mA
20
2
0.1
0.01
-50
0
50
100
T_j (°C)
150

Fig. 7.

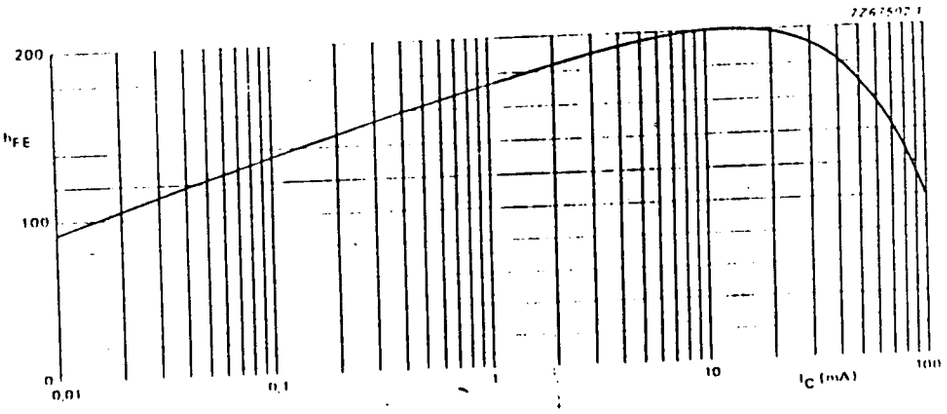


Fig. 2 BC546A, BC547A and BC548A
V_{CE} = 5 V; T_j = 25 °C; typical values.

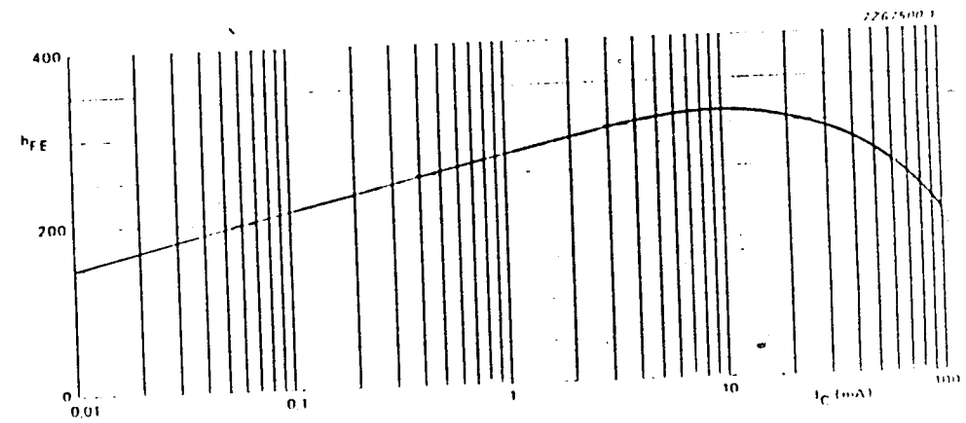


Fig. 3 BC546B, BC547B and BC548B
V_{CE} = 5 V; T_j = 25 °C; typical values.

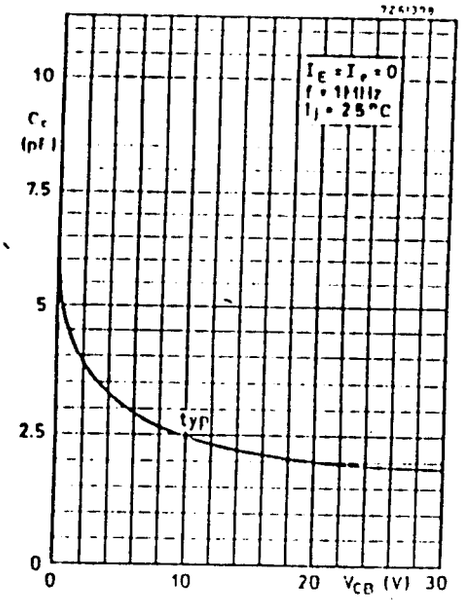

$I_E = I_e = 0$
f = 1 MHz
T_j = 25 °C
C_e (pF)
10
7.5
5
2.5
0
typ
0
10
20
V_{CB} (V)
30

Fig. 10.

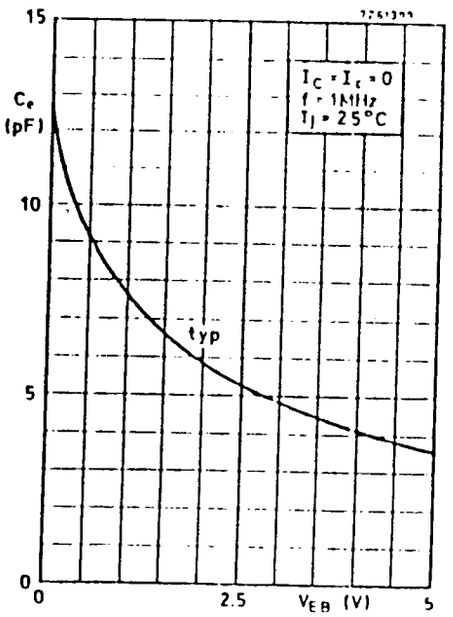

$I_C = I_c = 0$
f = 1 MHz
T_j = 25 °C
C_e (pF)
15
10
5
0
typ
0
2.5
V_{EB} (V)
5

Fig. 11.

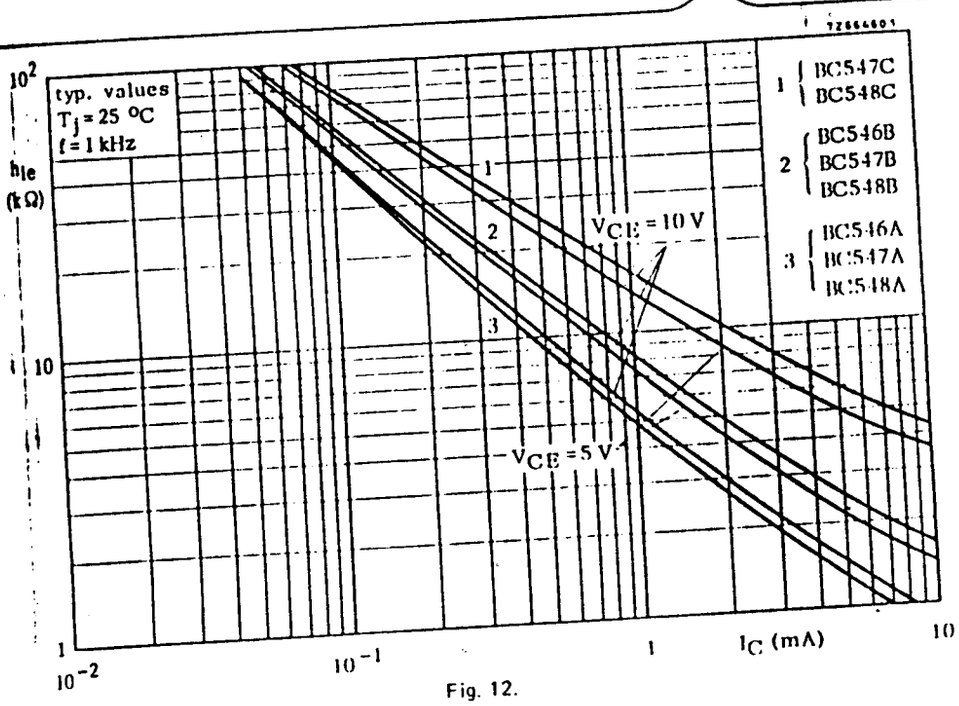

72664601
typ. values
T_j = 25 °C
f = 1 kHz
h_{fe}
(kΩ)
10^2
10
1
10^{-2}
10^{-1}
1
10
I_C (mA)
V_{CE} = 10 V
V_{CE} = 5 V
1
2
3
1 { BC547C BC548C
2 { BC546B BC547B BC548B
3 { BC546A BC547A BC548A

Fig. 12.

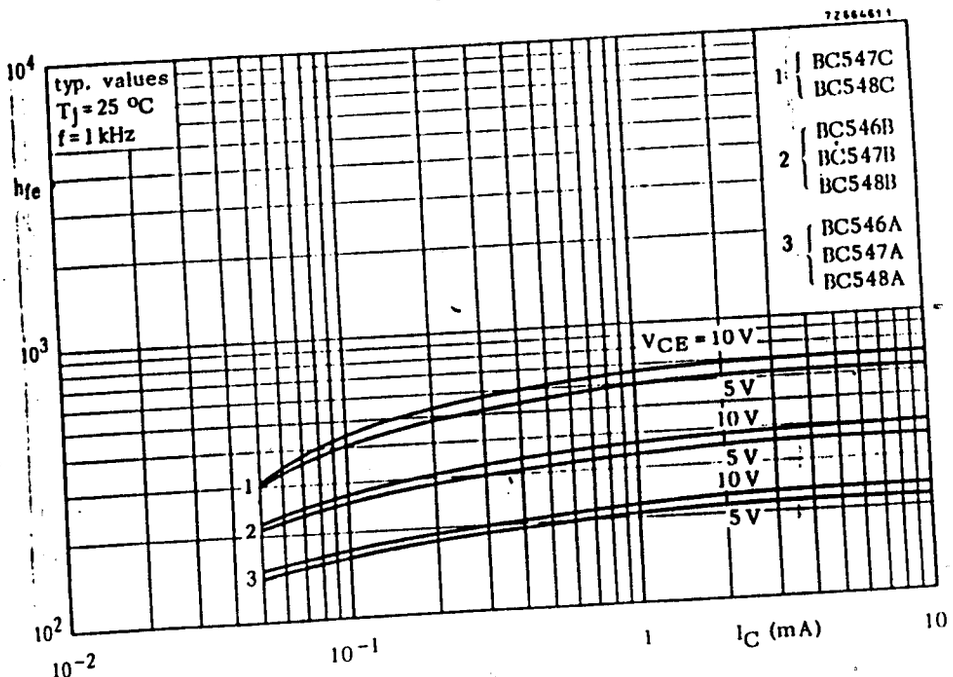

72664611
typ. values
T_j = 25 °C
f = 1 kHz
h_{fe}
10^4
10^3
10^2
10^{-2}
10^{-1}
1
10
I_C (mA)
V_{CE} = 10 V
5 V
10 V
5 V
10 V
5 V
1
2
3
1 { BC547C BC548C
2 { BC546B BC547B BC548B
3 { BC546A BC547A BC548A

Fig. 13.

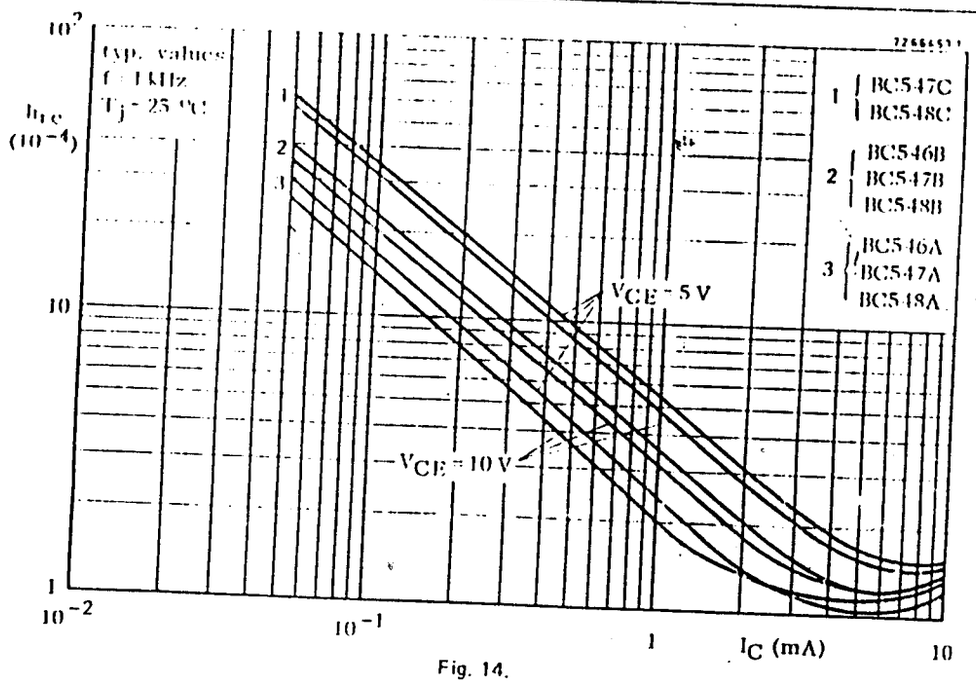

typ. values
f = 1 kHz
T_j = 25 °C
h_{fe} (10^{-4})
10^2
10
1
10^{-2}
10^{-1}
1
10
I_C (mA)
V_{CE} = 5 V
V_{CE} = 10 V
1 BC547C BC548C
2 BC546B BC547B BC548B
3 BC546A BC547A BC548A

Fig. 14.

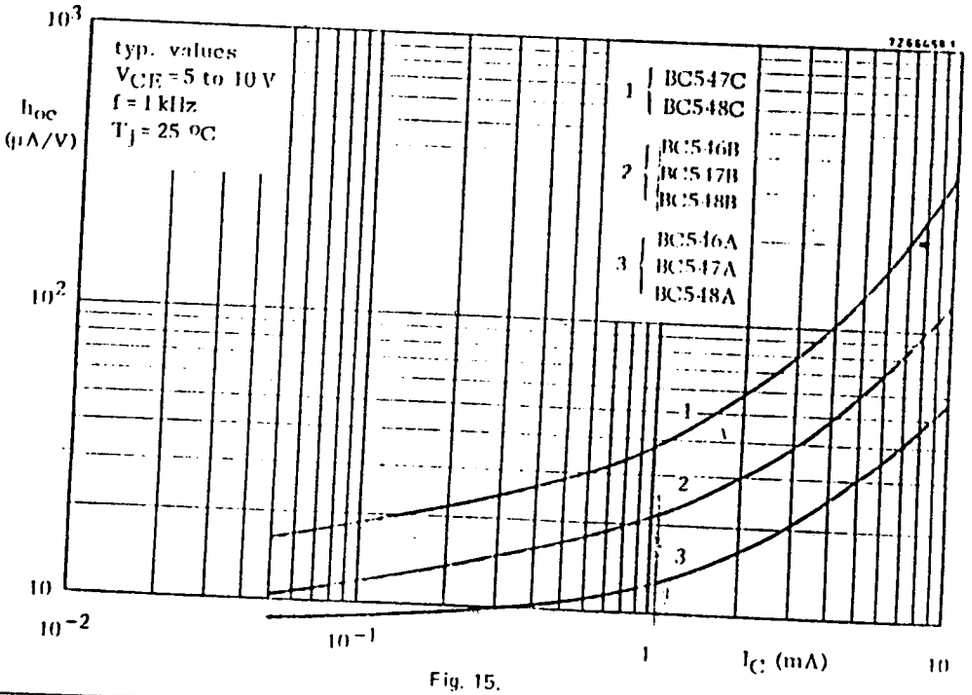

typ. values
V_{CE} = 5 to 10 V
f = 1 kHz
T_j = 25 °C
h_{oe} (μA/V)
10^3
10^2
10
10^{-2}
10^{-1}
1
10
I_C (mA)
1 BC547C BC548C
2 BC546B BC547B BC548B
3 BC546A BC547A BC548A

Fig. 15.

Low power quad op amps

LM124/224/324/324A/ SA534/LM2902

DESCRIPTION

The LM124/SA534/LM2902 series consists of four independent, high-gain, internally frequency-compensated operational amplifiers designed specifically to operate from a single power supply over a wide range of voltages.

UNIQUE FEATURES

In the linear mode, the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.

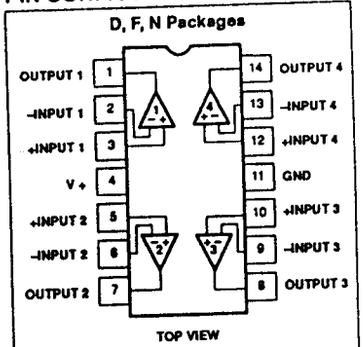
The unity gain crossover frequency and the input bias current are temperature-compensated.

FEATURES

- Internally frequency-compensated for unity gain
- Large DC voltage gain: 100dB
- Wide bandwidth (unity gain): 1MHz (temperature-compensated)
- Wide power supply range Single supply: $3V_{DC}$ to $30V_{DC}$ or dual supplies: $\pm1.5V_{DC}$ to $\pm15V_{DC}$
- Very low supply current drain: essentially independent of supply voltage (1mW/op amp at $+5V_{DC}$)
- Low input biasing current: $45nA_{DC}$ (temperature-compensated)
- Low input offset voltage: $2mV_{DC}$ and offset current: $5nA_{DC}$
- Differential input voltage range equal to the power supply voltage
- Large output voltage: $0V_{DC}$ to V_{CC}-1.5V_{DC} swing

PIN CONFIGURATION

D, F, N Packages



TOP VIEW

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic DIP	-55°C to +125°C	LM124N
14-Pin Ceramic DIP	-55°C to +125°C	LM124F
14-Pin Plastic DIP	-25°C to +85°C	LM224N
14-Pin Ceramic DIP	-25°C to +85°C	LM224F
14-Pin Plastic DIP	0°C to +70°C	LM324N
14-Pin Ceramic DIP	0°C to +70°C	LM324F
14-Pin Plastic SO	0°C to +70°C	LM324D
14-Pin Plastic DIP	0°C to +70°C	LM324AN
14-Pin Plastic SO	0°C to +70°C	LM324AD
14-Pin Plastic DIP	-40°C to +85°C	SA534N
14-Pin Ceramic DIP	-40°C to +85°C	SA534F
14-Pin Plastic SO	-40°C to +85°C	SA534D
14-Pin Plastic SO	-40°C to +85°C	LM2902D
14-Pin Plastic DIP	-40°C to +85°C	LM2902N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	32 or ±16	V_{DC}
V_{IN}	Differential input voltage	32	V_{DC}
V_{IN}	Input voltage	-0.3 to +32	V_{DC}
P_D	Maximum power dissipation, T_A=25°C (still-air)[1]		
	N package	1420	mW
	F package	1190	mW
	D package	1040	mW
	Output short-circuit to GND one amplifier V_{CC}<15V_{DC} and T_A=25°C	Continuous	
I_{IN}	Input current (V_{IN}<-0.3V)[3]	50	mA
T_A	Operating ambient temperature range		
	LM324/A	0 to +70	°C
	LM224	-25 to +85	°C
	SA534/LM2902	-40 to +85	°C
	LM124	-55 to +125	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:

1. Derate above 25°C at the following rates:
   F package at 9.5mW/°C
   N package at 11.4mW/°C
   D package at 8.3mW/°C
2. Short-circuits from the output to V_{CC}+ can cause excessive heating and eventual destruction. The maximum output current is approximately 40mA, independent of the magnitude of V_{CC}. At values of supply voltage in excess of +15V_{DC} continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction.
3. This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input bias clamps. In addition, there is also lateral NPN parasitic transistor action on the IC chip. This action can cause the output voltages of the op amps to go to the V+ rail (or to ground for a large overdrive) during the time that the input is driven negative.

DC ELECTRICAL CHARACTERISTICS

V_{CC}=5V, T_A=25°C unless otherwise specified

SYMBOL	PARAMETER	TEST CONDITIONS	LM124/LM224			LM324/SA534/LM2902			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage[1]	R_S=0Ω		±2	±5		±2	±7	mV
		R_S=0Ω, over temp.			±7			±9	mV
$\Delta V_{OS}/\Delta T$	Temperature drift	R_S=0Ω, over temp.		7			7		μV/°C
I_{BIAS}	Input current[2]	$I_{IN}(+)$ or $I_{IN}(-)$		45	150		45	250	nA
		$I_{IN}(+)$ or $I_{IN}(-)$, over temp.		40	300		40	500	nA
$\Delta I_{BIAS}/\Delta T$	Temperature drift	Over temp.		50			50		pA/°C
I_{OS}	Offset current	$I_{IN}(+)$ $I_{IN}(-)$		±3	±30		±5	±50	nA
		$I_{IN}(+)$-$I_{IN}(-)$, over temp.			±100			±150	nA
V_{OS}	Offset voltage[1]	R_S = 0Ω		±2	±5		±2	±7	mV
		R_S = 0Ω, over temp.			±7			±9	mV
$\Delta V_{OS}/\Delta T$	Temperature drift	R_S = 0Ω, over temp.		7			7		μV/°C
I_{BIAS}	Input current[2]	I_{IN} (+) or I_{IN} (−)		45	150		45	250	nA
		I_{IN} (+) or I_{IN} (−), over temp.		40	300		40	500	nA
$\Delta I_{BIAS}/\Delta T$	Temperature drift	Over temp.		50			50		pA/°C
I_{OS}	Offset current	I_{IN} (+) − I_{IN} (−)		±3	±30		±5	±50	nA
		I_{IN} (+) − I_{IN} (−), over temp.			±100			±150	nA
$\Delta I_{OS}/\Delta T$	Temperature drift	Over temp.		10			10		pA/°C
V_{CM}	Common-mode voltage range[3]	V_{CC}≤30V	0		V_{CC}-1.5	0		V_{CC}-1.5	V
		V_{CC}≤30V, over temp.	0		V_{CC}-2	0		V_{CC}-2	V
CMRR	Common-mode rejection ratio	V_{CC}=30V	70	85		65	70		dB
V_{OUT}	Output voltage swing	R_L=2kΩ, V_{CC}=30V, over temp.	26			26			V
V_{OH}	Output voltage high	R_L≤10kΩ, V_{CC}=30V, over temp.	27	28		27	28		V
V_{OL}	Output voltage low	R_L≤10kΩ, V_{CC}=5V, over temp.		5	20		5	20	mV
I_{CC}	Supply current	R_L=∞, V_{CC}=30V, over temp.		1.5	3		1.5	3	mA
		R_L=∞, V_{CC}=5V, over temp.		0.7	1.2		0.7	1.2	mA
A_{VOL}	Large-signal voltage gain	V_{CC}=15V (for large V_O swing), R_L≥2kΩ	50	100		25	100		V/mV
		V_{CC}=15V (for large V_O swing), R_L≥2kΩ, over temp.	25			15			V/mV
	Amplifier-to-amplifier coupling[5]	f=1kHz to 20kHz, input referred		-120			-120		dB
PSRR	Power supply rejection ratio	R_S≤0Ω	65	100		65	100		dB
I_{OUT}	Output current source	V_{IN}+=+1V, V_{IN}-=0V, V_{CC}=15V	20	40		20	40		mA
		V_{IN}+=+1V, V_{IN}-=0V, V_{CC}=15V, over temp.	10	20		10	20		mA
	sink	V_{IN}-=+1V, V_{IN}+=0V, V+=15V	10	20		10	20		mA
		V_{IN}-=+1V, V_{IN}+=0V, V_{CC}=15V, over temp.	5	8		5	8		mA
		V_{IN}-=+1V, V_{IN}+=0V, V_O=200mV	12	50		12	50		μA
I_{SC}	Short-circuit current[4]		10	40	60	10	40	60	mA

DC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LM124/LM224			LM324/SA534/LM2902			UNIT
			Min	Typ	Max	Min	Typ	Max	
GBW	Unity gain bandwidth			1			1		MHz
SR	Slow rate			0.3			0.3		V/μs
V_{NOISE}	Input noise voltage	f=1kHz		40			40		nV/√Hz
V_{DIFF}	Differential input voltage[3]				V_{CC}			V_{CC}	V

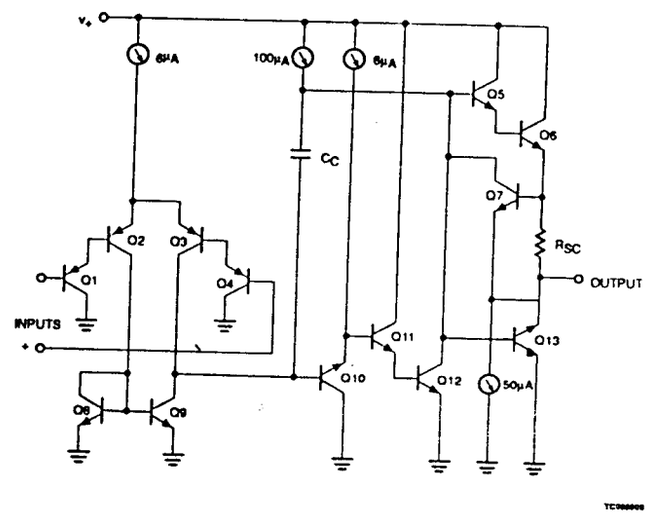
DC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LM124A			UNIT
			Min	Typ	Max	
V_{OS}	Offset voltage[1]	R_S=0Ω		±2	±3	mV
		R_S=0Ω, over temp.			±5	mV
$\Delta V_{OS}/\Delta T$	Temperature drift	R_S=0Ω, over temp.		7	30	μV/°C
I_{BIAS}	Input current[2]	$I_{IN}(+)$ or $I_{IN}(-)$		45	100	nA
		$I_{IN}(+)$ or $I_{IN}(-)$, over temp.		40	200	nA
$\Delta I_{BIAS}/\Delta T$	Temperature drift	Over temp.		50		pA/°C
I_{OS}	Offset current	$I_{IN}(+)-I_{IN}(-)$		±5	±30	nA
		$I_{IN}(+)-I_{IN}(-)$, over temp.			±75	nA
$\Delta I_{OS}/\Delta T$	Temperature drift	Over temp.		10	300	pA/°C
V_{CM}	Common-mode voltage range[3]	V_{CC}≤30V	0		V_{CC}-1.5	V
		V_{CC}≤30V, over temp.	0		V_{CC}-2	V
CMRR	Common-mode rejection ratio	V_{CC}=30V	65	85		dB
V_{OUT}	Output voltage swing	R_L=2kΩ, V_{CC}=30V, over temp.	26			V
V_{OH}	Output voltage high	R_L≤10kΩ, V_{CC}=30V, over temp.	27	28		V
V_{OL}	Output voltage low	R_L≤10kΩ, V_{CC}=5V, over temp.		5	20	mV
I_{CC}	Supply current	R_L=∞, V_{CC}=30V, over temp.		1.5	3	mA
		R_L=∞, V_{CC}=5V, over temp.		0.7	1.2	mA
A_{VOL}	Large-signal voltage gain	V_{CC}=15V (for large V_O swing), R_L≥2kΩ	25	100		V/mV
		V_{CC}=15V (for large V_O swing), R_L≥2kΩ, over temp.	15			V/mV
	Amplifier-to-amplifier coupling[5]	f=1kHz to 20kHz, input referred		-120		dB
PSRR	Power supply rejection ratio	R_S≤0Ω	65	100		dB
I_{OUT}	Output current source	$V_{IN}+$=+1V, $V_{IN}-$=0V, V_{CC}=15V	20	40		mA
		$V_{IN}+$=+1V, $V_{IN}-$=0V, V_{CC}=15V, over temp.	10	20		mA
	sink	$V_{IN}-$=+1V, $V_{IN}+$=0V, V_+=15V	10	20		mA
		$V_{IN}-$=+1V, $V_{IN}+$=0V, V_{CC}=15V, over temp.	5	8		mA
		$V_{IN}-$=+1V, $V_{IN}+$=0V, V_O=200mV	12	50		μA
I_{SC}	Short-circuit current[4]		10	40	60	mA
V_{DIFF}	Differential input voltage[3]				V_{CC}	V
GBW	Unity gain bandwidth			1		MHz
SR	Slew rate			0.3		V/μs
V_{NOISE}	Input noise voltage	f=1kHz		40		nV/√Hz

NOTES:

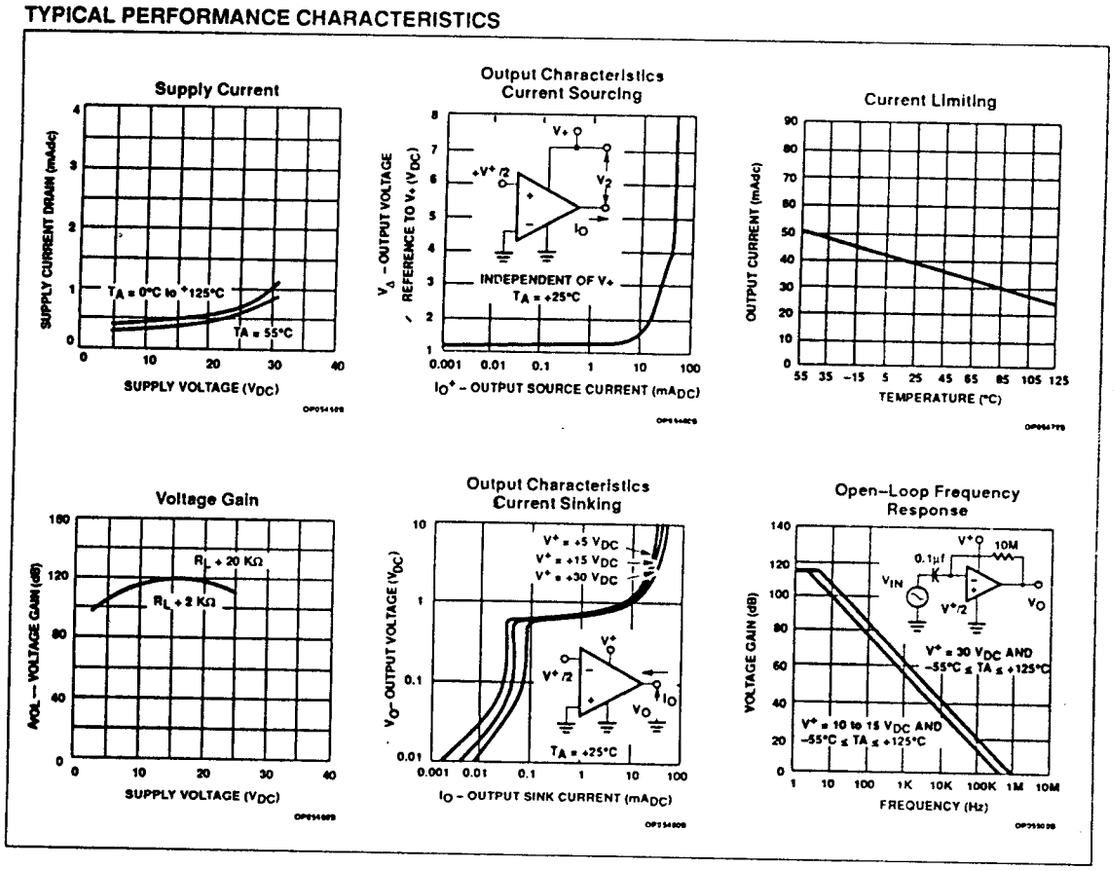
1. V_O ≈ 1.4V_{DC}, R_S=0Ω with V_{CC} from 5V to 30V and over full input common-mode range (0V_{DC} to V_{CC} -1.5V)
2. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
3. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V_{CC} -1.5, but either or both inputs can go to +32V without damage.
4. Short-circuits from the output to V_{CC} can cause excessive heating and eventual destruction. The maximum output current is approximately 40mA independent of the magnitude of V_{CC}. At values of supply voltage in excess of +15V_{DC}, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.
5. Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of coupling increases at higher frequencies.

EQUIVALENT CIRCUIT



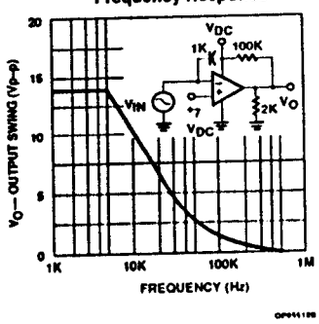
EQUIVALENT SCHEMATIC

TYPICAL PERFORMANCE CHARACTERISTICS

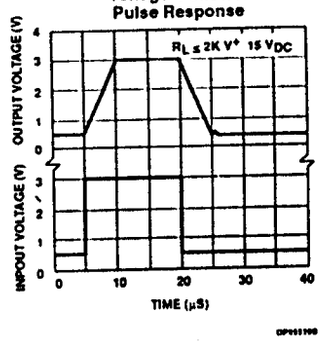


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

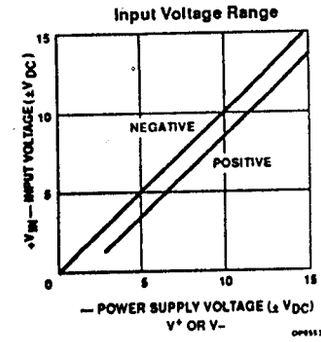
Large–Scale Frequency Response



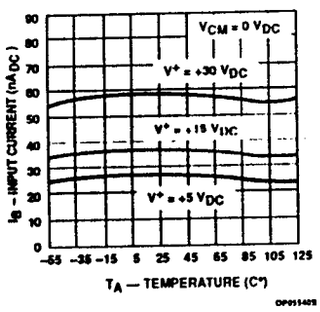
Voltage–Follower Pulse Response



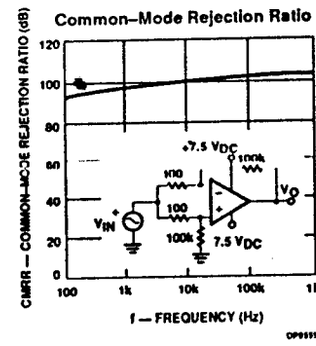
Input Voltage Range



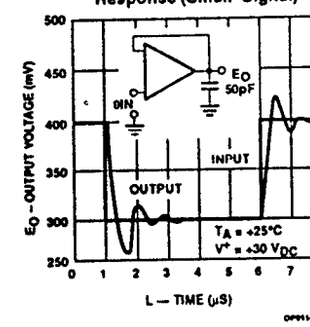
Input Current



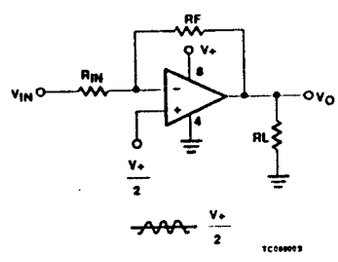
Common–Mode Rejection Ratio



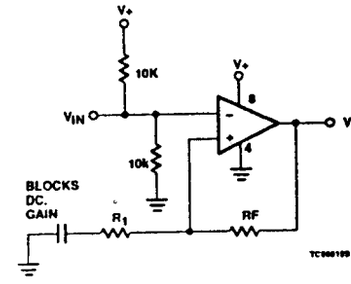
Voltage–Follower Pulse Response (Small–Signal)



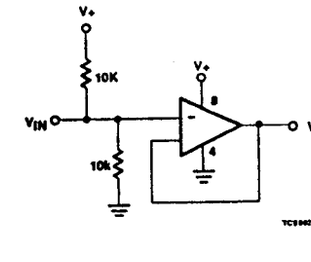
TYPICAL APPLICATIONS



Single Supply Inverting Amplifier



Non–Inverting Amplifier



Input Biasing Voltage–Follower

UM92870 Series

Integrated DTMF Receiver

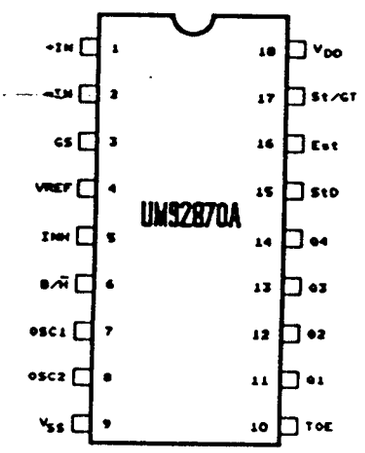
Features

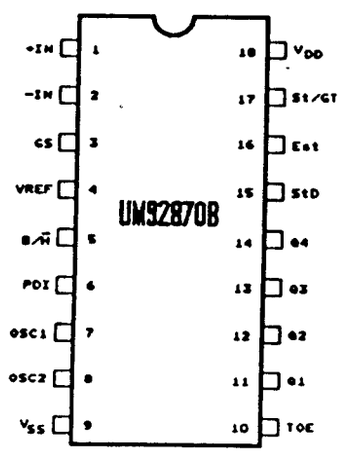
- Full DTMF receiver in 18-pin plastic packages
- Single 5-volt power supply
- Internal gain setting amplifier
- Adjustable guard time
- Built-in dial-tone filter
- Uses inexpensive 3.5795 MHz crystal
- CMOS for low power consumption
- Tristate outputs
- Early steering output

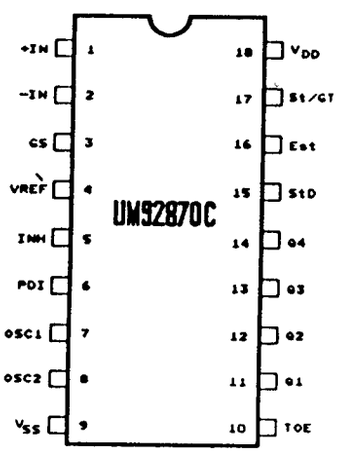
General Description

The UM92870 is a complete DTMF receiver designed to detect standard DTMF signals. It includes a differential input amplifier, filter section, decoder section, and steering logic circuits. The differential input amplifier allows adjustment of gain and choice of input configuration. The filter section provides a dial tone filter for dial-tone rejection and separates the dual-tone signal into low-group and high-group tones. The decoder decodes all 16 DTMF tone pairs into a four bit code. The steering logic circuits allow the designer to tailor system parameters such as talk-off and noise immunity. The UM92870 is packaged in 3 standard 18-pin DIP configurations and requires only a few external passive components.

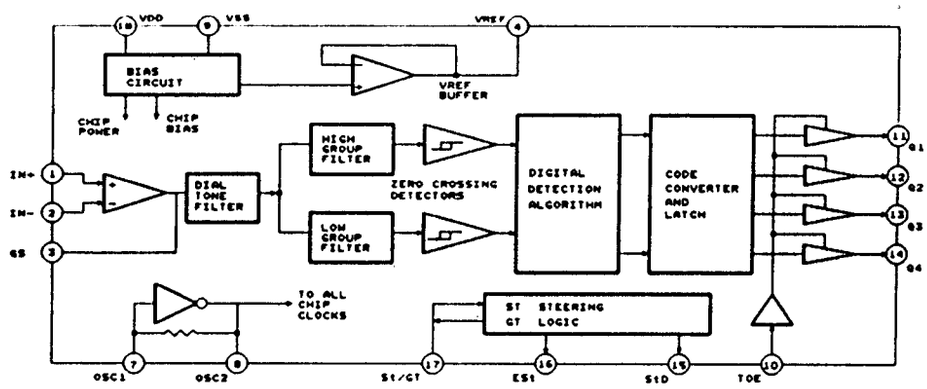
Pin Configurations







Block Diagram



Absolute Maximum Ratings*

Power Supply Voltage . . . . . 5V ± 10%
Applied Voltage (on any pin) . . . . . Vss -0.3V to VDD + 0.3V
Current (at any pin) 10mA
Operating Temperature . . . . . -20°C to + 70°C
Storage Temperature . . . . . -55°C to +150°C
Package Power Dissipation . . . . . 1,000 mW

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (Voltages are with respect to ground (Vss) unless otherwise stated)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Operating Supply Voltage	VDD	4.5	5.0	5.5	V	
Operating Supply Current	IDD		3.0	9.0	mA	
Power Consumption	PD		15	45	mW	f = 3.58MHz VDD = 5V
Power Down Current	IPD		6.2	100	μA	
High level input	VIH	3.5			V	
Low level input voltage	VIL			1.5	V	

DC Electrical Characteristics (Continued)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Input leakage current	I_{IH} / I_{IL}		0.1		μA	V_{IN} = V_{SS} or V_{DD}
Pull up (source) current	I_{SO}		7.5	15	μA	TOE (pin 10) = 0 V
Input impedance (±IN)	R_{IN}		10		MΩ	@ 1KHz
Steering threshold voltage	V_{TST}	2.2	2.4	2.5	V	
Low level output voltage	V_{OL}			0.03	V	No load
High level output voltage	V_{OH}	4.97			V	No load
Output low (sink) current	I_{OL}	1	2.5		mA	V_{OUT} = 0.4V
Output high (source) current	I_{OH}	0.4	0.8		mA	V_{OUT} = 4.6V
V_{REF} output voltage	V_{REF}	2.4		2.8	V	No load
V_{REF} output resistance	R_{OR}		1		KΩ	

Gain Setting Amplifier

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Input leakage current	I_{IN}			100	nA	$V_{SS} \le V_{IN} \le V_{DD}$
Input resistance	R_{IN}	10			MΩ	
Input offset voltage	V_{OS}			25	mV	
Power supply rejection	P_{SRR}	50			dB	1KHz
Common mode rejection	C_{MRR}	40			dB	-3.0V ≤ V_{IN} ≤ 3.0V
DC open loop voltage gain	A_{VOL}	32			dB	
Open loop unity gain bandwidth	F_C	0.3			MHz	

Gain Setting Amplifier (Continued)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Output voltage swing	V_O	4.5			V_{PP}	R_L> 100 KΩ to Vss
Maximum capacitive load (GS)	R_L			100	pF	
Maximum resistive load (GS)	R_L			50	KΩ	
Common mode range	V_{CM}	2.5			V_{PP}	No Load

V_{DD} = 5V , Vss = 0V, T_A = 25°C

AC Characteristics (Voltages are with respect to ground (Vss) unless otherwise stated)

Parameter	Min.	Typ.	Max.	Unit	Notes
SIGNAL CONDITIONS					
Valid input signal levels (each tone of composite signal)	-29			dBm	1, 2, 3, 5, 6, 9
	-27.5			mV_{RMS}	1, 2, 3, 5, 6, 9
			+1	dBm	1, 2, 3, 5, 6, 9
			833	mV_{RMS}	1, 2, 3, 5, 6, 9
Positive twist accept		10		dB	2, 3, 6, 9
Negative twist accept		10		dB	2, 3, 6, 9
Freq. deviation accept			±2.5%		2, 3, 5, 9
Freq. deviation reject	±3.5%				2, 3, 5, 9
Third tone tolerance		-16		dB	2, 3, 4, 5, 9, 10
Noise tolerance		-12		dB	2, 3, 4, 5, 7, 9,10
Dial tone tolerance		+22		dB	2, 3, 4, 5, 8, 9,11

Notes: 1. dBm = decibels above or below a reference power of 1 mW into a 600 ohm load

2. Digit sequence consists of all DTMF tones
3. Tone duration = 40 ms, tone pause = 40 ms
4. Signal condition consists of nominal DTMF frequencies
5. Both tones in composite signal have an equal amplitude
6. Tone pair has deviated by ±1.5%, ±2 Hz
7. Bandwidth limited (3 KHz) Gaussian noise
8. The precise dial tone frequencies are (350 Hz and 440 Hz) ±2%
9. For an error rate of better than 1 in 10,000
10. Referenced to lowest level frequency component in DTMF signal
11. Referenced to the minimum vaild accept level

AC Characteristics (Continued) (Voltages are with respect to ground (Vss) unless otherwise stated)

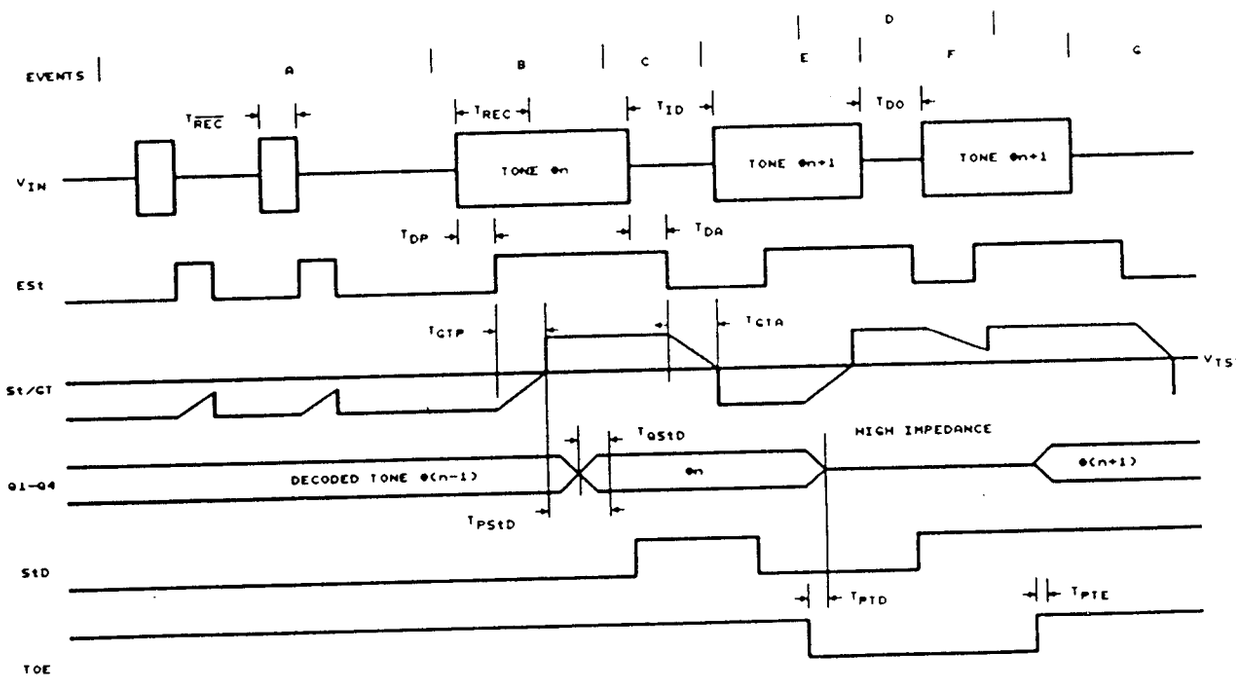
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
TIMING						
Tone present detect time	T_{DP}	5	11	20	ms	See timing diagram
Tone absent detect time	T_{DA}	0.5	4	8.5	ms	See timing diagram
Tone duration accept	T_{REC}			40	ms	User adjustable
Tone duration reject	$\overline{T_{REC}}$	20			ms	User adjustable
Interdigit pause accept	T_{ID}			40	ms	User adjustable
Interdigit pause reject	T_{DD}	20			ms	User adjustable
OUTPUT						
Propagation delay (St to StD)	T_{PStD}		12		μs	TOE = V_{DD}
Output data setup (Q to StD)	T_{QStD}		3.4		μs	TOE = V_{DD}

AC Characteristics (Continued) (Voltages are with respect to ground (Vss) unless otherwise stated)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Propagation delay (TOE to Q enable)	TPTE		50		ns	RL = 10 KΩ CL = 50 pF
Propagation delay (TOE to Q disable)	TPTD		300		ns	RL = 10 KΩ CL = 50 pF
CLOCK						
Crystal/Clock frequency	Fc	3.579	3.579	3.5831	MHz	
Clock input rise time	TLHCL			110	ns	Ext. Clock
Clock input fall time	THLCL			110	ns	Ext. Clock
Clock input duty cycle	DCCL	40	50	60	%	Ext. Clock
Capacitive load (osc2)	CLO			30	pF	

VDD = 5V, Vss = 0V, TA = 25°C and Fc = 3.579 MHz using test circuit figure 1.

Timing Waveform



Explanation of Events

A. Tone bursts detected. Tone duration invalid. Output not updated

B. Tone #n detected. Tone duration valid. Tone decoded and latched in output

C. End of tone #n detected. Tone absent duration valid. Output remains latched until next valid tone.

D. Output switched to high impedance state.

E. Tone #n+1 detected. Tone duration valid. Tone decoded and latched in output (currently high impedance)

F. Acceptable dropout of tone #n+1. Tone absent duration invalid. Output remains latched

G. End of tone #n+1 detected. Tone absent duration valid. Output remains latched until next valid tone.

Explanation of Symbols

V_{IN}	DTMF composite input signal
Est	Early steering output indicates detection of valid tone frequencies
St/GT	Steering input/Guard Time output. Drives external RC timing circuit.
Q1-Q4	Four-bit decoded tone output
StD	Delayed steering output. Indicates that valid frequencies have been present/absent for the required guard time, thus constituting a valid signal.
TOE	Tone output enable (input). A low level shifts Q1-Q4 to its high impedance state.
$T_{\overline{REC}}$	Maximum DTMF signal duration not detected as valid
T_{REC}	Minimum DTMF signal duration required for valid recognition
T_{ID}	Minimum time between valid DTMF signal
T_{DO}	Maximum allowable dropout during valid DTMF signal
T_{DP}	Time to detect the presence of valid DTMF signals
T_{DA}	Time to detect the absence of valid DTMF signals
T_{GTP}	Guard time, tone present
T_{GTA}	Guard time, tone absent

Pin Descriptions

Pin No.	Designation	I/O	Description
1	IN+	I	Non-inverting input of op-amp
2	IN-	I	Inverting input of op-amp
3	GS	I	Gain select. Gives access to output of front end differential amplifier for connection of feedback resistor.
4	VREF	O	Reference Voltage output. May be used to bias the inputs at midrail, V_{DD} / 2.
5, 6	INH, B/$\overline{H}$, PDI	I,I	INH: DTMF signal control. When this pin is pulled high, detection of tone pairs containing the 1633Hz component is inhibited. To detect all 16 standard digits this pin must be pulled low. B/$\overline{H}$: Digital output format control. When this pin is pulled low, the UM92870 output is given in hexadecimal code. When input is high, output is in 2-of-8 binary code. Output codes are shown in Table 1. PDI: power down input. To enter power down mode, this pin must be pulled high. UM92870A — Pin No. 5, 6 — INH, B/$\overline{H}$ UM92870B — Pin No. 5, 6 — B/$\overline{H}$, PDI UM92870C — Pin No. 5, 6 — INH, PDI
7	OSC1	I	Clock input
8	OSC2	I	Clock output. A 3.5795 MHz crystal connected betwwen OSC1 and OSC2 completes the oscillator circuit.
9	VSS	I	Negative power supply input
10	TOE	I	Three-state output enable. Logic high enables the output from Q1 through Q4
11 - 14	Q1 - Q4	O	Three-state output. When enabled by TOE, provides the code which corresponds to the last valid tone-pair received. See Table 1
15	StD	O	Delayed steering output. Presents a logic high when a received tone-pair has been registered and the output latch updated; returns to logic low when the voltage on St/GT falls below V_{TST}
16	Est	O	Early steering output. Presents a logic high once the digital algorithm has detected a valid tone pair. Any subsequent loss of signal condition will cause Est to return to a logic low.
17	St/GT	I/O	Steering input/guard time output (bi-directional). A voltage greater than V_{TST} detected at St causes the device to register the detected tone pair and update the output latch. A voltage less than V_{TST} output acts to reset the external steering time constant; its state is a function of Est and the voltage on St.
18	VDD	I	Positive power supply input

Digit	TOE	Hexadecimal				Binary Coded 2 of 8				Low Group Frequency (Hz)	High Group Frequency (Hz)
		Q4	Q3	Q2	Q1	Q4	Q3	Q2	Q1		
1	H	0	0	0	1	0	0	0	0	697	1209
2	H	0	0	1	0	0	0	0	1	697	1336
3	H	0	0	1	1	0	0	1	0	697	1477
4	H	0	1	0	0	0	1	0	0	770	1209
5	H	0	1	0	1	0	1	0	1	770	1336
6	H	0	1	1	0	0	1	1	0	770	1477
7	H	0	1	1	1	1	0	0	0	852	1209
8	H	1	0	0	0	1	0	0	1	852	1336
9	H	1	0	0	1	1	0	1	0	852	1477
0	H	1	0	1	0	1	1	0	1	941	1336
*	H	1	0	1	1	1	1	0	0	941	1209
#	H	1	1	0	0	1	1	1	0	941	1477
A	H	1	1	0	1	0	0	1	1	697	1633
B	H	1	1	1	0	0	1	1	1	770	1633
C	H	1	1	1	1	1	0	1	1	852	1633
D	H	0	0	0	0	1	1	1	1	941	1633
ANY	L	Z	Z	Z	Z	Z	Z	Z	Z	-	-

L = LOGIC LOW, H = LOGIC HIGH, Z = HIGH IMPEDANCE

Table 1. DTMF Signal Output Codes

Functional Description

The UM92870 series monolithic DTMF receivers offer small size,low power consumption and high performance. The general operation is described as follows:

Differential Input Amplifier

To aid design flexibility, the UM92870 series provides a differential input operational amplifier as well as a bias source (VREF) which is used to bias the input at midrail. Adjustment of gain is achieved by connecting a feedback resistor to the op-amp output (GS). Figure 1 shows the differential configuration with the op-amp connected for unity gain and VREF biasing the input at VDD/2. Figure 2 shows the differential configuration, which permits the adjustment of gain with the feedback resistor, R5.

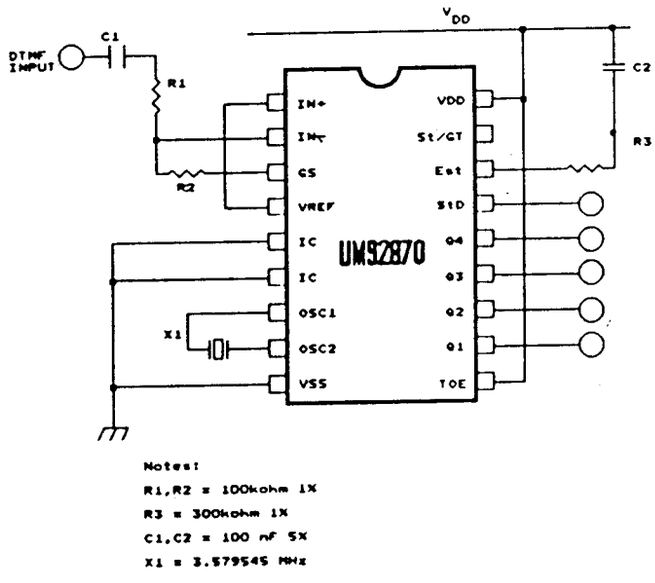


Figure 1. Single Ended Input Configuration

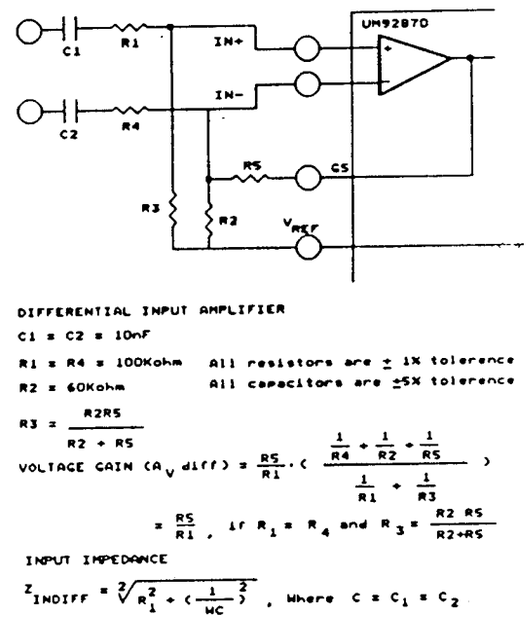


Figure 2. Differential Input Configuration

Filter Section

The differential input stage is followed by a low pass continuous RC active filter which performs an anti-aliasing function. Dial tone at 350Hz and 440Hz is then rejected by a third order switched capacitor notch filter.(See figure 3) The signal,still in its composite form, is then split into its individual high and low frequency components by two sixth order switched capacitor bandpass filters. Each component tone is then smoothed by an output filter and squared up by a hard limiting comparator. If the original DTMF input signals are valid tones, then the outputs of the comparators will be two rectangular waves.

Decoder Section

The resulting rectangular waves are applied to a decoder where a counting algorithm measures and averages their periods. This averaging algorithm has been developed to ensure an optimum combination of immunity to talk-off and tolerance to the presence of interfering frequencies (third tones) and noise. When the decoder recognizes the presence of a valid tone pair, the Early Steering (Est) output will go to an active state.

Steering Circuit

Est indicates that two tones of proper frequency have been detected and initiates an RC timing circuit. If both tones are present for the minimum guard time,which is determined by the external RC network, the DTMF signal is decoded and the resulting data is latched in the output register. Figure 4 gives the simple steering circuit. A logic high on Est cause Vc to reach the threshold (V_{TST}) of the steering logic. When the voltage on Vc rises above V_{TST} it causes the device to register the detected tone pair and update the output latch. At this point, the GT output is activated and drives Vc to V_{DD}. GT continues to drive high as long as Est remains high.
Finally, the Delayed Steering (StD) output is raised and indicates that new data is available. The contents of the output latch are made available on the four-bit output bus by raising the three-state control input (TOE) to a logic high. The steering circuit can be used to validate the interdigit pause between signals. Thus, as well as rejecting signals too short to be considered valid, the receiver will tolerate signal interruptions (drop out) too short to be considered a valid pause. This facility,together with the capability of selecting the steering time constant externally, allows the designer to tailor performance to meet a wide variety of system requirements. Component values in Figure 4 are chosen according to the formula:

$T_{REC} = T_{DP} + T_{GTP}$

$T_{GTP} \sim 0.67RC$

The value of T_{DP} is a device parameter (see AC Characteristics) and TREC is the minimum signal duration to be recognized by the receiver. A value for C of 0.1 uF is recommended for most applications, leaving R to be selected by the designer. For example, a suitable value of R for a T_{REC} of 40ms would be 300k. A typical circuit using this steering configuration is shown in Figure 1. The timing requirements for most telecommunication applications are satisfied with this circuit.

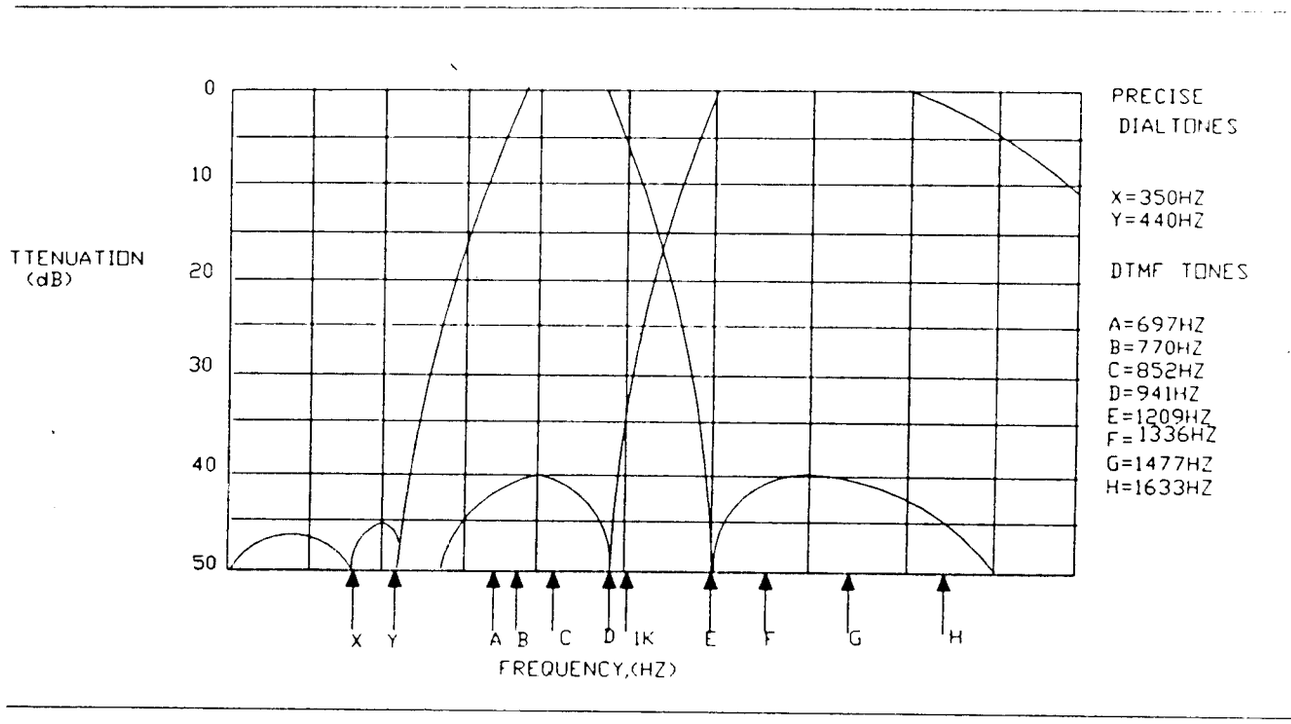


Figure 3. Filter Response

Guard Time Adjustment

Different steering arrangements may be used to select, independently, the guard times for tone present (TGTP) and tone absent (TGTA). This may be necessary to meet system specifications which place both "accept" and "reject" limits on both tone duration and interdigital pause. Guard time adjustment also allows the designer to tailor system parameters such as "talk-off" and "noise immunity". Increasing TREC improves talk-off performance since it reduces the probability that tones simulated by speech will maintain signal conditions long enough to be registered Alternately, a relatively short TREC with a long TDO would be appropriate for extremely noisy environments where fast acquisition time and immunity to tone drop-outs ae required. Design information for guard time adjustment is shown in figure 5.

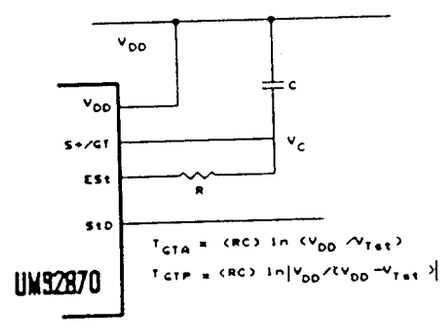


Figure 4. Basic Steering Circuit

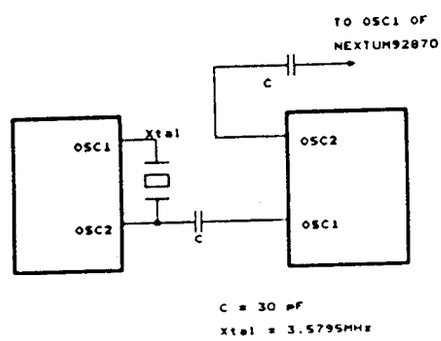
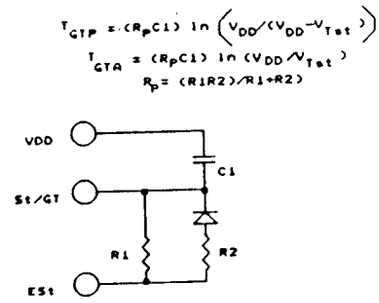


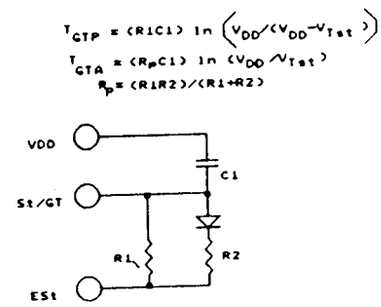
Figure 6. Oscillator Connection

Crystal Oscillator

The internal clock circuit is completed with the addition of an external 3.5795MHz crystal and is normally connected as shown in figure 1 (Single Ended Input Configuration). However, it is possible to configure several devices employing only a single oscillator crystal. The oscillator output of the first device in the chain is coupled through a 30pF capacitor to the oscillator input (OSC1) of the next device. Subsequent devices are connected in a similar fashion. Refer to figure 6 for details.The problems associated with unbalanced loading are not a concern with the arrangment shown, i.e., precision balancing capacitors are not required.



a) decreasing TGTP (TGTP < TGTA)



b) decreasing TGTA (TGTP > TGTA)

Figure 5. Guard Time Adjustment

Application Circuits

The design of a DTMF receiving system can generally be broken down into three functional blocks.The first consideration is the interface to the transmission medium. This may be as simple as a few passive components to adequately configure the UM92870's input stage or as complex as some form of demodulation, multiplexing or analog switching system. The second functional block is the DTMF receiver itself. The system's parameters can be optimized on this block. The third is the output control logic. This may be as simple as a 4 to 16 line decoder, controlling a specific function for each DTMF code, or as complex as a full computer handling system protocols and adaptively varying the tone receiver's parameters to adjust for changing signal conditions. Consider, for example, an existing pair of wires circulating throughout a plant.By connecting DTMF receivers at strategic points along this path one could conceivably control the whole plant from a single DTMF transmitter (Fig.7) Each DTMF receiver would monitor the common line until its specific I.D was received, at which time it would transfer data to its functional control logic. With some simple logic a circuit can be devised to recognize a sequence of programmed DTMF codes. Figure 8 illustrates a method of detecting a DTMF code sequence of arbitrary length, N. Initially, after a RESET has occurred, Qo of the presettable shift register is set logically high, the remaining outputs are reset. This activates the first bus buffer which applies its output to the Y inputs of a 4-bit comparator. When a valid DTMF signal is received its data appears at the comparators "X" inputs, a comparison occurs and the result appears at the "X=Y" output. After Std rises, the UM92870 output data is valid and strobes "X=Y" into the "VALID DIGIT" latch. The shift register advances one position which enables the next bus buffer. If the result of the comparison was true then the "VALID DIGIT" output is high. If all digits of the sequence match then the high output from the shift register "wraps around" from Qn-1 to Qo, which strobes the "LAST DIGIT" latch high. This activates the three input NAND gate indicating a "match" condition. If non-matching data is received any time during the detection sequence the "ERROR" flip-flop is reset which disables the NAND gate until a system "RESET" occurs.

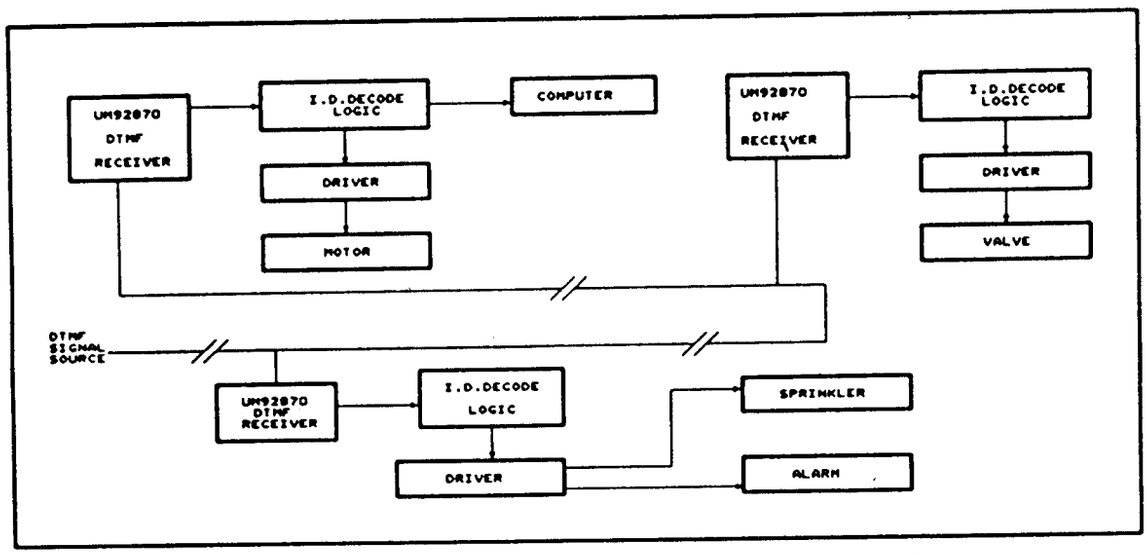


Figure 7. Distributed Control System

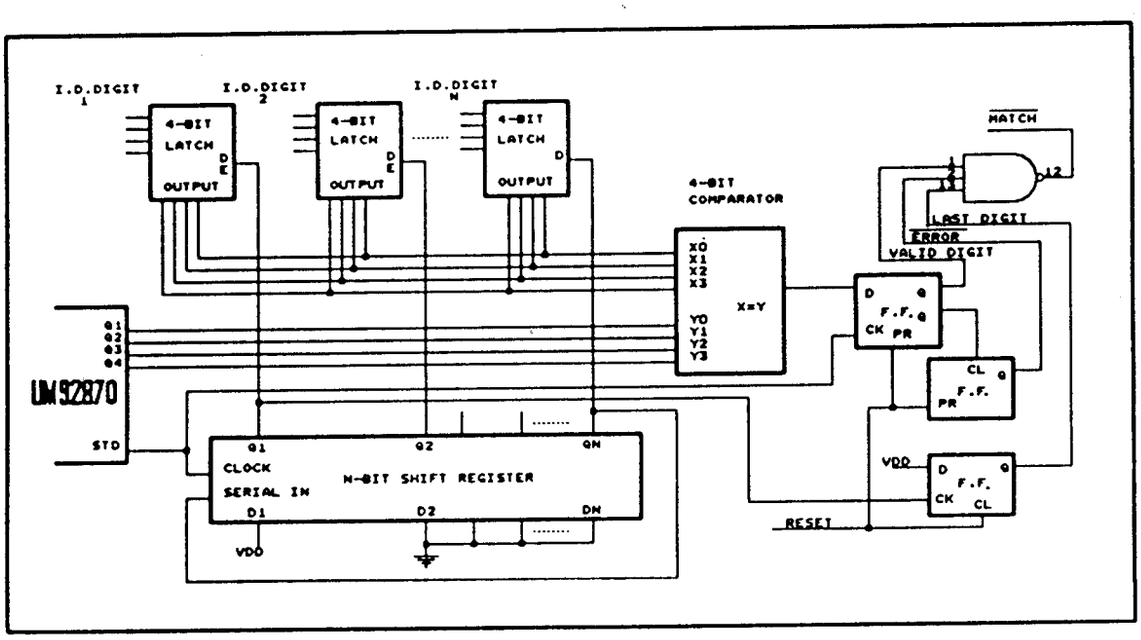


Figure 8. N-character Sequence Identifier

Figure 9 shows a household DTMF remote control system with an optional home computer. Remote ON/OFF control is given to electric appliances such as a slow cooker, exterior lighting and garage heater. An electro-mechanical solenoid operated valve allows remote control of a garden sprinkler. Video buffs could interface to their VCR remote control inputs and record T.V. shows with a few keystrokes of their friend's telephone. This would enhance the function of timers which are currently available on most VCR's. Schedule changes or unexpected broadcasts could be captured from any remote location featuring a Touch-Tone phone. Security systems could be controlled and a microphone could be switched in for remote audio monitoring. Interfacing a home computer to the data port makes an excellent family message center. At the remote end messages are entered from a telephone keypad. The computer responds with voice messages generated by a speech synthesizer.

DTMF have a variety of applications, including use in PABXs, central office, mobile radio, color video phone, distributed control systems, inquiry systems, and other remote control systems. Due to their high noise immunity, DTMF signals constitute a communication method with a very low error rate, and are utilized as data carriers in a variety of communication systems.

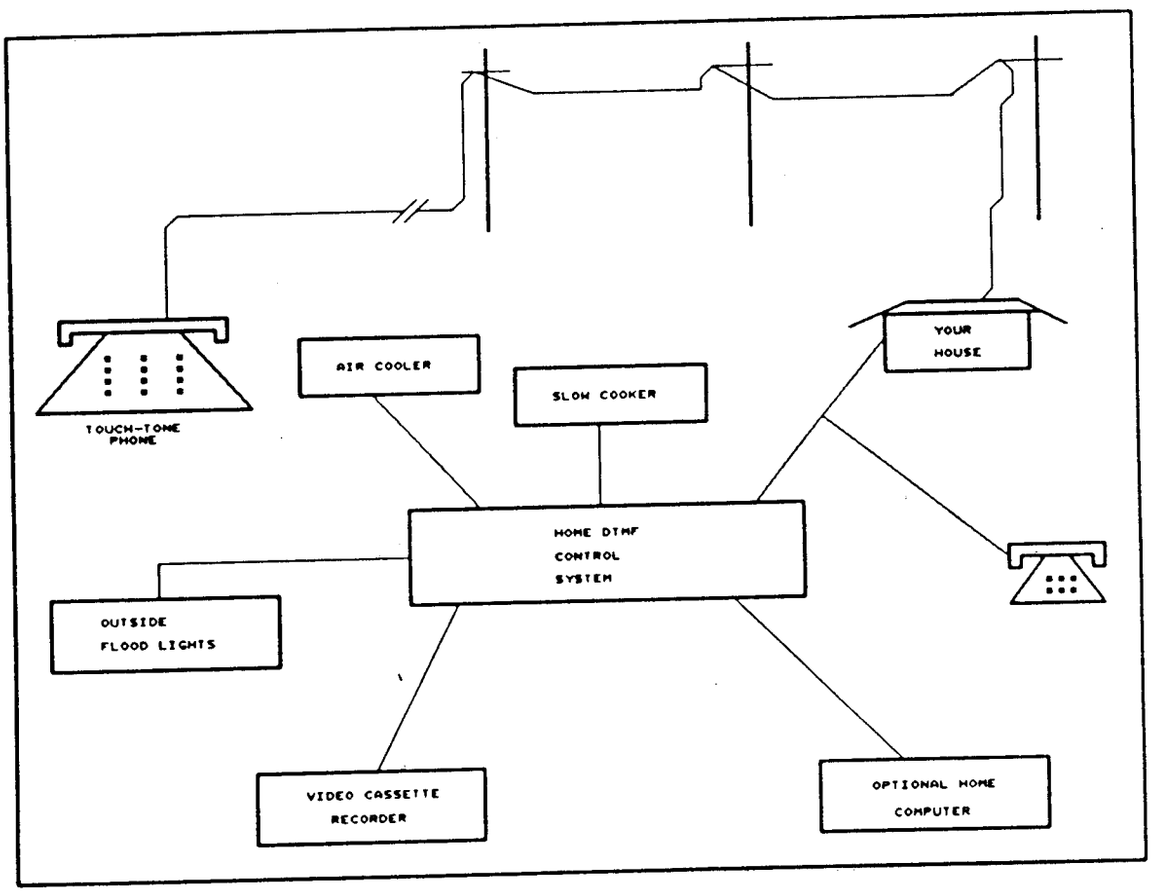


Figure 9. DTMF Remote Control System

Ordering Information

Part No.	Pin No. 5	Pin No. 6	Package
UM92870A	INH	B/$\overline{H}$	18L - DIP
UM92870B	B/$\overline{H}$	PDI	18L - DIP
UM92870C	INH	PDI	18L - DIP

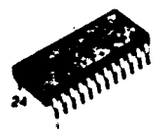
SPEL

74LS154

LINE-TO-16-LINE DECODERS/DEMULTIPLEXERS

DESCRIPTION

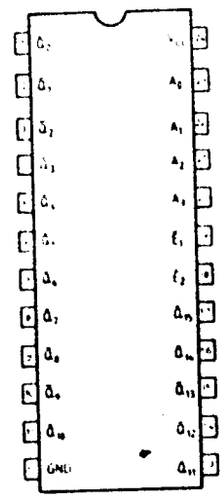
LS154 is a 4-line-to 15-line decoder. It provides coding of four binary-coded inputs into one of fteen mutually exclusive outputs when both strobe inputs. E_1 and E_2, are in the low state. ch of the strobe input can be used as a data put to perform the demultiplexing function by ing the 4 input lines to address the output line d having the other strobe input low. When ther strobe input is high, all outputs are high.



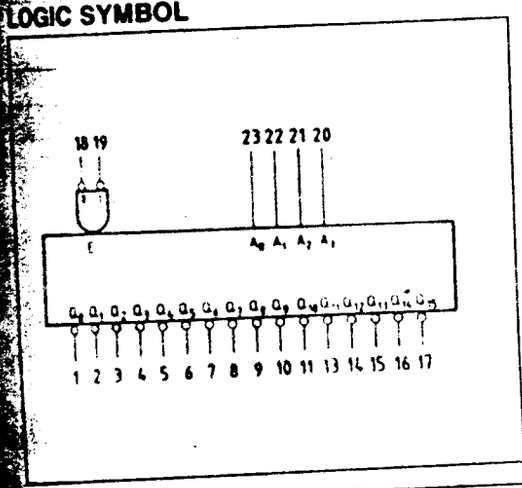
Plastic Package

PIN CONNECTION (top view)

DUAL IN LINE



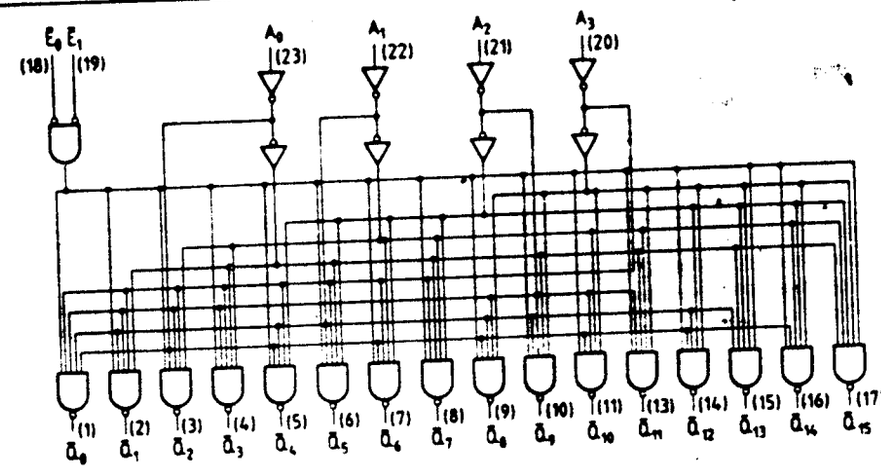
LOGIC SYMBOL



74LS154

SPEL

LOGIC DIAGRAM



V_{CC} = Pin 24
GND = Pin 12
( ) = Pin numbers

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	Input Voltage, Applied to Input	−0.5 to 7	V
V_O	Output Voltage, Applied to Output	0 to 5	V
I_I	Input Current, Into Inputs	−30 to 1	mA
I_O	Output Current, Into Outputs	50	mA

GUARANTEED OPERATING RANGES :

SUPPLY VOLTAGE : 4.75 – 5.25 VOLTS
TEMPERATURE : 0 – 70°C

TRUTH TABLE

INPUTS						OUTPUTS														
E_0	E_1	A_3	A_2	A_1	A_0	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care

AC WAVEFORMS

Fig. 1

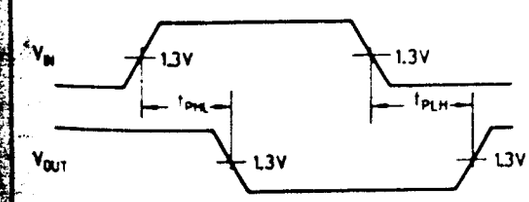
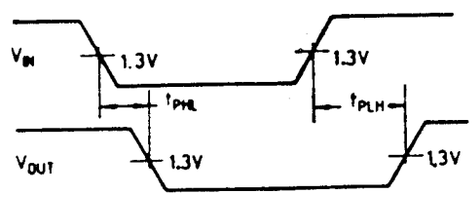


Fig. 2



SPEL

74LS32

QUAD 2-INPUT OR GATE

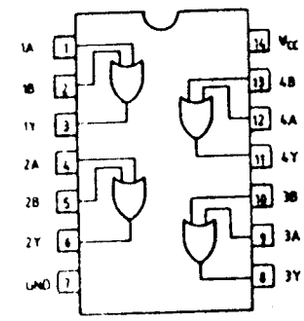
DESCRIPTION

74LS32 is a high speed QUAD 2-INPUT OR GATE fabricated in LOW POWER SCHOTTKY technology.

Plastic Package

PIN CONNECTION (top view)

DUAL IN LINE



LOGIC DIAGRAM AND TRUTH TABLE

A	B	Y
L	L	L
X	H	H
H	X	H

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to 7	V
V_I	Input Voltage, Applied to Input	-0.5 to 15	V
V_O	Output Voltage, Applied to Output	-0.5 to 5.5	V
I_I	Input Current, Into Inputs	-30 to 5	mA
I_O	Output Current, Into Outputs	50	mA

GUARANTEED OPERATING RANGES :

SUPPLY VOLTAGE : 4.75 – 5.25 VOLTS
TEMPERATURE : 0 – 70°C

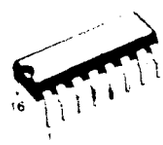
SPEL

74LS147/148

10-LINE-TO-4-LINE AND 8-LINE-TO-3-LINE PRIORITY ENCODERS

DESCRIPTION

These priority Encoders decode the inputs to ensure that only the highest order data line is encoded. All inputs and outputs data of both devices are active at the low logic level. The LS147 encodes nine data lines to four-line (8-4-2-1) BCD > The implied decimal zero condition requires no input condition because zero is enclosed when all nine data lines are at a high logic level. The LS148 encloses eigh data lines to three line (4-2-1) binary (octal) Cascadind circuitry (Enable input EI and Enable Output EO) has been provided to allow octal expansion without needing external circuitry.

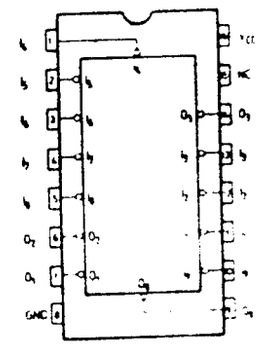


Plastic Package

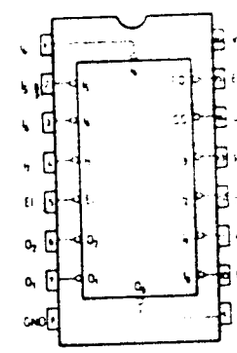
PIN CONNECTION (top view)

DUAL IN LINE

LS147



LS148



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	0 to 10	V
I_I	Input Current, Into Inputs	– 30 to 5	mA
I_O	Output Current, Into Outputs	50	mA

GUARANTEED OPERATING RANGES :

SUPPLY VOLTAGE · 4.75 – 5 25 VOLTS
TEMPERATURE 0 – 70 C

74LS147/148

SPEL

TRUTH TABLE

LS147

INPUTS									OUTPUTS			
1	2	3	4	5	6	7	8	9	D	C	B	A
H	H	H	H	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	X	L	L	H	H	L
X	X	X	X	X	X	X	L	H	L	H	H	H
X	X	X	X	X	X	L	H	H	H	L	L	L
X	X	X	X	X	L	H	H	H	H	L	L	H
X	X	X	X	L	H	H	H	H	H	L	H	L
X	X	X	L	H	H	H	H	H	H	L	H	H
X	X	L	H	H	H	H	H	H	H	H	L	L
X	L	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	L

LS148

INPUTS									OUTPUTS				
EI	0	1	2	3	4	5	6	7	A2	A1	A0	GS	EO
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

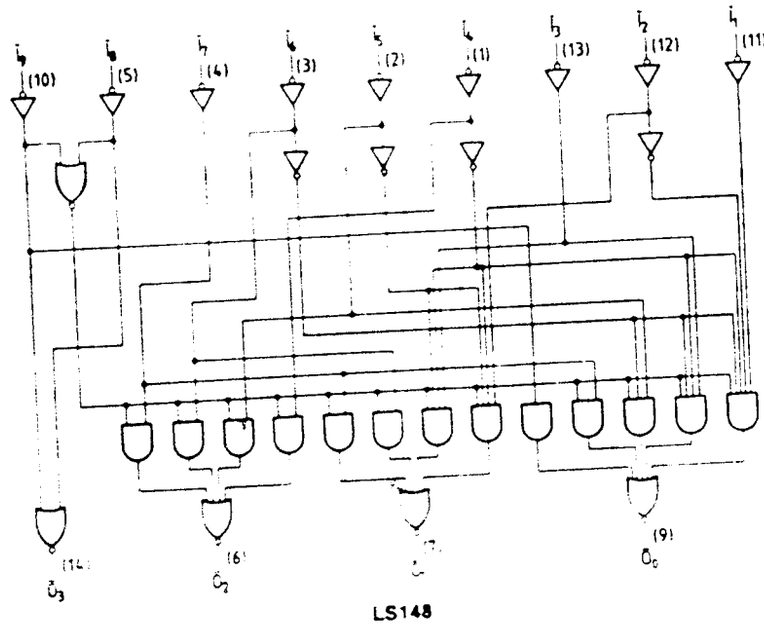
L = LOW Voltage Level - H = HIGH Voltage Level - X = Don't Care

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

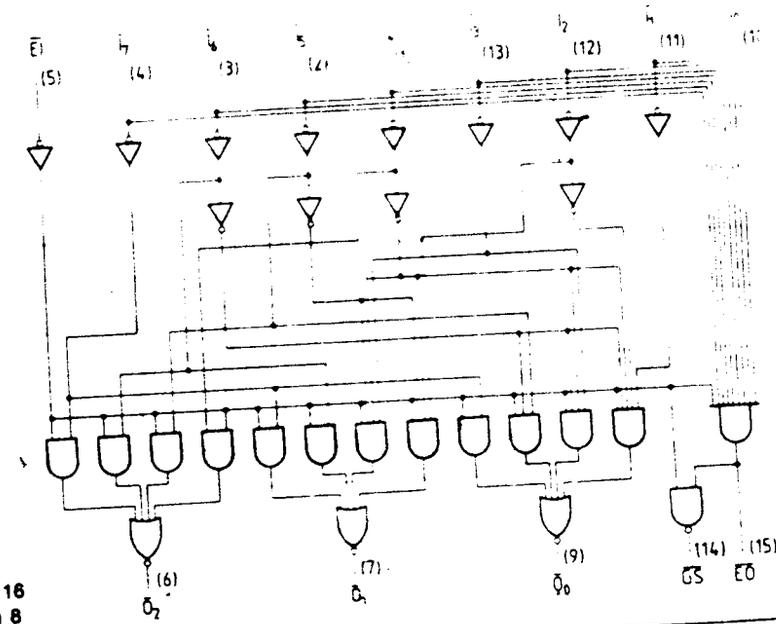
Symbol	Parameter	Limits			Test Conditions (Note 1)		Units
		Min.	Typ.	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed input HIGH Voltage for all Inputs		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed input LOW Voltage for all Inputs		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = - 18mA		V
V_{OH}	Output HIGH Voltage	2.7	3.5		V_{CC} = MIN, I_{OH} = - 400µA, V_{IN} = V_{IH} or V_{IL} per Truth Table		V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0mA	V_{CC} = MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table	V
			0.35	0.5	I_{OL} = 8.0mA		
I_{IH}	Input HIGH Current All Others Inputs 1-7 (LS148)			20 40	V_{CC} = MAX, V_{IN} = 2.7V		µA
	All Others Inputs 1-7 (LS148)			0.1 0.2	V_{CC} = MAX, V_{IN} = 7.0V		mA
I_{IL}	Input LOW Current All Others Inputs 1-7 (LS148)			- 0.4 - 0.8	V_{CC} = MAX, V_{IN} = 0.4V		mA
I_{OS}	Output Short Circuit Current (Note 2)	- 20		- 120	V_{CC} = MAX, V_{OUT} = 0V		mA
I_{CC}	Power Supply Current			20	V_{CC} = MAX, Inputs 7, EI, GND, Others Open		mA
				17	V_{CC} = MAX, A Inputs		

FUNCTIONAL BLOCK DIAGRAMS

LS147



LS148



V_{CC} = Pin 16
GND = Pin 8
( ) = Pin number

AC CHARACTERISTICS : T_A = 25 C (74LS147)

Symbol	From (Input)	To (Output)	Waveforms	Limits Min.	Typ.	Max.	Test Conditions	Units
t_{PLH}	Any	Any	In-phase output		12	18	C_L = 15pF	ns
t_{PHL}					12	18		
t_{PLH}	Any	Any	Out-of-phase output		21	33	R_L = 2 kΩ	ns
t_{PHL}					15	23		

Notes:
1) For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
2) Not more than one output should be shorted at a time.
3) Typical values are at V_{CC} = 5.0V, T_A = 25°C
4) Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

AC CHARACTERISTICS : T_A = 25°C (74LS148)

Symbol	From (Input)	To (Output)	Waveforms	Limits Min.	Typ.	Max.	Test Conditions	Units
t_{PLH}	1 thru 7	A0, A1 or A2	In-Phase output		14	18	C_L = 15pF R_L = 2kΩ	ns
t_{PHL}					15	25		
t_{PLH}	1 thru 7	A0, A1 or A2	Out-of-Phase output		20	36		ns
t_{PHL}					16	29		
t_{PLH}	0 thru 7	EO	Out-of-Phase output		7.0	18		ns
t_{PHL}					25	40		
t_{PLH}	0 thru 7	GS	In-Phase output		35	55		ns
t_{PHL}					9.0	21		
t_{PLH}	EI	A0, A1 or A2	In-Phase output		16	25		ns
t_{PHL}					12	25		
t_{PLH}	E1	GS	In-Phase output		12	17		ns
t_{PHL}					14	36		
t_{PLH}	E1	E0	In-Phase output		12	21		ns
t_{PHL}					23	35		

Dual timer

NE/SA/SE556/NE556-1

DESCRIPTION

Both the 556 and 556-1 Dual Monolithic timing circuits are highly stable controllers capable of producing accurate time delays or oscillation. The 556 and 556-1 are a dual 555. Timing is provided by an external resistor and capacitor for each timing function. The two timers operate independently of each other, sharing only V_{CC} and ground. The circuits may be triggered and reset on falling waveforms. The output structures may sink or source 200mA.

FEATURES

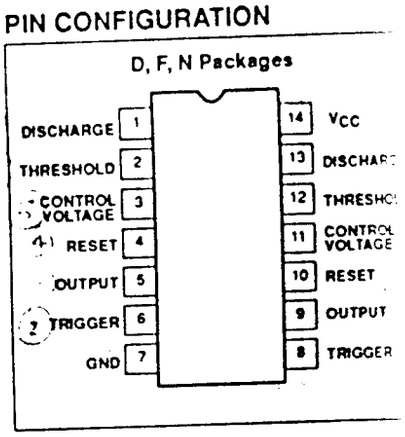
- Turn-off time less than 2µs (556-1, 1C)
- Maximum operating frequency >500kHz (556-1, 1C)
- Timing from microseconds to hours
- Replaces two 555 timers
- Operates in both astable and monostable modes
- High output current
- Adjustable duty cycle
- TTL compatible
- Temperature stability of 0.005%/°C
- SE556-1 compliant to MIL-STD or JAN available from Signetics' Military Division

APPLICATIONS

- Precision timing
- Sequential timing
- Pulse shaping
- Pulse generator
- Missing pulse detector

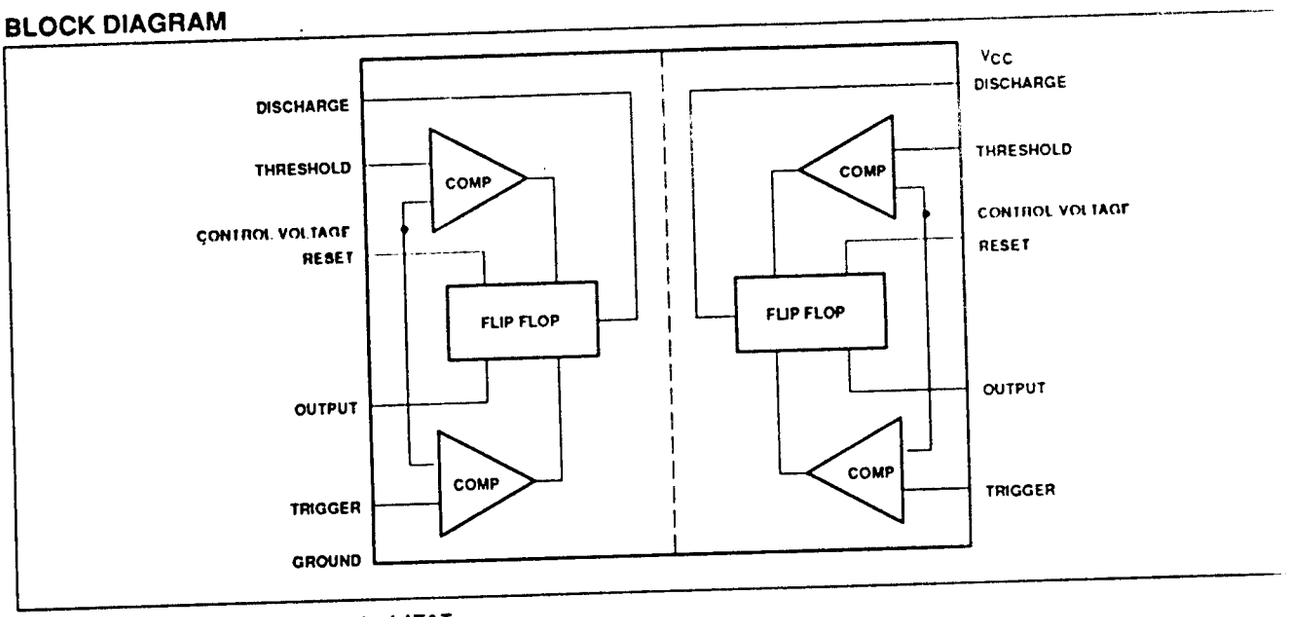
PIN CONFIGURATION

D, F, N Packages



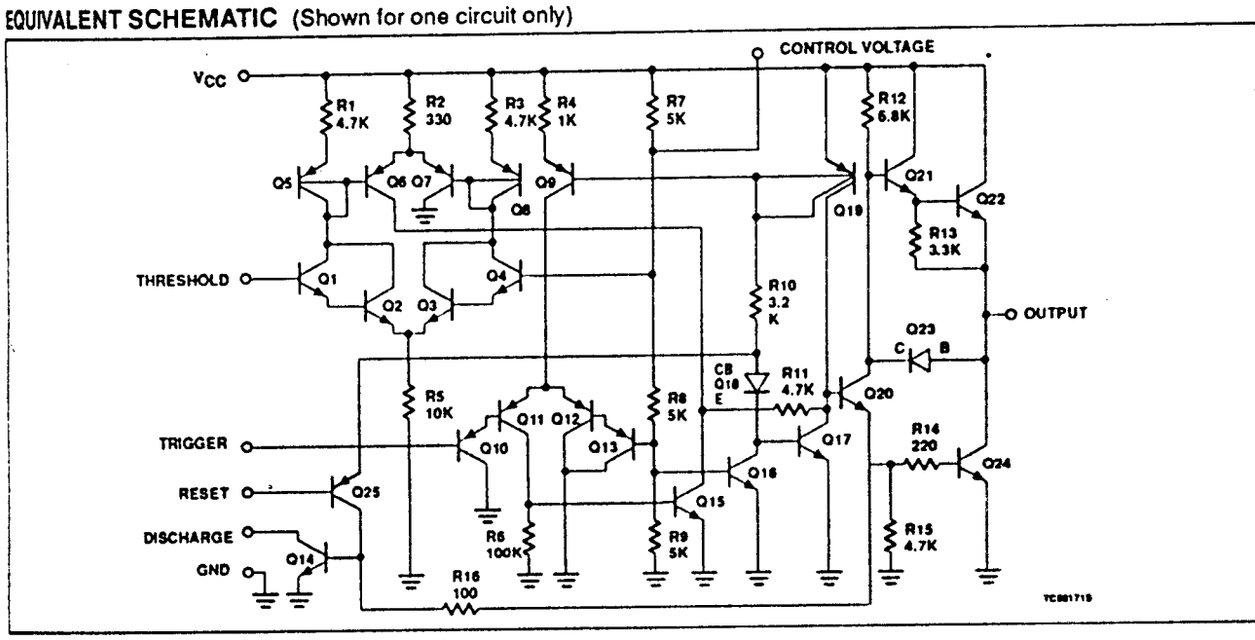
- Tone burst generator
- Pulse width modulation
- Time delay generator
- Frequency division
- Touch-Tone® encoder
- Industrial controls
- Pulse position modulation
- Appliance timing
- Traffic light control

BLOCK DIAGRAM



®Touch-Tone is a registered trademark of AT&T

EQUIVALENT SCHEMATIC (Shown for one circuit only)



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
14-Pin Plastic SO	0 to +70°C	NE556D
14-Pin Cerdip	0 to +70°C	NE556F
14-Pin Plastic DIP	0 to +70°C	NE556N
14-Pin Cerdip	0 to +70°C	NE556-1F
14-Pin Plastic DIP	0 to +70°C	NE556-1N
14-Pin Plastic DIP	-40°C to +85°C	SA556N
14-Pin Cerdip	-55°C to +125°C	SE556F
14-Pin Plastic DIP	-55°C to +125°C	SE556N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage		
	NE/SA556, 556-1, SE556C, SE556-1C	+16	V
	SE556-1, SE556	+18	V
P_D	Maximum allowable power dissipation[1]	800	mW
T_A	Operating temperature range		
	NE556-1, NE556	0 to +70	°C
	SA556	-40 to +85	°C
	SE556	-55 to +125	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	+300	°C

NOTES:
1. The junction temperature must be kept below 125°C for the D package and below 150°C for the N and F packages. At ambient temperatures above 25°C, where this limit would be exceeded, the Maximum Allowable Power Dissipation must be derated by the following:
   D package 115°C/W
   N package 80°C/W
   F package 100°C/W

ELECTRICAL CHARACTERISTICS

T_A=25°C, V_{CC}=+5V to +15V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	SE556/556-1			NE/SA556/SE556C NE556-1/SE556-1C			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply voltage		4.5		18	4.5		16	V
I_{CC}	Supply current (low state)[1]	V_{CC}=5V, R_L=∞		6	10		6	12	mA
		V_{CC}=15V, R_L=∞		20	24		20	30	mA
	Timing error (monostable)	R_A=2kΩ to 100kΩ							
t_M	Initial accuracy[2]	C=0.1μF		0.5	2.0		0.75	3.0	%
$\Delta t_M/\Delta T$	Drift with temperature	T=1.1 RC		30	100		50	150	ppm/°C
$\Delta t_M/\Delta V_S$	Drift with supply voltage			0.05	0.2		0.1	0.5	%/V
	Timing error (astable)	R_A, R_B=1kΩ to 100kΩ							
t_A	Initial accuracy[2]	C=0.μF		4	6		5	13	%
$\Delta t_A/\Delta T$	Drift with temperature	V_{CC}=15V		400	500		400	500	ppm/°C
$\Delta t_A/\Delta V_S$	Drift with supply voltage			0.15	0.6		0.3	1	%/V
V_C	Control voltage level	V_{CC}=15V	9.6	10.0	10.4	9.0	10.0	11.0	V
		V_{CC}=5V	2.9	3.33	3.8	2.6	3.33	4.0	V
V_{TH}	Threshold voltage	V_{CC}=15V	9.4	10.0	10.6	8.8	10.0	11.2	V
		V_{CC}=5V	2.7	3.33	4.0	2.4	3.33	4.2	V
I_{TH}	Threshold current[3]	V_{CC} = 15V, V_{TH} = 10.5V		30	250		30	250	nA
V_{TRIG}	Trigger voltage	V_{CC}=15V	4.8	5.0	5.2	4.5	5.0	5.6	V
		V_{CC}=5V	1.45	1.67	1.9	1.1	1.67	2.2	V
I_{TRIG}	Trigger current	V_{TRIG}=0V		0.5	0.9		0.5	2.0	μA
V_{RESET}	Reset voltage[5]		0.4	0.7	1.0	0.4	0.7	1.0	V
	Reset current	V_{RESET}=0.4V	0.4	0.1	0.4	0.4	0.1	0.6	mA

ELECTRICAL CHARACTERISTICS (Continued)

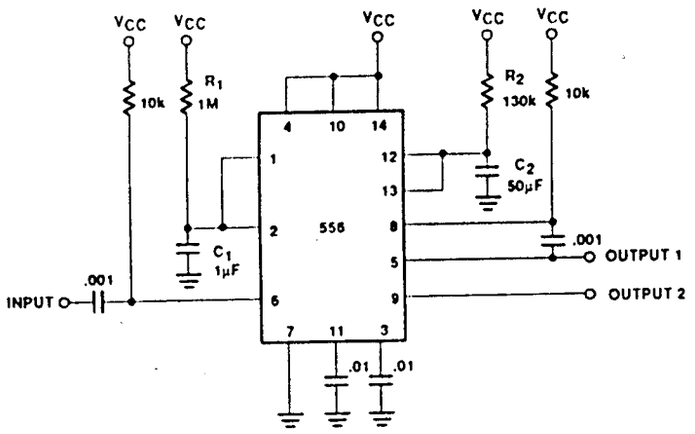
SYMBOL	PARAMETER	TEST CONDITIONS	SE556/556-1			NE/SA556/SE556C, NE556-1/SE556-1C			UNIT
			Min	Typ	Max	Min	Typ	Max	
I_{RESET}	Reset current	V_{RESET}=0V		0.4	1.0		0.4	1.5	mA
V_{OL}	Output voltage (low)	V_{CC}=15V I_{SINK}=10mA		0.1	0.15		0.1	0.25	V
		I_{SINK}=50mA		0.4	0.5		0.4	0.75	V
	SE556	I_{SINK}=100mA		2.0	2.25				V
	NE/SA556						2.0	3.2	V
	NE556-1						2.0	2.5	V
		I_{SINK}=200mA		2.5			2.5		V
		V_{CC}=5V I_{SINK}=8mA		0.1	0.2		0.25	0.3	V
		I_{SINK}=5mA		0.05	0.15		0.15	0.25	V
V_{OH}	Output voltage (high)	V_{CC}=15V I_{SOURCE}=200mA		12.5			12.5		V
		I_{SOURCE}=100mA	13.0	13.3		12.75	13.3		V
		V_{CC}=5V I_{SOURCE}=100mA	3.0	3.3		2.75	3.3		V
t_{OFF}	Turn-off time[6] NE556-1	V_{RESET}=V_{CC}		0.5	2.0		0.5		µs
t_R	Rise time of output			100	200		100	300	ns
t_F	Fall time of output			100	200		100	300	ns
	Discharge leakage current			20	100		20	100	nA
	Matching characteristics[4]								
	Initial accuracy[2]			0.5	1.0		1.0	2.0	%
	Drift with temperature			10			±10		ppm/°C
	Drift with supply voltage			0.1	0.2		0.2	0.5	%/V

NOTES:
1. Supply current when output is high is typically 1.0mA less.
2. Tested at V_{CC}=5V and V_{CC}=15V.
3. This will determine maximum value of R_A+R_B. For 15V operation, the max total R=10MΩ, and for 5V operation, the maximum total R=3.4MΩ.
4. Matching characteristics refer to the difference between performance characteristics for each timer section in the monostable mode.
5. Specified with trigger input high. In order to guarantee reset the voltage at reset pin must be less than or equal to 0.4V. To disable reset function, the voltage at reset pin has to be greater than 1V.
6. Time measured from a positive-going input pulse from 0 to 0.4 V_{CC} into the threshold to the drop from high to low of the output. Trigger is tied to threshold.

TYPICAL APPLICATIONS

One feature of the dual timer is that by utilizing both halves it is possible to obtain sequential timing. By connecting the output of the first half to the input of the second half via a 0.001μF coupling capacitor sequential timing may be obtained. Delay t_1 is determined by the first half and t_2 by the second half delay.

The first half of the timer is started by momentarily connecting Pin 6 to ground. When it is timed out (determined by $1.1R_1C_1$) the second half begins. Its duration is determined by $1.1R_2C_2$.

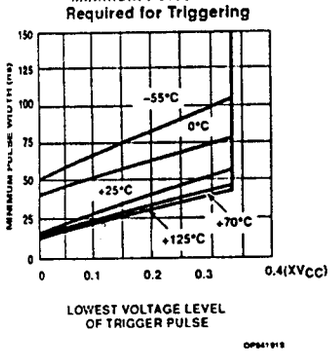


NOTE:
All resistor values are in Ω.

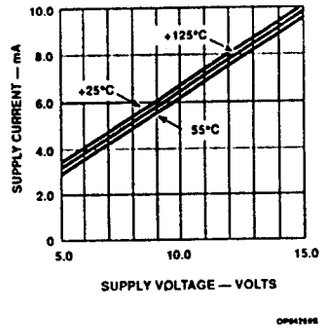
Sequential Timer

?ICAL PERFORMANCE CHARACTERISTICS

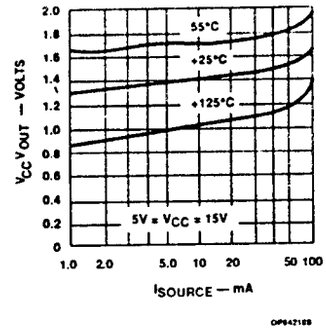
Minimum Pulse Width Required for Triggering



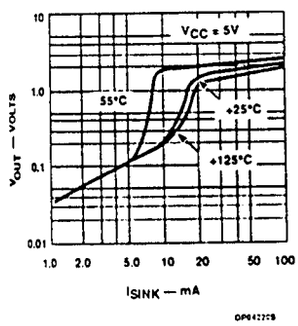
Supply Current VS Supply Voltage



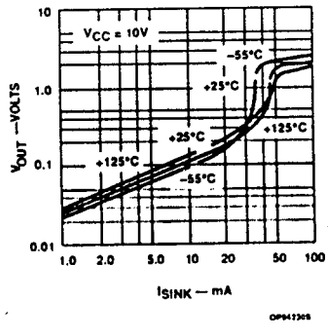
High Output Voltage Drop vs Output Source Current



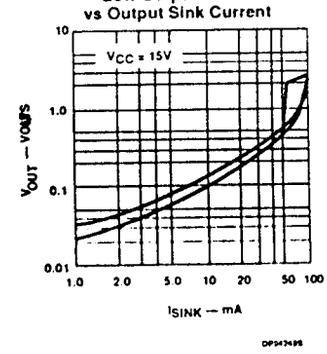
Low Output Voltage vs Output Sink Current



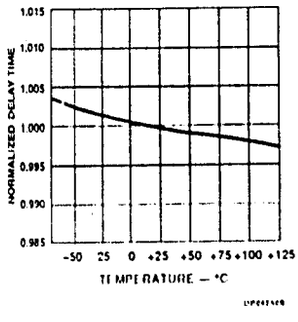
Low Output vs Output Sink Current



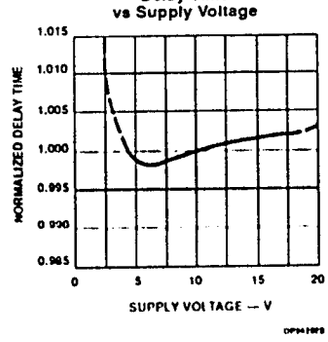
Low Output Voltae vs Output Sink Current



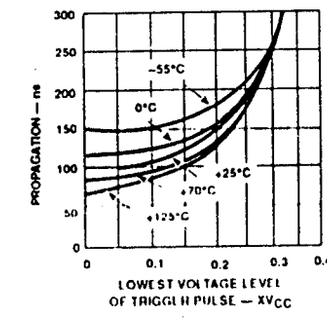
Delay Time vs Temperature



Delay Time vs Supply Voltage



Propagation Delay vs Voltage Level of Trigger Pulse



MITEL

ISO2-CMOS MT8870C/MT8870C-1
Integrated DTMF Receiver

9161-002-094-NA ISSUE 1 November 1987

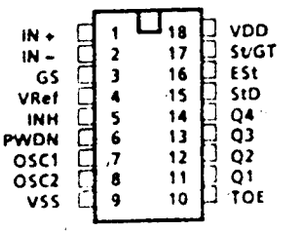
Features

- Complete DTMF Receiver
- Low Power Consumption
- Internal Gain Setting Amplifier
- Adjustable Guard Time
- Central Office Quality
- Power-down Mode
- [illegible] bit Mode

Applications

- Receiver System for British Telecom (BT) or CEPT Spec (MT8870C-1)
- Paging Systems
- Repeater Systems/Mobile Radio
- Credit Card Systems
- Remote Control
- Personal Computers
- Telephone Answering Machine

Pin Connections



Ordering Information

MT8870CE/MT8870CE-1	Plastic DIP
MT8870CC/MT8870CC-1	Cerdip
MT8870CS/MT8870CS-1	SOIC
	-40 °C to +85 °C

Description

The MT8870C/MT8870C-1 is a complete DTMF receiver integrating both the bandsplit filter and digital decoder functions, fabricated in Mitel's double poly ISO2-CMOS technology. The filter section uses switched capacitor techniques for high and low group filters; the decoder uses digital counting techniques to detect and decode all 16 DTMF tone-pairs into a 4-bit code. External component count is minimized by on chip provision of a differential input amplifier, clock oscillator and latched three-state bus interface.

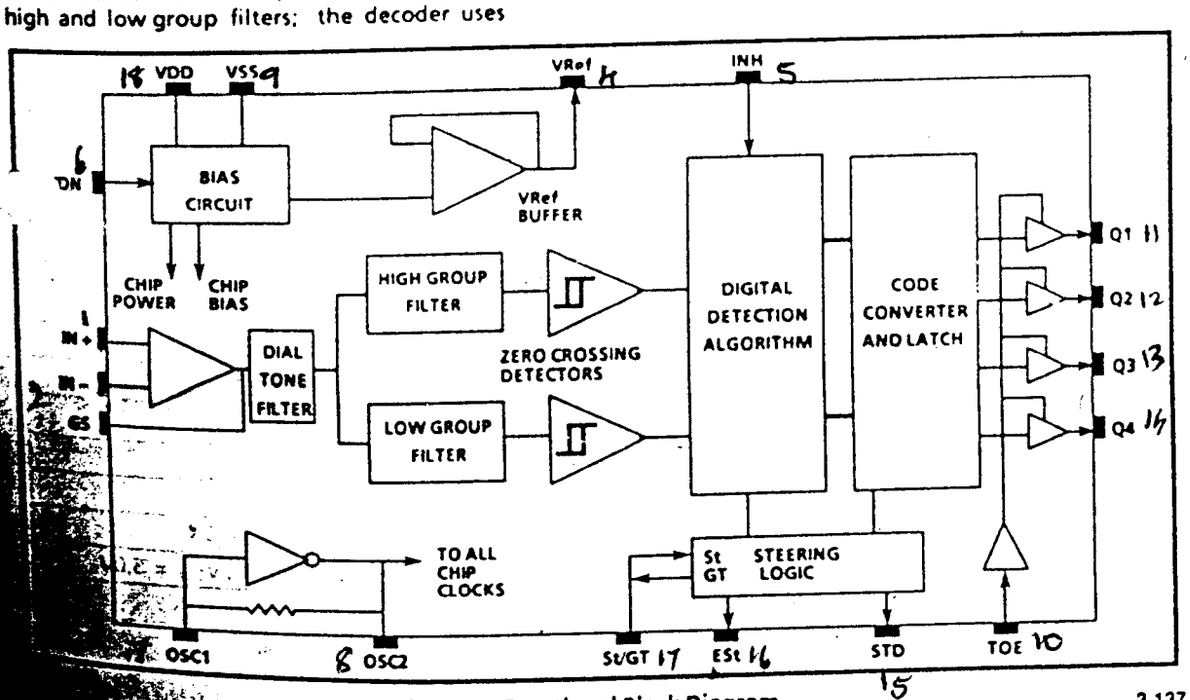


Figure 1 - Functional Block Diagram

Functional Description

The GTE G8870-1 DTMF Integrated Receiver provides the design engineer with not only low power consumption, but high performance in a small 18-pin DIP or 20-pin PLCC package configuration. The G8870-1's internal architecture consists of a band-split filter section which separates the high and low tones of the received pair, followed by a digital decode (counting) section which verifies both the frequency and duration of the received tones before passing the resultant 4-bit code to the output bus.

Filter Section

Separation of the low-group and high-group tones is achieved by applying the dual-tone signal to the inputs of two 9th-order switched capacitor bandpass filters. The bandwidths of these filters correspond to the bands enclosing the low-group and high-group tones (See Figure 3). The filter section also incorporates notches at 350 Hz and 440 Hz which provides excellent dial tone rejection. Each filter output is followed by a single-order switched capacitor section which smooths the signals prior to limiting. Signal limiting is performed by high-gain comparators, These comparators are provided with a hysteresis to prevent detection of unwanted low-level signals and noise. The outputs of the comparators provide full-rail logic swings at the frequencies of the incoming tones.

Decoder Section

The G8870-1 decoder uses a digital counting technique to determine the frequencies of the limited tones and to verify that these tones correspond to standard DTMF frequencies. A complex averaging algorithm is used to protect against tone simulation by extraneous signals (such as voice) while providing tolerance to small frequency variations. The averaging algorithm has been developed to ensure an optimum combination of immunity to "talk-off" and tolerance to the presence of interfering signals (third tones) and noise. When the detector recognizes the simultaneous presence of two valid tones (known as "signal condition"), it raises the "Early Steering" flag (ESt). Any subsequent loss of signal condition will cause ESt to fall.

Steering Circuit

Before the registration of a decoded tone pair, the receiver checks for a valid signal duration (referred to as "character-recognition-condition"). This check is performed by an external RC time constant driven by ESt. A logic high on ESt causes Vc (See Figure 4) to rise as the capacitor discharges. Providing signal condition is maintained (ESt remains high) for the validation period (t_{GTF}), Vc reaches the threshold (V_{TSt}) of the steering logic to register the tone pair, thus latching its corresponding 4-bit code (See Figure 2) into the output latch. At this point, the GT output is activated and drives Vc to V_{DD}. GT continues to drive high as long as ESt remains high. Finally, after a short delay to allow the output latch to settle, the "delayed steering" output flag (StD) goes high, signaling that a received tone pair has been registered. The contents of the output latch are made available on the 4-bit output bus by raising the three-state control input (TOE) to a logic high. The steering circuit works in reverse to validate the interdigit pause between signals. Thus, as well as rejecting signals too short to be considered valid, the receiver will tolerate signal interruptions (drop outs) too short to be considered a valid pause. This capability, together with the capability of selecting the steering time constants externally, allows the designer to tailor performance to meet a wide variety of system requirements.

Guard Time Adjustment

In situations which do not require independent selection of receive and pause, the simple steering circuit of Figure 4 is applicable. Component values are chosen according to the following formula:

$$t_{REC} = t_{DP} + t_{GTP}$$

$$t_{GTP} = 0.67\ RC$$

The value of t_{DP} is a parameter of the device and t_{REC} is the minimum signal duration to be recognized by the receiver. A value for C of 0.1 uF is recommended for most applications, leaving R to be selected by the designer. For example, a suitable value of R for a t_{REC} of 40 milliseconds would be 300K. A typical circuit using this steering configuration is shown in Figure 1. The timing requirements for most telecommunication applications are satisfied with this circuit. Different steering arrangements may be used to select independently the guard times for tone-present (t_{GTP}) and tone-absent (t_{GTA}). This may be necessary to meet system specifications which place both accept and reject limits on both tone duration and interdigit pause.

Guard time adjustment also allows the designer to tailor system parameters such as talk-off and noise immunity. Increasing t_{REC} improves talk-off performance, since it reduces the probability that tones simulated by speech will maintain signal condition for long enough to be registered. On the other hand, a relatively short t_{REC} with a long t_{DP} would be appropriate for extremely noisy environments where fast acquisition time and immunity to drop-outs would be requirements. Design information for guard time adjustment is shown in Figure 5.

Input Configuration

The input arrangement of the G8870-1 provides a differential input operational amplifier as well as a bias source (V_{REF}) which is used to bias the inputs at mid-rail.

Provision is made for connection of a feedback resistor to the op-amp output (GS) for adjustment of gain.

In a single-ended configuration, the input pins are connected as shown in Figure 1 with the op-amp connected for unity gain and V_{REF} biasing the input at ½V_{DD}. Figure 6 shows the differential configuration, which permits the adjustment of gain with the feedback resistor R_5.

2) Not more than one output should be shorted at a time.
3) Measure I_{CC} with all inputs grounded and all output open.
4) Typical values are at $V_{CC} = 5.0V$, $T_A = 25°C$
5) Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

BILL OF MATERIAL

S.NO.	DESCRIPTION	QUANTITY/ UNIT	LOCATION
1.	IC - 1240	1	U1
2.	IC - 4013	2	U2,U9
3.	UM66	1	U3
4.	IC - 7404	2	U4,U5
5.	IC - 4081	2	U6,U8
6.	IC - 8870	1	U7
7.	IC - 74LS148	4	U10,U11,U12,U13
8.	IC - 74LS154	1	U14
9.	IC - 556	1	U16
10.	IC - 74LS32	3	U15,U17,U18
11.	IC - LM324	1	U19.
RESISTORS			
12.	1.2KΩ	2	R1,R2
13.	20KΩ	1	R3
14.	10KΩ	12	R4,R6,R10,R11,R35, R40,R45,R50,R54,R55, R57
15.	600KΩ	1	R5
16.	4.7KΩ	2	R7,R8
17.	470KΩ	2	R9,R17
18.	100KΩ	4	R14,R14A,R12,R13
19.	450KΩ	1	R15
20.	560KΩ	1	R15A
21.	330KΩ	1	R16
22.	5.6KΩ	12	R18,R19,R21,R24,R25,R27, R29,R31,R34,R39,R44,R49
23.	120 Ω	8	R19A,R20,R22,R23,R26,R28, R30,R32
24.	22 KΩ	4	R36,R41,R46,R51
25.	220 Ω	8	R37,R38,R42,R43,R47,R48, R52,R53

CAPACITORS

26.	CECE - 1μf	3	C1,C10,C10A
27.	CECE - 470μf	1	C2
28.	CECR - 100nf	4	C3,C5,C6,C7
29.	CECR - 10nf	2	C4,C8
30.	CECE - 10μf	5	C9,C11,C12,C13,C14
31.	CECE - 100μf	1	C9A
32.	CECE - 0.01μf	2	C10b,C10c

TRANSISTORS

33.	BC546	4	Q1,Q2,Q3,Q4
34.	MPSA44	8	Q5,Q6,Q7,Q8,Q9,Q10,Q11,Q12

DIODES

35.	ZENER DIODE 4V7	9	D1,D8,D11,D16,D19,D26,D27, D28,D29
36.	IN4148	23	D2,D3,D4,D5,DA1,D6A,D6D, D7, D9,D10,12,D13,D14,D15,D17, D18,D20,D21,D22,D23,D24,D25
37.	IN4004	8	IN POWER SUPPLY CARD
38.	RELAYS	10	RL1,RL2,RL3,RL4,RL5,RL6, RL7, RL8, RL9, RL10.
39.	FEED BRIDGE COIL	4	L1,L2,L3,L4,L5,L6,L7,L8.
40.	TRANSFORMER	1	-
41.	REGULATOR IC's (7824 & 7805)	2	POWER SUPPLY CARD