Micro Controller Based Real Time Clock/Calendar/Timer

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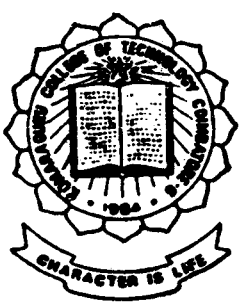

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Certificate

This is to Certify that the Report entitled

"MICROCONTROLLER BASED REAL TIME CLOCK/TIMER/CALENDAR"

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Dedicated to

"Our Beloved Parents"

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Synopsis

SYNOPSIS

This project is concerned with the design of an 8051 microcontroller based Real Time Clock (RTC) with control applications. The application includes a timer which is used for displaying the real time and for controlling a D.C Motor.

Time is displayed in seconds, minutes, hours along with day of week, day of month and month of year. A leap year provision is provided here. A relay is used to perform the on/off control for a d.c.motor. It's operational period is programmable. A 4 x 4 matrix Keypad is interfaced to the microcontroller using 8279 keyboard display controller. Its function is to facilitate entering of parameters for the system by the user. The seven segment display is also driven from the Keyboard/Display controller.

This application mainly suits small requirements in an industrial environment where it replaces manual control with automatic control. It main functions are programmable control of machines using relays. It can also be extended to include other sophisticated controls.

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Introduction

1. INTRODUCTION

The earlier generation of computers, as we all know originated from the vacuum tubes. Semiconductor technology development led to the invention of the transistor, which is the most indispensable device in present day electronics. Integrated circuit technology made it possible to integrate a lot of devices on a single chip and further technology improvements reduced the cost and size of ICs. This eventually led to the micro controller which is flooding the electronics industry on account of its wide spread usage. A microcontroller is a microprocessor with peripherals on chip facility. It is one of the most accurate time measuring devices. The reason behind its accuracy is the presence of an external crystal which controls the oscillator frequency. It has the capacity to control the operational period of a machine with appropriate interfaces.

The real time clock IC MM58274 which plays the main role in this project. It performs the time keeping in the system. A description about its functions, features, modes of operation and applications are provided in a later section.

Memory requirements of the system are met by external memory ICs. 8K program memory and 8k data memory is provided by IC 2764 ROM and IC 6264

RAM respectively. These are both interfaced with the controller using decoders and latches.

In order to take care of scanning the keyboard, displaying and refreshing of data and thereby minimise the controller's functions, a keyboard/display interface is used. It is the INTEL Chip 8279 which handles the functions mentioned above. The display used here is [illegible] a seven segment common anode display. The multiplexed displays are driven by BC108 transistors which in turn are driven by the outputs from the IC8279.

All peripherals used in this system are connected using memory mapped I/O configuration. The hardware has been designed using the above mentioned devices.

The software is written in the assembly language of the 8051 microcontroller. A top-down modular design approach has been followed. The entire logic and the program are explained in chapter 7.

This system can be extended for control of machines other than d.c.motors and it is very flexible because it is mainly controlled through software.

8051 Microcontroller

2. 8051 MICROCONTROLLER.

2.1 INTRODUCTION

The 8051 is the original member of the MCS-51 family and is the core for all MCS-51 devices. The features of 8051 core are :

* 8 bit CPU optimised for control applications.
* Extensive Boolean processing capabilities.
* 64K program memory address space
* 64K data memory address space.
* On Chip ROM
* On chip data RAM.
* 32 bi-directional and individually addressable I/O lines.
* 16 bit counters/timers.
* Full duplex UART
* On chip clock oscillator.

2.2 ARCHITECTURE

The architectural features of MCS-8051 include memory, ports and drivers, timing and control, interrupt serial port and timer blocks, ALU, PSW and oscillator.

The program memory consists of PC incrementer, buffer and program address register. These are inter-connected among themselves and to the ports P0 & P2.

The RAM addresses are pointed out by the RAM address register. The RAM is connected to other parts via the data bus.

The accumulator, B register, PSW are a part of the data memory and are categorised as special function registers and occupy the upper 128 bytes.

The timing and control registersare used for synchronisation.

There are four ports each with a latch and output drivers. Port 0 is used as a multiplexed address/data bus and port 2 is used as a higher order address bus.

There are 5 interrupts in 8051 with two priority levels. They are the two external interrupts, two timer interrupts and one serial interrupt.

The timer/counter is two in number. The serial port is used for serial data communication.

The oscillator provides the time keeping signals and produces machine cycles for syncronising the initial operation of the processor.

2.3. MEMORY ORGANISATION

All MCS-51 devices have separate address spaces for program and data memory. The logical separation of program and data memory allows the data memory to be accessed by 8-bit addresses, which can be more quickly stored and manipulated by an 8 - bit CPU. Nevertheless, 16 - bit data memory addresses can also be generated through the DPTR register. Program memory can only be read, not written to. There can be upto 64k bytes of program memory. In the ROM version the lowest 4K bytes of program memory are provided on-chip. The read strobe for external program memory access is the signal $\overline{\text{PSEN}}$.

Data memory occupies a separate address space. Upto 64K bytes of external RAM can be addressed in the external data memory space. The CPU generates read and write signals $\overline{\text{RD}}$ and $\overline{\text{WR}}$, as needed during external data memory accesses.

2.3.1 PROGRAM MEMORY

After reset, the CPU begins execution from location 0000H. Each interrupt is assigned a fixed location in program memory. It extends from 0003H to 0033H

for 5 interrupts. If the interrupt is not going to be used, its service location is available as general purpose program memory. The interrupt service locations are spaced at 8-byte intervals.

The lowest 4K bytes program memory can be either in the on-chip ROM or in an external ROM. This selection is made by strapping the $\overline{EA}$ pin to either Vcc or Vss. If $\overline{EA}$ pin is strapped to Vcc then program fetches to addresses 0000H through 0FFFH are directed to the internal ROM. Program fetches to addresses 1000H through FFFFH are directed to external ROM. If $\overline{EA}$ pin is strapped to Vss, then all program fetches are directed to external ROM. The read strobe to external ROM, $\overline{PSEN}$ is used for all external program fetches.

The hardware configuration for external program execution is shown in figure 2.3.1. 16 I/O lines (Ports 0 and 2) are dedicated to bus functions during external program fetches. Port 0 serves as a multiplexed address/data bus. It outputs the low byte of the program counter (PCL), and then goes into a float state awaiting the arrival of the code byte from the program memory. During the time that the lower order byte of the program counter is valid on P0, the signal ALE (Address Latch Enable) clocks this byte into an address latch. Meanwhile, port 2

emits the high order byte of the program counter (PCH). Then $\overline{\text{PSEN}}$ strobes the ROM and the code byte is read into the microcontroller.

Program memory addresses are always 16-bits wide, even though the actual amount of program memory used may be less than 64 K bytes. External program execution sacrifices two of the 8-bit ports, P0 and P2 to the function of addressing the program memory.

2.3.2 DATA MEMORY

Fig 2.3.2 shows the external and internal data memory spaces available to the MCS - 51 user.

For accessing external RAM, port 0 serves as a multiplexed address/ data bus to the RAM. The CPU generates read and write signals as needed during external RAM accesses. There can be upto 64k bytes of external data memory. External data memory addresses can be either 1 or 2 bytes wide. One byte addresses are often used in conjunction with one or more I/O lines to page the RAM. Two byte addresses can also be used, in which case the higher order addressed byte is emitted at port 2.

Internal data memory is divided into 3 blocks, which are generally referred to as the lower 128, upper 128 and SFR space. Internal data memory addresses are always one byte wide which implies an address space of only 256 bytes. However, the addressing modes for internal RAM can in fact accommodate 384 bytes using a simple trick. Direct addresses higher than 7FH access one memory space, and indirect addresses higher than 7FH access a different memory space. Thus the upper 128 and the SFR space occupy the same block of addresses, 80H through FFH, although they are physically separate entities.

The lower 128 bytes of RAM are present in all MCS-51 devices. The lowest 32 bytes are grouped in to four banks of 8 registers. Program instructions call out these registers as R0 through R7. Two bits in the program status word (PSW) select which register bank is currently in use. This allows more efficient use of code space since register instructions are shorter than instructions that use direct addressing.

The next 16 bytes above the register banks form a block of bit - addressable memory space. The MCS 51 instruction set includes a wide selection of single bit instructions and the 128 bits in this area can be directly addressed by these instructions. All of the bytes in the lower 128 can be accessed by either direct or indirect addressing.

SFRs include port latches, timers, peripheral control etc. These registers can be accessed only by direct addressing.

2.3.2.1 SPECIAL FUNCTION REGISTERS (SFR)

A map of the on chip memory area called SFR space is shown in fig.2.3.3. All of the addresses are not occupied and the user software should not write 1's to these locations.

ACCUMULATOR

Acc is the accumulator register. The mnemonics for acc-specific instructions refer to Acc as A.

B REGISTER

The B register is used during multiply & divide operations. For other instructions it can be treated as another scratch pad register.

PSW

The PSW register contains program status information.

Stack Pointer

The SP register is 8 bits wide. It is incremented before data is stored during PUSH and CALL executions. While the stack may reside anywhere in the on-chip

RAM, the SP is initialised to 07H after a reset. This causes the stack to begin at location 08H.

DATA POINTER

The data pointer consists of a higher order byte (DPH) and a lower order byte (DPL). Its intended function is to hold a 16-bit address. It can also be used as two 8-bit registers.

PORT 0 - 3

P0, P1, P2, P3 are the SFR latches of ports 0,1,2,3.

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SERIAL DATA BUFFER

The serial data buffer is actually two separate registers, a transmit buffer and a receive buffer registers. When data is moved to SBUF, it goes to the transmit buffer. When data is moved from SBUF, it comes from the receive buffer.

TIMER REGISTERS

Register pairs (TH0, TL0) , (TH1, TL1) are the 16 - bits counting registers for timer/counter 0,1 respectively.

CONTROL REGISTERS

SFRs IP, IE, TMOD, TCON, SCON and PCON contain control and status bits for the interrupt system, the timer/counters and the serial port.

Those SFRs that have their bits assigned for various functions are listed in this section. A brief description of each bit is provided for quick reference.

PSW:PROGRAM STATUS WORD. BIT ADDRESSABLE

CY	AC	F0	RS1	RS0	OV	-	P

CY	PSW:7	Carry Flag
AC	PSW:6	Auxillary Carry Flag
F0	PSW:5	Flag 0 available to the user for general purpose
RS1	PSW:4	Register Bank selector bit 1.
RS0	PSW:3	Register Bank selector bit 0
0V	PSW:3	Overflow Flag
-	PSW.1	User definable flag.
P	PSW.0	Parity flag.

PCON:POWER CONTROL REGISTER NOT BIT ADDRESSABLE

SMOD	-	-	-	GF1	GF0	PD	IDL

SMOD Double baud rate bit. If Timer 1 is used to generate baud rate and SMOD = 1, the baud rate is doubled when the Serial Port is used in modes 1,2 or 3.

-	Not implemented, reserved for future use.
-	Not implemented, reserved for future use.
-	Not implemented, reserved for future use.
GF1	General purpose flag bit.
GF0	General purpose flag bit.
PD	Power down bit, Setting this bit activates power down operation in the 80C51BH. (Available only in CHMOS).
IDL	Idle Mode bit, Setting this bit activates Idle Mode operation in the 80C51BH (Available only in CHMOS).

If 1's are written to PD and IDL at the same time, PD takes precedence.

INTERRUPTS

In order to use any of the interrupts in the MCS - 51, the following three steps must be taken.

1. Set the EA (enable all) bit in the IE register to 1.
2. Set the corresponding individual interrupt enable bits in the IE register to 1.
3. Begin the interrupt service routine at the corresponding vector address of that interrupt. See Table below.

Interrupt Vector	Vector Address
IE0	0003H
TF0	000BH
IE1	0013H
TF1	001BH
RI & TI	0023H

In addition, for external interrupts, pins INT0 and INT1 (P3.2 and P3.3) must be set to 1, and depending on whether the interrupts is to be level-or-transition activated, bits IT0 or IT1 in the TCON register may need to be set to 1.

ITx = 0 level-activated

ITx = 1 transition-activated

IE : INTERRUPT ENABLE REGISTER-BIT ADDRESSABLE

If the bit is 0, the corresponding interrupt is disabled. If the bit is 1, the corresponding interrupt is enabled.

EA	-	ET2	ES	ET1	EX1	ET0	EX0

EA — IE.7 Disables all interrupts. If EA = 0, no interrupt will be acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.

\- — IE.6 Not implemented, reserved for future use.

ET2 — IE.5 Enables or diables the Timer 2 overflow or capture interrupt (8052 only)

ES — IE.4 Enables or disables the serial port interrupt

ET1 — IE.3 Enables or disables the timer 1 overflow interrupt.

EX1 — IE.2 Enables or disables External Interrupt 1.

ET0 — IE.1 Enables or disables the Timer 0 overflow interrupt.

EX0 — IE.0 Enables or disables External Interrupt 0.

User software should not write 1's to reserved bits. These may be used in future MCS-51 products to invoke new features. In that case, the reset or inactive value of the bit will be 0, and its active value will be 1.

IP. INTERRUPT PRIORITY REGISTER-BIT ADDRESSABLE

If the bit is 0, the corresponding interrupt has a lower priority.

-	-	PT2	PS	PT1	PX1	PT0	PX0

--	IP.7 Not implemented. Reserved for future use.
--	IP.6 Not implemented. Reserved for future use.
PT2	IP.5 Defines the Timer 2 interrupt priority level (8052 only)
PS	IP.4 Defines the Serial Port interrupt priority level.
PT1	IP.3 Defines the Timer 1 interrupt priority level.
PX1	IP.2 Defines External Interrupt 1 priority level.
PT0	IP.1 Defines the timer 0 interrupt priority level.
PX0	IP.0 Defines the External Interrupt 0 priority level.

User software should not write 1's to reserved bits. These may be used in future MCS-51 products to invoke new features. In that case, the reset or inactive value of the new bit will be 0, and its active value will be 1.

TCON: TIMER/COUNTER CONTROL REGISTER-BIT ADDRESSABLE

TF1	TR1	TF0	TR0	IE1	IT1	ITE	IT0

TF1 — TCON:7 Timer 1 overflow flag. Set by hardware when the Timer/Counter 1 overflows. Cleared by hardware as processor vectors to the interrupt service routine.

TR1 — TCON:6 Timer 1 run control bit. Set/Cleared by software to turn Timer/counter 1 ON/OFF.

TF0 — TCON:5 Timer 0 overflow flag. Set by hardware when external interrupt edge is detected.

TR0 — TCON:4 Timer 0 run control bit. Set/cleared by softwareto turn Timer/Counter 1 ON/OFF.

IE1 — TCON:3 External Interrupt 1 edge flag. Set by hardware when External Interrupt edge is detected. Cleared by hardware when interrupt is processed.

IT1 — TCON.2 Interrupt 1 type control bit. Set/Cleared by software to specify falling edge/low level triggered External Interrupt.

IE0 — TCON.1 External Interrupt 0 edge flag. Set by hardware when External Interrupt edge detected. Cleared by hardware when interrupt is processed.

IT0 — TCON.0 Interrupt 0 type control bit. Set/Cleared by software to specify falling edge/low level triggered External Interrupt.

TMOD: TIMER/COUNTER MODE CONTROL REGISTER-NOT BIT ADDRESSABLE

GATE	C/T	M1	M0	GATE	C/T	M1	M0

GATE — When TRx (in TCON) is set and GATE=1, TIMER/COUNTERx will run only while INTx pin is high (hardwarecontrol). When GATE=0,TIMER/COUNTERx will run onlywhile TRx=1 (software control).

C/T	Timer or Counter selector. Cleared for Timer operation (input from internal system clock). Set for Counter operation (input from T x input pin)
M1	Mode selector bit
MO	Mode selector bit

2.3.3 ACCESSING EXTERNAL MEMORY

Accesses to external memory are of two types : accesses to external program memory and accesses to external data memory. Accesses to external program memory use signal $\overline{\text{PSEN}}$ as the read strobe. Accesses to external data memory use $\overline{\text{RD}}$ and $\overline{\text{WR}}$ to strobe the memory.

Fetches from external program memory always use a 16 - bit address. Accesses to external data memory can use either a 16 - bit address or an 8- bit address.

Whenever a 16 -bit address is used, the higher byte of the address comes out on port 2, where it is held for the duration of the read or write cycle. If an 8 - bit address is being used the contents of port 2 SFR remain at port 2 pins throughout the external memory cycle. This will facilitate paging.

In any case, the lower byte of the address is time multiplexed with the data byte on port 0. The ADDR/DATA signal drives both FETs in the port 0 output buffer. Signal ALE should be used to capture the address byte into an external latch. The address byte is valid at the negative transition of ALE. Then, in a write cycle, the data byte to be written appears on port 0 just before write pin is activated, and remains there until after write pin is deactivated. In a read cycle, the incoming byte is accepted at port 0 just before the read strobe is deactivated.

During any access to external memory, the CPU writes 0FFF H to the port 0 latch thus obliterating whatever information the

port 0 SFR may have been holding. If user writes to port 0 during an external memory fetch, the incoming code byte is corrupted. External program memory is accessed whenever $\overline{EA}$ signal is active or whenever the PC contains a number larger than 0FFFH. When the CPU is executing from external program memory , all 8 - bits of port 2 are dedicated to an output function and may not be used for general purpose I/O. During external program fetches they output the higher order byte of the PC.

2.4 PORT STRUCTURES

All four ports in the 8051 are bi-directional. Each consists of a latch, an output driver and an input buffer.

The output drivers of ports 0 & 2, and the input buffers of port 0, are used in accesses to external memory. In this application, port 0 outputs the low byte of the external memory address, time-multiplexed with the byte being written or read. Port 2 outputs the higher byte of the external memory address when the address is 16 - bits wide. Otherwise the port 2 pins continue to emit the P2 SFR content.

All the P3 pins and two P1 pins are multi-functional. They are not only port pins, but also serve the functions of various special features. The alternate functions can only be activated if the corresponding bit latch in the port SFR contain a "1".

Figure 2.4.1. shows a functional diagram of a typical bit latch and I/O buffer in each of the 4 ports.The bit latch is represented as type 0 flip flop which will clock in a value from the internal bus in response to a "read latch" signal from the CPU. The level of the port pin itself is placed on the internal bus in response to a "read latch" signal from the CPU.

The output drivers of ports 0 and 2 are switchable to an internal ADDR and ADDR/DATA bus by an internal CONTROL signal for use in external memory accesses, the P2 SFR remains unchanged ,but the port 0 SFR gets 1's written to it.

Port 1, 2 and 3 have internal pull - ups. Port 0 has open drain outputs. Each I/O line can be independently used as an input or output. To be used as an input the port bit latch must contain a 1, which turns off the output driver FET. Because ports 1, 2, & 3 have fixed internal pull ups they are sometimes called "quasi bi-directional" ports. Port 0 is considered "true" bi-directional, because when configured as an input it floats.

In the execution of an instruction that changes the value in a port latch, the new value arrives at the latch during S6 of the final machine cycle of the instruction. However, port latches are in fact sampled by their output buffers only during phase 1 of any clock period. Consequently the new value in the port latch won't actually appear at the output pins until the next phase 1.

2.4.1 PORT 0

Port 0 is an 8 - bit open drain bi-directional I/O port . As an output port each pin can sink 8 LS TTL inputs. Port 0 pins that have 1's written to them float, and in that state can be used as high-impedance inputs. Port 0 is also the multiplexed lower order address and data bus during accesses to external program and data memory. In this application it uses strong internal pull-ups when emitting 1's and can source and sink 8 LS TTL inputs.

2.4.2 PORT 1

Port 1 is an 8- bit bi-directional I/O port with internal pull-ups. The port 1 output buffers can sink and source 4 LS TTL inputs. Port 1 pins that have 1's written to them are pulled high by the internal pull-ups and in that state can be used as inputs. As inputs port 1 pins that are externally being pulled low will source current because of the internal pull-ups. Port 1 also receives the lower order address byte during the programming of the EPROM parts and during program verification of the ROM and EPROM parts.

2.4.3 PORT 2

Port 2 is an 8- bit bi-directional I/O port with internal pull-ups. The port 2 output buffers can sink/source 4 LS TTL inputs. Port 2 emits the higher order address byte during fetches from external program memory and during accesses to external data memory that use 16- bit addresses. In this application it uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8 - bit addresses, port 2 emits the contents of the P2 SFR.

2.4.4 PORT 3

Port 3 is an 8 - bit bi-directional I/O port with internal pull-ups. The port 3 output buffers can sink/source 4 LS TTL inputs. Port 3 pins that have is written to

them are pulled high by the internal pull-ups, and in that state can be used as inputs. As inputs, port 3 pins that are externally pulled low will source current because of the pull-ups. Port 3 also serves the functions of various special features of the MCS-51 family, as listed below:

PORT PIN	ALTERNATIVE FUNCTION
P 3.0	RxD (Serial input port)
P 3.1	TxD (Serial output port 1)
P 3.2	INT 0 (External Interrupt 0)
P 3.3	INT 1 (External interrupt 1)
P 3.4	TO (Timer 0 external input)
P 3.5	T1 (Timer 1 external input)
P 3.6	WR (External data memory write strobe)
P 3.7	RD (External data memory read strobe)

2.5 TIMER/COUNTERS

The 8051 has two 16 - bit Timer/Counter registers - Timer 0 and Timer 1. They can be configured to operate either as timer or event counters.

In the "Timer" function, the register is incremented every machine cycle. Thus, one can think of it as counting machine cycles. Since a machine cycle consists of 12 oscillator periods, the count rate is 1/12 of the oscillator frequency.

In the "counter" function, the register is incremented in response to a 1 to 0 transition at its corresponding external input pin, T0 and T1. In this function, the

external input is sampled during S5P2 of every machine cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during S3P1 of the cycle following the one in which the transition was detected. Since it takes 2 machine cycles to recognise a 1-to-0 transition, the maximum count rate is 1/24 of the oscillator frequency. For a signal to be sampled, its level should be held for atleast one full machine cycle. Timer 0 and Timer 1 have four operating modes.

TIMER 0 AND TIMER 1

The timer or counter function is selected by control bits in the SFR TMOD. These two timer/counters have four operating modes, which are selected by bit pairs (M1, M0) in TMOD. Modes 0,1 and 2 are the same for both timer/counters. Mode 3 is different. The four operating modes are described as follows:

MODE 0

Either Timer in Mode 0 is an 8-bit counter with a divide by 32 prescaler. Fig.2.5.1 shows the mode 0 operation as it appears to timer 1. In this mode, the timer register is configured as a 13-bit register. As the count rolls from all 1's to all 0's it sets the timer interrupt flag TF1. The counter input is enabled to the timer when TR1=1 and either Gate 0=0 or INT1=1. TR1 is a control bit in the SFR

TCON. Gate is in TMOD. The 13- bit register consists of all 8-bits of TH1 and the lower 5 bits of TL1. The upper 3 bits of TL1 are indeterminate. Mode 0 operation is the same for Timer 0 as for Timer 1.

MODE 1

Mode 1 is the same as mode 0, except that the timer register is being seen with all 16 bits.

MODE 2

Mode 2 configures the timer register as an 8-bit counter with automatic reload, as shown in fig.2.5.2. Overflow from TL1 not only sets TF1, but also reloads TL1 with the contents of TH1, which is preset by a switch. The reload leaves TH1 unchanged. Mode 2 operation is the same for timer/counter 0.

MODE 3

Timer 1 in mode 3 simply holds its count. The effect is same as setting TR1=0. Timer 0 in mode 3 establishes TL0 and TH0 as two separate counters. The timer 0 control bits: Gate, TF0, TR0, C/T ,INT0, TH0 is locked into a timer function and takes over the use of TR1 and TF1 from timer 1. Thus TH0 now controls the timer 1 interrupt.

Mode 3 is provided for applications requiring an extra 8-bit timer or counter. With timer 0 in mode 3, an 8051 can look like it has three timer/counters. When timer0 is in mode3, timer1 can be turned on and off by switching it out of and into its own mode 3, or can still be used by the serial port as a baud rate generator or any application not requiring an interrupt.

2.6 SERIAL INTERFACE

The serial port is full duplex. It is also receive-buffered meaning it can commence reception of a second byte before a previously received byte has been read from the receive register. The serial port receive and transmit registers are both accessed at SFR SBUF. Writing to SBUF loads the transmit register and reading SBUF accesses a physically separate receive register.

The serial port can operate in 4 modes:

MODE 0

Serial data enters and exits through RxD. TxD outputs the shift clock. 8 bits are transmitted/received (LSB first). The baud rate is fixed at 1/12 the oscillator frequency. Mode 0 baud rate = (Oscillator frequency/12.)

MODE 1

10 bits are transmitted or received - a start bit (0), 8 data bits (LSB first) and a stop bit (1). When receiving the stop bit goes into RB8 in SFR SCON. The baud rate is variable.

Mode 2

11 bits are transmitted or received - start bit (0), 8 data bits, a programmable 9th data bit, and a stop bit. On transmit, the 9th data bit can be asigned the value of 0 or 1. On receive, the 9th data bit goes into RB8 in SFR SCON, while the stop bit is ignored. The baud rate is programmable to either 1/32 or 1/64 the oscillator frequency.

Mode 3

11 bits are transmitted or received - a start bit (0), 8 data bits, a programmable 9th data bit and a stop bit. Mode3 is the same as mode2 in all respects except the baud rate. The baud rate in mode3 is variable.

In all four modes, transmission is initiated by any instruction that uses SBUF as a destination register. Reception is initiated in the other modes by the incoming start bit if REN = 1.

The serial port interrupt is generated by the logical OR of RI and TI. Neither of these flags is cleared by hardware when the service routine is vectored to. It is done by software.

Each interrupt source can also be individually programed to one of two priority levels by setting or clearing a bit in the SFR named IP (Interrupt priority).

A low - priority interrupt can be interrupted by a higher priority interrupt, but not by another low- priority interrupt. A high - priority interrupt can't be interrupted by any other interrupt source.

If two interrupt requests of different priority levels are received simultaneously, the request of higher priority level is serviced. If interrupt requests of the same priority level are received simultaneously, an internal polling sequence determines which request is serviced. Thus within each priority level there is a second priority structure determined by the polling sequence.

In operation, all the interrupt flags are latched into the interrupt control system during state 5 of every machine cycle. The samples are polled during the following machine cycle. If the flag for an enabled interrupt is found to be set, the

interrupt system generates an LCALL to the appropriate location in program memory, unless some other condition blocks the interrupt.

The hardware generated LCALL causes the contents of only the PC to be pushed onto the stack, and reloads the PC with the beginning address of the service routine. Having only the PC be automatically saved allows the programmer to decide how much time to spend saving which other registers.

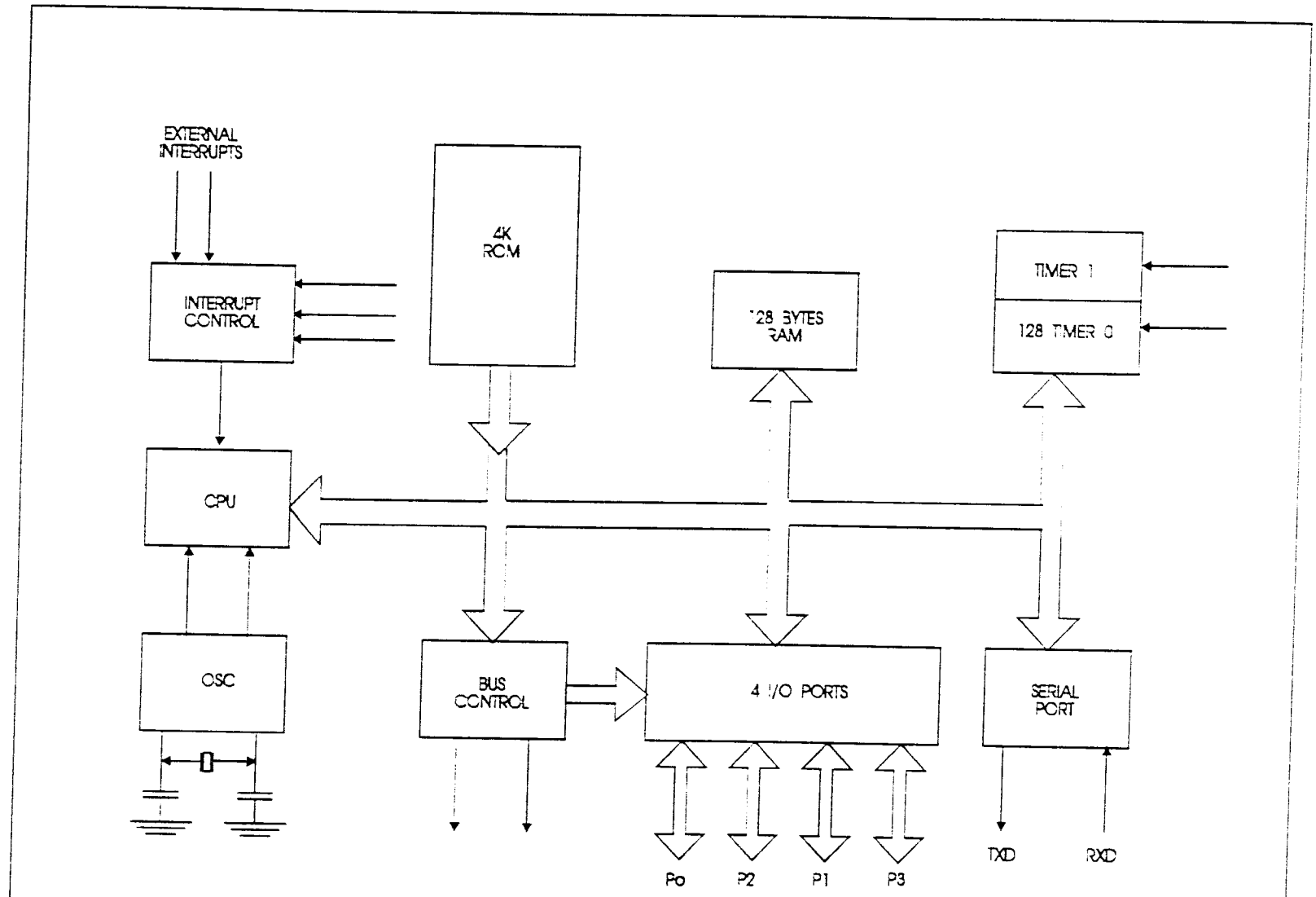


FIGURE 2.2.1 BASIC ARCHITECTURAL BLOCK DIAGRAM OF MCS-51

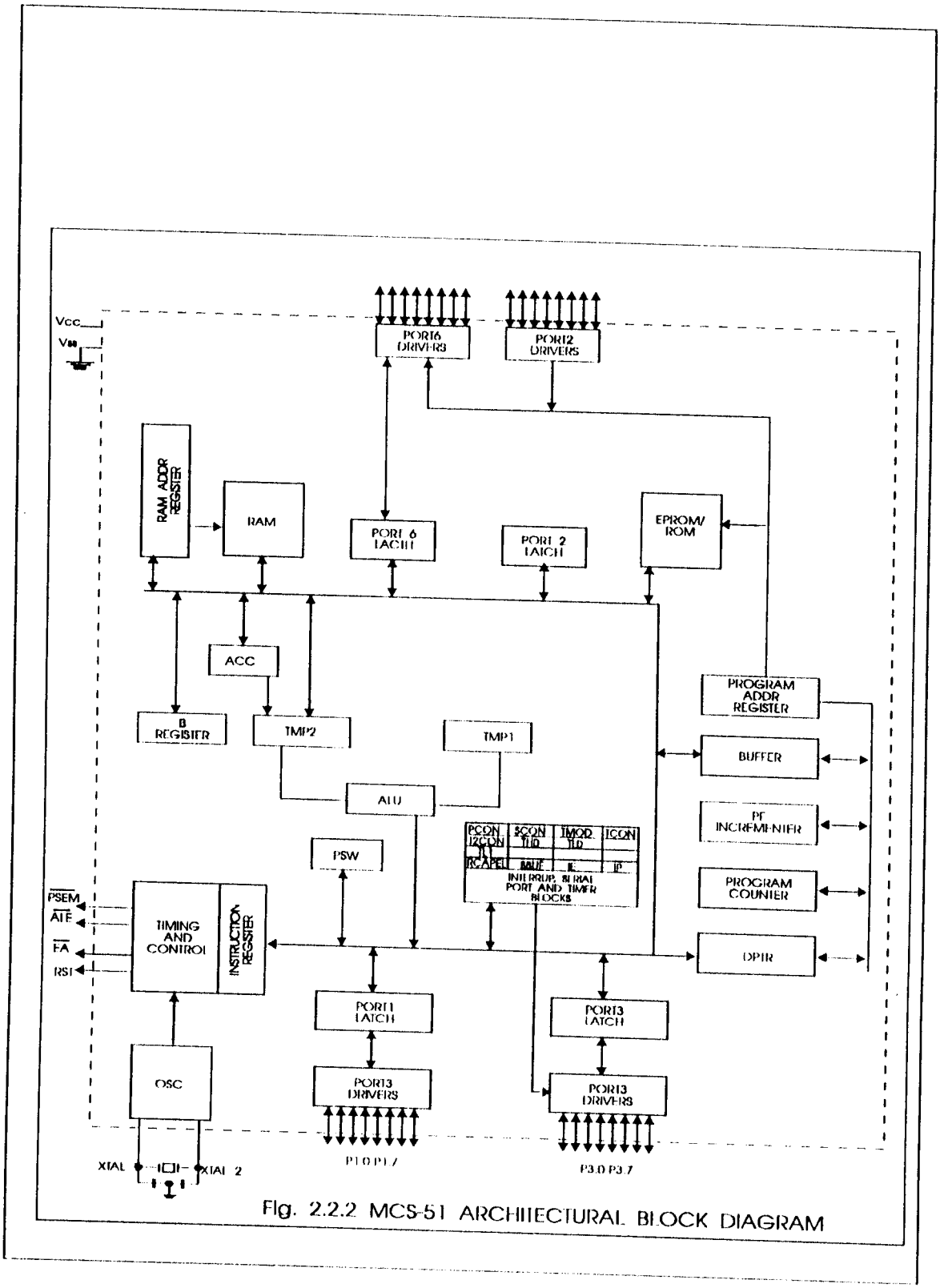


Fig. 2.2.2 MCS-51 ARCHITECTURAL BLOCK DIAGRAM

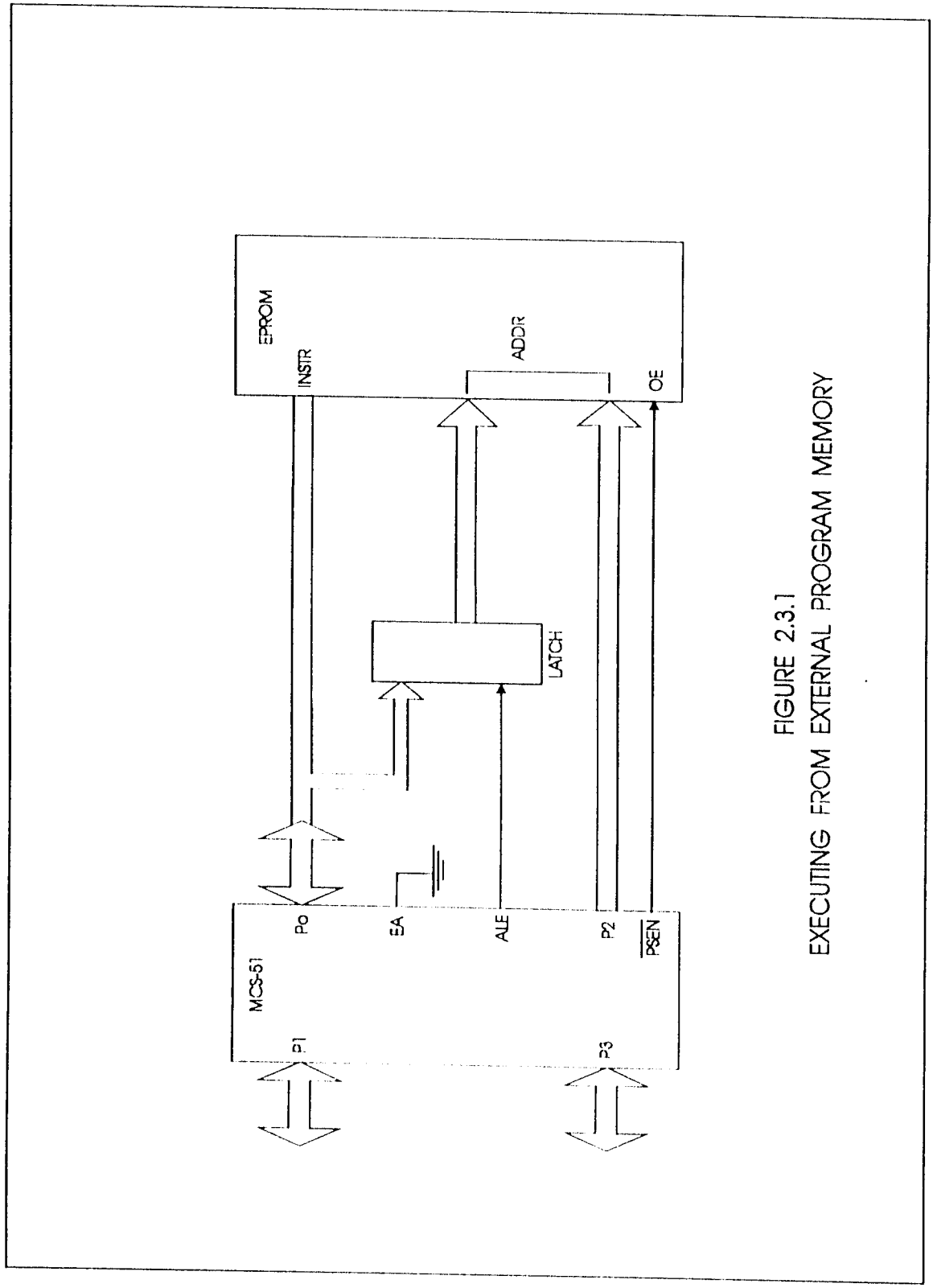


FIGURE 2.3.1
EXECUTING FROM EXTERNAL PROGRAM MEMORY

Figure 2.3.2
DATA MEMORY STRUCTURE OF 8051

8 BYTES

F8								FF
F0	B							F7
E8								EF
E0	ACC							E7
D8								DF
D0	PSW							D7
C8								CF
C0								C7
B8	IP							BF
B0	P3							B7
A8	IE							AF
A0	P2							A7
98	SCON	SBUF						9F
90	P1							97
88	TCON	TMOD	TL0	TL1	TH0	TH1		8F
80	P0	SP	DPL	DPH				PCON 87

FIGURE 2.3.3.
SPECIAL FUNCITON REGISTERS MAP

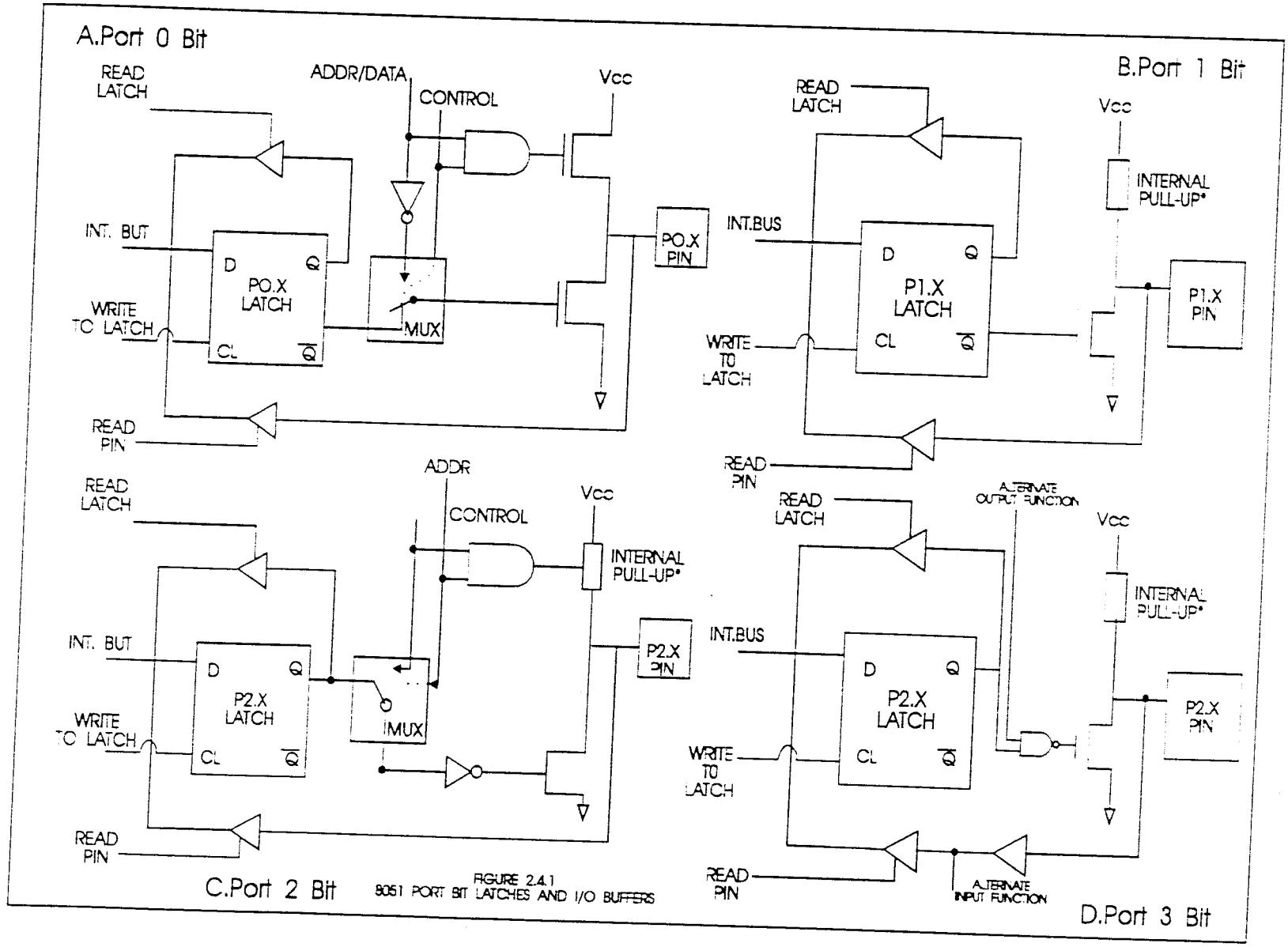


FIGURE 2.4.1
8051 PORT BIT LATCHES AND I/O BUFFERS

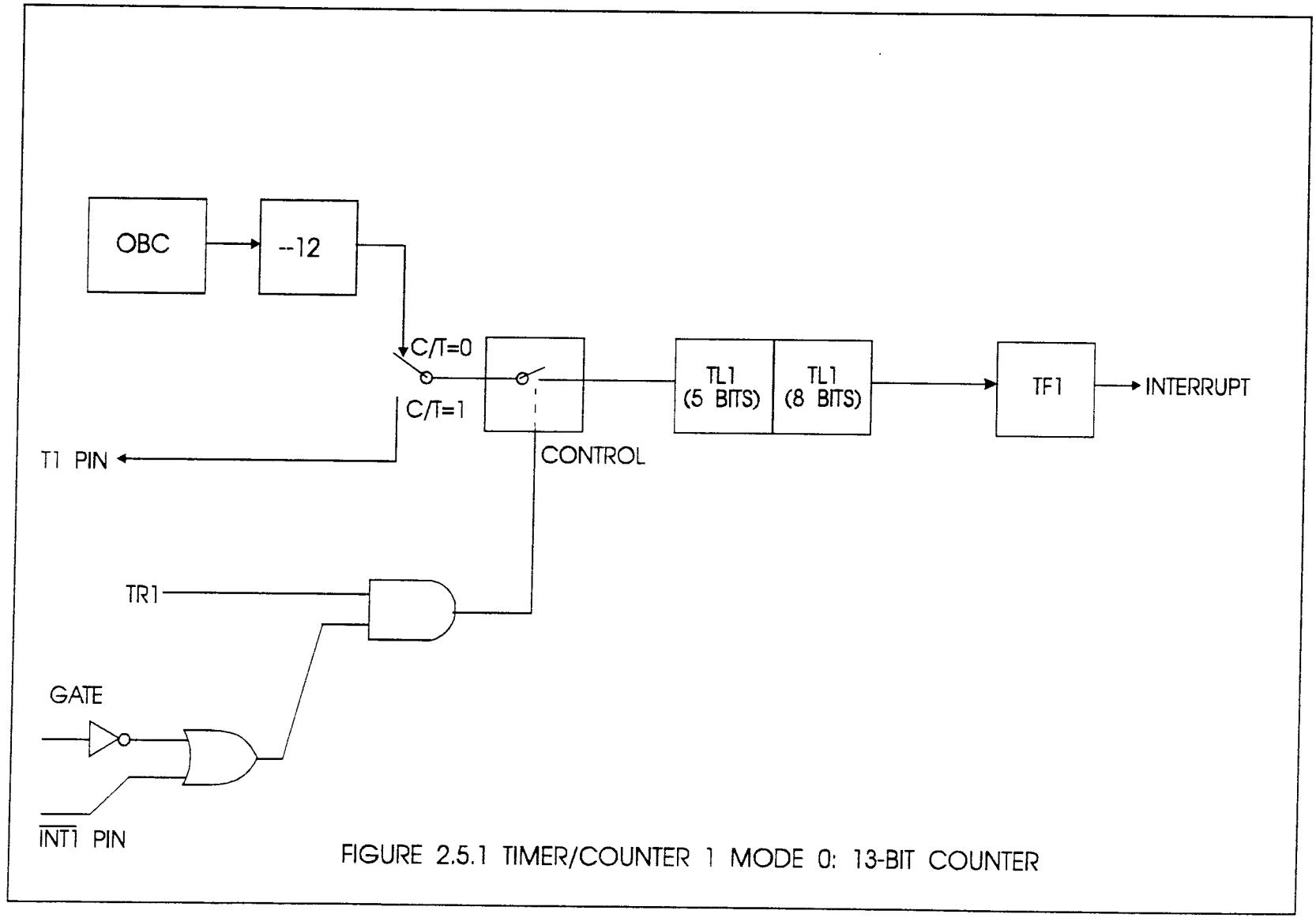


FIGURE 2.5.1 TIMER/COUNTER 1 MODE 0: 13-BIT COUNTER

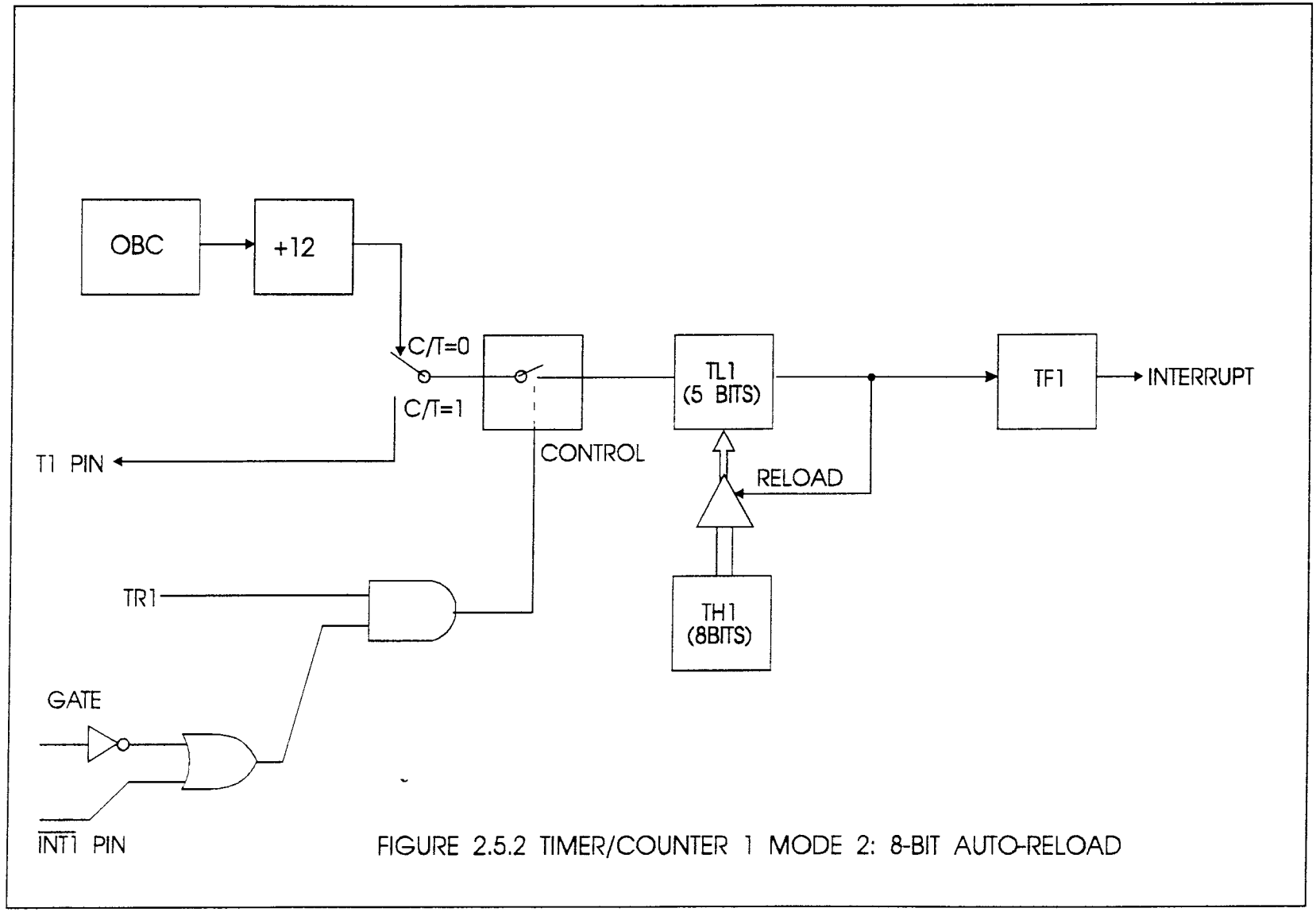


FIGURE 2.5.2 TIMER/COUNTER 1 MODE 2: 8-BIT AUTO-RELOAD

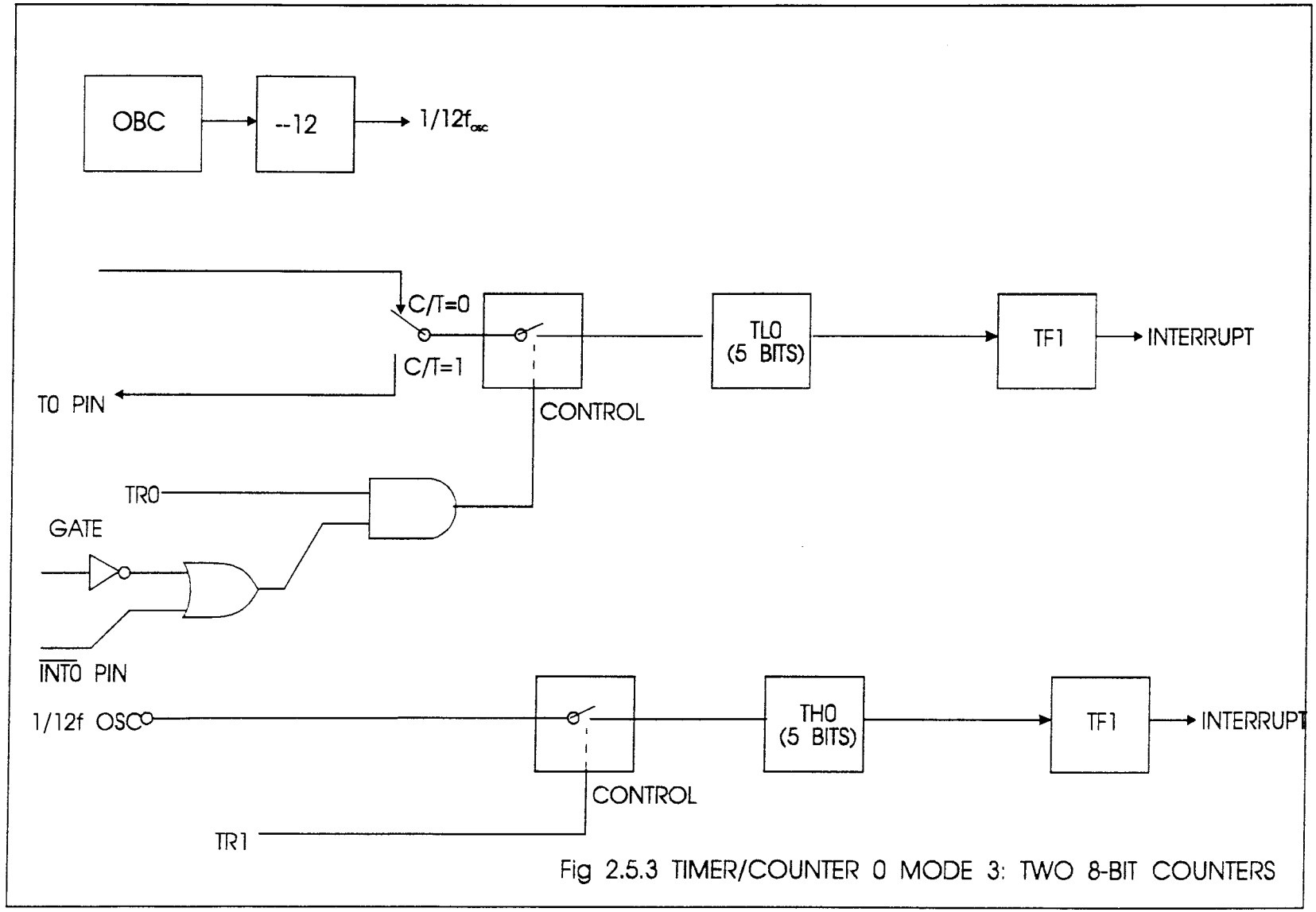


Fig 2.5.3 TIMER/COUNTER 0 MODE 3: TWO 8-BIT COUNTERS

Real Time Clock

MM58274C

3. REAL TIME CLOCK

3.1 INTRODUCTION

RTC MM58274C IC performs the time keeping function of the system. It is fabricated using low threshold metal gate CMOS technology and is designed to operate in bus - oriented microprocessor systems. This IC is mainly microprocessor compatible. The crystal oscillator is a CMOS amplifier with on-chip bias resistor.

3.2 FEATURES

* MM58274C maintains time keeping from tenths of seconds to tens of years in independently accessible registers.
* It has got the provision of leap year register.
* 12/24 hour operation is possible with an hours counter.
* There is a simple testing for time rollover by means of data changed flag.
* Fully TTL- compatible.
* Low power standby operation of the order of 10 microamps at 2.2 V.

Figure 3.1 shows the block diagram of RTC in detail. It shows an address decoder block that decodes an address for the R/W multiplexer. There is a buffer inside to which 4 data lines are connected. The transfer between buffer and R/W

multiplexer is dual. There are three dividers assembled in a block that produce a 10 Hz frequency pulse from the on chip crystal frequency. The main block is the timer which is capable of generating interrupts at certain intervals.

Thus a R/W logic control to which the control bus is connected takes care of the commands in and out of the chip.

3.3 SYSTEM DESCRIPTION

The system is capable of giving easy error free time reading by a testable data changed flag (DCF) and simplified interrupt control. When the device is in test mode, a buffered oscillator signal appears on the interrupt output. This allows easy oscillator setting when the device is initially powered up in a system.

3.3.1 CRYSTAL OSCILLATOR

The crystal oscillator consists of a CMOS inverter/amplifier with an on chip bias resistor. External capacitances and a crystal are sufficient to complete the time keeping oscillator circuit. A trimmer capacitor is present in the circuit to tune the crystal load impedance thereby optimising oscillator stability. When an external oscillator itself is used, it must be connected to the oscillator input, and the oscillator output is floated. The device when in test mode, the oscillator is

gated on to the interrupt output pin giving a buffered oscillator to set the frequency initially given.

3.3.2 DIVIDER CHAIN

A 10 Hz frequency pulse is got in three stages. The first stage is a non integer divider which reduces the 32.768 KHz input to 30.72 KHz. The second stage is a ripple counter giving an output of 60 Hz. The third stage is a Johnson counter generating an output of 10 Hz. This output is gated with the crystal to provide clock setting pulses. The setting pulse drives all time registers which are clocked synchronously by this signal.

3.3.3 COUNTERS

3.3.3.1 SECONDS COUNTERS

There are three counters for seconds:

Tenths of seconds

Units of seconds

Tens of seconds

The tenths of seconds register is reset to '0' by accessing the clock start/stop bit of control register. The units and tens of seconds are set up by the processor,

giving time setting to the nearest second. All three registers can he read by the processor for time output.

3.3.3.2 MINUTES COUNTERS

There are two minutes counters:

Units of minutes

Tens of minutes

Both registers may be read or written from as required.

3.3.3.3 HOURS COUNTERS

There are two hours counters:

Units of hours

Tens of hours

Both registers may be used to read and write as desired.

In 12-hour mode, tens of hours register has only one active bit and the other 3 bits are set to logic 0. AM/PM indication is provided by data bit 1.

In 24 hour mode tens of hours register reads out 2 bits of data, and the rest two bits set to logic 0. Data bit 1 reads out 0.

3.3.3.4. DAYS COUNTER

There are two days counters:

Units of days

Tens of days

The days counter will count up to 28,29,30,31 depending on the state of the months counters and the leap year counter. The microcontroller has full read/write access to these registers.

3.3.3.5 MONTHS COUNTERS

There are two months counters.

Units of months.

Tens of months.

Both these counters have full read write access.

3.3.3.6. YEAR COUNTERS

There are two years counters.

Units of years

Tens of years

Both these counters have full read/write access. The years count upto 99 and roll over to 00.

3.3.3.7 DAYS OF WEEK COUNTER

The day of week counter increments as the time rolls over from 23:59 to 00:00 in 24 hours mode and 11:59 P.M to 12:00 A.M in 12 hour mode.

3.4 CONTROL REGISTERS

There are three registers which control different operations of the clock.

The clock setting register

The interrupt register

The control register

The layouts of the above are shown in figure 3.2. ~~below~~.

3.4.1 CLOCK SETTING REGISTER

The clock setting register programs the time keeping of the clock. The 12/24 hour mode select and the A.M/P.M indicator for 12 hour mode occupy bits 0 and 1 respectively. Data bits 2 and 3 set the leap year counter.

3.4.2 INTERRUPT REGISTER

The interrupt register controls the operation of the interrupt timer, selecting the required delay period and either single or repeated interrupt.

3.4.3 CONTROL REGISTER

The control register is responsible for controlling the operations of the clock and supplying status information to the processor. This register appears as two different parts- One with write only access and one with read only access.

The write only register consists of a bank of four latches which control the internal processes of the clock. A logic 1 written into the test bit puts the device into test mode. This facilitates testing of the device and oscillator frequency setting. For normal operation, this bit must be logic 0.

There is a clock start/stop bit that stops and maintains the time keeping of the circuit.

The next bit is the interrupt select bit which determines the two registers that are mapped to the interrupt register addresses to be accessed.

The interrupt start/stop bit controls the running of the interrupt timer. It is programmed in the same way as the clock start/stop bit.

CLOCK SETTING REGISTER LAYOUT

Functions	Data Bits Used DB3 DB2 DB1 DB0	Comments	Access
Leap Year Counter	x x	0 Indicates a Leap Year	R/W
AM/PM indicator (12-Hour Mode)	x	0=AM 1=PM 0 in 24-Hour Mode	R/W
12/24-Hour Select Bit	x	0=12 Hour Mode 1=24 Hour Mode	R/W

INTERRUPT CONTROL REGISTER

Function	Comments	Control word DB3 DB2 DB1 DB0
No Interrupt	Interrupt output cleared, start/stop bit set to 1.	x 0 0 0
0.1 Second		0/1 0 0 1
0.5 Second		0/1 0 1 0
1 Second	DB3= 0 for single interrupt	0/1 0 1 1
5 Seconds	DB3=1 for repeated interrupt	0/1 1 0 0
10 Seconds		0/1 1 0 1
30 Seconds		0/1 1 1 0
60 Seconds		0/1 1 1 1

CONTROL REGISTER LAYOUT

Access (addr0)	DB3	DB2	DB1	DB0
Read from:	Data changed flag	0	0	Interrupt flag
Write To:	Test 0=Normal 1=Test Mode	Clock Start/Stop 0=Clock Run 1=Clock Run	Interrupt Select 0=Clock Setting Register 1=Interrupt Register	Interrupt Start/Stop 0=Interrupt Run 1=Interrupt Stop

3.5 DEVICE OPERATION

3.5.1 TEST MODE

This is the mode that is used for testing the device after fabrication and packaging. This mode is also used for initial set up of the oscillator frequency.

The oscillator which is a 32.768 KHz crystal is gated onto the interrupt output to provide a buffered output for initial frequency setting. When an interrupt is programmed, this crystal oscillator output is switched off to allow high speed testing. The interrupt output will then function as normal.

3.5.2 INITIALISATION

The following steps are to be followed for proper initialisation.

(1) The clock and interrupt timers are both halted. Test mode and interrupt register are selected.

(2) The oscillator is gated onto the interrupt output.

(3) After setting the oscillator frequency, the clock register is selected by the interrupt select bit.

(4) Write 0001 to all registers ensuring start with a valid BCD value in each register.

(5) Set the 12/24 hours mode by writing into the clock setting registers.

(6) After the clock initialisation by starting the time, control register is disabled.

The final control register write should be synchronised with an external time source.

3.6 INTERRUPT PROGRAMMING

The interrupt timer generates interrupts at time intervals which are programmed into the interrupt register. In the single interrupt mode, interrupt timing stops when a time-out occurs. The processor restarts timing by writing logic 0 into start/stop bit.

In repeated interrupt mode the interrupt timer continues to count with no intervention by the processor necessary.

Generally, once if the interrupt register has been used to set up the delay time and to select single or repeat, it takes no further part in the working of the interrupt system. All the activities by the processor then take place in the control register.

3.7 APPLICATIONS

Taking notice of the applications of MM 58274C RTC, with reference to our project, it is used for controlling a D.C Motor operation with a relay. This part is taken care of in the software.

The other applications include

3.7.1 CLOCK AS A MICROPROCESSOR WATCH DOG

The microprocessor, in its main program, writes to the clock, stopping and restarting the timer. The timer runs till the main loop stops execution. If execution is stopped for some reason, microprocessor initialises interrupt to restore operations.

3.7.2 THE JAPANESE CALENDAR

Taking notice of the programmable leap year counter, it is possible to program the Japanese showa calendar. The normal procedure is to program the number of years since last leap year. It is a value from 0 to 3 written into the counter.

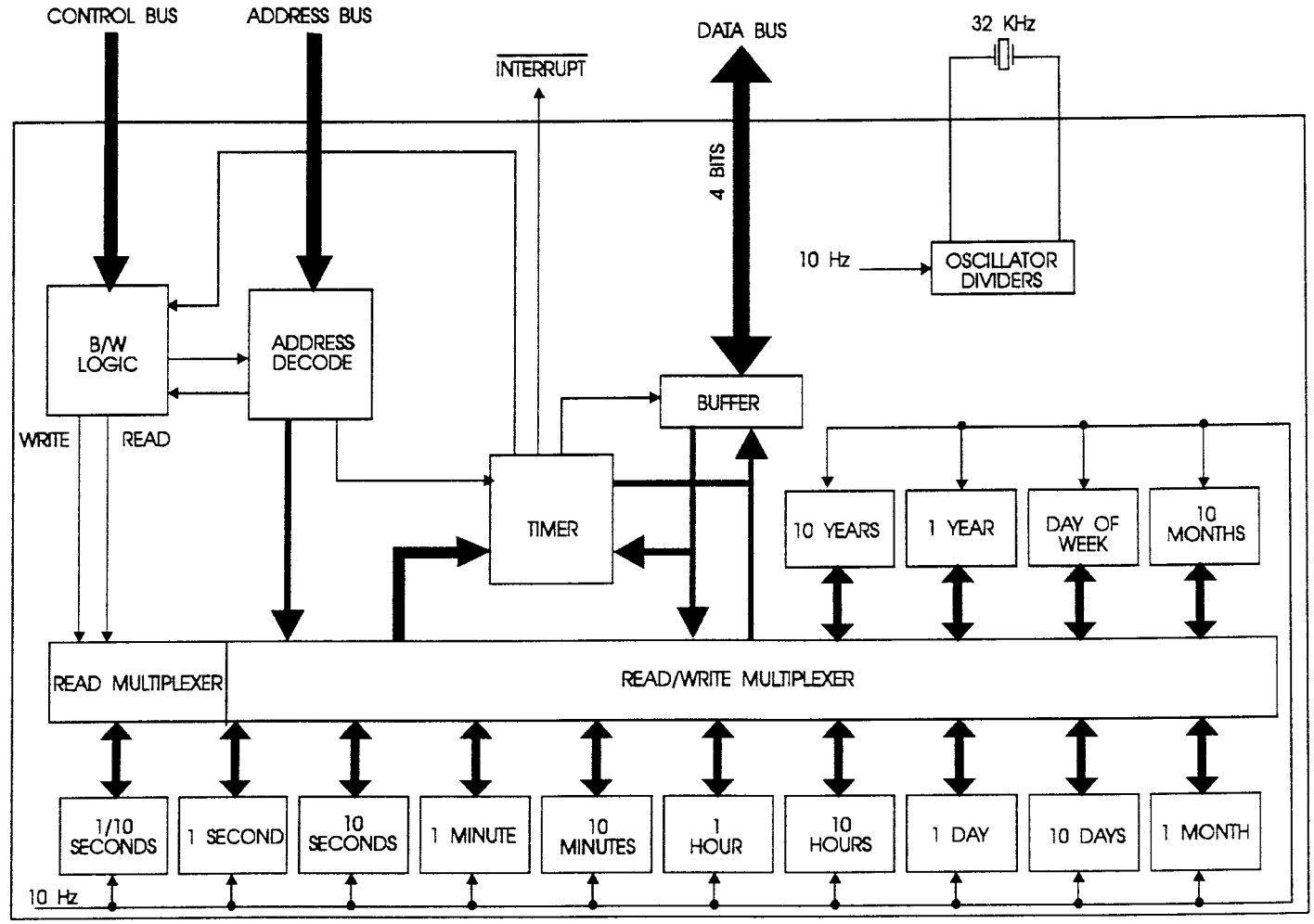


FIGURE 3.1
BLOCK DIAGRAM OF THE INTERNAL STRUCTURE OF RTC MM58274

Memory

4. MEMORY

4.1 INTRODUCTION

A Memory unit is a collection of storage registers together with the associated circuits needed to transfer information in and out of registers. The storage units in a memory are called memory registers. A memory word generally may represent a group of alphanumeric characters or any binary code information.

Memory units whose components lose stored information with time or when power goes down is said to be volatile. But in contrast, non-volatile memory store the information even after removal of power. Depending on the type of access, memory can be classified as read only memory (ROM), and random access memory (RAM). In our project, HM6264 RAM and 27C64 UV erasable PROM's are used for the required storage.

4.2 EPROM-2764

As the name indicates, EPROM's are Erasable programmable read only memories. These are programmable with data and can be erased with an exposure to UV rays. Standby mode is facilitated with very low power consumption.

4.2.1. FEATURES

They have very high noise immunity features like ± 10% Vcc tolerance ,maximum latch-up immunity, high performance speeds of the order of 150 ns maximum access time. The 27C64 has a non-multiplexed addressing interface and is pin compatible.

4.2.2. MODES OF OPERATION

The modes of operation of 27C64 ROM can be tabulated. Our project utilises the modes like read, program verify and standby modes. The other modes like program inhibit, two line output control are also possible.

4.2.2.1. READ MODE

In order to obtain data at the outputs, 27C64 has two control functions, and both must be logically active. Chip enable is the power control and it should be used for device selection. Output enable is the output control and should be used to get data from the output pins. The address access times and the delay from chip enable to output pin gets compensated assuming a certain delay before addresses become stable.

4.2.2.2. PROGRAM INHIBIT

Programming of multiple EPROM's in parallel with different data can be easily accomplished with this mode. It inhibits the other devices from being programmed.

4.2.2.3 PROGRAM VERIFY

A verify (read) should be performed on the programmed bits to determine that correct program has been entered.

4.2.2.4 STANDBY MODE

This mode is entered when chip enable or address latch enable are in the CMOS high state. During this state the outputs are in a high impedance state independent of the $\overline{OE}$ input.

4.2.2.5 TWO LINE OUTPUT CONTROL

Since EPROM's are usually used in larger memory arrays, Intel has provided two control lines which accommodate this multiple memory connection. This control allows lowest possible memory power consumption and complete assurance that output bus contention will not occur. In this mode, the deselected

memory devices are in their low power standby mode and their output pins go active only when data is desired from a particular memory device.

4.2.2.6 INTELLIGENT IDENTIFIER MODE

This mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This helps in automatic matching of the device to be programmed with its corresponding programming algorithm.

4.2.3 ERASURE CHARACTERISTICS

The characteristics are such that erasure begins to occur upon exposure to light with wavelengths shorter than 4000 A°. Sunlight and certain types of fluorescent lamps have wavelengths in the range of 3000 - 4000 A°. Exposure of the device to high intensity UV rays for longer periods may cause permanent damage.

4.3 RAM - 6264

IC HM6264 Random access memory is used as a data memory in this system. It is a high speed static CMOS RAM with a capacity of 8192 X8 bits.

The accessing time is as fast as 150 ns at a maximum. Its standby operation consumes less power. A single 5V supply is sufficient to program this IC. The

major feature of this IC is that, it is pin out compatible with 64K EPROM HM482764. Also no clock or timing strobe is being required.

8279 Keyboard/ Display Interface

5. 8279 KEYBOARD/DISPLAY INTERFACE

5.1 INTRODUCTION

When interfacing a keyboard or display to microprocessor or microcontroller, the software or hardware approach can be used. The problem encountered in the software approach is that there is an additional burden on the CPU. If the CPU is involved in a lengthy task, effective software approach becomes complicated. Hence we go in for the dedicated keyboard display interface like the Intel 8279. When using the 8279 each seperate step involved in interfacing the keyboard/display which previously had to be done by software i.e., by the microprocessor, is now completley taken over by 8279.

5.2 BLOCK DIAGRAM

8279 has four major sections - keyboard, scan, display and the MPU interface.

5.3 DISPLAY SECTION

When some letters or numbers have to be displayed, the seven segment codes for the letters or numbers are written in the 16 byte display RAM. The 8279 outputs the binary number for the first digit to the decoder (in the encoded scan

mode) to turn on the first one of the digit driver transistors. 8279 then outputs the seven segment codes for the first of the display digits.

The 8279 then outputs on the A & B lines a code which turnsoff all the segments. The display is blanked here to prevent 'ghosting' of information from one digit to the next when the digit strobe is switched to the next digit. While the displays are blanked, 8279 sends out the BCD code for the next digit to the decoder, to enable digit-2 driver transistors. It then sends out the seven segment code for digit-2 on the A & B lines. This then lights the desired pattern on digit 2. After 490µs the 8279 blanks the display again and goes on to digit 3. The 8279 steps through all the digits and then returns to digit 1 and repeats the cycle. Since each digit requires about 490µs, the 8279 gets back to digit 1 after about 5.1 ms for an 8 digit display and back to digit 1 after about 10.3 ms for 16 digit display. The time it takes back to a digit 1 again is reffered to as the scan time.

The main advantage underlying the use of 8279 is that once the seven segment code is loaded into the internal RAM, it keeps the display refreshed automatically.

8279 can be connected and initialised to refresh a wide variety of displays.

5.4 KEYBOARD SECTION

When interfacing a keyboard three main tasks to be carried out are

1. Detecting a keypress
2. Debouncing a keypress
3. Encoding

The tasks involved are putting a low on a row of the keyboard matrix and checking the column of the matrix. If any keys are pressed in that row, a low will be present on the column which connects the key, because pressing a key shorts a row to a column. If no low is found on the columns the low is stepped to next row and the columns are checked again. If a low is found on a column, then after a debounce time, the column is checked again. If the keypress is valid, a compact code representing the keypressed is sent.

The following describes how 8279 performs the above mentioned functions.

The column links of the keyboard are connected to the return lines RL0 - RL7 of the 8279. As a low is put on each row by the scan lines SL0-SL3 and the decoder, the 8279 checks the return lines one at a time to see if any of them are low.

If 8279 finds any of the return lines low indicating a keypress, it waits for a debounce tine and checks again. If the keypress is still present the 8279 produces an 8-bit code which represents the key pressed. This is stored in an internal 8-byte FIFO RAM. The FIFO RAM can store about 8 codes before overflowing. When the 8279 finds a valid keypress, two actions are executed. It asserts its interrupt request pin, IRQ high and increments the FIFO count in an internal status register. When the FIFO has a character it can be detected on an interrupt basis or the status word can be checked.

5.5 INTIALISING AND COMMUNICATING WITH 8279.

The 8279 has only two internal addresses which are selected by the logic level on the address line A0. When A0 is low, 8279 is enabled for reading from or writing data into it. A0 being high selects the control/status register.

8279 has only one control register. Hence the control words are differentiated on the basis of the first three bits.

CONTROL WORD

Code	1	0	0	AI	A	A	A	A

The CPU sets up the 8279 for a write to the Display RAM by first writing the command. After writing the command with A_0=1, all subsequent writes with A_0=0 will be to the Display RAM. The addressing and auto-increment functions are identical to those for the Read Display RAM. However, this command does not affect the source of subsequent Data Reads; the CPU will read from whichever RAM (Display or FIFO/Sensor) which was last specified. If, indeed, the Display RAM was last specified, the Write Display RAM will, nevertheless, change the next read location.

Display Write inhibits/Blanking.

					A	B	A	B
Code	1	0	1	X	IW	IW	BL	BL

The IW Bits can be usd to mask ~~nibble An and~~ nibble A and B in applications requiring separate 4-bit display ports. By setting the IW flag (IW = 1) for one of the ports, the port becomes marked so that entries to the display RAM from the CPU do not affect that port. Thus, if each nibble is input to a BCD decoder, the CPU may write a digit to the Display RAM without affecting the other digit being displayed. It is important to note that bit B_0 corresponds to bit D_0 on the CPU bus and that bit A_3 corresponds to bit D_7

If the user wishes to blank the display, the BL flags are available for each nibble. Thus last clear command issued determines the code to be used as "blank" This code defaults to all zeros after a reset. Note that both BL flags must be set to blank a display formatted with a single 8-bit port.

Clear

Code	1	1	0	C_D	C_D	C_D	C_F	C_A

The C_D bits are available in this command to clear all rows of the Display RAM to a selectable blanking code as follows.

C_D C_D C_D

0 x All Zeros (x=Dont' care)
1 0 AB=Hex 20 1D010 0000)
1 1 All ones
Enable clear display when = 1 (or by C_A = 1)

During the time the display RAM is being cleared (~160 µs) it my not be written to. The most significant bit of the FIFO status word is set during this time. When the Display RAM becomes available again, it automatically resets.

If the C_F bit is asserted (C_F=1), the FIFO status is cleared and the interrupt output line is reset. Also, the sensor RAM becomes available gain, it automatically resets.

C_A, the clear All bit, has the combined effect of C_D and C_F, it uses the C_D clearing code of the Display RAM and also clears FIFO status. Furthermore, it resynchornizes the internal timing chain.

End Interrupt/Error Mode set

Code	1	1	1	x	x	x	x	x	x=Don'Care

For the sensor matrix this command lowers the IRQ line and enables further writing into RAM. The IRQ line would have been raised upon the detection of a change in a sensor value. This would have also inhibited further writing into the RAM until reset.

For the N-Key rollover mode - if the bit is programmed to "1" the chip will operate in the special Error mode.

Keyboard/Display Mode Set

	MSB							LSB
Code	0	0	0	D	D	K	K	K

Where DD is the Display mode and KKK is the Keyboard Mode.

DD

0 0 8 8-bit character display - Left entry

0 1 16 8-bit character display - Left entry

1 0 8 8-bit character display - right entry

1 1 16 8-bit character display - Left entry

Note that when decoded scan is set in keyboard mode, the display is reduced to 4 characters independent of display mode set.

K K K

0 0 0 Encoded Scan Keyboard - 2 Key Lockout

0 0 1 Decoded Scan Keyboard - 2 Key Lockout

0 1 0 Encoded Scan Keyboard - N Key Rollover

0 1 1 Decoded Scan Keyboard - N Key Rollover

1 0 0 Encoded Scan Sensor Matrix

1 0 1 Decoded Scan Sensor Matrix

1 1 0 Strobed input, Encoded Display Scan

1 1 1 Strobed input, Decoded Display Scan

Program Clock

0	0	1	P	P	P	P	P

All timing and multiplexing signals for the 8279 are generated by an internal prescaler. This prescaler divides the external clock (pin 3) by a

programmable integer. Bits PPPPP determine the value of this integer which ranges from 2 to 31. Choosing a divisor that yields 100 KHz will give the specified scan and debounce times. For instance, if Pin 3 of the 8279 is being clocked by a 2 MHz signal, PPPPP should be set to 10100 to divide the clock by 20 to yield the proper 100 KHz operational frequency.

Read FIFO/Sensor RAM

Code

0	1	0	AI	X	A	A	A

x=Don't Care

The CPU sets up the 8279 for a read of the FIFO/Sensor RAM by first writing this command. In the Scan Keyboard mode, the Auto-Increment flag(AI) and the RAM address bits (AAA) are irrelevant. The 8279 will automatically drive the data bus for each subsequent read ($A_0 = 0$) in the same sequence in which the data first entered the FIFO, All subsequent reads will be from the FIFO until another command is issued.

In the Sensor Matrix Mode, the RAM address bits AAA select one of the 8 rows of the Sensor RAM. If the AI flag is set (AI=1), each successive read will be from the subsequent row of the sensor RAM.

Read Display RAM

Code	0	1	1	A1	A	A	A	A

The CPU sets up the 8279 for a read of the Display RAM by first wirting this command. The address bits AAAA select one of the 16 rows address of the Display RAM. If the A1 flag is set (A1 = 1), the row address will be incremented after each ~~following~~ read or write to the Display Ram. Since the same counter is used for both reading and writing, this command sets the next read or write address and the sense of the Auto-Incremented mode for both operations.

5.6 MODES

When the 8279 is used with the keyboard, it can be operated either in the encoded scan mode or decoded scan mode. When used in the encoded scan mode the binary count sequence, is sent on the lines SL0-SL3 and an external decoder is used to produce the stepping lows.

In the decoded mode, the 8279 directly outputs the stepping lows on the four scan lines.

Also it can be operated with 2-key lockout or N-key roll over. In the two-key lock out mode, one key must be relesed before an other keypress is

detected and processed. In the N-key roll over mode, if 2 keys are pressed nearly together, the keypresses will be detected, debounced and the codes stored.

In addition to being used to scan keyboard, the 8279 can also be used to scan a matrix of switch sensors such as metal strips and magnetic sensors. In sensor matrix mode 8279 scans all the sensors and stores the condition of upto 64 switches in the FIFO RAM. If the condition of any switch changes, an IRQ signal is sent out to the processor (An interupt service procedure will do the requrired job.)

The 8279 requires an internal clock frequency of 100KHz. An available clock frequency such as 2.5 MHz can be applied to its clock input and can be divided to the required 100KHz. The program clock control word is used for this.

The final control word required for intialisation is the clear word. This is sent to 8279 to tell it as to what code it has to sent when switching from one segment to another. This can be used to clear the display RAM and FIFO RAM. The lower two bits labelled C_d in the control word specify the desired blanking code which depends on the hardware.

The write display RAM control word tells the 8279 that the data later sent to 8279 should be put in the display RAM and where in the display RAM it should be put. If 1 is put in the auto increment bit, the internal pointer will be automatically incremented.

To read code from FIFO RAM.

Read FIFO sensors RAM is sent to the control/staus address. The number of keys pressed can be read from the status word.

Hardware

6. HARDWARE

6.1.INTRODUCTION:

The backbone behind this system is the RTC 58274 and the microcontroller 8051. The timing data provided by the RTC is processed by the 8051. The other chips included for display,keyboard entry, decoding and memory are Intel 8279 IC,IC2764-ROM chip,IC6264-RAM chip and 7-segment displays. Memory mapping scheme has been employed for 8051 to access these chips.

The mapping scheme comprises of IC74AS373 latch, IC74LS138, IC74154 decoders, IC7404 Not gate, IC7432 OR gate.

6.2 ADDRESS/DATA BUS DEMULTIPLEXING

The microcontroller 8051 has an 8-bit data bus and 16-bit address bus. Port 0 acts as the multiplexed lower order address/ data bus and port P2 acts as the higher order address bus. In account of this multiplexing external demultiplexing has to be done. During every machine cycle the lower order address is present in the multiplexed, address/data bus only during the first T-state.

Since the low address byte has to be present at the input of the external memory chip IC for the entire machine cycle, the low byte has to be latched during the first T-state.

IC74AS373 latches have been utlised to serve the above purpose. It is enabled by the ALE pulse sent by the 8051. During normal operation it is emitted at 1/6th of the oscillator frequency. Thus when the ALE is pulse sent the lower order address found on port 0 is stored in the latch and A0-A7 is available at the output of the latch while the higher order address A8-A15 is found on port 2.

6.3 MEMORY MAPPING

Due to the availability of the 16-bit address bus the addresses accessable are 0000-FFFFH. The system uses 8K of RAM and 8K of ROM. $\overline{EA}$ pin of 8051 has been tied to ground. Thus the ROM memory accessible is completely external.

Partial decoding has been done. The underlying reason is that, 8K of ROM and 8K of RAM is sufficient for our requirements. Exhaustive decoding would result in an increase in the complexity of the hardware design on account of the additional chips which have to incorporated.

6.3.1. ADDRESS ALLOCATION

The addresses alloted for the various peripherals are as follows.

ROM: - 0000 - 1FFFH

RAM: - 4000 - 5FFFH

RTC: - 6000 - 600FH

8279: - A001 AND A002H

RELAY: - E000H

PROMPT LEDs: - 8000H

In the memory mapping scheme address lines A_{15}, A_{14}, A_{13} are employed for decoding 74LS138 is a 3-to-8 decoder where three inputs are the Address lines A_{15} A_{14} A_{13}. The output enable pin $\overline{0E}$ is grounded and the enable pin G is tied to ALE pin of 8051.

Depending on the values of A_{15} A_{14} A_{13}, the outputs of the decoder are used to enable the various chips.

When 000 is present on A_{15} A_{14} A_{13}, first output Y_o of IC74LS138 enables the ROM Chip IC2764. The address lines A0-A12 are used for internal selection of the ROM chip.

IC6264 is selected by the third output Y_2 IC4LS138 since 010 on the address lines A_{15} A_{14} A_{13} covers the address range 4000-5FFF.

The fourth output Y_3 of the decoder is tied to the chip select pin of the RTC. Therefore 011 on the address lines A15A14A13 enables the chip.

The keyboard/display interface has two internal addresses. A001H for data and A002H for control/status access. The sixth output Y_5 of the decoder selects 8279 when 101 is found on A_{15} A_{14} A_{13}.

The address 8000 selects the buffer for the prompt LEDS. since Y_4 of 74LS138 is tied to enable pin of the buffer.

6.4 DISPLAY

The data to be displayed are the seconds, minutes, hours in 24 hour format, day of week, day of month, year & month of year. Seven segment displays are used to serve the above purpose.

Display section is completely controlled by 8279 which is operated in the encoded scan keyboard mode.

External decoding is implemented by using IC74154 which is a 4 to 16 decoder. The 4 inputs are provided by SL0 to SL3 of 8279.

The seven segment displays employed in this system are common anode displays. Hence to turn them on, a low is required, and the corresponding data comes from A0-A3, B0-B3 of 8279.

To satisfy the current requirements of the seven segment display BC108 transistors have been utilised whose collector output drives the display.

CALCULATION OF BASE RESISTANCE

Required I_c = 150mA; V_{ol}(74154) = 0.4

$$\beta =$$

$$I_B = \frac{150mA}{\beta} =$$

$$R_B = \frac{4.3 - 0.4}{\beta}$$

Since 8279 is being operated in the encoded scan keyboard mode the required external decoding has been done by IC 74154. This is a 4 to 16 decoder

whose four inputs are provided by SL_0 to SL_3. Each output of the decoder drives the base of the PNP power transistor whose collector is connected to the anode point of the display.

6.5 KEYBOARD

The keyboard employed is a 4 by 4 matrix keyboard which consists of the digits 0 to 9 and the keys RUN,RESET,SET,FUTURE, FREEZE & NEXT. The columns of the keyboard are connected to RL_0 to RL_3 of 8279, while rows are connected to RL_4-RL_7.

SET KEY

The purpose of the SET key is to load the present time into the RTC chip. All the numerical keys pressed after pressing set key will be stored in the RTC.

FUTURE KEY

The numerals entered after pressing the FUTURE key decides the time at which the relay must change state.

RUN KEY

RUN key is used to initiate the running of the RTC chip if the time is re-entered.

RESET

Pressing RESET key resets the entire system

FREEZE KEY

FREEZE key completely blanks the display, while RTC continues to time keep.

NEXT KEY

Pressing of NEXT key decides the change of state of the motors.

6.6 INTERRUPTS

8051 has a completely vectored interrupt procedure. INT 0 is driven by RTC while the 8279 sends its interrupt on INT 1. The 8051 is programmed such that interrupt sent by RTC is accorded higher priority. IE0 is vectored to address 0003H and IE1 is vectored to address 0013H.The interrupt service subroutines are written in these addresses.

Two interrupt service subroutines are called during the functioning of the system. Interrupt IEO is serviced under higher priority conditions to implement

data comparison IE1 is accorded lower priority and its corresponding subroutine takes care of the keyboard / display software interface.

For servicing a particular subroutine, when control transfer takes place, the interrupts are disabled by software and enabled when control is transferred back to the main program.

The RTC generates interrupts every second. The other interrupt sevice subroutine is serviced when the micro controller senses the interrupt sent by 8279.

6.7 PROMPTING LEDs

The hardware has been so designed that the user is prompted when invalid data is entered. For each unit of time like seconds, minutes, hours etc., an LEDs is provided which glows for entry of invalid data. Check for invalid data is done by software. The LEDs are connected to the outputs of the buffer.

The buffer employed in 74LS241 which is a tristate buffer. It is enabled for the address 8000. The address line A_{14} and A_{13} are given as inputs to a NOR gate whose output along with A_{15} are fed as inputs to an AND gate. LED current

SOFTWARE

The program source code is written in this section to fulfill the hardware implementation. The source code consists of modules that are further divided into several subprograms (Subroutines). There is a main program which is interrupted by two interrupt serve subroutines. One subroutine is an interrupt that caters to the need of 8279 and the other one caters to the need of RTC interrupting for every second.

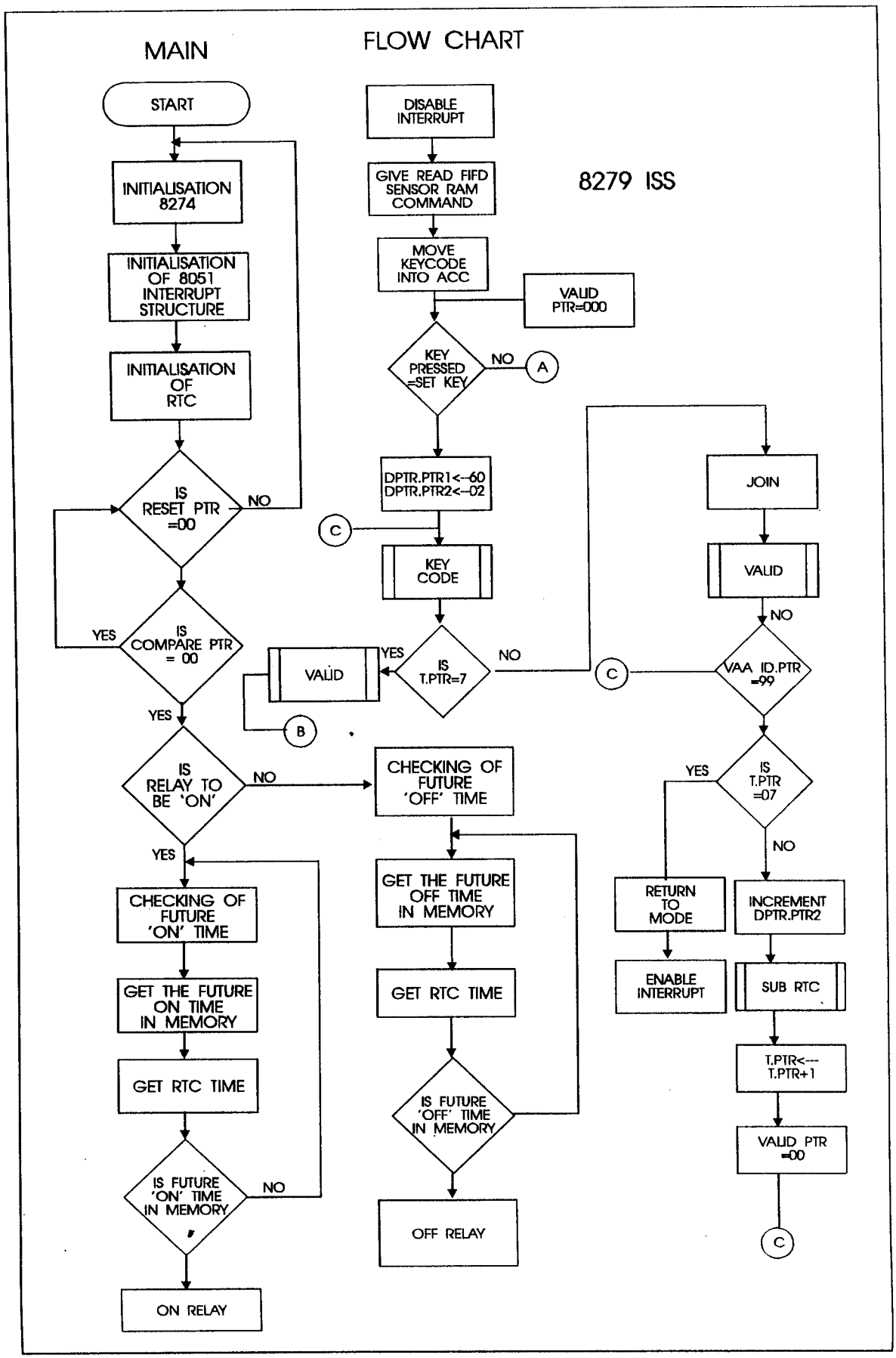
The main program does the initialisation and if FUTURE key has been pressed, executes the instructions for implementing relay control. It does the job of initialising 8279, RTC, 8051 interrupt structure. The interrupt service subroutine of RTC is executed by the controller every second, when the interrupt is activated. The seconds value is moved to the accumulator and added with the starting address of the look up table. The value from this new address is sent to the 8279 which takes care of the multiplexed display. By the above mentioned procedure. the remaining contents of the real time clock are displayed.

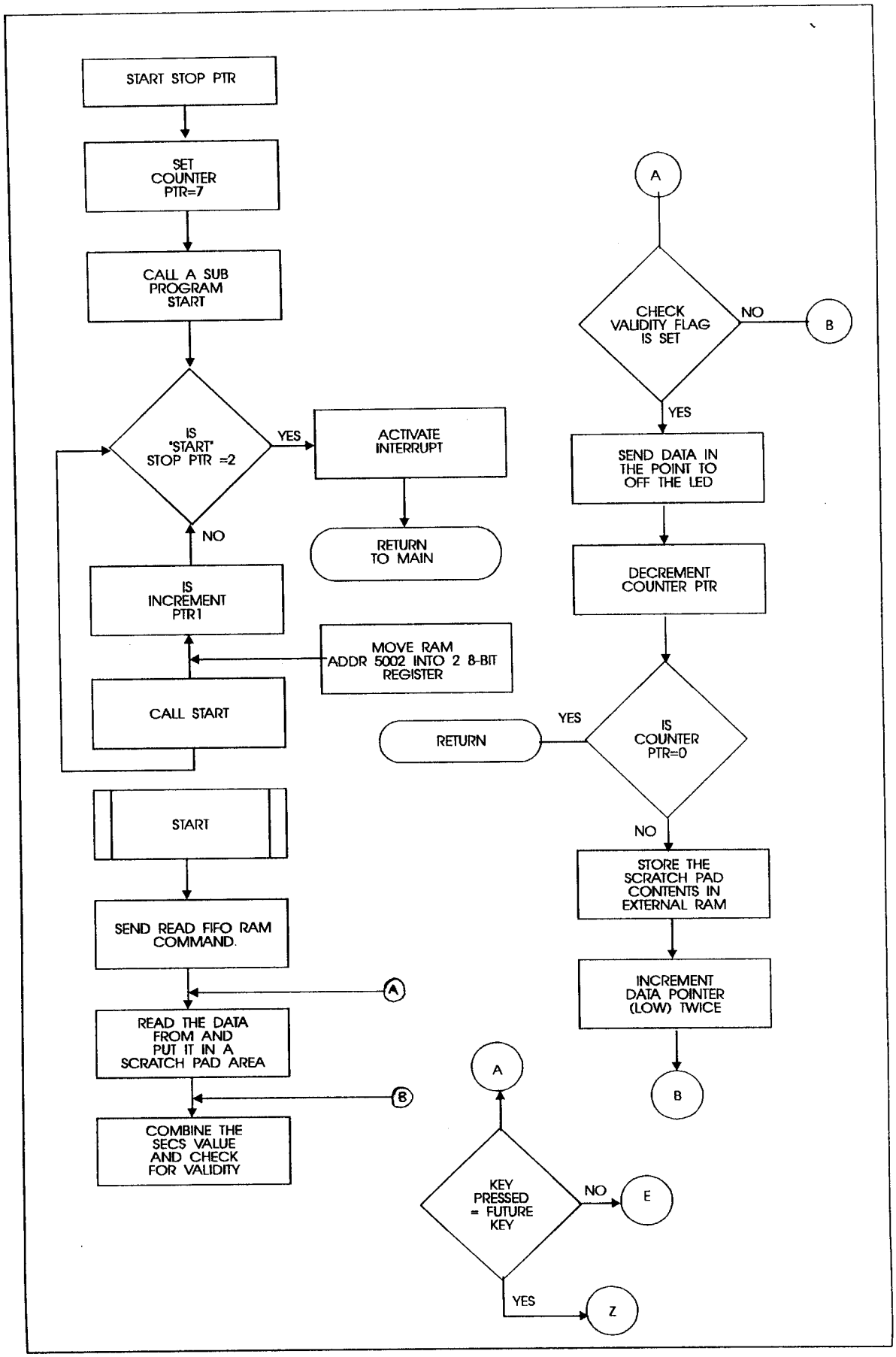
The 8279 interrupt service subroutine takes care of the keyboard interface. If pressing of the set key the values transfers control to the subroutine, the numerical keys pressed thereafter are transferred to the RTC, thus stoing the present time.

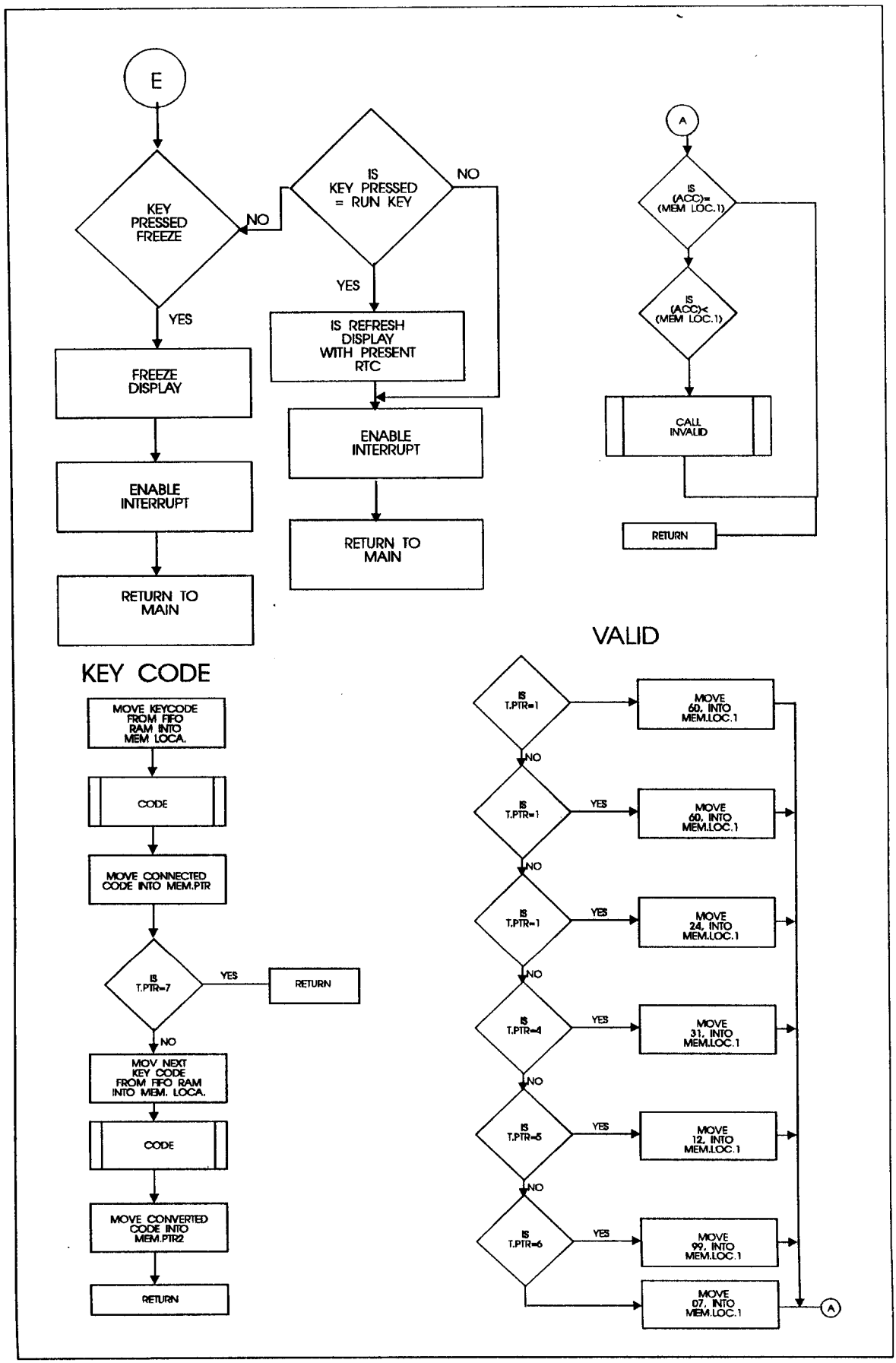
This is written in a modular form. The key code subroutine transfers the data from the first two locations of the FIFO RAM to locations in the data memory. The validity of the data entered, is checked by comparing it with the maximum possible valid data. In case of invalid data, the subroutine named invalid, sends the data to the time invalid indicating LEDs corresponding.

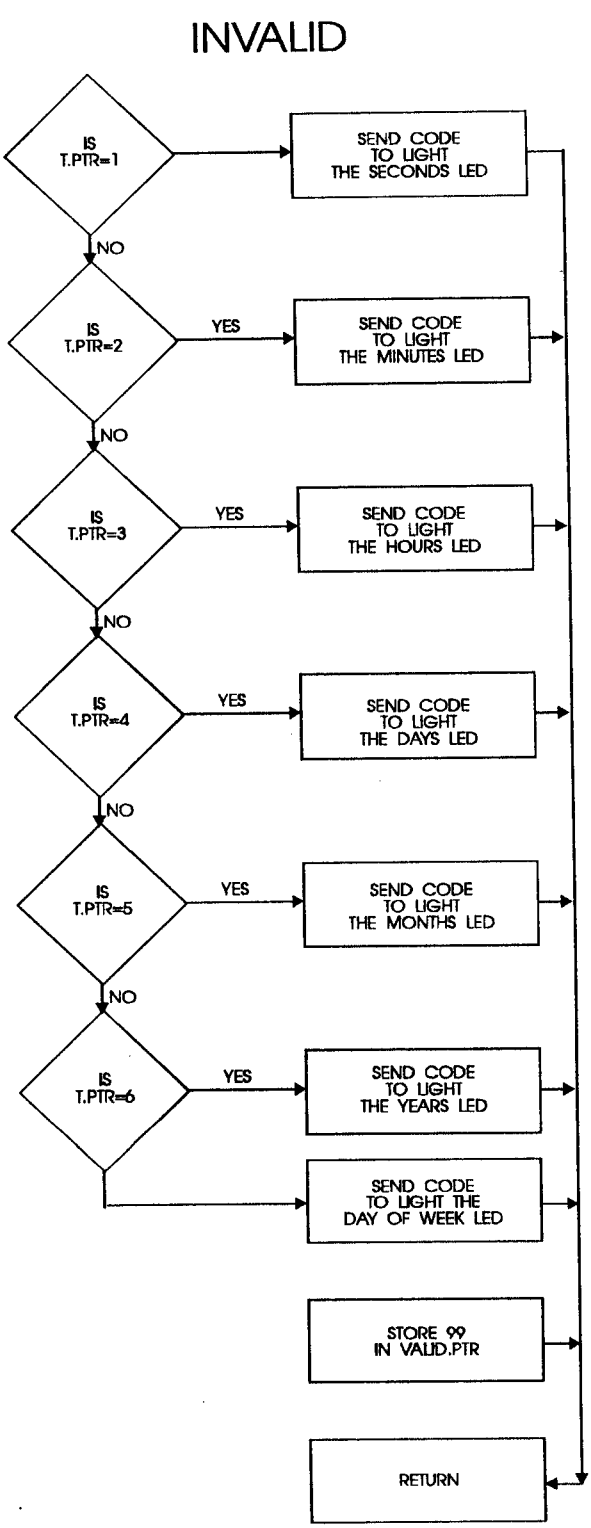
The conversion of the data pressed from the contact matrix format to decimal format is implemented using subroutine code . This iss also transfers the data entered after pressing the future key by the required memory locations which is utilised in the main program.

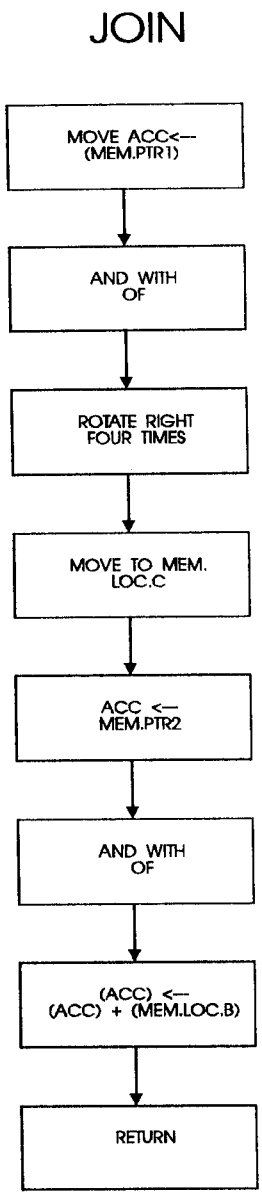
The counter join subroutine combine the units and the tenths value of the entered data to check validity. The software has been written utilising the instruction set of 8051 and since it is in a modular format, it is flexible for future changes.


MAIN
FLOW CHART
8279 ISS
START
INITIALISATION 8274
INITIALISATION OF 8051 INTERRUPT STRUCTURE
INITIALISATION OF RTC
IS RESET PTR =00
NO
YES
IS COMPARE PTR = 00
YES
IS RELAY TO BE 'ON'
NO
YES
CHECKING OF FUTURE 'ON' TIME
GET THE FUTURE ON TIME IN MEMORY
GET RTC TIME
IS FUTURE 'ON' TIME IN MEMORY
NO
ON RELAY
DISABLE INTERRUPT
GIVE READ FIFD SENSOR RAM COMMAND
MOVE KEYCODE INTO ACC
VALID PTR=000
KEY PRESSED =SET KEY
NO
A
DPTR.PTR1<--60
DPTR.PTR2<--02
C
KEY CODE
IS T.PTR=7
YES
VALID
B
NO
CHECKING OF FUTURE 'OFF' TIME
GET THE FUTURE OFF TIME IN MEMORY
GET RTC TIME
IS FUTURE 'OFF' TIME IN MEMORY
OFF RELAY
JOIN
VALID
NO
VAA ID.PTR =99
C
YES
IS T.PTR =07
YES
RETURN TO MODE
ENABLE INTERRUPT
NO
INCREMENT DPTR.PTR2
SUB RTC
T.PTR<--- T.PTR+1
VALID PTR =00
C


START STOP PTR
SET COUNTER PTR=7
CALL A SUB PROGRAM START
IS "START" STOP PTR =2
YES
ACTIVATE INTERRUPT
RETURN TO MAIN
NO
IS INCREMENT PTR1
MOVE RAM ADDR 5002 INTO 2 8-BIT REGISTER
CALL START
START
SEND READ FIFO RAM COMMAND.
A
READ THE DATA FROM AND PUT IT IN A SCRATCH PAD AREA
B
COMBINE THE SECS VALUE AND CHECK FOR VALIDITY
A
CHECK VALIDITY FLAG IS SET
NO
B
YES
SEND DATA IN THE POINT TO OFF THE LED
DECREMENT COUNTER PTR
IS COUNTER PTR=0
YES
RETURN
NO
STORE THE SCRATCH PAD CONTENTS IN EXTERNAL RAM
INCREMENT DATA POINTER (LOW) TWICE
B
A
KEY PRESSED = FUTURE KEY
NO
E
YES
Z


E
KEY PRESSED FREEZE
NO
YES
FREEZE DISPLAY
ENABLE INTERRUPT
RETURN TO MAIN
IS KEY PRESSED = RUN KEY
NO
YES
IS REFRESH DISPLAY WITH PRESENT RTC
ENABLE INTERRUPT
RETURN TO MAIN
A
IS (ACC)= (MEM LOC.1)
IS (ACC)< (MEM LOC.1)
CALL INVALID
RETURN
KEY CODE
MOVE KEYCODE FROM FIFO RAM INTO MEM LOCA.
CODE
MOVE CONNECTED CODE INTO MEM.PTR
IS T.PTR=7
YES
RETURN
NO
MOV NEXT KEY CODE FROM FIFO RAM INTO MEM. LOCA.
CODE
MOVE CONVERTED CODE INTO MEM.PTR2
RETURN
VALID
IS T.PTR=1
MOVE 60, INTO MEM.LOC.1
NO
IS T.PTR=1
YES
MOVE 60, INTO MEM.LOC.1
NO
IS T.PTR=1
YES
MOVE 24, INTO MEM.LOC.1
NO
IS T.PTR=4
YES
MOVE 31, INTO MEM.LOC.1
NO
IS T.PTR=5
YES
MOVE 12, INTO MEM.LOC.1
NO
IS T.PTR=6
YES
MOVE 99, INTO MEM.LOC.1
MOVE 07, INTO MEM.LOC.1
A


INVALID
IS T.PTR=1
SEND CODE TO LIGHT THE SECONDS LED
NO
IS T.PTR=2
YES
SEND CODE TO LIGHT THE MINUTES LED
NO
IS T.PTR=3
YES
SEND CODE TO LIGHT THE HOURS LED
NO
IS T.PTR=4
YES
SEND CODE TO LIGHT THE DAYS LED
NO
IS T.PTR=5
YES
SEND CODE TO LIGHT THE MONTHS LED
NO
IS T.PTR=6
YES
SEND CODE TO LIGHT THE YEARS LED
SEND CODE TO LIGHT THE DAY OF WEEK LED
STORE 99 IN VALID.PTR
RETURN


JOIN
MOVE ACC<-- (MEM.PTR1)
AND WITH OF
ROTATE RIGHT FOUR TIMES
MOVE TO MEM. LOC.C
ACC <-- MEM.PTR2
AND WITH OF
(ACC) <-- (ACC) + (MEM.LOC.B)
RETURN

PROGRAM

MAIN	MOV DPTR, #A001	
	MOV A,# 08	Keyboard display mode set
	MOV @DPTR, A	
	MOV A, #	Program Clock
	MOV @ DPTR, A	
	MOV A, #D2	Clear
	MOV @ DPTR, A	
	MOV A8, #85	Interrupt enable
	MOV B8, #04	Interrupt priority
	MOV D0, #08	PSW Inialisation
	MOV DPTR, #6000	
	MOV A,# 0F	
	MOV @DPTR, A	
	MOV DPTR, #600F	
	MOV A, #00	
	MOV X @ DPTR, A	
	MOV DPTR, #6000	RTC Initialization
	MOV A, #605	
	MOV X @ DPTR, A	
	MOV A, #01	
L1	INC DPTR	
	MOV X @ DPTR, A	
	CJNE 82, # 0E, L1	
	AJMP L1	
	INC DPTR	
	MOV A, #01	
	MOV X @ DPTR, A	
	MOV A, #05	
	MOV X @ DPTR, A	
	MOV DPTR, #6000	
	MOV A, #00	
	MOV X@ DPTR, A	
R2	CJNE 38, #00, R1	
	CJNE 39, #00, L3	
	AJMP R2	

R1	AJMP MAIN	
L3	MOV D0, #04	Intialise PSW
	MOV R5, #20	
	MOV A, 90	
	CJME A, #20, A4	Checking pervious status of port 1
	MOV R5, #00	
	MOV R2, #50	
	AJMP L7	
L4	MOV R2, #40	
	MOV R5, #20	
L7	MOV R3, #07	Intialise Counter
	MOV DPTR #4004	
	MOV 83, R2	
L0	MOVX A, @DPTR	future time in location 55
	MOV 55, A	
	MOV 83, 60	
	MOV X A, @DPTR	; Getting RTC time
	CJME A, 55,L1	Comparing RTC time and future time
	INC DPTR	If equal check next value else go back
	MOV 83, R2	to main
	DEC R2	
	CJME R3, #00, LO	
	MOV 90, R5	Moving data to port 1.
L1	AJMP MAIN	
ISS	MOV 81, #7F	Intialise stack point
	MOV A8, #00	
	MOV DPTR #8000	
	MOV A, #80	
	MOV @ DPTR, A	
	MOV D0, #04	Intialise PSW
	PUSH A	Saving contents registers and DPTR
	PUSH R5	
	PUSH R2	
	PUSH R3	
	PUSH DPL	
	PUSH DPH	
	PUSH 55	

	MOV D0, #10	
	MOV DPTR, #6002	
L2	PUSH 82	RTC time in Accumulator
	PUSH 83	
	MOV A, @DPTR	
	MOV DPTR #1000	
	MOV A, A+ @ DPTR	
	MOV R3, A	Equivalent 7 segment code in R3
	MOV DPTR, #A001	
	MOV A, #90	
	MOVX @ DPTR, A	Send to 8279 for display
	MOV A, R3	
	INC DPTR	
	MOVX, @ DPTR, A	
	MOV A, R3	
	INC DPTR	
	MOVX, @ DPTR, A	
	POP 83	
	POP 82	
	CJNE 2, #00, L3	
	MOV D0, #04	
	POP 55	Retrieve Contents of Registers and
	POP DPH	DPTR
	POP DPL	
	POP R3	
	POP R2	
	POP R5	
	POP A	
	MOV A8, #85	
	MOV DPTR, #8000	
	MOV A, #00	
	MOV @ DPTR, A	
L3	INC DPTR	
	AJMP L2	
	RETI	
ISS2	MOV A8, #00	
	MOV 81, #7F	

	MOV D0, #04	PSW initialisation
	PUSH A	
	PUSH R5	
	PUSH R2	
	PUSH R3	
	PUSH DPL	
	PUSH DPH	
	PUSH 55	
	MOV D0, #18	
	MOV DPTR, #A001	
	MOV A, #50	Read FIFO sensor RAM command
	MOV @ DPTR, A	
	MOV 40, #00	
	MOV R3, #01	
	INC DPTR	
	MOVX A, @DPTR	
	CJNE A, # , N1	Check if future key
	MOV R5, #60	
	MOV R4, #02	
R1	CALL KEY CODE	Get key code
	CJNE R3, #07, L4	
	CALL VALID	
	AJMP N1	
L4	CALL JOIN	
	CALL VALID	Check for validity of key code
N1	MOV A, #99	
	CJNE A, #40, M1	
	AJMP R1	
M1	CJNE R3, #07, S1	
	MOV D0, #04	
	POP 55	
	POP DPH	
	POP DPL	
	POP R3	
	POP R2	
	POP R5	
	POP A	
	MOV A8, #85	

	RETI	
S1	INC R4	
	MOV 82, R4	
	MOV 83, R5	
	CALL SUB RTC	
	INC R3	
	MOV 40, #00	
	AJMP R1	
SUB RTC	CJNE R3, #07, Y1	If data entered for DOW then no
	MOV, A, 45	combination
	MOV @ DPTR, A	
	AJMP Y2	
Y1	MOV A, 46	
	MOV @ DPTR, A	
	INC DPTR	
	MOV A, 45	
	MOV @ DPTR, A	
Y2	MOV DPTR, #8000	Data valid
	MOV A, #00	
	MOVX @ DPTR A	
	RET	
VALID	CJNE R3, #01, A1	If data is for seconds it should be
	MOV 50, # 3C	< 60
	AJMP R1	
L1	CJNE R3, #02, L2	If data is for minutes it should be less
	MOV 50, #3C	than 60
	AJMP R1	
L2	CJNE R3, #08, L3	If data is for hours it is less than 24
	MOV 50, #18	
L3	CJNE R3, #04, L4	If data is for date it should be for < 31
	MOV 50, #1F	
	AJMP R1	
L4	CJNE R3, #05, L5	If data is for months it should be < 12
	MOV 50, #0C	
	AJMP R1	
L5	CJNE R3, #06, L6	If data is for years it should be < 99
	MOV 50, #63	
	AJMP R1	

L6	MOV 50, #07	
	CJNE A, 50, Z1	
Z2	RET	
Z1	JC Z2	Check data is invalid
	CALL INVALID	
	RET	
INVALID	MOV DPTR, #8000	Depending on the value of R3
	CJNE R3, #01, N1	check for validity of corresponding
	MOV A, #01	data and indicate
	MOV X @ DPTR, A	
	AJMP N8	
N1	CJNE R3, #02, N2	
	MOV A, #02	
	MOV @ DPTR, A	
	AJMP N8	
N2	CJNE R3, #03, N3	
	MOV A, #04	
	MOVX @ DPTR , A	
	AJMP N8	
N3	CJNE R4, #04, N4	
	MOV A, #08	
	MOV X, @ DPTR, A	
	AJMP N8	
N4	MOV R3, #05, N5	
	MOV A, #10	
	MOVX @ DPTR, A	
	AJMP N8	
N5	CJNE R3, #06, N6	
	MOV A, #20	
	MOVX @ DPTR, A	
	AJMP N8	
N6	MOV A, #40	
	MOV @ DPTR ,A	
N8	MOV 40, #99	
	RET	
KEYCODE	MOV DPTR #A002	To get the key from keycode
	MOV X, A, @ DPTR	
	MOV D0, #10	

	MOV R4, A	
	CALL CODE	
	MOV 45, R7	
	MOV D0, #18	
	CJNE R3, #07, S1	
	RET	
S1	MOV A, # DPTR	
	MOV D0, #10	
	MOV R4, A	
	CALL CODE	
	MOV 46, R7	
	MOV D0, #18	
	RET	
JOIN	MOV A, 45	To join two 4-bit data
	ANL A, #0F	
	RR	
	RR	
	RR	
	RR	
	MOV 47, A	
	MOV A, 46	
	ANL A, #0F	
	ADD 47	
	RET	
CODE	MOV DPTR, #15,FF	
	MOV R7, #00	
M2	MOV A, @ DPTR	
	MOV 35, A	
	CJNE R4, 35,M1	
	INC R7	
	RET	
M1	INC DPTR	
	AJMP M2	
FUTURE	CJNE A, # FREEZE	Check of future key
	MOV A8, #00	If yes, check for validity
	MOV 39, #01	and store datas
	MOV R1, #01	
	MOV R0, #07	

	MOV R6, #02	
	MOV R7, #40	
	CALL START	
	CJNE R1, #02, rel 3	
	MOV D0, #04	
	POP 55	
	POP DPH	
	POP DPL	
	POP R3	
	POP R2	
	POP R5	
	POP A	
	MOV A8, #85	
	MOV 39, #00	
	RETI	
rel3	INC R1	
	MOV R0, #07	
	MOV R6, #02	
	MOV R5, #50	
	CALL START	
	AJMP S2	
START	MOV R3, #02	
L1	MOV DPTR, #A002	
	MOVX A, @ DPTR	
	MOV D0, #10	
	MOV R4, A	
	ACALL CODE	
	MOV 30, R7	
	MOV DPTR, #A002	
	MOVX A, @ DPTR	
	MOV R4, A	
	ACALLCODE	
	MOV 31, R7	
	MOV D0, #18	
	ACALL COMBINE	
	ACALL VALID	
	MOV A, #99	
	CJNE A, #99, rel ad1	

	AJMP L1	
rel ad1	MOV DPTR, #8000	
	MOV A, #00	
	MOVX @ DPTR	
	DEC R0	
	CJNE R0, #00, rel 2	
	RET	
rel 2	MOV 82, R6	
	MOV 83, R7	
	MOV A, 31	
	MOV @ DPTR, A	
	INC DPTR	
	MOV A, 30	
	MOV @ DPTR	
	INC R3	
	INC R6	
	INC R6	
	AJMP L1	
COMBINE	MOV A, 30	
	ANL A, #0F	
	RR	
	RR	
	RR	
	RR	
	MOV R2, A	
	MOV A, 31	
	ANL A, #0F	
	ADD A, R2	
	RET	
FREEZE	CJNE A, # , RUN	Check if FREEZE key
	MOV DPTR, #A001	If yes, blank the display
	MOV A, #	
	MOV D0, #04	
	POP 55	
	POP DPH	
	POP DPL	
	POP R3	
	POP R2	

	POP R5	
	POP A	
	MOV A8, #85	
	RETI	
RUN	CJNE A, # , L5	Check if RUN key
	MOV D0, #04	
	POP 55	
	POP DPH	
	POP DPL	
	POP R3	
	POP R2	
	POP R5	
	POP A	
	MOV A8, #85	
	RETI	
RESET	MOV 38, #FF	Check if RESET key
L5	POP 55	If yes, goto main
	POP DPH	
	POP DPL	
	POP R3	
	POP R2	
	POP R5	
	POP A	
	MOV A8, #85	
	RETI	

Conclusion

CONCLUSION

The microcontroller based real time Clock/Calendar/Timer can be improved for further applications in industries. This real time clock can be implemented as μP watch dog and as a Japanese showa calendar. Further extension of its application includes:

* Traffic light control
* Street light switching
* Time study

The factors that support the above improvements are:

* It is mainly software controlled
* Crystal accuracy of the microcontroller

Bibliography

BIBLIOGRAPHY

1. *"Digital Logic and Computer Design"* - **MORRIS MANO**

2. *"Microprocessor Architecture, Programming and Applications"* Second Edition, New age International Private ltd.- **R.S.GAONKAR**

3. *"Microprocessors and Interfacing Programming and Hardware"* - **DOUGLAS .V. HALL**, Tata McGraw Hill.

4. National Semiconductor *"Advanced peripherals real time clock handbook"*

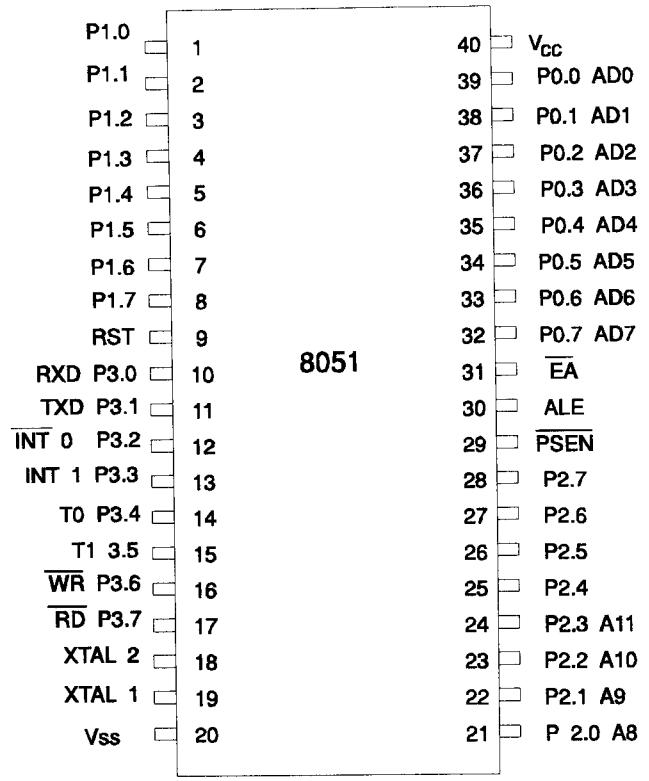
5. *TTL - IC's Data Book.*

6. *Memory Components Handbook*

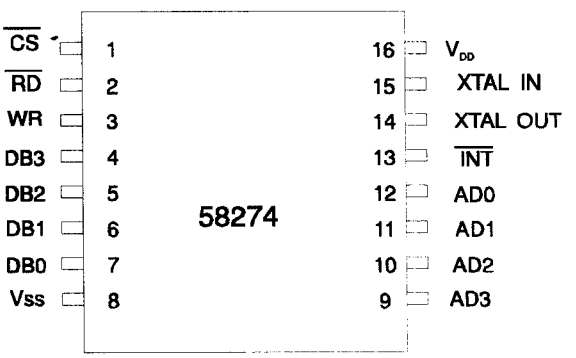
7. *Intel Microcontroller Manual* - Vol. II.

8. *"Fundamentals of Computers"* - **V.RAJARAMAN**

Annexure



MCS-51 CONNECTIONS



MM58274C TOP VIEW

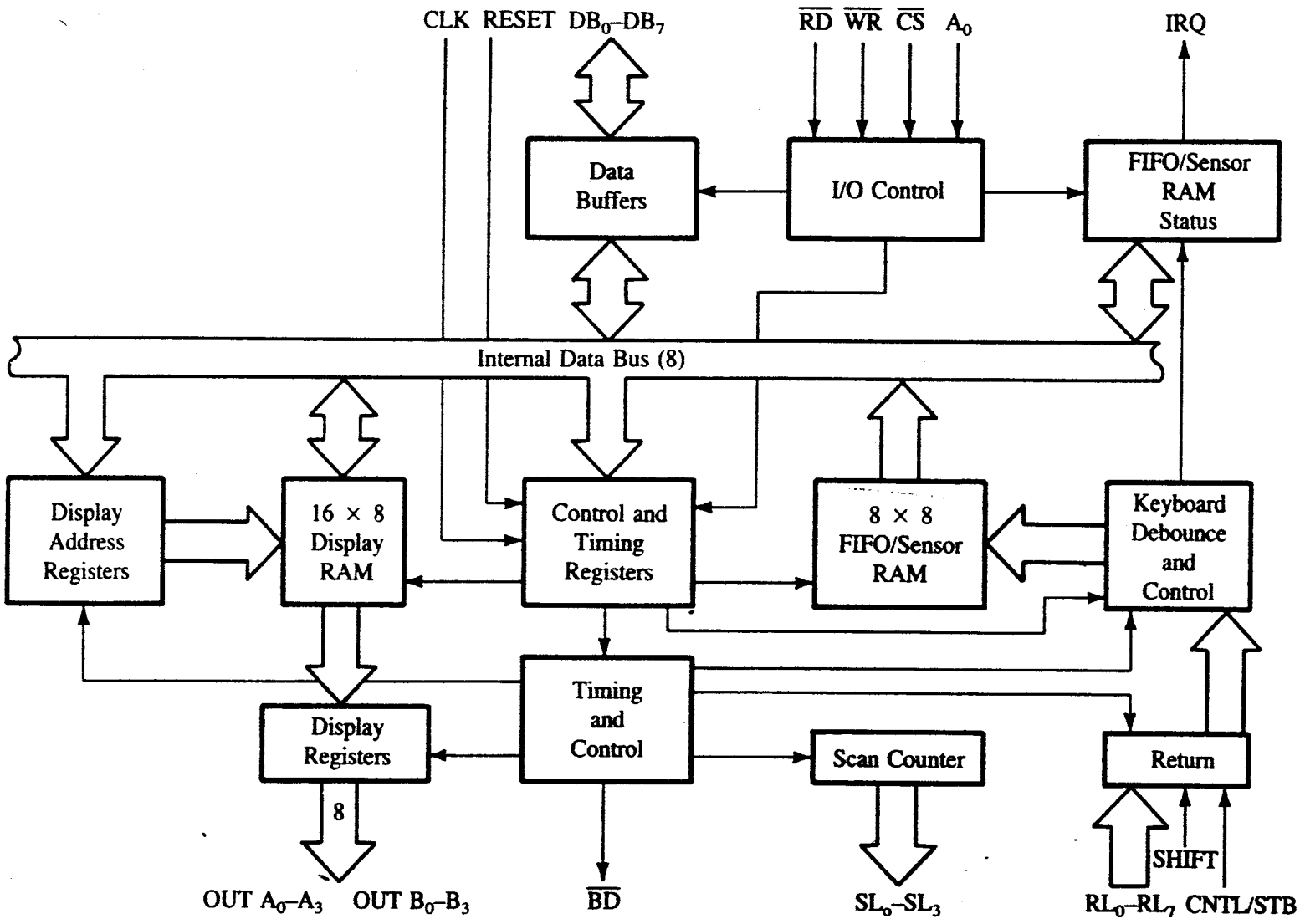
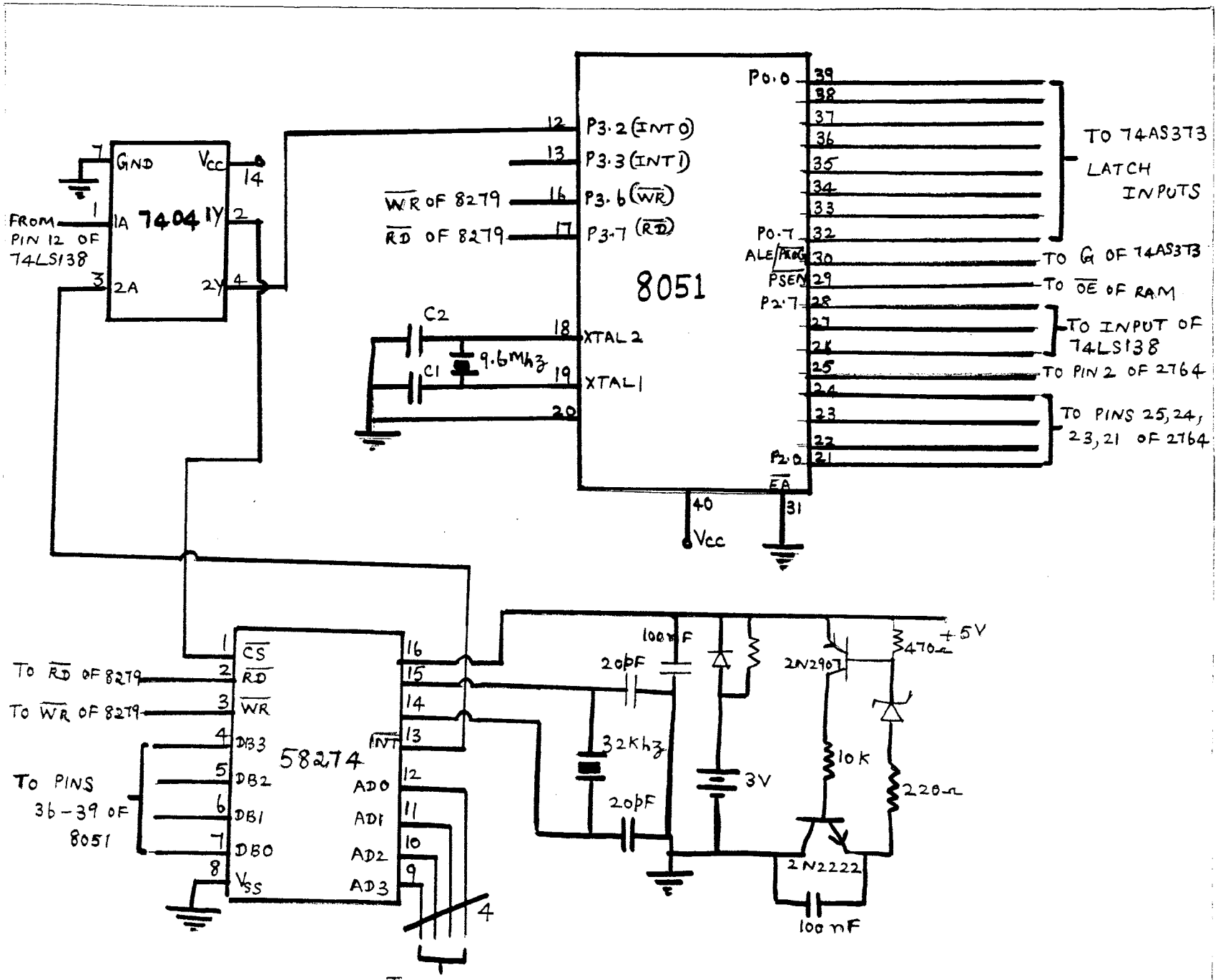
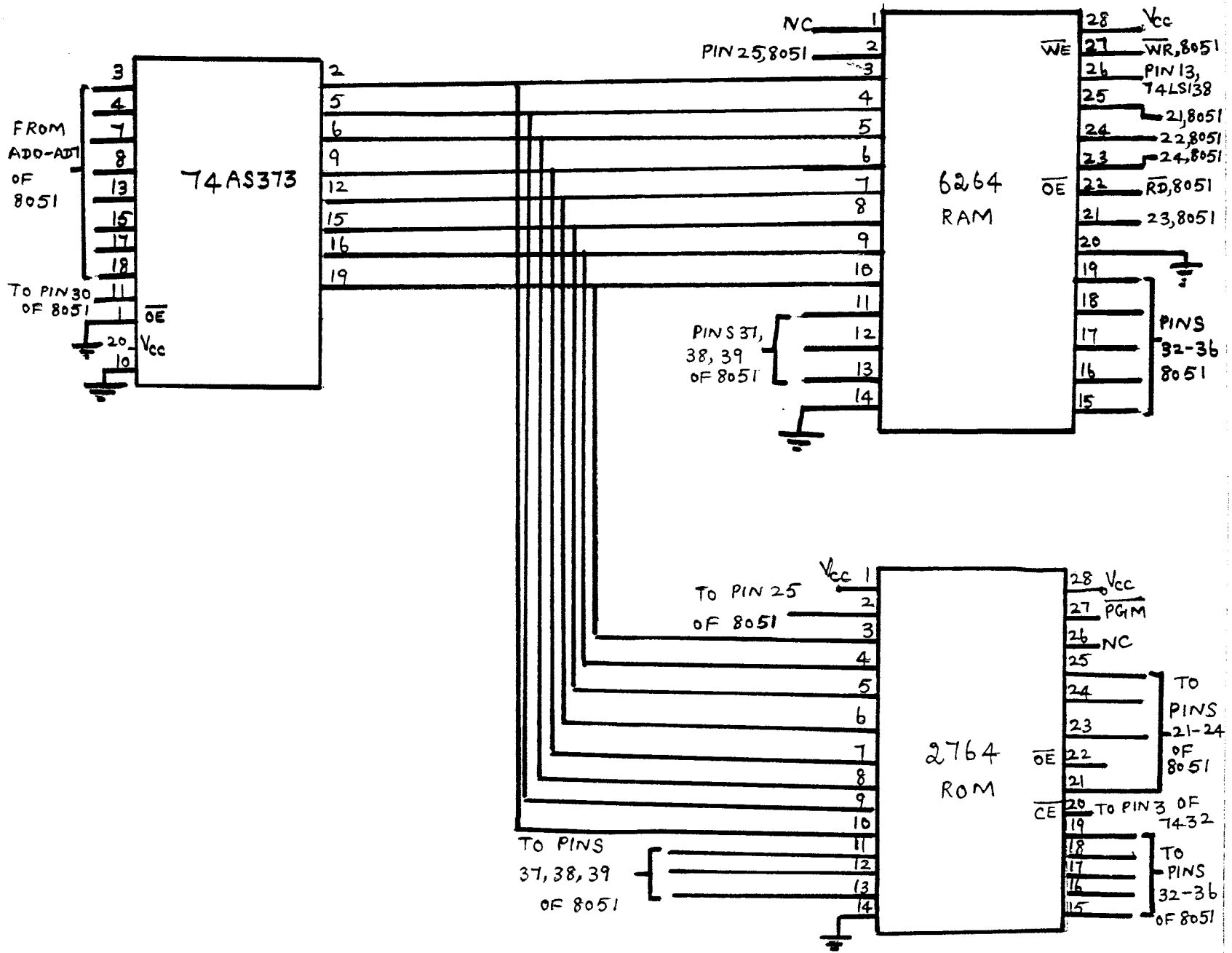
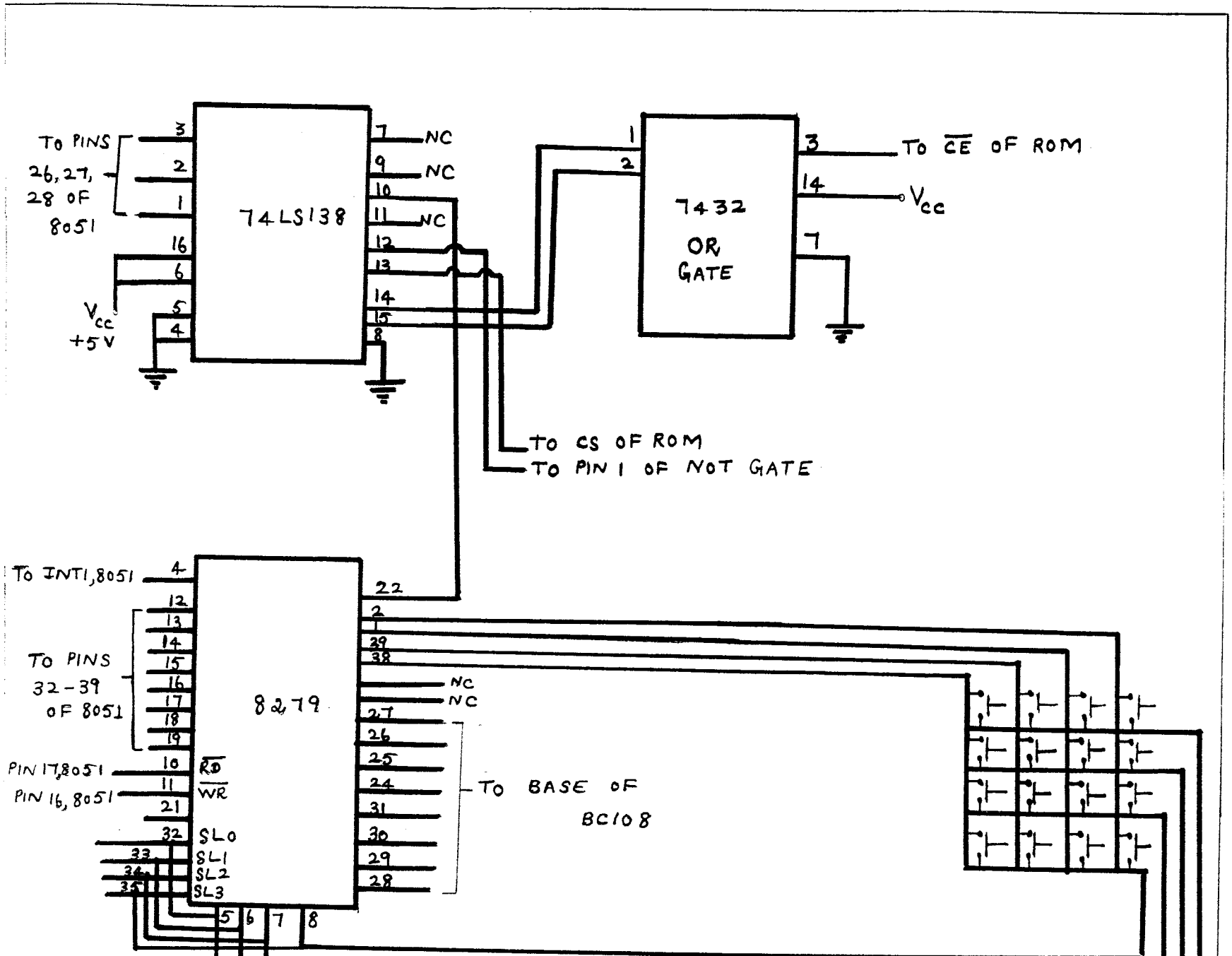
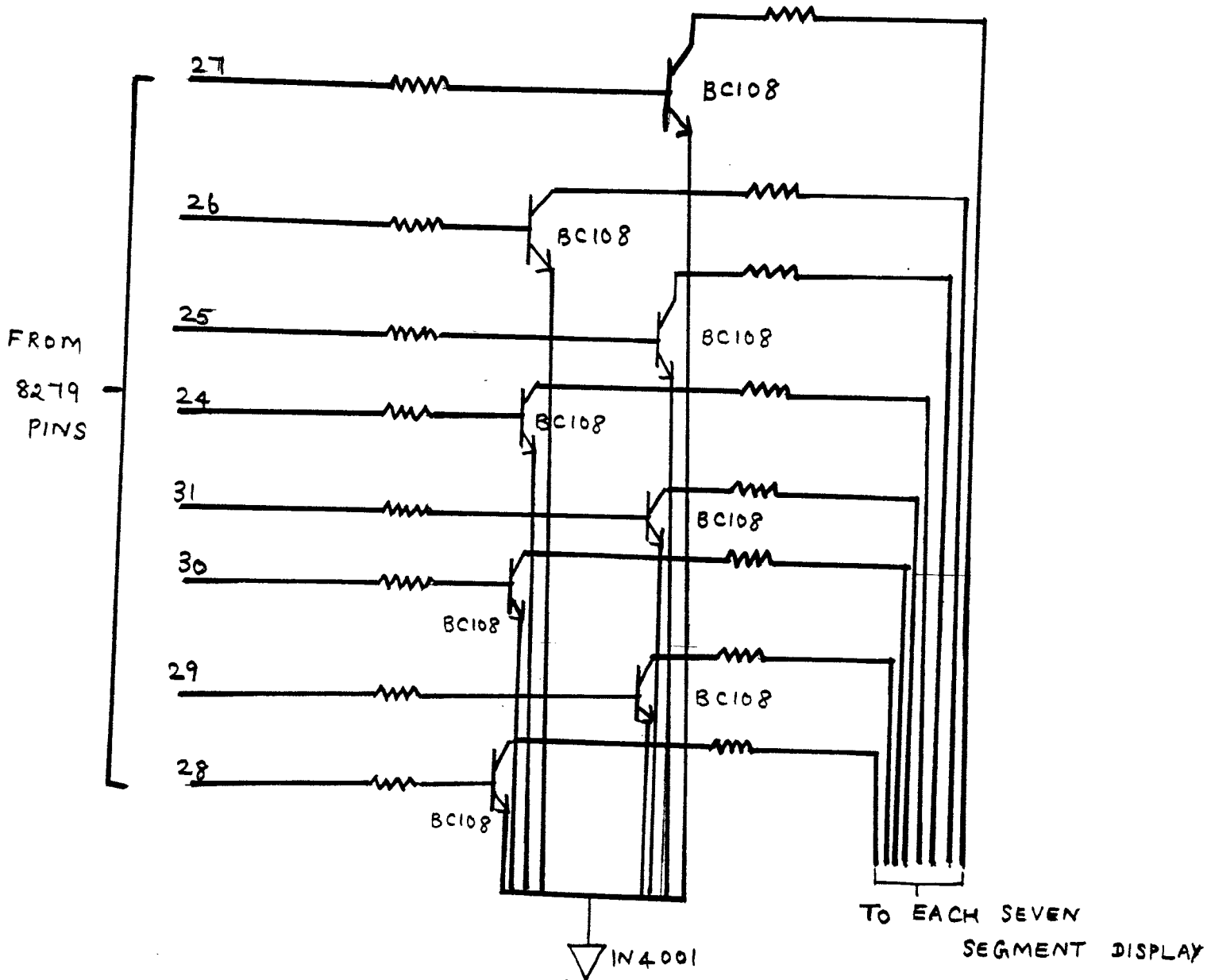


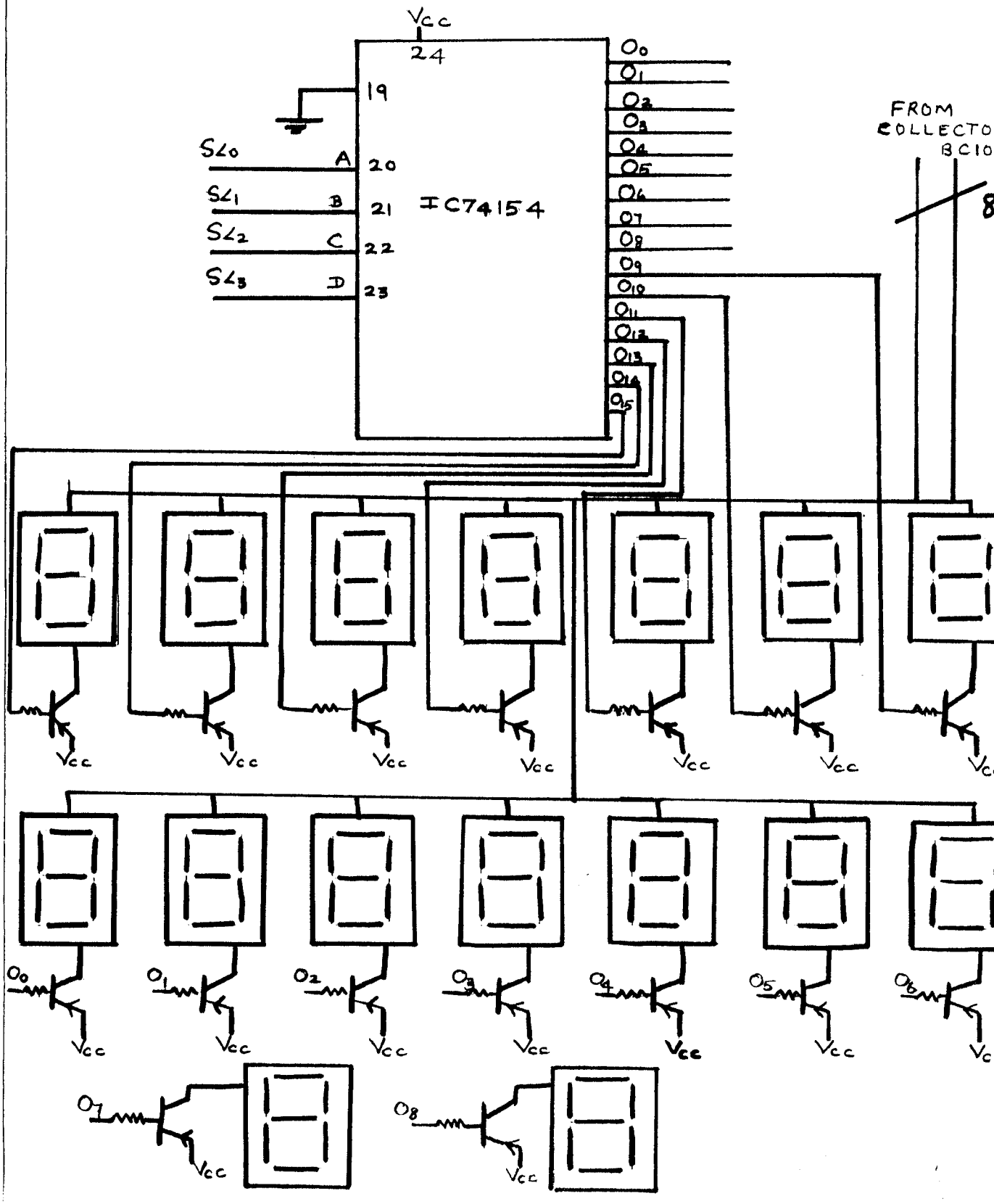
FIGURE 14.18
The 8279 Logic Block Diagram

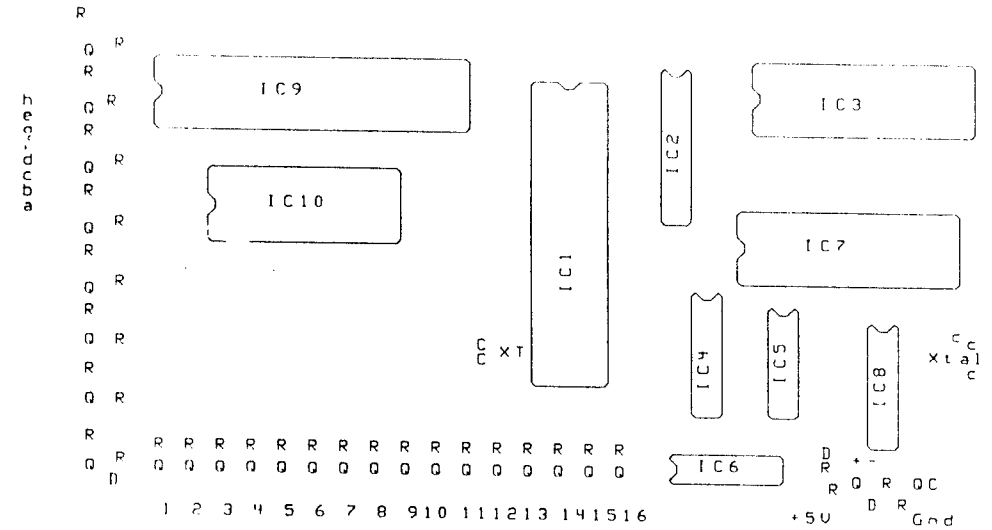

8051
P0.0
P0.7
ALE/PROG
PSEN
P2.7
P2.0
EA
P3.2 (INT0)
P3.3 (INT1)
P3.6 (WR)
P3.7 (RD)
XTAL2
XTAL1
Vcc
TO 74AS373 LATCH INPUTS
TO G OF 74AS373
TO OE OF RAM
TO INPUT OF 74LS138
TO PIN 2 OF 2764
TO PINS 25,24, 23,21 OF 2764
WR OF 8279
RD OF 8279
C2
C1
9.6MHz
FROM PIN 12 OF 74LS138
7404
GND
Vcc
1A
1Y
2A
2Y
58274
CS
RD
WR
INT
DB3
DB2
DB1
DB0
Vss
AD0
AD1
AD2
AD3
TO RD OF 8279
TO WR OF 8279
TO PINS 36-39 OF 8051
100nF
20pF
32kHz
3V
2N2907
2N2222
470Ω
10k
220Ω
+5V

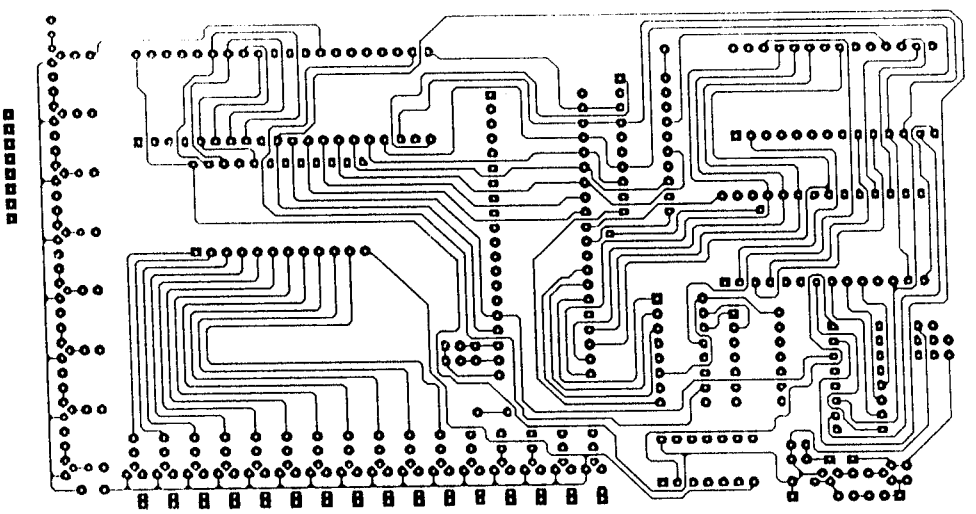

74AS373
FROM AD0-AD7 OF 8051
TO PIN 30 OF 8051
OE
Vcc
6264 RAM
NC
PIN 25, 8051
WE
OE
WR, 8051
PIN 13, 74LS138
21, 8051
22, 8051
24, 8051
RD, 8051
23, 8051
PINS 32-36 8051
PINS 37, 38, 39 OF 8051
2764 ROM
TO PIN 25 OF 8051
PGM
CE
TO PIN 3 OF 74-32
TO PINS 21-24 OF 8051
TO PINS 32-36 OF 8051
TO PINS 37, 38, 39 OF 8051

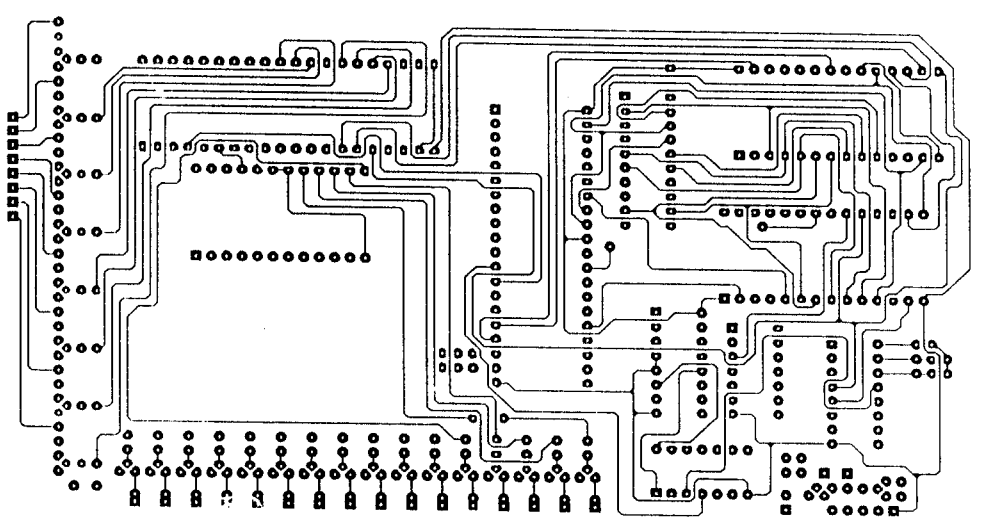

TO PINS 26, 27, 28 OF 8051
74LS138
NC
NC
NC
V_{cc} +5V
7432 OR GATE
TO $\overline{CE}$ OF ROM
V_{cc}
TO CS OF ROM
TO PIN 1 OF NOT GATE
TO INT1, 8051
TO PINS 32-39 OF 8051
8279
PIN 17, 8051
PIN 16, 8051
$\overline{RD}$
$\overline{WR}$
SL0
SL1
SL2
SL3
NC
NC
TO BASE OF BC108


FROM
8279
PINS
27
26
25
24
31
30
29
28
BC108
BC108
BC108
BC108
BC108
BC108
BC108
BC108
IN4001
TO EACH SEVEN
SEGMENT DISPLAY


Vcc
24
19
IC74154
A
B
C
D
20
21
22
23
FROM
COLLECTO
BC10
Vcc


IC9
IC10
IC1
IC2
IC3
IC7
IC4
IC5
IC8
IC6
XT
Xtal
+5V
Gnd
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16



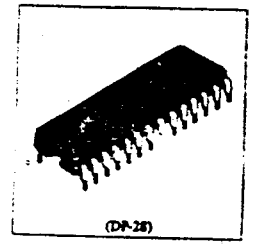


HM6264P-10, HM6264P-12, HM6264P-15

8192 word × 8-bit High Speed Static CMOS RAM

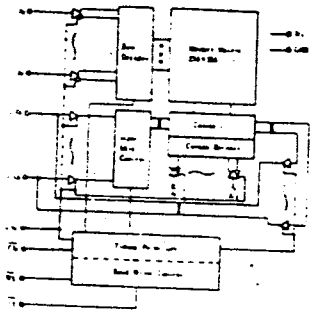
FEATURES

- Fast access Time — 100ns/120ns/150ns (max.)
- Low Power Standby — Standby: 0.1mW (typ.)
- Low Power Operation — Operating: 200mW (typ.)
- Single +5V Supply
- Completely Static Memory — No clock or Timing Strobe Required
- Equal Access and Cycle Time
- Common Data Input and Output: Three State Output
- Directly TTL Compatible: All Input and Output
- Standard 28pin Package Configuration
- Pin Out Compatible with 64K EPROM HN482764

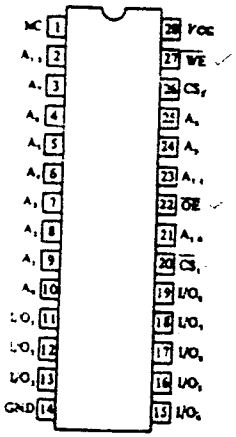


(DP-28)

BLOCK DIAGRAM



PIN ARRANGEMENT



(Top View)

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage *	V_T	−0.5 ** to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Storage Temperature (Under Bias)	T_{bias}	−10 to +85	°C

* With respect to GND. ** Pulse width 50ns: −3.0V

TRUTH TABLE

WE	$\overline{CS_1}$	CS_2	$\overline{OE}$	Mode	I/O Pin	V_{CC} Current	Note
X	H	X	X	Not Selected (Power Down)	High Z	I_{SB}, I_{SB1}	
X	X	L	X		High Z	I_{SB}, I_{SB1}	
H	L	H	H	Output Disabled	High Z	I_{CC}, I_{CC1}	
H	L	H	L	Read	Dout	I_{CC}, I_{CC1}	
L	L	H	H	Write	Din	I_{CC}, I_{CC1}	Write Cycle (1)
L	L	H	L		Din	I_{CC}, I_{CC1}	Write Cycle (2)

H = High, L = Low, X = H or L

MOTOROLA

MCM63256

Product Preview

256K BIT READ ONLY MEMORY

The MCM63256 is a MOS mask programmable byte-organized Read Only Memory (ROM). The MCM63256 is organized as 32,768 bytes of 8 bits and is fabricated using Motorola's high performance N-channel silicon gate technology (HMOS). This device is designed to provide maximum circuit density and reliability with highest possible performance while maintaining low power dissipation and wide operating margins and remaining fully compatible with TTL inputs and outputs.

The active level of the Chip Enable and the Output Enable, along with the memory contents, are defined by the user. The Chip Enable input deselects the device and puts the chip in a power-down mode.

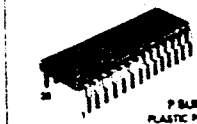
- Single ± 10% +5 Volt Power Supply
- Fully Static Periphery — No Clocking Required on Chip Enable
- Automatic Power Down
- Power Dissipation
  - 100 mA Active Maximum (Unloaded)
  - 15 mA Standby Maximum
- Current Surge Suppression When Powering Up Device
- Program Layer Used in Process for Quick Turnaround Time
- 150 ns Maximum Access from Address and Chip Enable
- 28-Pin JEDEC Standard Package and Pinout

ADDITIONAL FEATURE

- Address 14/15 is User Selectable for Either Pin 27 or Pin 1

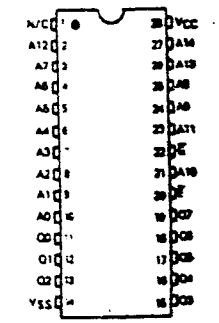
HMOS
N-CHANNEL, SILICON GATE

32,768 × 8 BIT
READ ONLY MEMORY



P SUFFIX
PLASTIC PACKAGE
CASE 710

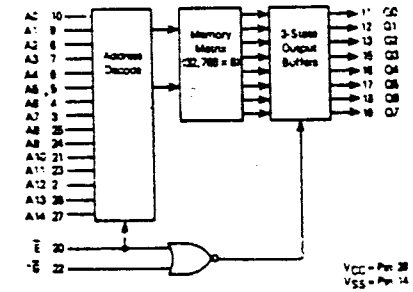
PIN ASSIGNMENT



PIN NAMES

A0-A14	Address
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
Q0-Q7	Data Output
VCC	+5 V Power Supply
VSS	Ground

BLOCK DIAGRAM



*Active levels defined by the user

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

MP-350/R-MC

64K (8K x 8) CHMOS PRODUCTION AND UV ERASABLE PROMS

- **CHMOS Microcontroller and Microprocessor Compatible**
  - **87C64-Integrated Address Latch**
  - **Universal 28 Pin Memory Site, 2-line Control**
- **Low Power Consumption**
  - **100 μA Maximum Standby Current**
- **Noise Immunity Features**
  - **±10% V_{CC} Tolerance**
  - **Maximum Latch-up Immunity Through EPI Processing**
- **High Performance Speeds**
  - **150 ns Maximum Access Time**
- **New Quick-Pulse Programming™ Algorithm (1 second programming)**
  - **Use with Plastic DIP and PLCC EPROMs**
- **Available in 28-Pin Cerdip and Plastic DIP Package and 32-Lead PLCC Package.**

(See Packaging Spec, Order #231369)

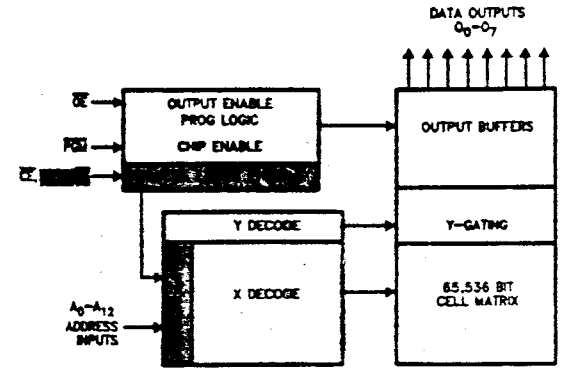
Intel's 27C64 and 87C64 CHMOS EPROMs are 64K bit 5V only memories organized as 8192 words of 8 bits. They employ advanced CHMOS*II-E circuitry for systems requiring low power, high performance speeds, and immunity to noise. The 87C64 has been optimized for multiplexed bus microcontroller and microprocessor compatibility while the 27C64 has a non-multiplexed addressing interface and is plug compatible with the standard Intel 2764A (HMOS II-E).

The 27C64 and 87C64 are offered in both a ceramic DIP, Plastic DIP, and Plastic Leaded Chip Carrier (PLCC) Packages. Cerdic packages provide flexibility in prototyping and R&D environments, whereas Plastic DIP and PLCC EPROMs provide optimum cost effectiveness in production environments. A new Quick-Pulse Programming™ Algorithm is employed on Plastic DIP and PLCC devices which may speed up programming by as much as one hundred times. In the absence of Quick-Pulse compatible programming equipment and with Cerdip devices, the Intelligent Programming Algorithm may be utilized.

The 87C64 incorporates an address latch on the address pins to minimize chip count in multiplexed bus systems. Designers can eliminate the address latch by tieing address and data pins of the 87C64 directly to the processor's multiplexed address/data pins. On the falling edge of the ALE input (ALE/$\overline{CE}$), address information at the address inputs (A_0–A_{12}) of the 87C64 is latched internally. The address inputs are then ignored as data information is passed on the same bus.

The highest degree of protection against latch-up is achieved through Intel's unique EPI processing. Prevention of latch-up is provided for stresses up to 100 mA on address and data pins from −1V to V_{CC} + 1V.

*HMOS and CHMOS are patented processes of Intel Corporation.



Shaded Areas represent the 87C64 version

290000-1

Figure 1. Block Diagram

VIKRAMASINGHA COLLEGE OF TECHNOLOGY
ACC. NO. 2914
LIBRARY

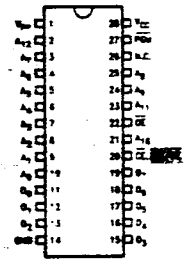
June 1986
Order Number: 290000-005

Pin Names	
A_0–A_{12}	ADDRESSES
O_0–O_7	OUTPUTS
$\overline{OE}$	OUTPUT ENABLE
$\overline{CE}$	CHIP ENABLE
ALE/$\overline{OE}$	ADDRESS LATCH ENABLE /CHIP ENABLE
$\overline{PGM}$	PROGRAM STROBE
N.C.	NO CONNECT
D.U.	DON'T USE

27C64/87C64
P27C64

27256	27128	2732A	2716
V_{PP}	V_{PP}		
A_{12}	A_{12}		
A_7	A_7	A_7	A_7
A_6	A_6	A_6	A_6
A_5	A_5	A_5	A_5
A_4	A_4	A_4	A_4
A_3	A_3	A_3	A_3
A_2	A_2	A_2	A_2
A_1	A_1	A_1	A_1
A_0	A_0	A_0	A_0
O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2
Gnd	Gnd	Gnd	Gnd

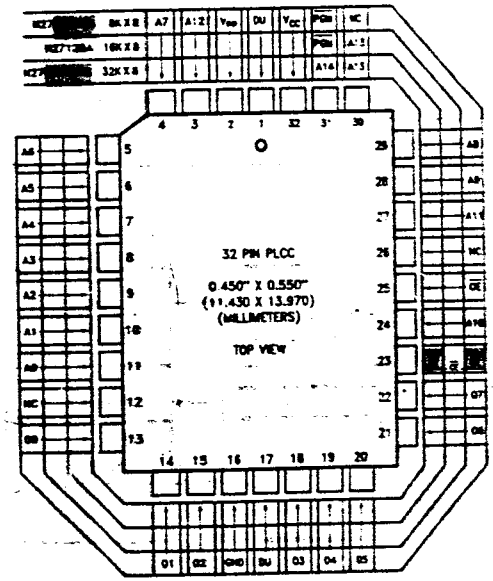
2716	2732A	27128	27256
V_{CC}	V_{CC}	V_{CC}/$\overline{PGM}$	V_{CC}
A_8	A_8	A_{13}	A_{14}
A_9	A_9	A_8	A_8
V_{PP}	A_{11}	A_9	A_9
$\overline{OE}$	$\overline{OE}$/V_{PP}	A_{11}	A_{11}
A_{10}	A_{10}	$\overline{OE}$	$\overline{OE}$
$\overline{CE}$	$\overline{CE}$	A_{10}	A_{10}
O_7	O_7	$\overline{CE}$	$\overline{CE}$
O_6	O_6	O_7	O_7
O_5	O_5	O_6	O_6
O_4	O_4	O_5	O_5
O_3	O_3	O_4	O_4
		O_3	O_3



290000-2

NOTE:
Intel "Universal Site" Compatible EPROM Pin Configurations are shown in the adjacent blocks to 27C64 Pins.
Shaded Areas [illegible] represent the 87C64 version

Figure 2. Pin Configuration



290000-11

Figure 3. PLCC(N) Lead Configuration

Extended Temperature (Express) EPROMs

The Intel EXPRESS EPROM family is a series of electrically programmable read only memories which have received additional processing to enhance product characteristics. EXPRESS processing is available for several densities of EPROM, allowing the choice of appropriate memory size to match system applications.

EXPRESS EPROM products are available with 168 ±8 hour, 125°C dynamic burn-in using Intel's standard bias configuration. This process exceeds or meets most industry specifications of burn-in. The standard EXPRESS EPROM operating temperature range is 0°C to 70°C. Extended operating temperature range (−40°C to +85°C) EXPRESS products are available. Like all Intel EPROMs, the EXPRESS EPROM family is inspected to 0.1% electrical AQL. This may allow the user to reduce or eliminate incoming inspection testing.

EXPRESS EPROM Product Family

PRODUCT DEFINITIONS

Type	Operating Temperature (°C)	Burn-in 125°C (hr)
C	0 to +70	168 ±8
-	−40 to +85	NONE
-	−40 to +85	168 ±8
I	−40 to +125	NONE

EXPRESS Options

27C64/87C64 Versions

Speed Versions	Packaging Options: Cerdip	PLCC	Plastic DIP
−1	T, L, Q	T	T
−15	T, L, Q	T	T
−2	T, L, Q	T	T
−20	T, L, Q	T	T
−STD	T, L, Q, A	T	T
−25	T, L, Q, A	T	T
−3	T, L, Q, A	T	T
−30	T, L, Q, A	T	T

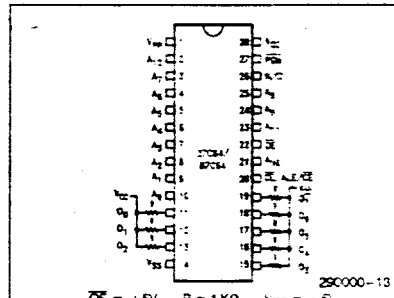
READ OPERATION

D.C. CHARACTERISTICS

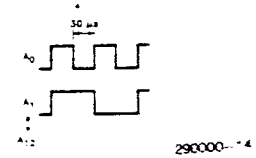
Electrical Parameters of EXPRESS EPROM products are identical to standard EPROM parameters except for

Symbol	Parameter		27C64 87C64 Min	27C64 87C64 Max	Test Conditions
I_{SB}	V_{CC} Standby Current (mA)	CMOS		0.1	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$
		TTL		1.0	
I_{CC1}(1)	V_{CC} Active Current (mA)	TTL		20, 30	$\overline{OE} = \overline{CE} = V_{IL}$
	V_{CC} Active Current at High Temperature	TTL		20, 30	$\overline{OE} = \overline{CE} = V_{IL}$ $V_{PP} = V_{CC}$, $T_{ambient} = 85°C$

NOTE:
1. See notes 4 and 6 of Read Operation D.C. Characteristics.



290000-13



290000-14

Binary Sequence from A_0 to A_{12}

Burn-In Bias and Timing Diagrams

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature
During Read ..... 0°C to +70°C(2)
Temperature Under Bias ..... −10°C to +80°C
Storage Temperature ..... −65°C to +150°C
Voltage on Any Pin with
Respect to Ground ..... −2.0V to 7V(1)
Voltage on Pin A_9 with
Respect to Ground ..... −2.0V to +13.5V(1)
V_{PP} Supply Voltage with Respect to Ground
During Programming ..... −2.0V to +14V(1)
V_{CC} Supply Voltage with
Respect to Ground ..... −2.0V to +7.0V(1)

*NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

READ OPERATION D.C. CHARACTERISTICS $0°C \le T_A \le +70°C$

Symbol	Parameter		Notes	Min	Typ(3)	Max	Unit	Test Condition
I_{LI}	Input Leakage Current				0.01	1.0	µA	$V_{IN} = V_{CC} = 5.5V$
I_{LO}	Output Leakage Current				0.01	1.0	µA	$V_{OUT} = V_{CC} = 5.5V$
I_{PP_1}	V_{PP} Current Read		6			100	µA	$V_{PP} = V_{CC}$
I_{SB}	V_{CC} Current Standby with Inputs—	CMOS	5			100	µA	$\overline{CE} = V_{IH}$
		TTL	4			1.0	mA	
I_{CC_1}	V_{CC} Current Active		4, 6			20, 30	mA	$\overline{CE} = V_{IL}$, f = 5 MHz, $I_{OUT} = 0$ mA
V_{IL}	Input Low Voltage (±10% Supply) (TTL)			−0.5		0.8	V	$V_{PP} = V_{CC}$
	Input Low Voltage (CMOS)			−0.2		0.2	V	$V_{PP} = V_{CC}$
V_{IH}	Input High Voltage (±10% Supply) (TTL)			2.0		$V_{CC}+0.5$	V	$V_{PP} = V_{CC}$
	Input High Voltage (CMOS)			$V_{CC}-0.2$		$V_{CC}+0.2$	V	$V_{PP} = V_{CC}$
V_{OL}	Output Low Voltage					0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage			3.5			V	$I_{OH} = -2.5$ mA
I_{OS}	Output Short Circuit Current		7	100			mA	
V_{PP}	V_{PP} Read Voltage		8	$V_{CC}-0.7$		V_{CC}	V	

NOTES:
1. Minimum D.C. input voltage is −0.5V. During transitions, the inputs may undershoot to −2.0V for periods less than 20 ns. Maximum D.C. voltage on output pins is V_{CC} + 0.5V which may overshoot to V_{CC} + 2V for periods less than 20 ns.
2. Operating temperature is for commercial product defined by this specification. Extended temperature options are available in EXPRESS and Military version.
3. Typical limits are at $V_{CC} = 5V$, $T_A = +25°C$.
4. 20 mA for STD and −3 versions; 30 mA for −2 and 150 ns versions.
V_{IL}, V_{IH} levels at TTL inputs.
5. A19/$\overline{CE}$ or $\overline{CE}$ is V_{CC} ± 0.2V. All other inputs can have any value within spec.
6. Maximum Active power usage is the sum I_{PP} + I_{CC}. The maximum current value is with Outputs O_0 to O_7 unloaded.
7. Output shorted for no more than one second. No more than one output shorted at a time. I_{OS} is sampled but not 100% tested.
8. V_{PP} may be one diode voltage drop below V_{CC}. It may be connected directly to V_{CC}.

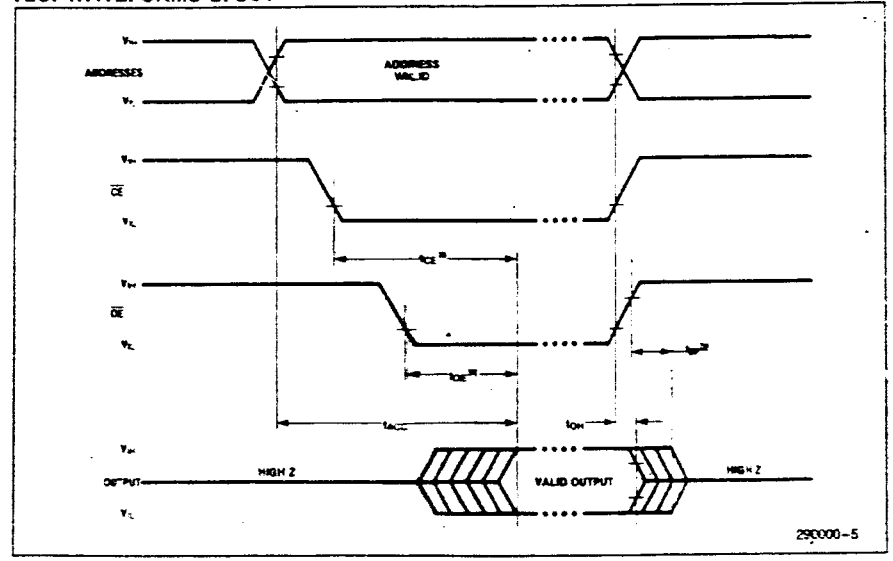
READ OPERATION

A.C. CHARACTERISTICS 27C64(1) $0°C \le T_A \le +70°C$

Versions (3)		$V_{CC} \pm 5\%$	P27C64-1 27C64-1 N27C64-1		P27C64-2 27C64-2 N27C64-2		P27C64 27C64 N27C64		P27C64-3 27C64-3 N27C64-3		Unit
		$V_{CC} \pm 10\%$	27C64-15 N27C64-15 P27C64-15		27C64-20 N27C64-20 P27C64-20		27C64-25 N27C64-25 P27C64-25		27C64-30 N27C64-30 P27C64-30		
Symbol	Characteristic		Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay			150		200		250		300	ns
t_{CE}	$\overline{CE}$ to Output Delay			150		200		250		300	ns
t_{OE}	$\overline{OE}$ to Output Delay			75		75		100		120	ns
t_{DF}(2)	$\overline{OE}$ High to Output High Z			35		55		60		105	ns
t_{OH}(2)	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Change-Whichever is First		0		0		0		0		ns

NOTES:
1. A.C. characteristics tested at $V_{IH} = 2.4V$ and $V_{IL} = 0.45V$.
Timing measurements made at $V_{OL} = 0.8V$ and $V_{OH} = 2.0V$.
2. Guaranteed and sampled.
3. Mode Number Prefixes: No prefix = Cerdip; P = Plastic DIP; N = PLCC.

A.C. WAVEFORMS 27C64



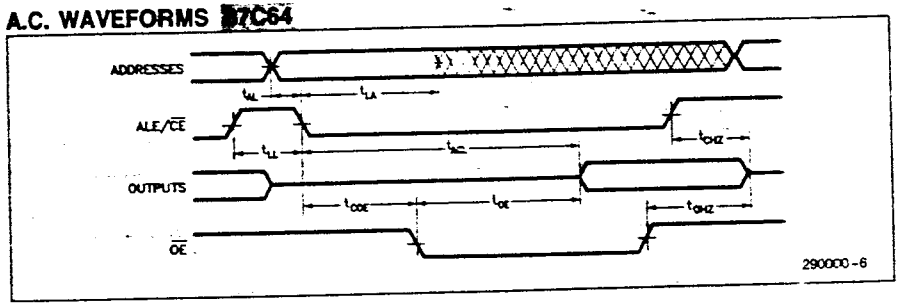
NOTES:
1. Typical values are for $T_A = 25°C$ and nominal supply voltages.
2. This parameter is only sampled and is not 100% tested.
3. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.

A.C. CHARACTERISTICS 87C64(1) [illegible] T_A = 0°C to +70°C

Versions (3)		V_{CC} ±5%	87C64-1 N87C64-1		87C64-2 N87C64-2		87C64 N87C64		87CS4-3 N87C64-3		Unit
		V_{CC} ±10%	87C64-15 N87C64-15		87C64-20 N87C64-20		87C64-25 N87C64-25		87CS4-30 N87C64-3C		
Symbol	Parameter		Min	Max	Min	Max	Min	Max	Min	Max	
t_{LL}	Chip Deselect Width		50		50		60		75		ns
t_{AL}	Address to $\overline{CE}$-Latch Set-up		7		20		25		30		ns
t_{LA}	Address Hold from $\overline{CE}$-LATCH		25		45		50		60		ns
t_{ACL}	CE-Latch Access Time			150		200		250		300	ns
t_{CE}	Output Enable to Output Valid			75		75		100		120	ns
t_{COE}	ALE/$\overline{CE}$ to Output Enable		20		45		50		60		ns
t_{CHZ}(2)	Chip Deselect to Output in High Z			45		50		60		75	ns
t_{OHZ}(2)	Output Disable to Output in High Z			35		50		60		75	ns

NOTES:
1. A.C. characteristics tested at V_{IH} = 2.4V and V_{IL} = 0.45V.
   Timing measurements made at V_{OL} = 0.8V and V_{OH} = 2.0V
2. Guaranteed and sampled.
3. Model Number Prefixes: No prefix = Cerdip; P = Plastic DIP; N = PLCC.

A.C. WAVEFORMS 87C64

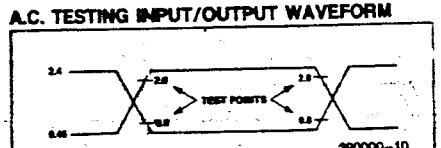


CAPACITANCE(1) T_A = 25°C, f = 1.0 MHz

Symbol	Parameter	Max	Unit	Conditions
C_{IN}	Address/Control Capacitance	6	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	12	pF	V_{OUT} = 0V

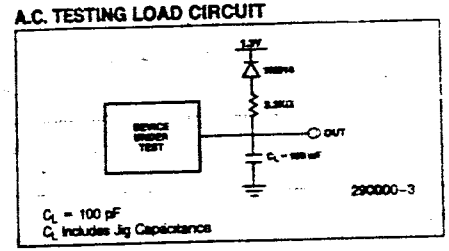
NOTE:
1. Sampled. Not 100% tested.

A.C. TESTING INPUT/OUTPUT WAVEFORM



A.C. Testing: Inputs are driven at 2.4V for a Logic "1" and 0.45V for a Logic "0". Timing measurements are made at 2.0V for a logic "1" and 0.8V for a Logic "0".

A.C. TESTING LOAD CIRCUIT



C_L = 100 pF
C_L includes Jig Capacitance

DEVICE OPERATION

The modes of operation of the 27C64/87C64 are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and 12V on A_9 for intelligent Identifier mode.

Table 1. Mode Selection for 27C64 and 87C64

Pins / Mode	ALE/$\overline{CE}$ $\overline{CE}$	$\overline{OE}$	$\overline{PGM}$ (7)	A_9	A_0	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	V_{IH}	X(1)	X	V_{CC}	5.0V	D_{OUT}
Output Disable	V_{IL}	V_{IH}	V_{IH}	X	X	V_{CC}	5.0V	High Z
Standby	V_{IH}	X	X	X	X	V_{CC}	5.0V	High Z
Programming	V_{IL}	V_{IH}	V_{IL}	X	X	(4)	(4)	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	X	X	(4)	(4)	D_{OUT}
Program Inhibit	V_{IH}	X	X	X	X	(4)	(4)	HIGH Z
intelligent Identifier(3) -Manufacturer	V_{IL}	V_{IL}	V_{IH}	V_H(2)	V_{IL}	V_{CC}	V_{CC}	89 H (6) 88 H (6)
intelligent Identifier(3) -27C64	V_{IL}	V_{IL}	V_{IH}	V_H(2)	V_{IH}	V_{CC}	V_{CC}	07 H
intelligent Identifier(3, 5) -87C64	V_{IL}	V_{IL}	V_{IH}	V_H(2)	V_{IH}	V_{CC}	V_{CC}	37 H

NOTES:
1. X can be V_{IL} or V_{IH}.
2. V_H = 12.0V ± 0.5V.
3. A_1–A_8, A_{10}–A_{12} = V_{IL}.
4. See Table 2 for V_{CC} and V_{PP} voltages.
5. ALE/$\overline{CE}$ has to be toggled in order to latch in the addresses and read the signature codes.
6. The Manufacturer's identifier reads 89H for Cerdip devices; 88H for Plastic DIP and PLCC devices.
7. In Read Mode tie $\overline{PGM}$ to V_{CC}.

Read Mode: 27C64

The 27C64 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output enable ($\overline{OE}$) is the output control and should be used to gate data from the output pins. Assuming that addresses are stable, the address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after a delay of t_{OE} from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

Read Mode: 87C64

The 87C64 was designed to reduce the hardware interface requirements when incorporated in processor systems with multiplexed address-data busses. Chip count (and therefore power and board space) can be minimized when the 87C64 is designed as shown in Figure 4. The processor's multiplexed bus (AD_{0-7}) is tied to both address and data pins of the 87C64. All address inputs of the 87C64 are latched when ALE/$\overline{CE}$ is brought low, thus eliminating the need for a separate address latch.

The 87C64 internal address latch is directly enabled through the use of the ALE/$\overline{CE}$ line. As the transition occurs on the ALE/$\overline{CE}$ from the TTL high to the low state, the last address presented at the address pins is retained. Data is then enabled onto the bus from the EPROM via the $\overline{OE}$ pin.

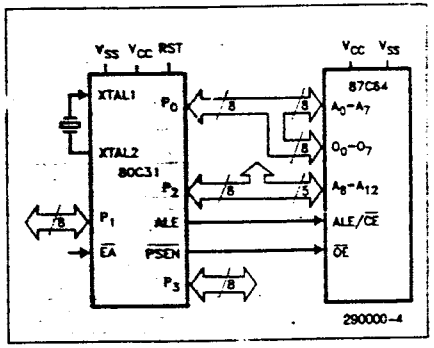


Figure 4. 80C31 with 87C64 System Configuration

Standby Mode

The 27C64 and 87C64 have Standby modes which reduce the maximum V_{CC} current to 100 µA. Both are placed in the Standby mode when $\overline{CE}$ or ALE/$\overline{CE}$ are in the CMOS-high state. When in the Standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, Intel has provided 2 control lines which accommodate this multiple memory connection. The two control lines allow for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To use these two control lines most efficiently, $\overline{CE}$ (or ALE/$\overline{CE}$) should be decoded and used as the primary device selecting function, while $\overline{OE}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are active only when data is desired from a particular memory device.

SYSTEM CONSIDERATIONS

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced by the falling and rising edges of Chip Enable. The magnitude of these transient and inductive current peaks is dependent on the output capacitive and inductive loading of the device. The associated transient voltage peaks can be suppressed by complying with Intel's Two-Line Control, and by properly selected decoupling capacitors. It is recommended that a 0.1 µF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor for low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7 µF bulk electrolytic capacitor should be used between V_{CC} and GND for every eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage droop caused by the inductive effect of PC board-traces.

PROGRAMMING MODES

Caution: Exceeding 14V on V_{PP} will permanently damage the device.

Initially, and after each erasure, all bits of the EPROM are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The device is in the programming mode when V_{PP} is raised to its programming voltage (See Table 2) and $\overline{CE}$ (or ALE/$\overline{CE}$) and $\overline{PGM}$ are both at TTL low and $\overline{OE}$ = V_{IH}. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

Program Inhibit

Programming of multiple EPROMS in parallel with different data is easily accomplished by using the Program Inhibit mode. A high-level $\overline{CE}$ (or ALE/$\overline{CE}$) or $\overline{PGM}$ input inhibits the other devices from being programmed.

of both $\overline{CE}$ or ALE/$\overline{CE}$ and $\overline{OE}$ of the parallel EPROMs may be common. A TTL-level pulse applied to the $\overline{PGM}$ input with V_{PP} at its programming voltage and $\overline{CE}$ (or ALE/$\overline{CE}$) = V_{IL} will program the selected device.

Program Verify

A verify (read) should be performed on the programmed bits to determine that they have been correctly programmed. The verify is performed with $\overline{OE}$ and $\overline{CE}$ (or ALE/$\overline{CE}$) at V_{IL}, $\overline{PGM}$ at V_{IH}, and V_{CC} and V_{PP} at their programming voltages. Data should be verified a minimum of t_{OE} after the falling edge of $\overline{CE}$.

int$_e$ligent Identifier™ Mode

The int$_e$ligent Identifier Mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ±5°C ambient temperature range that is required when programming the device.

To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the EPROM. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during the int$_e$ligent Identifier Mode.

Byte 0 (A0 = V_{IL}) represents the manufacturer code and byte 1 (A0 = V_{IH}) the device identifier code. These two identifier bytes are given in Table 1. ALE/$\overline{CE}$ of the 87C64 has to be toggled in order to latch in the addresses and read the Signature Codes.

INTEL EPROM PROGRAMMING SUPPORT TOOLS

Intel offers a full line of EPROM Programmers providing state-of-the-art programming for Intel programmable devices. The modular architecture of Intel's EPROM programmers allows you to add new support as it becomes available, with very low cost add-ons. For example, even the earliest users of the iUP-FAST 27/K module may take advantage of Intel's new Quick-Pulse Programming Algorithm, the fastest in the industry.

Intel EPROM programmers may be controlled from a host computer using Intel's PROM Programming

a growing list of industry standard hosts including the IBM PC, XT, AT, and PC/DOS compatibles, Intel Development Systems, Intel iPDS Personal Development System, and the Intel Network Development System (NDS-II). Stand-alone operation is also available, including device previewing, editing, programming, and download of programming data from any source over an RS232C port.

For further details consult the EPROM Programming section of the Development Systems Handbook.

ERASURE CHARACTERISTICS (FOR CERDIP EPROMS)

The erasure characteristics are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000-4000Å range. Data shows that constant exposure to room level fluorescent lighting could erase the EPROM in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the device is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15 Wsec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 µW/cm^2 power rating. The EPROM should be placed within 1 inch of the lamp tubes during erasure. The maximum integrated dose an EPROM can be exposed to without damage is 7258 Wsec/cm^2 (1 week @ 12000 µW/cm^2). Exposure of the device to high intensity UV light for longer periods may cause permanent damage.

CHMOS NOISE CHARACTERISTICS

Special EPI processing techniques have enabled Intel to build CHMOS with features adding to system reliability. These include input/output protection to latch-up. Each of the data and address pins will not latch-up with currents up to 100 mA and voltages from −1V to V_{CC} + 1V.

Additionally, the V_{PP} (programming) pin is designed to resist latch-up to the 14V maximum device limit.

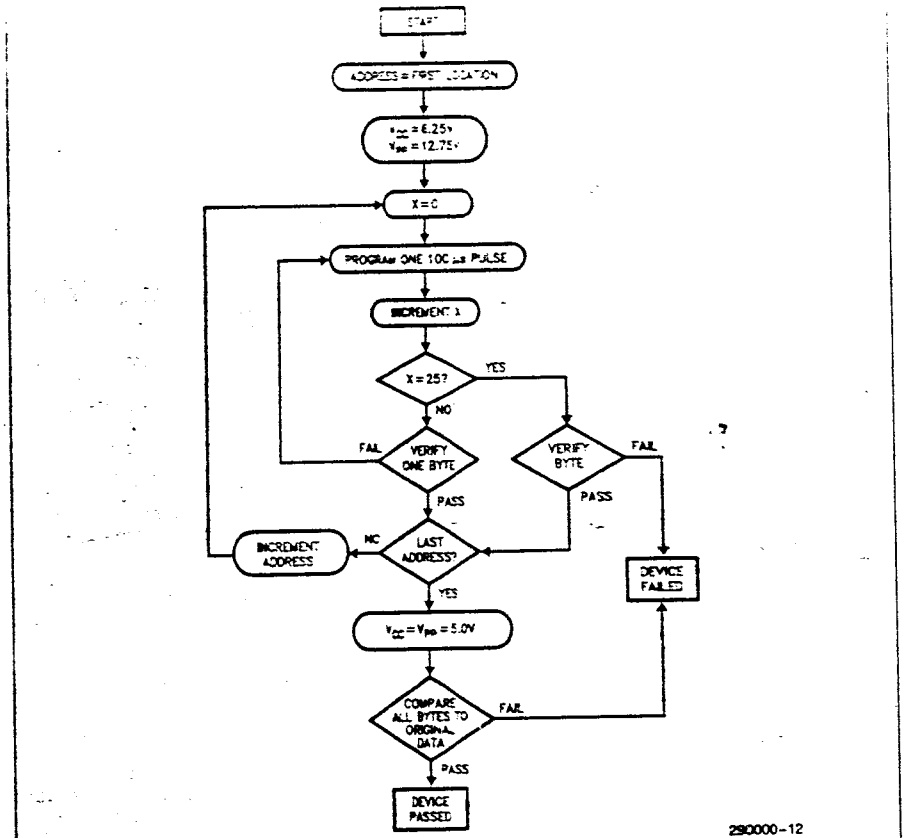


Figure 5. Quick-Pulse Programming™ Algorithm

Quick-Pulse Programming™ Algorithm (for Plastic DIP and PLCC EPROMs)

Intel's Plastic DIP and PLCC EPROMs can now be programmed using the Quick-Pulse Programming Algorithm, developed by Intel to substantially reduce the throughput time in the production environment. This algorithm allows these devices to be programmed in under one second, almost a hundred fold improvement over previous algorithms. Actual programming time is a function of the PROM programmer being used.

The Quick-Pulse Programming Algorithm uses initial pulses of 100 microseconds followed by a byte verification to determine when the address byte has been successfully programmed. Up to 25 100 µs pulses per byte are provided before a failure is recognized. A flowchart of the Quick-Pulse Programming Algorithm is shown in Figure 5.

For the Quick Pulse Programming Algorithm, the entire sequence of programming pulses and byte verifications is performed at V_{CC} = 6.25V and V_{PP} at 12.75V. When programming of the EPROM has been completed, all bytes should be compared to the original data with $V_{CC} = V_{PP} = 5.0V$.

In addition to the Quick-Pulse Programming Algorithm, PLCC EPROMs are also compatible with Intel's int$_e$ligent Programming Algorithm.

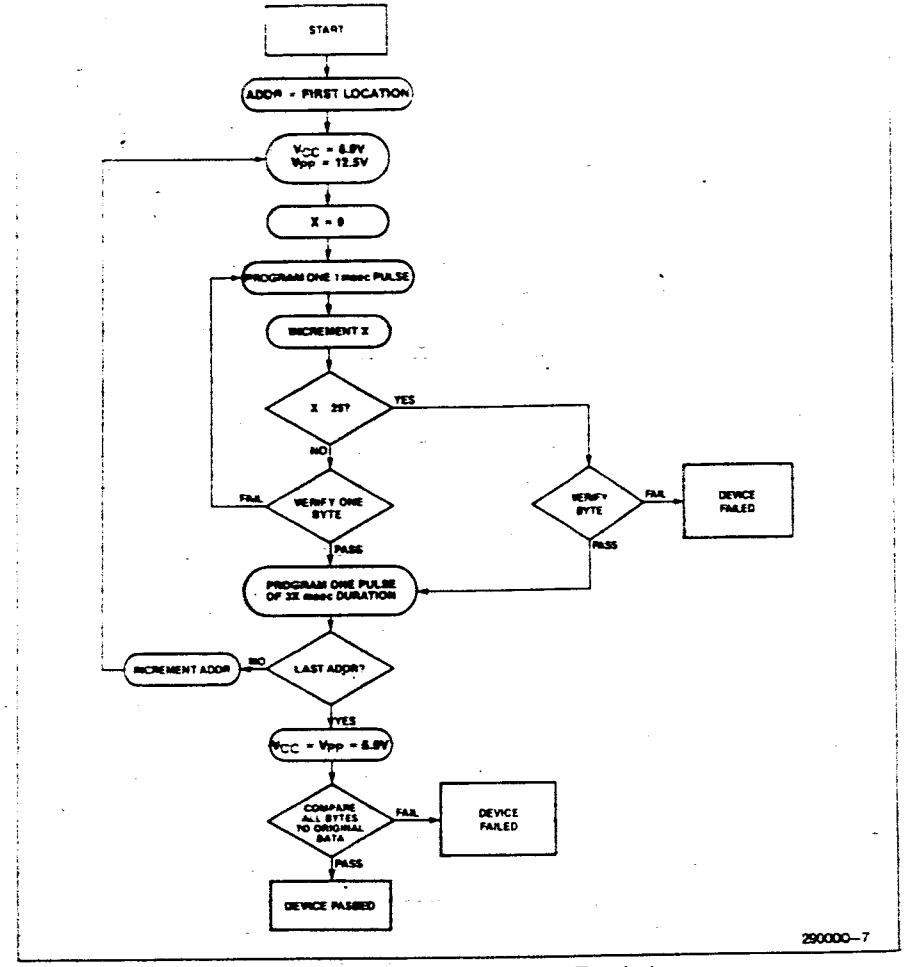


Figure 6. int$_e$ligent Programming™ Flowchart

int$_e$ligent Programming™ Algorithm

The int$_e$ligent Programming Algorithm has been a standard in the industry for the past few years. A flowchart of the int$_e$ligent Programming Algorithm is shown in Figure 6.

The int$_e$ligent Programming Algorithm utilizes two different pulse types: initial and overprogram. The duration of the initial pulse(s) is one millisecond, which will then be followed by a larger overprogram pulse of length 3X msec. X is an iteration counter and is equal to the number of the initial one millisecond pulses applied to a particular location, before a correct verify occurs. Up to 25 one-millisecond pulses per byte are provided for before the overprogram pulse is applied.

The entire sequence of program pulses and byte verifications is performed at V_{CC} = 6.0V and V_{PP} = 12.5V. When the int$_e$ligent Programming cycle has been completed, all bytes should be compared to the original data with $V_{CC} = V_{PP} = 5.0V$.

D.C. PROGRAMMING CHARACTERISTICS (27C64/87C64) T_A = 25° ±5°C

Table 2

Symbol	Parameter	Limits			Test Conditions (Note 1)
		Min	Max	Unit	
I_{LI}	Input Current (All Inputs)		1.0	µA	$V_{IN} = V_{IL}$ or V_{IH}
V_{IL}	Input Low Level (All Inputs)	−0.1	0.8	V	
V_{IH}	Input High Level	2.0	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage During Verify		0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage During Verify	3.5		V	I_{OH} = −2.5 mA
I_{CC2}(4)	V_{CC} Supply Current		30	mA	
I_{PP2}(4)	V_{PP} Supply Current (Program)		30	mA	$\overline{CE}$ = V_{IL}
V_{ID}	A9 Intelligent Identifier Voltage	11.5	12.5	V	
V_{PP}	Intelligent Programming Algorithm	12.0	13.0	V	
	Quick-Pulse Programming Algorithm	12.5	13.0	V	
V_{CC}	Intelligent Programming Algorithm	5.75	6.25	V	
	Quick-Pulse Programming Algorithm	6.0	6.5	V	

A.C. PROGRAMMING CHARACTERISTICS 27C64

T_A = 25°C ±5°C, See Table 2 for V_{CC} and V_{PP} Voltages

Symbol	Parameter	Limits				Conditions (Note 1)
		Min	Typ	Max	Unit	
t_{AS}	Address Setup Time	2			µs	
t_{OES}	$\overline{OE}$ Setup Time	2			µs	
t_{DS}	Data Setup Time	2			µs	
t_{AH}	Address Hold Time	0			µs	
t_{DH}	Data Hold Time	2			µs	
t_{DFP}	$\overline{OE}$ High to Output Float Delay	0		130	ns	(Note 3)
t_{VPS}	V_{PP} Setup Time	2			µs	
t_{VCS}	V_{CC} Setup Time	2			µs	
t_{CES}	$\overline{CE}$ Setup Time	2			µs	
t_{PW}	$\overline{PGM}$ Initial Program Pulse Width	95	100	105	µs	Quick-Pulse
		0.95	1.0	1.05	ms	Intelligent
t_{OPW}	$\overline{PGM}$ Overprogram Pulse Width	2.85		78.75	ms	(Note 2)
t_{OE}	Data Valid from $\overline{OE}$			150	ns	

A.C. CONDITIONS OF TEST

Input Rise and Fall Times (10% to 90%) ..... 20 ns

Input Pulse Levels ..... 0.45V to 2.4V

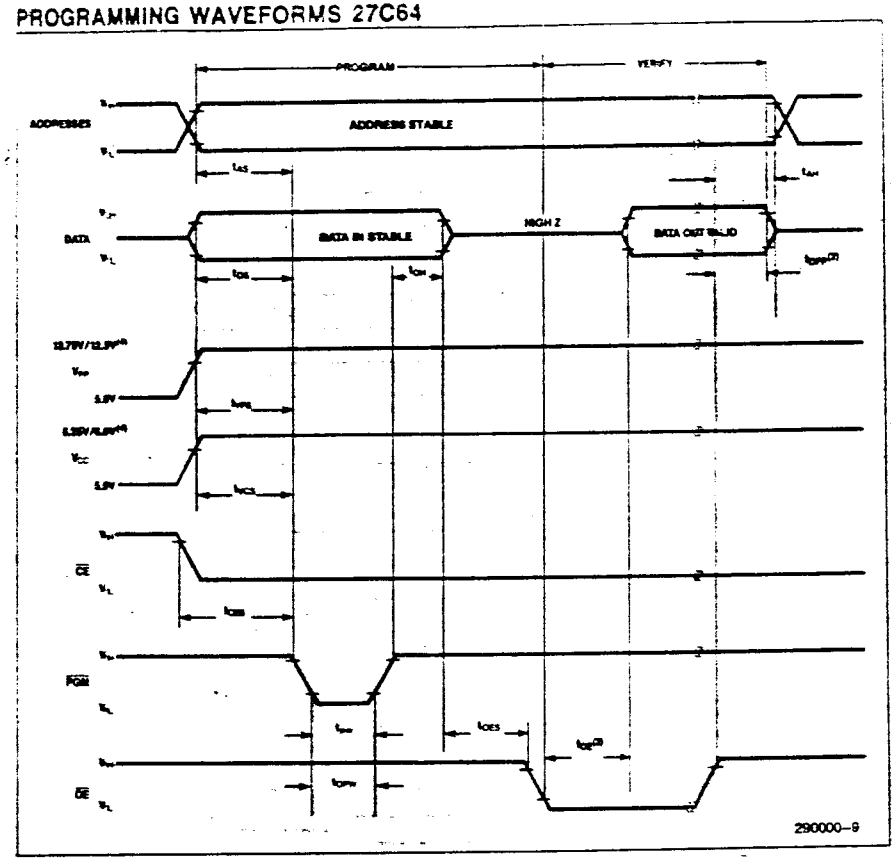
Input Timing Reference Level ..... 0.8V and 2.0V

Output Timing Reference Level ..... 0.8V and 3.5V

NOTES:

1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. The length of the overprogram pulse (Intelligent Programming Algorithm) may vary from 2.85 msec to 78.75 msec as a function of the iteration counter value X.
3. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.
4. The maximum current value is with outputs O_0 to O_7 Unloaded.

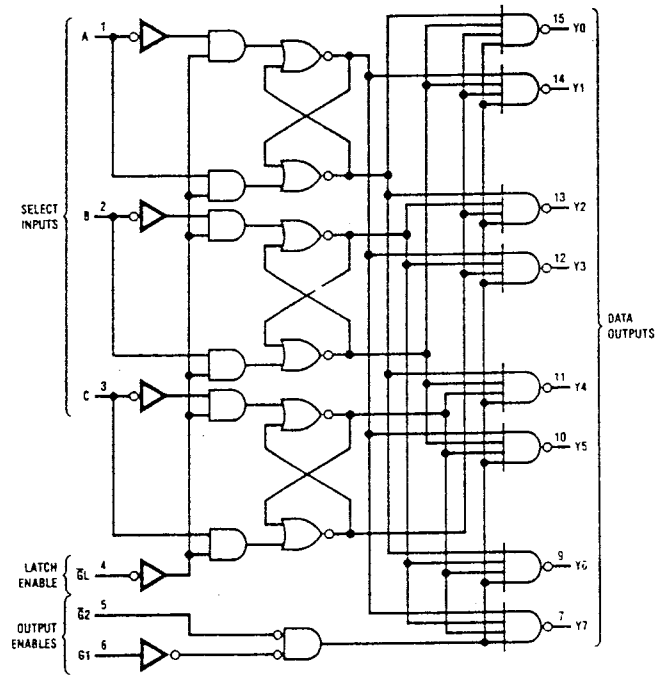
PROGRAMMING WAVEFORMS 27C64



NOTES:

1. The Input Timing Reference Level is 0.8V for V_{IL} and 2V for a V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the 27C64, a 0.1 µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients which can damage the device.
4. 12.75V V_{PP}/6.25V V_{CC} for Quick-Pulse Programming Algorithm; 12.5V V_{PP}/6.0V V_{CC} for Intelligent Programming Algorithm.

Logic Diagram



TL/F/6719-2

National Semiconductor

PRELIMINARY

DM54AS138/DM74AS138 3-to-8 Line Decoder/Demultiplexer

General Description

The DM54/74AS138 circuit is designed to be used in high performance memory decoding or data routing applications requiring very short propagation delay times. In high performance memory systems, this decoder can be used to minimize the effects of system decoding. When employed with high speed memories utilizing a fast enable circuit, the delay times of this decoder and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the Schottky-clamped system decoder is negligible.

The conditions at the binary select inputs and the three enable inputs select one of eight input lines. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

Features

- Designed specifically for high speed memory decoders and data transmission systems
- Incorporates 3 enable inputs to simplify cascading and/or data reception

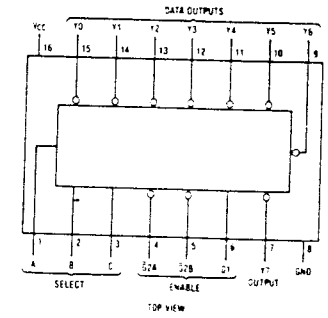
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to + 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagram

Dual-In-Line Package



DM54AS138 (J) DM74AS138 (J, N)

Function Table

Enable Inputs		Select Inputs			Outputs							
G1	$\overline{G2}$*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

*$\overline{G2} = \overline{G2A} + \overline{G2B}$

This document contains information on a product

Recommended Operating Conditions

Symbol	Parameter	DM54AS138			DM74AS138			Unit
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−2			−2	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Operating Free-Air Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free-air temperature range unless otherwise noted

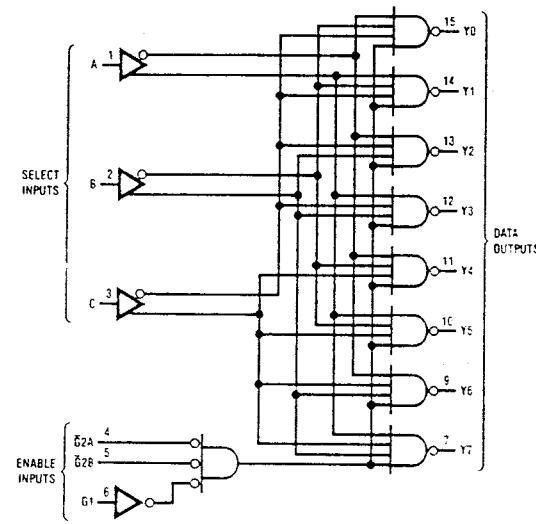
Parameter	Conditions	DM54AS138			DM74AS138			Unit
		Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	
V_{IK}	V_{CC} = 4.5V, I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5V to 5.5V, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	V_{CC} − 2			V_{CC} − 2			V
V_{OL}	V_{CC} = 4.5V, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min		0.35	0.5		0.35	0.5	V
I_I	V_{CC} = 5.5V, V_I = 7V							mA
I_{IH}	V_{CC} = 5.5V, V_I = 2.7V							μA
I_{IL}	V_{CC} = 5.5V, V_{IL} = 0.4V							mA
I_O	V_{CC} = 5.5V, V_O = 2.25V	−30		−112	−30		−112	mA
I_{CCL}	V_{CC} = 5.5V		14	20		14	20	mA
I_{CCH}	V_{CC} = 5.5V		13	19		13	19	mA

Switching Characteristics

Parameter	Input	Output	Conditions	DM54AS138			DM74AS138			Unit
				Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	
t_{PHL}	A, B, C	Y	V_{CC} = 4.5V to 5.5V, C_L = 50 pF, R_L = 500Ω, T_A = Min to Max	2		9	2	5.6	8	ns
t_{PHL}	A, B, C	Y		2		11	2	6.4	9	ns
t_{PLH}	$\overline{G2}$	Y		2		8	2	5.8	7.5	ns
t_{PHL}	$\overline{G2}$	Y		2		9	2	5.5	7.5	ns
t_{PLH}	G1	Y		2	11.5		2		9	ns
t_{PHL}	G1	Y		2	10		2		8.5	ns

Note 1: See Section 1 for test waveforms and output load.

Diagram



National Semiconductor

DM54LS373/DM74LS373, DM54LS374/DM74LS374 TRI-STATE® Octal D-Type Transparent Latches and Edge-Triggered Flip-Flops

General Description

These 8-bit registers feature totem-pole TRI-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the DM54/74LS373 are transparent D-type latches meaning that while the enable (G) is high the Q outputs will follow the data (D) inputs. When the enable is taken low the output will be latched at the level of the data that was set up.

(Continued next page)

Features

- Choice of 8 Latches or 8 D-Type Flip-Flops in a Single Package
- TRI-STATE Bus-Driving Outputs
- Full Parallel-Access for Loading
- Buffered Control Inputs
- Clock/Enable Input Has Hysteresis to Improve Noise Rejection
- P-N-P Inputs Reduce D-C Loading on Data Lines

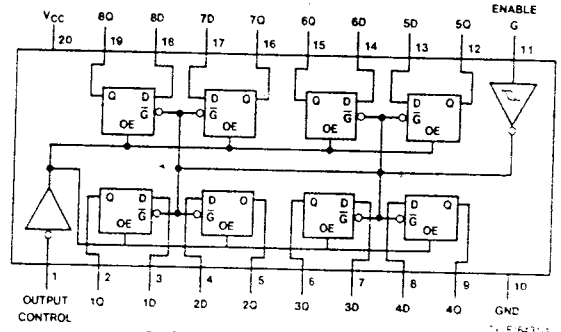
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

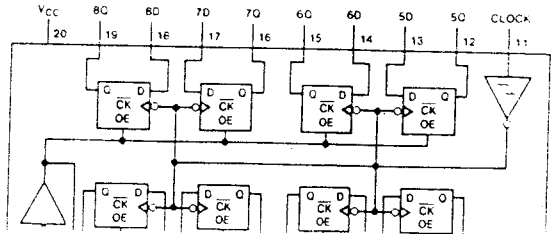
Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection Diagrams

Dual-In-Line Package



54LS373 (J) 74LS373 (N)



General Description (continued)

The eight flip-flops of the DM54/74LS374 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the logic states that were set up at the D inputs.

Schmitt-trigger buffered inputs at the enable/clock lines simplify system design as ac and dc noise rejection is improved by typically 400 mV due to the input hysteresis. A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the latches or flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

Function Tables

DM54/74LS373

Output Control	Enable G	D	Output
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

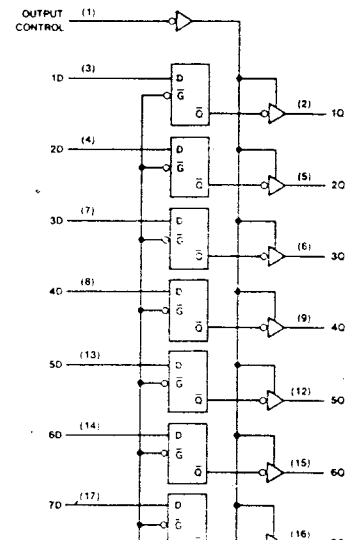
DM54/74LS374

Output Control	Clock	D	Output
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

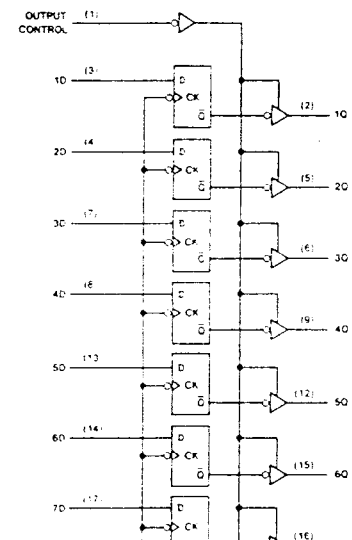
H = High Level (Steady State), L = Low Level (Steady State), X = Don't Care
↑ = Transition from low-to-high level, Z = High Impedance State
Q_0 = The level of the output before steady-state input conditions were established

Logic Diagram

DM54/74LS373
Transparent Latches



DM54/74LS374
Positive-Edge-Triggered Flip-Flops



...ended Operating Conditions

Symbol	Parameter		DM54LS374			DM74LS374		
			Min	Nom	Max	Min	Nom	Max
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25
V_{IH}	High Level Input Voltage		2			2		
V_{IL}	Low Level Input Voltage				0.7			0.8
I_{OH}	High Level Output Current				−1			−2.6
I_{OL}	Low Level Output Current				12			24
f_{CLK}	Clock Frequency (Note 2)		0		35	0		35
f_{CLK}	Clock Frequency (Note 3)		0		20	0		20
t_w	Pulse Width	Clock High	15			15		
		Clock Low	15			15		
t_{su}	Data Setup Time (Note 1)		20↑			20↑		
t_h	Data Hold Time (Note 1)		0↑			0↑		
T_A	Free Air Operating Temperature		−55		125	0		70

Note 1: The symbol (↑) indicates the rising edge of the clock pulse is used for reference.
Note 2: $C_L = 45$ pF and $R_L = 667\Omega$.
Note 3: $C_L = 150$ pF and $R_L = 667\Omega$.

'LS374 Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.4	3.4		V
			DM74	2.4	3.1		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 12 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.7V, V_{IH} = Min, V_{IL} = Max				20	μA

...74 Electrical Characteristics (Continued)

...commended operating free air temperature (unless otherwise noted)

Parameter	Conditions		Min	Typ (Note 1)	Max	Units
Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V, V_{IH} = Min, V_{IL} = Max				−20	μA
Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
		DM74	−20		−100	
Supply Current	V_{CC} = Max			27	45	mA

...374 Switching Characteristics at V_{CC} = 5V and T_A = 25°C

...Section 1 for Test Waveforms and Output Load)

Parameter	$R_L = 667\Omega$						Units
	C_L = 45 pF			C_L = 150 pF			
	Min	Typ	Max	Min	Typ	Max	
...Maximum Clock Frequency	35	50		20	40		MHz
... Propagation Delay Time ...to High Level Output		15	28		21	32	ns
... Propagation Delay Time ...to Low Level Output		19	26		25	38	ns
... Output Enable Time ...High Level Output		20	28		29	44	ns
... Output Enable Time ...Low Level Output		21	28		29	44	ns
... Output Disable Time ...om High Level Output ...ote 3)		12	20				ns
... Output Disable Time ...om Low Level Output ...ote 3)		14	25				ns

...ote 1: All typicals are at V_{CC} = 5V, T_A = 25°C.
...ote 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.
...ote 3: C_L = 5 pF.

National Semiconductor

DM54LS154/DM74LS154 4-Line to 16-Line Decoders/Demultiplexers

General Description

Each of these 4-line-to-16-line decoders utilizes TTL circuitry to decode four binary-coded inputs into one of sixteen mutually exclusive outputs when both the strobe inputs, G1 and G2, are low. The demultiplexing function is performed by using the 4 input lines to address the output line, passing data from one of the strobe inputs with the other strobe input low. When either strobe input is high, all outputs are high. These demultiplexers are ideally suited for implementing high-performance memory decoders. All inputs are buffered and input clamping diodes are provided to minimize transmission-line effects and thereby simplify system design.

Features

- Decodes 4 binary-coded inputs into one of 16 mutually exclusive outputs
- Performs the demultiplexing function by distributing data from one input line to any one of 16 outputs
- Input clamping diodes simplify system design
- High fan-out, low-impedance, totem-pole outputs
- Typical propagation delay
  - 3 levels of logic 23 ns
  - Strobe 19 ns
- Typical power dissipation 45 mW

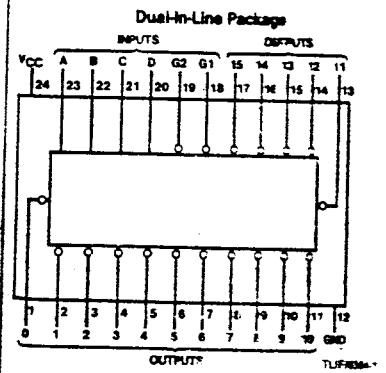
Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to 150°C

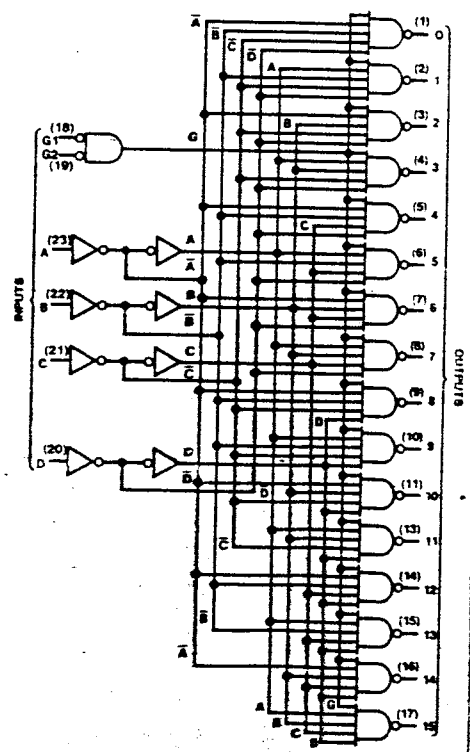
Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Connection and Logic Diagrams

Dual-In-Line Package



54LS154 (J) 74LS154 (N)



Recommended Operating Conditions

Symbol	Parameter	DM54LS154			DM74LS154			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			9	14	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open and all inputs grounded.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	R_L = 2 kΩ						Units
		C_L = 15 pF			C_L = 50 pF			
		Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time Low to High Level Output	Data to Output		18	30		22	35	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Data to Output		18	30		24	35	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Strobe to Output		12	20		15	25	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Strobe to Output		16	25		23	35	ns

Function Table

Inputs					Outputs													
G1	G2	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
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L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
H	X	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = High Level, L = Low Level, X = Don't Care