Telemetry Using Fiber Optic Link

P-1338

Project Work

Submitted by

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In partial fulfilment of the requirements for
the award of the degree of
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CERTIFICATE

This is to certify that the report entitled

"Telemetry using Fiber Optic link"

has been submitted by

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in partial fulfilment of the requirements for the award of degree of Bachelor of Engineering in the Electronics and Communication Engineering branch of the Bharathiar University, Coimbatore - 641 046, during the academic year 1997 - '98.

Guide

Head of the department

certified that the candidate was examined by us in the project work viva- voce examination held on 1.5.1998 *and the university register number is* _____.

Internal Examiner

External Examiner

DEDICATED
TO
OUR FAMILY

WITH LOVE
AND
GRATITUDE

ACKNOWLEDGEMENT

ACKNOWLEDGEMENT

Flowers acknowledge with their fragrance
Birds acknowledge with their flutter
Stars acknowledge with their twinkle
While we acknowledge from our heart.

We are grateful and indebted to our beloved Principal ***Dr. S. Subramanian***, for providing all the necessary facilities in the college to complete our project.

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To ask help is human

While giving help is divine

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SYNOPSIS

SYNOPSIS

Telemetry, is the science of sensing and measuring physical information at some remote location and transmitting the data to a convenient location where it is received and recovered.

The project uses optical fiber as a transmitting medium due to its various inherent advantages. Three parameters namely line voltage, line frequency and temperature have been selected for measurement in our project.

In telemetry, there comes a necessity to measure and record large quantities of data. If this data has to be acquired quickly, and repetitively, automatic data acquisition systems are needed. In our project we have used a microprocessor for data acquisition and storage, as microprocessors are very efficient and easy to use.

Our project finds a wide range of industrial applications because telemetry and automatic data acquisition makes work easier and also saves much time.

INTRODUCTION

INTRODUCTION

1.1 *Need for telemetry*

Measurements, of any kind plays a vital role in any industry. Measurements are of various kinds and the data measured are required by many people for processing. This led to the evolution of telemetry which reduced the time involved in transferring the measured values to the required place and also made these measurements almost real time for may critical applications. Telemetry may be classified into the following types based on

a. Type of modulation

    1. Analog telemetry system
    2. Digital telemetry system

b. Type of transmitting medium used

    1. Radio frequency (RF) or Wireless telemetry system
    2. Fibre optic telemetry system

1.2 *Disadvantages of RF telemetry system*

1. Require transmitting and receiving antenna which consume large space.
2. High noise interference from the surrounding environment
3. Causes electromagnetic interference (EMI) to the near by equipment's
4. Less data security
5. High transmission loss

1.3 *Advantages of fiber optic telemetry*

The many limitations in RF telemetry have been over come using fiber optic telemetry.

The advantages in using fiber optic telemetry are as follows.

1. Enormous potential band width is available
2. Small size and weight
3. Electrical isolation from the surroundings
4. Immunity to interference and cross talk
5. High signal security
6. Low transmission loss
7. Ruggedness and flexibility
8. System reliability and ease of maintenance
9. Potential low cost

Due to various above mentioned advantages optical fiber is chosen as the medium for transmission.

1.4 *General fiber optic communication system*

An optical fiber transmission link comprises of the elements shown in the fig.1.a. The key sections are a transmitter consisting of a light source and its associated drive circuitry, a cable offering mechanical and environmental protection to the optical fiber's contained inside, and a receiver consisting of a photo detector plus amplification and signal restoring circuitry. Additional components include optical connectors, splices, couplers or beam splitters and repeaters.

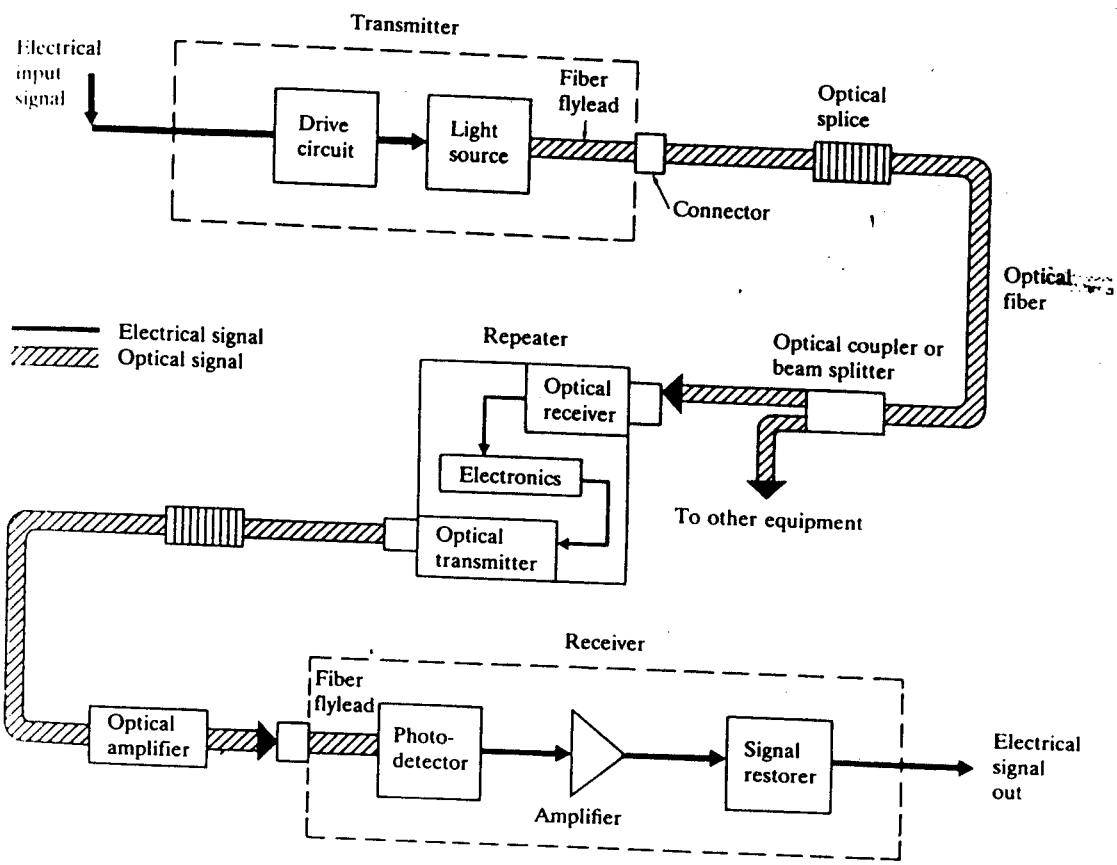


fig.1.a

1.5 *Selection of wavelength* (λ)

One of the important portion of the electromagnetic spectrum encompasses the optical region shown in the fig.1.b which is widely used in optical fibre communication. In this region it is customary to specify the band of interest in terms of wavelength, instead of frequency as in the radio region. The optical spectrum ranges from about 50η m (ultraviolet) to about 100η m (far infrared), the visible spectrum being the 400η m to 700η m band.

One of the principal characteristics of an optical fiber is it a attenuation as a function of wavelength as shown in fig.1.c.

There are three wavelength bands which are used for optical fibre communication and they are namely,

First window	:	Around 850ηm
Second window	:	Around 1300ηm
Third window	:	Around 1550ηm

This project uses the first wavelength band : 850ηm to 900ηm range, as it is very simple and less expensive.

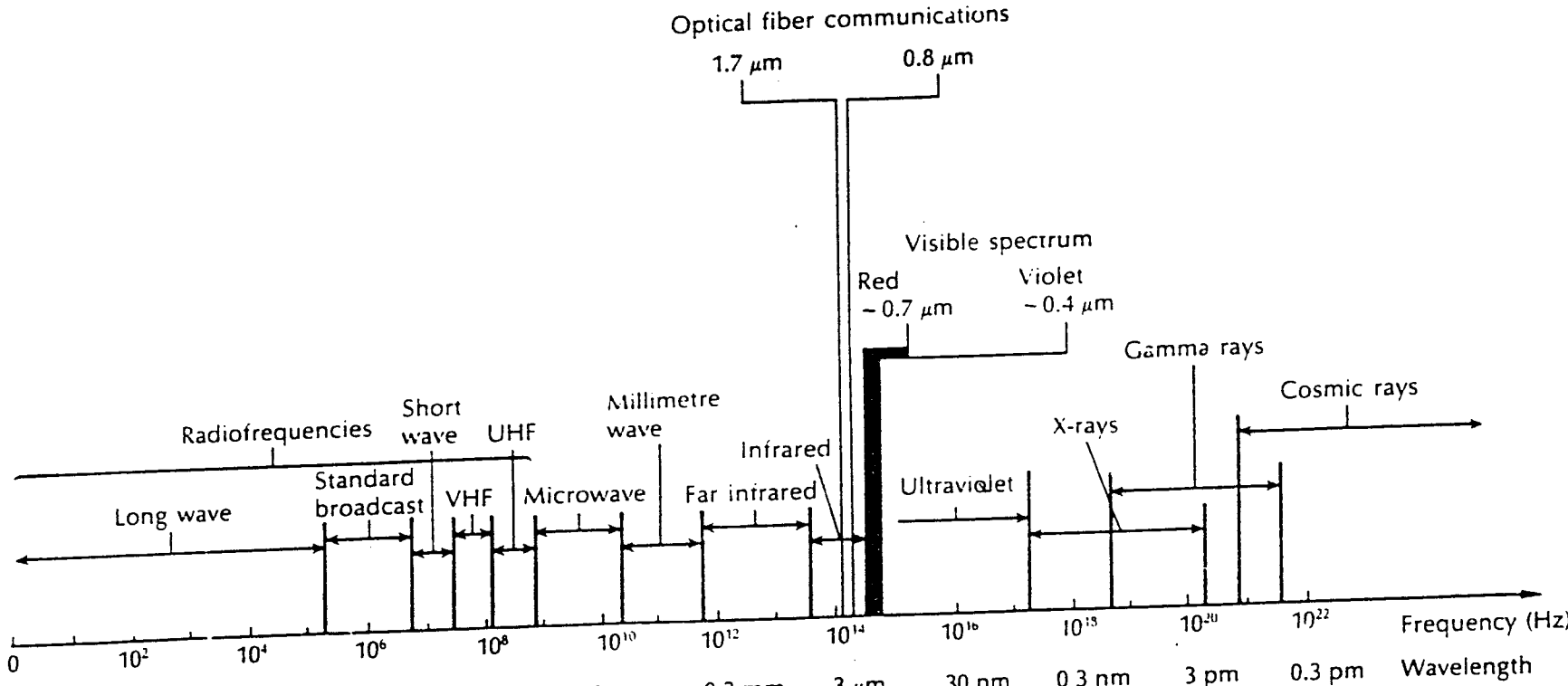

Optical fiber communications
1.7 μm
0.8 μm
Visible spectrum
Red
– 0.7 μm
Violet
– 0.4 μm
Gamma rays
Cosmic rays
X-rays
Ultraviolet
Infrared
Far infrared
Millimetre wave
Short wave
UHF
Radiofrequencies
Standard broadcast
VHF
Microwave
Long wave
0
10²
10⁴
10⁶
10⁸
10¹⁰
10¹²
10¹⁴
10¹⁶
10¹⁸
10²⁰
10²²
Frequency (Hz)
3000 km
30 km
300 m
3 m
3 cm
0.3 mm
3 μm
30 nm
0 3 nm
3 pm
0.3 pm
Wavelength

fig 1.b.

Chapter deals in detail with the various sensors used in the project along with their associated signal conditioning circuits.

The transmitter part is delt in detail in chapter 3 and chapter 4describes completely about the receiver.

The receiver uses a microprocessor and the software along with the flow chart is given in chapter 5.

The scope for further improvement is presented in chapter 7.

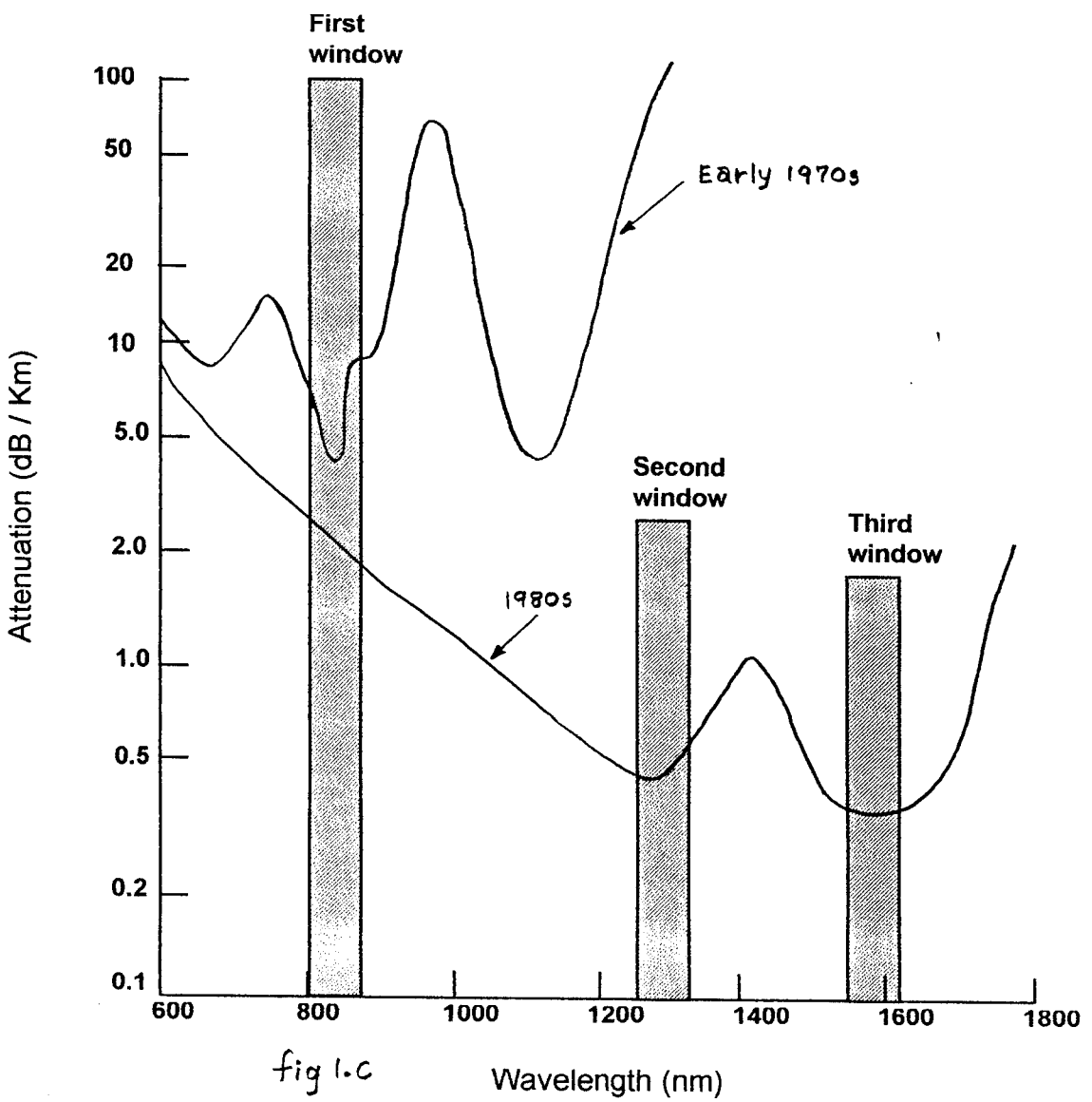


fig 1.c

SENSORS AND SIGNAL CONDITIONING

Sensors and signal conditioning

Sensors or transducers form a vital part in telemetry. Sensors are used to convert the analog parameters measured into equivalent electrical signals. As already mentioned three parameters are sensed in this project namely line voltage, line frequency and temperature. Various types of sensors are available based on the parameters to be measured. The transducers and the methods used may depend upon the instrumentation already available.

2.1 *Selection of sensors*

The factors influencing the choice of a transducer for measurement of a physical quantity are as follows :

Operating principle :

The transducers are many a times selected on he basis of operating principle used by them. The operating principles used may be resistive, inductive, capacitive, opto electronic, piezoelectric etc.

Sensitivity :

The transducers must be sensitive enough to produce detectable output.

Operating range :

The transducer should maintain the range requirements and have a good resolution over its entire range. The rating of the transducer should be sufficient so that it does not breakdown while working in the specified operating range.

Accuracy :

High degree of accuracy is assured if the transducer does not require frequent calibration and has a small value of repeatability. It may be emphasised that in most industrial applications, repeatability is of considerably more importance than obsolute accuracy.

Cross sensitivity :

Cross sensitivity is a further factor to be taken into account when measuring mechanical quantities. There are situations where the actual quantity being measured is in one plane and the transducer is subjected to variations in another plane. More than one promising transducer design had to be abandoned because the sensitivity to variations of the measured quantity in a plane perpendicular to the required plane has been such as to give completely erroneous results when the transducer has been used in practice.

Errors :

The transducer should maintain the expected input - output relationship as described by its transfer function so as to avoid errors.

Transient and frequency response :

The transducer should meet the desired time domain specifications like peak overshoot, rise time, settling time and small dynamic error. It should ideally have a flat frequency response curve. In practice, however, there will be cut off frequencies and higher cut off frequency should be high in order to have a wide bandwidth.

Loading effects :

The transducer should have a high input impedance and a low output impedance to avoid loading effects.

Environmental compatibility :

It should be assured that the transducer selected to work under specified environmental conditions maintains its input - output relationship and does not breakdown.

Insensitivity to unwanted signals :

The transducer should be minimally sensitive to unwanted signals and highly sensitive to desired signals.

Usage and ruggedness :

The ruggedness both of mechanical and electrical intensities of transducer versus its size and weight must be considered while selecting a suitable transducer.

Electrical aspects :

The electrical aspects that need consideration while selecting a transducer include the length and type of cable required.

Attention also must be paid to signal to noise ration in case the transducer is to be used in conjunction with amplifiers. Frequency response limitations must also be taken into account.

Stability and reliability :

The transducer should exhibit a high degree of stability to be operative during its operation and storage life.

Reliability should be assured in case of failure of transducer in order that the functioning of the instrumentation system continues uninterrupted.

Static characteristics :

Apart from low static error, the transducers should have a low non-linearity, low hysteresis, high resolution and a high degree of repeatability.

The transducer selected should be free from load alignment effects and temperature effects. It should not need frequent calibration, should not have any component limitations and should be preferably small in size.

2.2 *Need for signal Conditioning :*

The first stage in parameter measurement is the detector transducer stage as described before. The output of the first stage has to be modified before it becomes usable and satisfactory to drive the further stages. This process of modifying the transduced signal into a usable format for the final stage of measurement is known as signal conditioning.

Measurement of dynamic physical quantities requires faithful representation of their analog or digital output obtained from the intermediate stage i.e. signal conditioning stage and this places a severe strain on the signal conditioning equipment. The signal conditioning equipment may be required to do linear processes like amplifications, attenuation, integration, differentiation, addition and subtraction. They are also required to do non-linear processes like modulation, demodulation, sampling, filtering, clipping and clamping, squaring, linearizing or multiplication by another function etc.

2.3 *Line voltage measurement :*

For any voltage measurement, we need to step down the high line voltage to the required level before feeding to the signal conditioning stage. This voltage control can be done by any of the following methods

1. Voltage control by resistance potential divider

2. Reactance voltage control

3. Voltage control by tapped transformer

4. Voltage control by variac

5. Voltage control by induction regulator

This project uses a simple potential divider which steps down the line voltage to the required level. The circuit diagram for line voltage sensor is as shown in fig.2.a.

The circuit consists of a potential divider using two resistors. The reduced voltage is fed to a peak detector. The circuit is designed to measure line voltages from 200volts to 230 volts. The function of a peak detector is to compute the peak value of the input. The circuit follows the voltage peaks of a signal and stores the highest value on a capacitor. If a higher peak signal value comes along, this new value is stored. The highest peak value is stored until the capacitor is discharged. Whenever the input voltage exceeds the voltage across the capacitor, the diode is forward biased and the circuit

VOLTAGE SENSOR (200 V to 230 V)

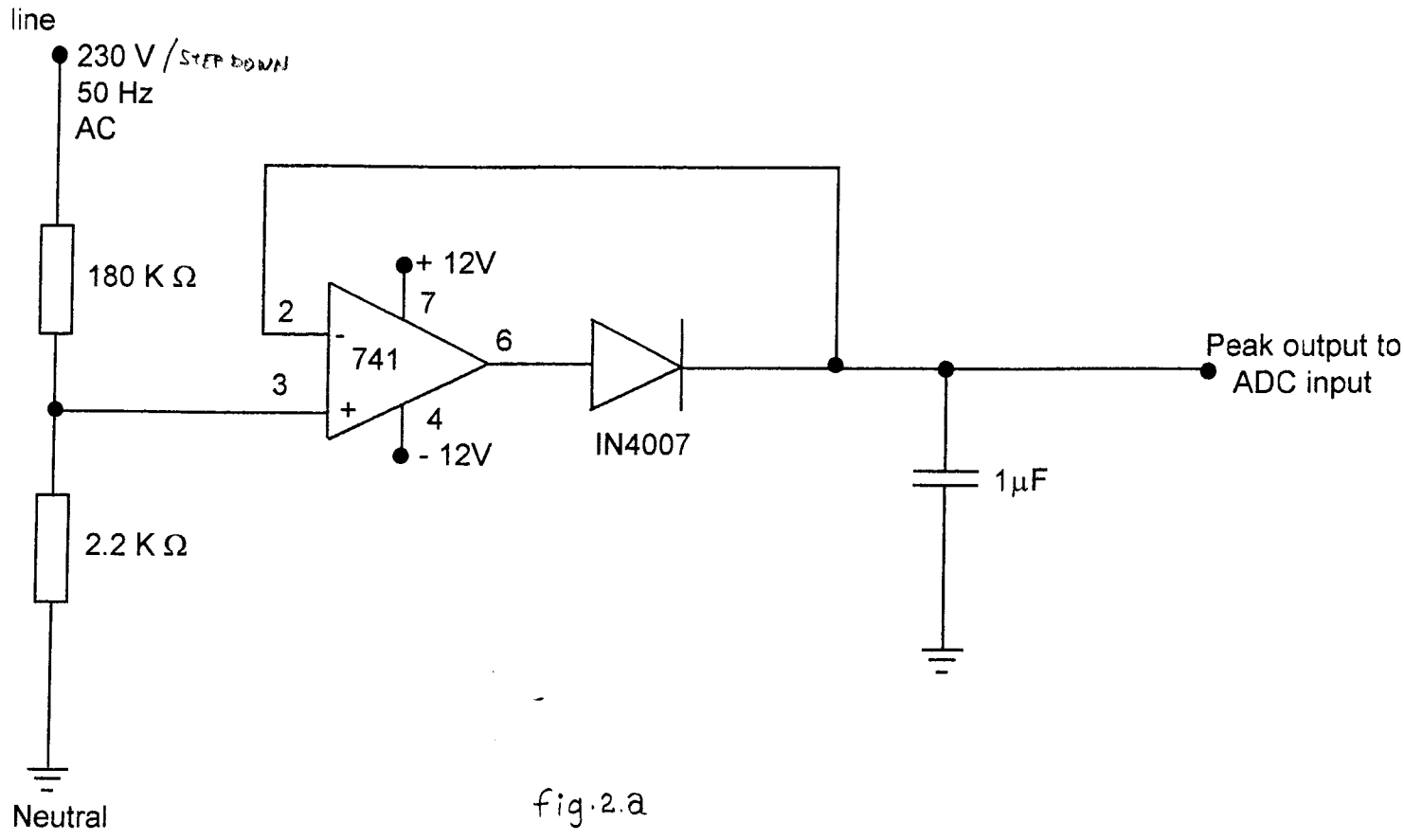


fig.2.a

becomes a voltage follower. The output voltage will follow the input voltage as long as it is higher than the capacitor voltage. When the input voltage is less than the capacitor voltage, the diode is reverse biased and the capacitor retains the same voltage.

Thus the peak value of the line voltage is detected and the output is given to the analog to digital converter (ADC) input.

2.4 *Line frequency measurement :*

The different types of frequency meters are

1. Mechanical resonance type
2. Electrical resonance type
3. Electrodynamometer type
4. Weston type
5. Ratio meter type
6. Saturable core type

The frequency can also be measured and compared by other arrangements like electronic counters, frequency bridges, stroboscopic methods and cathode ray oscilloscope.

The circuit diagram to measure the line frequency is shown in the fig.2.b.The line voltage is brought down to the required level by using a potential divider network using resistors. This is fed to an inverting zero - crossing detector. The line signal is nothing but a sine wave and zero - crossing detector converts this sine wave into a square wave. This square wave is passed through an integrated designed with a proper time constant. The output is a

FREQUENCY SENSOR (40 Hz to 50 Hz)

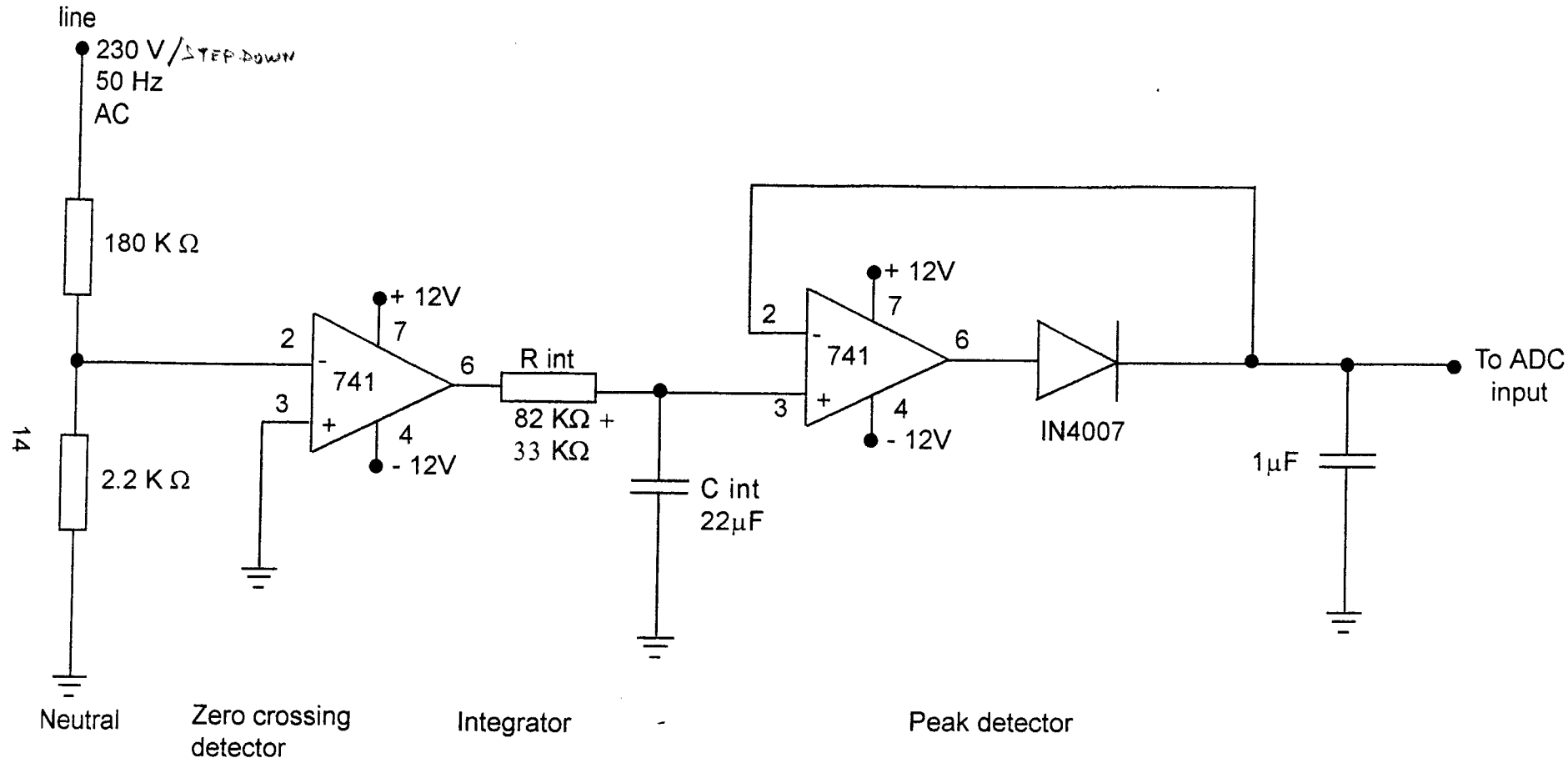


fig.2.b

triangular wave and this is fed to a peak detector, whose peak value is determined. The output of the peak detector is then fed to one of the inputs of the ADC.

2.5 *Temperature measurement :*

The commonly used devices for temperature measurement are

1. Resistance thermometer
2. Semiconductor thermometer
3. Thermistor
4. Thermocouple
5. Bimetallic thermometer
6. Radiation pyrometer

The project uses for semiconductor temperature sensor namely AD590, as shown in fig.2.c. It is a temperature dependent current source, producing a current of 1μA/°K. The current produced is passed through a 1KΩ resistor which produces a voltage and it is applied to an inverting amplifier. This output is again given to another amplifier which gives an output voltage of TTL device compatible levels. The gain of the amplifiers are adjustable and it is adjusted so that the output is +5 Volts for a 40°C temperature. Thus this gain adjustment is helpful in calibration purposes. This output is fed to one of the ADC inputs.

TEMPERATURE SENSOR (UPTO 40°C)

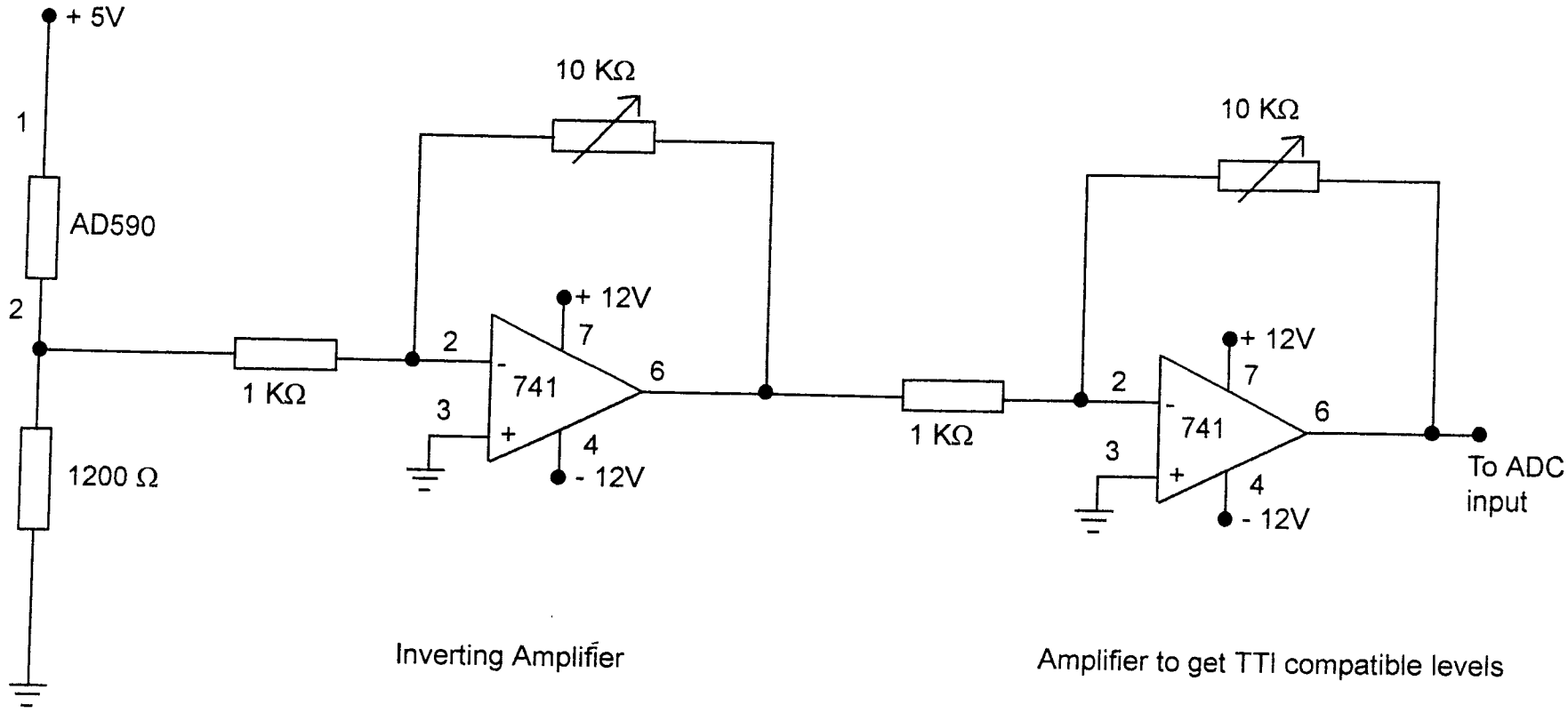


fig.2.c

TRANSMITTER

TRANSMITTER

As already seen in the basic functional block diagram of a fiber optic communication system, the transmitter is one of the most important and basic blocks present. The simplified block diagram of the transmitter used is as shown in fig. 3.a.

3.1 *Simplified block diagram :*

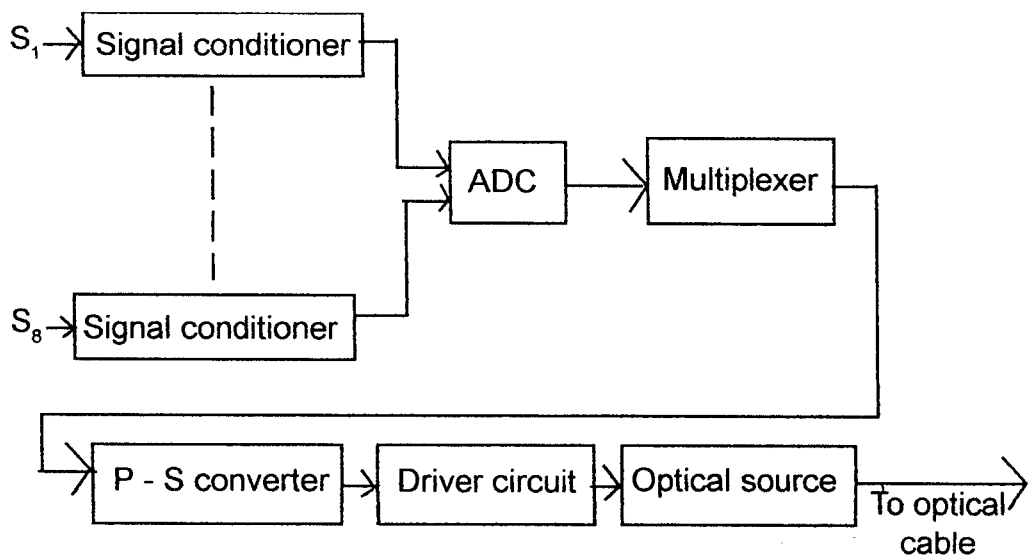


fig.3.a

As the above figure shows, the signal conditioned electrical signal from various sensors is fed to the input of the ADC. The ADC is used to digitize the analog signal obtained from the various sensors. The parallel digital data is converted into a serial data using a multiplexer. The parallel to serial converter is used to send the data bit by bit through the fiber along with start and stop bits. The serial data pulses are fed to the input of a driver circuit which drives the optical source (LED). Thus the signal is transmitted through the optical fiber

3.2 *Selection of light sources*

The properties required of a source for optical communication are

1. It must have a high radiance over a narrow band of wavelengths

2. The output should be easily modulated that it provides a wide signal band width

3. It should be efficient and reliable

4. The output power should be stable

5. Cost should be less

There are two types of semiconductor optical sources : the light emitting diode (LED) and the laser diode. Both operate in forward biased mode.

The radiation from an LED is incoherent and is emitted over a wide range of angles. It covers a broad spectrum of wavelengths, the r.m.s spectral spread varying from around 20ηm at 850ηm to about 80ηm at 1550ηm. The modulation rate is limited to about 100 Mhz.

The behaviour of the laser diode is more complicated. It is constructed so that above a certain threshold current, the light generation mechanism changes. The benefits to set against the increased complexity and cost are that the higher emissive area, and that significantly higher modulation frequencies may be used.

Both LED's and laser diodes consists of p - n junction constructed of direct band gap III - V semiconductor materials. When this junction is forward biased, electrons and holes are injected into the p and n regions respectively. These injected minority carriers can recombine either radiatively in which case a photon of energy $h\upsilon$ is emitted, or non radiatively where upon the recombination energy is dissipated in the form of heat.

In choosing an optical source compatible with the optical wave - guide, various characteristics of the fiber such as its geometry, its attenuation as a function of wavelength, its group delay distortion and its modal characteristics must be taken into account.

Some of the drawbacks of the laser diodes are

1. Their construction is more complicated, mainly because of the require ment of current confinement in a small lasing cavity.

2. The optical output power level is strongly dependent on temperature. This increases the complexity of the transmitter circuitry.

3. They are susceptible to catastrophic facet degradation which greatly reduces the device life time. This is mechanical damage of the facets that may arise after short operating times at high optical power densi ties.

Due to these draw backs LED's are preferred over laser diodes.

An important issue in any application is device reliability. Degradation of light sources can be divided into three basic categories : Internal damage and contact degradation, which hold both for laser diodes and LED's and damage to the facets of laser diodes. Since optical sources are adversely affected by high currents and high temperatures, it is recommended that in order to increase the light source life time, they may be operated at as low a current and temperature as is practical in a system. A LED design as an infrared source is used in the project. The various specifications for the LED used is given in the appendix.

3.3 *Circuit explanation:*

The circuit diagram for the transmitter is as shown in fig.3.b the working principle of the circuit is as follows.

The ADC is an 8 channel device. IC 0809 is used for this purpose. The clock for the circuit is derived from a circuit that uses IC 4049. Clock frequency is around 330 KHz. The sensor circuits are connected to the inputs of the ADC circuit. The channel address for ADC is obtained from a mod - 8 counter (IC 7493).

The digital signal from the ADC is given to an 8 input, single output i.e. 8:1 multiplexer (IC 74151). The channel address for the multiplexer is obtained from a mod - 10 counter (IC 7490). The digital data is serialised by the multiplexer. Along with the original data we add start and stop bits to identify them from the adjacent datas.

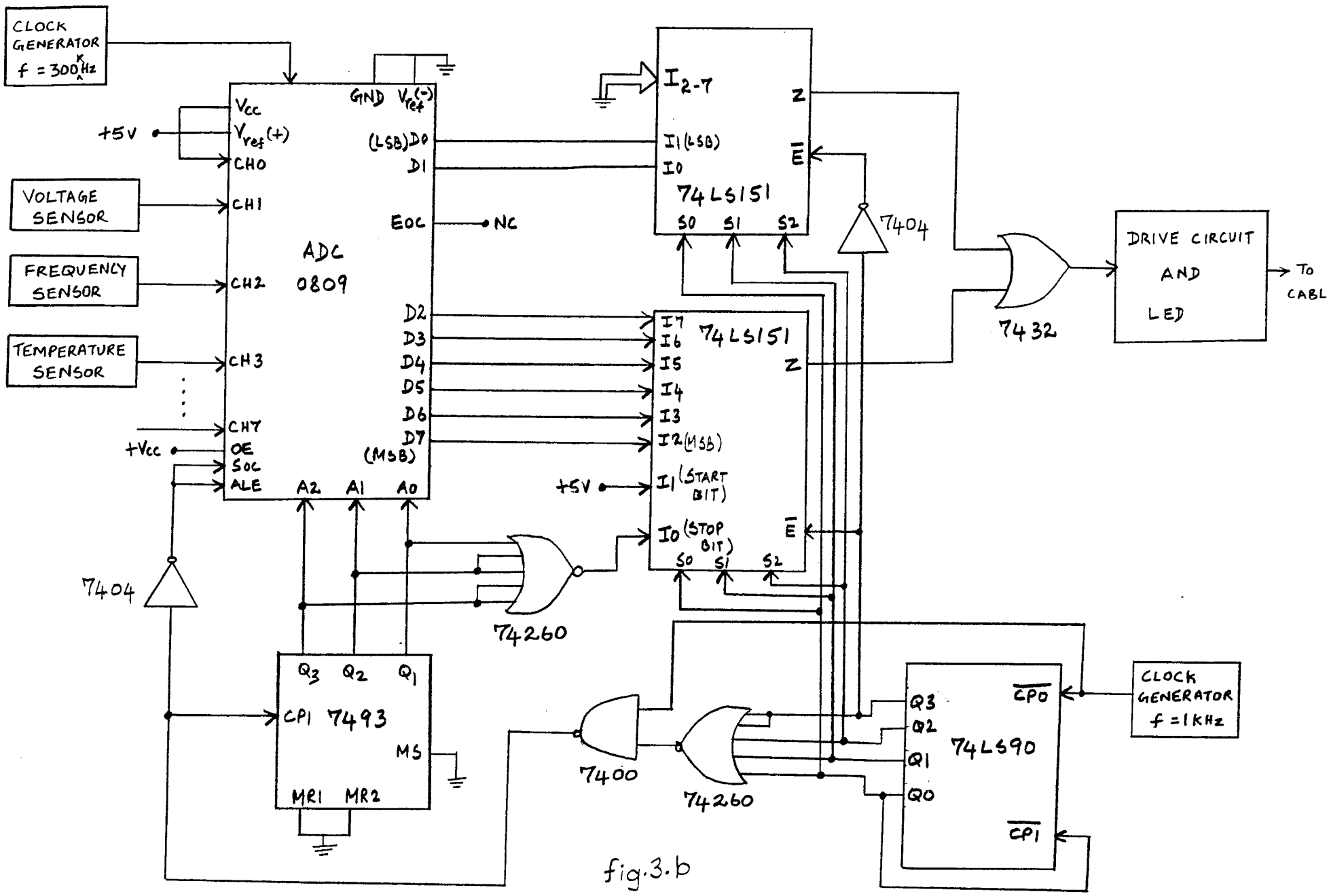

CLOCK GENERATOR
f = 300 KHz
+5V
VOLTAGE SENSOR
FREQUENCY SENSOR
TEMPERATURE SENSOR
+Vcc
Vcc
Vref(+)
CH0
CH1
CH2
CH3
CH7
OE
SOC
ALE
GND
Vref(-)
(LSB) D0
D1
EOC
NC
D2
D3
D4
D5
D6
D7
(MSB)
A2
A1
A0
ADC 0809
I2-7
I1 (LSB)
I0
Z
E
74LS151
S0
S1
S2
7404
7432
DRIVE CIRCUIT AND LED
To CABLE
I7
I6
I5
I4
I3
I2 (MSB)
I1 (START BIT)
I0 (STOP BIT)
74260
Q3
Q2
Q1
CP1
7493
MS
MR1
MR2
7400
CP0
Q0
74LS90
CLOCK GENERATOR
f = 1KHz

fig.3.b

Stop bit is derived from the channel address using NOR gate. Channel address is 000 for reference channel. Reference channel is used to identify the inputs from the sensors properly. When one set of datas are over, it is the responsibility of the reference channel to go back and read all the datas (second set) from the input sensors.

Stop bit is 0 for datas

Stop bit is 1 for reference channel

The start bit is 1 i.e. it is tied to +5v. 10 clock pluses are needed to convert the 10 bit parallel data into serial data using multiplexer for each channel. Only once in every 10 clock pluses from the clock generator (IC 555 in astable mode with frequency around 1 KHz), the channel address for ADC is changed. This is done by using a mod - 10 counter.

The serial data obtained in the form of pulses is passed through a driver circuit using a switching transistor 2N2222. The current levels are properly matched to drive the LED. The output from the driver circuit is given to the light source and the data is transmitted through the fiber.

RECEIVER

Receiver

4.1 *Simplified block diagram :*

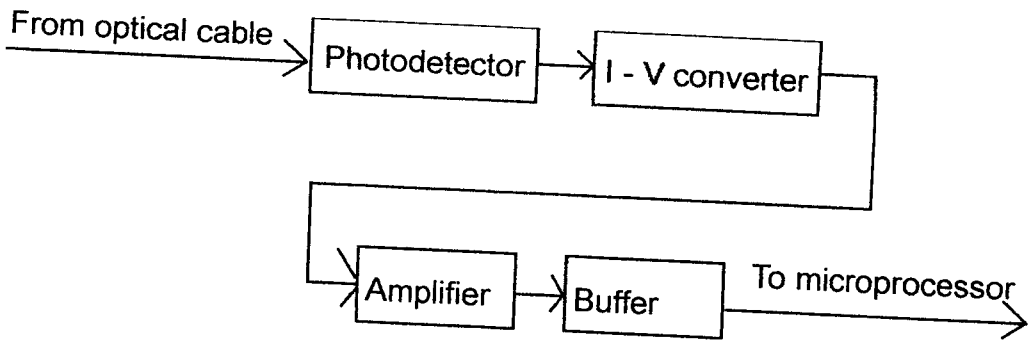


fig.4.a

The simplified block diagram of the receiver in the fig 4.a and it consists of the following important blocks.

1.Photodetector

2.I-V converter

3.Amplifier

4.Buffer

The received signal from the optical fiber is converted to an analog current signal by a photodetector. This current signal is converted into corresponding voltage by using a I-V converter.

The output voltage obtained from the I-V converter is amplified and then fed to a transistor buffer which modifies the received voltage into required TTL levels. This data is then manipulated or stored in a memory device.

4.2 *Selection of photo detectors :*

A photodetector is indispensable in any fiber optic system and it forms the key element in a receiver. A photodetector is used to convert the incident light variations into proportional current variations. Since the optical signal is generally weakened and distorted when it emerges from the end of the fiber ,the photodetector must meet very high performance requirements.

1. It should have a high response or sensitivity in the emission wave length range of the optical source being used.

2. There should be only a minimum addition of noise to the system

3. It should possess a fast response speed or sufficient bandwidth to han dle the desired data rate.

4. It should also be insensitive to variations in temperature.

5. They should be compatible with the physical dimensions of the optical fiber

6. Have a reasonable cost in relation to the other components of the sys tem.

7. Have a long operating life.

Several different types of photodetectors are in existence. Among these are

1. Photo multipliers
2. Pyroelectric detectors
3. Semiconductor-based
    - 3a. photo conductors
    - 3b. photo transistors
    - 3c. photo diodes

However ,many of these detectors do not meet one or more of the foregoing requirements. The photomulipliers are capable of very high gain and very low noise. Unfortunately, their large size and high voltage requirements make them unsuitable for optical fibre systems. Pyroelectric photodetectors involve the conversion of photons to heat. Photon absorption results in a temperature change of the detector material and this in turn results in changes in some temperature dependent parameters like electrical conductivity ,variation in the dielectric constant which is usually measured as a capacitive change. The response of this detector is quite flat over a broad spectral band , but its speed is limited by the detector cooling rate after it has been excited. Its principle use is for detecting high speed laser pulses , and it is not well suited for optical systems.

Of the semiconductor based photodetectors, the photodiode is used almost exclusive for fiber optic systems because of its small size , suitable material , high sensitivity , and fast response time. The two types of photodiodes commonly used are the p-i-n photodetector and the avalanche photodiode (APD). The project uses p-i-n photodiode and the features of p-i-n photodiodes are as follows.

4.3 *p-i-n photodiodes*

In this structure as shown in fig. 4.b., the intrinsic (i) region lies between the two extreme regions of the conductivity types. A sufficiently high reverse voltage applied to the diode produces a strong and almost homogeneous field which expands into the entire i region. Since this medium region can be made rather wide , the p-i-n structure offers the means for the fabrication of very fast detectors. Free carriers generated in the i region through the absorption of photons are rapidly swept off by the electric field towards the junction.

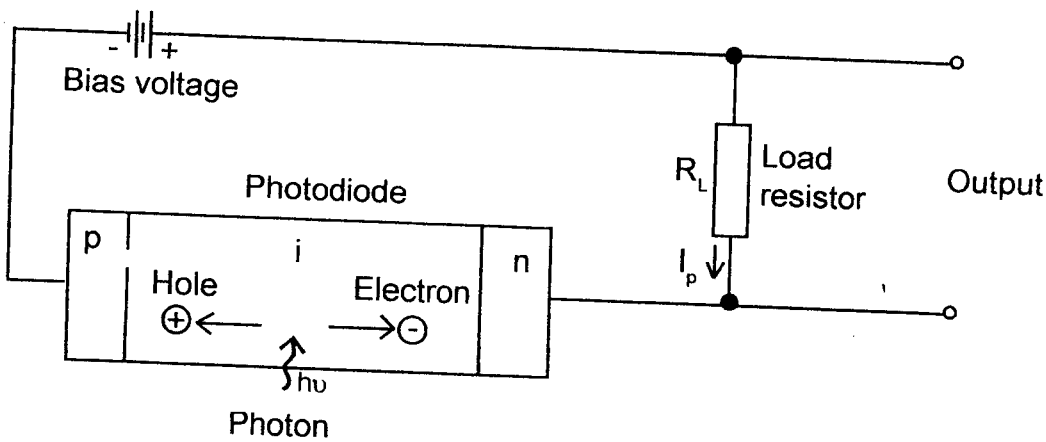


fig.4.b

It has a large width of space charge region and bandwidth covered is around 1GHz.

Advantages :

1. High current responsivity in combination with high speed at a wave length of about 0.9 m.

2. High responsivity in the long - wavelength region by way of increase in width of intrinsic region.

3. Small values of depletion capacitances.

4. Low operating voltages.

4.4 *Circuit explanation :*

The circuit diagram for the receiver is as shown in the fig.4.c. The receiver has three important blocks namely

1. I-V converter

2. Non-inverting amplifier

3. Switching transistor buffer

The p-i-n photodiode gives an output current that is proportional to an incident radiant energy or light. The current through these devices can be converted to voltage by using a I-V converter and thereby the amount of light or radiant energy incident on the photo device can be got.

RECEIVER

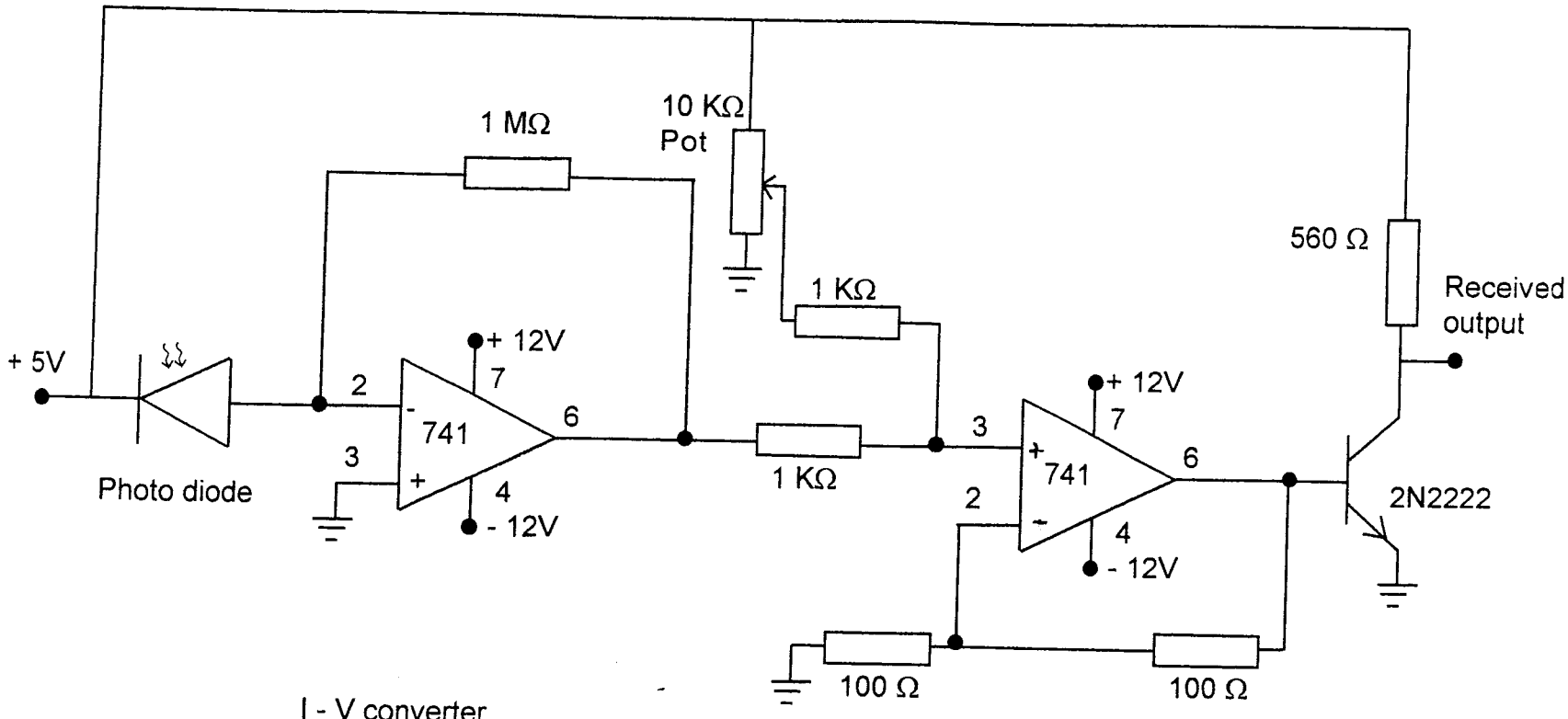
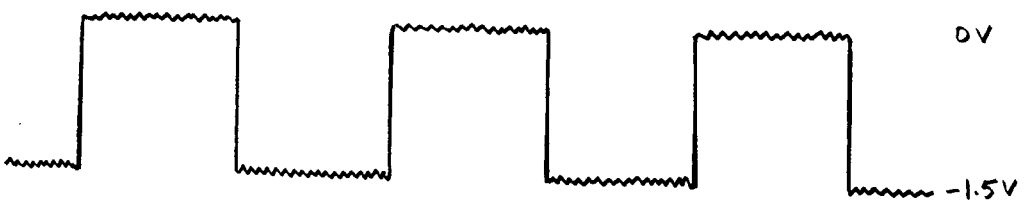


fig.4.c

The current flows through the feedback resistor of resistance 1MΩ. The output voltage V_0 is the product of the current and the feedback resistor of resistance 1MΩ. The resistor may sometimes be shunted with capacitor to reduce high frequency noise and the possibility of oscillations.

The output waveform of I-V converter is



In order to shift the output of the I-V converter above the ground , non-inverting adder circuit is used.

The output of the I-V converter is applied to the non-inverting input terminal and feedback is given. The circuit amplifies without inverting the input signal. It is negative feedback system as output is being fed back to the inverting input terminal. The gain can be adjusted to unity or more by proper selection of resistors.

The voltage after amplification is fed to a switching transistor buffer which is used to get voltage levels compatible to TTL levels.

The project uses 8085 microprocessor to receive the data and display the received data. The detailed description about the 8085 microprocessor is given below.

4.5 *8085 microprocessor :*

The microprocessor is a programmable logic device, designed with registers, flip-flops, and timing elements. The microprocessor has a set of instructions designed internally, to manipulate data and communicate with peripherals.

The microprocessor 8085 primarly performs four operations : memory read, memory write, I/O read and I/O write. For each operation, it generates the appropriate control signal. To communicate with a peripheral, the microprocessor unit identifies the peripheral or the memory location by its address, transfers data and provides timing signals.

The 8085 microprocessor has 16 address lines and 8 data lines. Address bus is a group of lines that are used to send a memory address or device address from the microprocessor unit to the memory location or the peripheral. Data bus is a group of bidirectional lines which are used to transfer data between the microprocessor unit and peripherals. The 8085 microprocessor has also got control bus that carries control signals generated by the microprocessor to provide timing of various operations.

The 8085 microprocessor has got six general purpose 8 bit registers to store data and an accumulator to perform arithmetic and logic operations.

I/O devices or peripherals can be interfaced with the 8085 microprocessor in two ways, peripheral I/O and memory - mapped I/O.

4.6 *Programmable peripheral interface - 8255 processor :*

The 8255 processor is a widely used, programmable, parallel, I/O interface device. It can be programmed to transfer data under various conditions, from simple I/O to interrupt I/O. It is flexible, versatile and economical but some what complex. It is an important general purpose I/O interface device that can be used with almost any microprocessor.

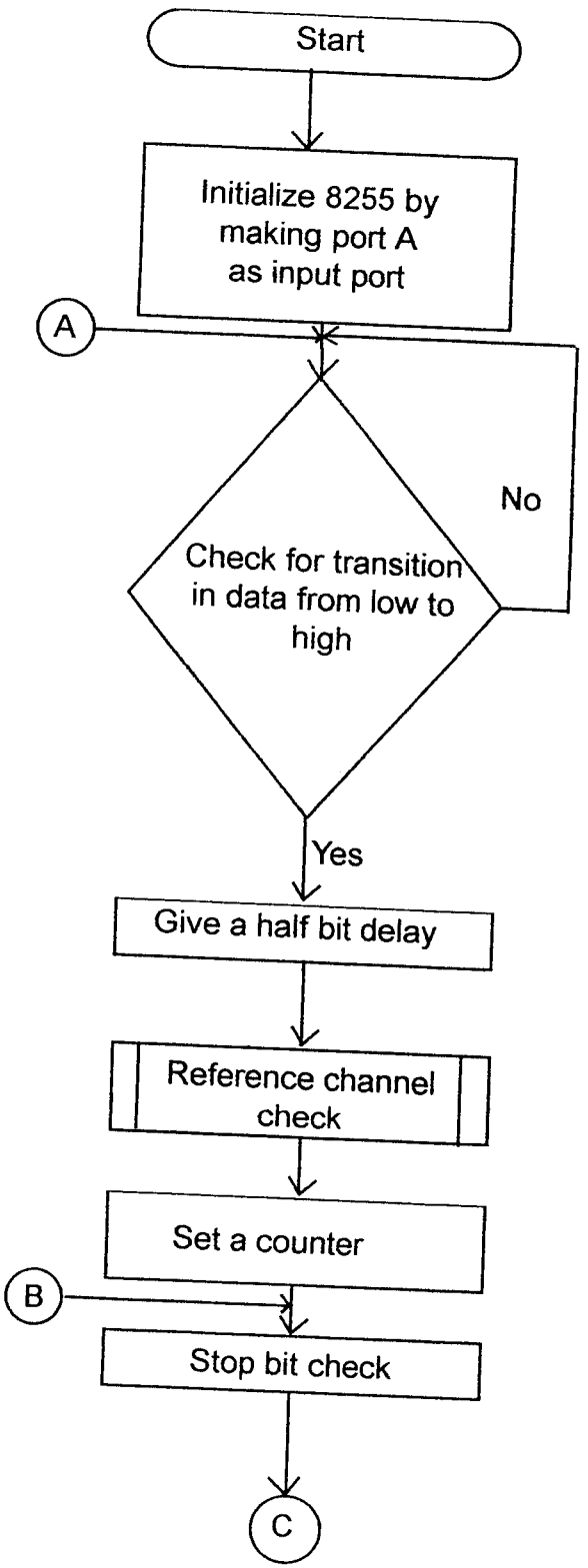
The 8255 has 24 I/O pins that can be grouped primarly in two 8 bit parallel ports : A and B, with the remaining 8 bits as port C.

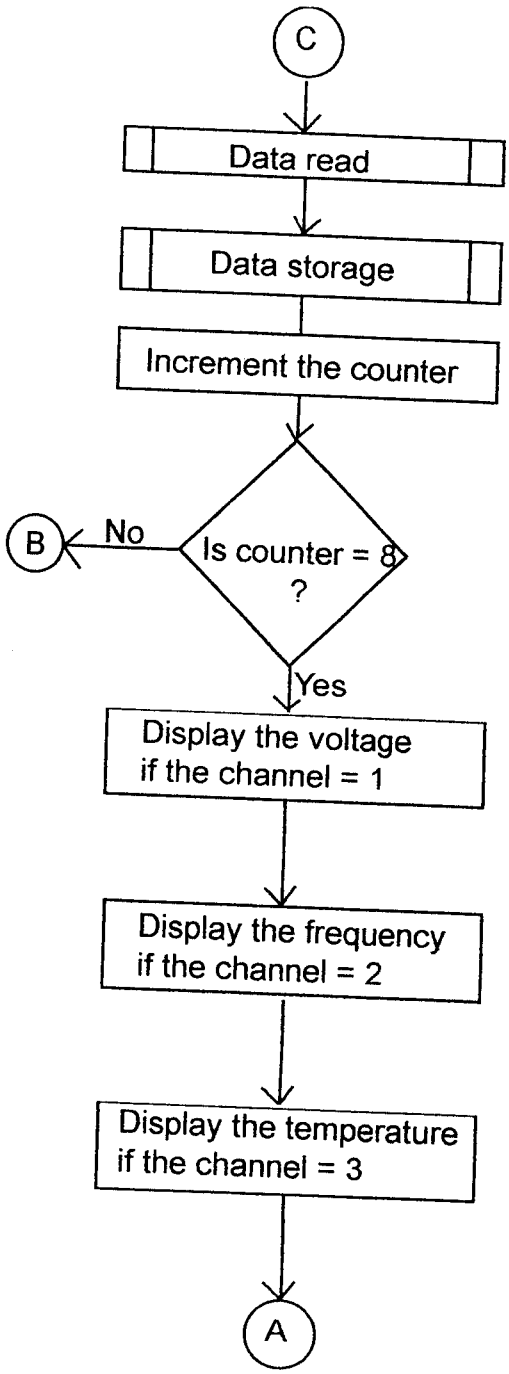
The project uses port A as input port. The received data i.e. the voltage, frequency and temperature will be displayed according to the channel order. The value of the received data will be displayed in the address field and the channel number in the data filed.

SOFTWARE

SOFTWARE

5.1 *Flow chart :*




C
Data read
Data storage
Increment the counter
B
No
Is counter = 8 ?
Yes
Display the voltage if the channel = 1
Display the frequency if the channel = 2
Display the temperature if the channel = 3
A

5.2 *MNEMONICS :*

MAIN

```
                    LXI   SP, 5500H
                    MVI   A, 9BH
                    OUT CR
START       :       LXI H,5000H
LH          :       CALL LHC
                    CALL HBD
                    JMP RCC
SDR         :       MVI D, 01H
RDR         :       CALL LHC
                    JMP SBC
PROCEED     :       CALL DR
                    CALL DS
                    INR D
                    MOV A,D
                    CPI 08H
                    JNZ RDR
                    LXI H, 4150H
                    MOV A, M
                    INR A
                    MOV M, A
                    CPI 01H
                    CZ VD
                    CPI 02H
```

```
                CZ FD
                CALL TD
                LXI H, 4150H
                MVI M, 00H
                JMP START
```

LHC :

```
RPL     :       IN PORTA
                ANI 01H
                CPI 00H
                JNZ RPL
RPH     :       IN PORTA
                ANI 01H
                CPI 01H
                JNZ RPH
                RET

***RCC***  :    MVI C, 0AH
TOP     :       IN PORTA
                ANI 01H
                CPI 01H
                JNZ LH
                DCR C
                JZ SDR
                CALL BD
                JMP TOP
```

```
SBC     :   CALL HBD
            IN PORTA
            ANI 01H
            CPI 01H
            JNZ LH
            JMP PROCEED

DR      :   MVI B, 00H
            MVI C, 08H
BR      :   CALL BD
            IN PORTA
            ANI 01H
            ORA B
            RLC
            MOV B,A
            DCR C
            JNZ BR
            RAR
            MOV B,A
            RET

DS      :   MOV M,D
            INX H
            MOV M,B
            INX H
            RET
```

```
BD      :   MVI E, E2H
            JMP RDD

HBD     :   MVI E,50H
RDD     :   DCR E
            JNZ RDD
            RET

VD      :   LXI H, ADDR1
            CALL DA
            LDA 5001H
            MVI H, 52H
            CALL DU
            LXI H, 5103H
            CALL DD
            CALL DED
            RET

DA      :   MVI C,08H
RD      :   MVI A, 03H
            CALL 0005H
            RET
```

```
DU      :   MOV L,A
            MOV A,M
            MOV B,A
            ANI 0FH
            MOV C,A
            MOV A,B
            ANI F0H
            RRC
            RRC
            RRC
            RRC
            RET

DD      :   MOV M,A
            INX H
            MOV M,C
            DCX H
            DCX H
            MVI C,09H
            JMP RD

DED     :   MVI E, 0AH
RL      :   LXI H, FFFFH
DCR     :   DCX H
```

```
        MOV A,L
        ORA H
        JNZ DCR
        DCR E
        JNZ RL
        RET

FD  :   LXI H, ADDR2
        CALL DA
        LDA 5003H
        MVI H, 53H
        CALL DU
        LXI H, 5109H
        CALL DD
        CALL DED
        RET

TD  :   LXI H, ADDR3
        CALL DA
        LDA 5005H
        MVI H, 54H
        CALL DU
        LXI H, 510FH
        CALL DD
        CALL DED
        RET
```

CONCLUSION

CONCLUSION

This project, as already explained can be used in any industry for the pupose of measurements. The project uses three sensors, for measuring line voltage, line frequency and temperature. All the sensors were successfully tested.

Optical fiber is used as the transmitting medium and it finds a wide usage in modern industries. The project has proved very efficient due to its high channel capacity, less interference and compactness.

The use of microprocessor in the receiver has reduced the complexity in acquring and displaying the data. The microprocessor has improved the userfriendliness and can be operated by any layman in the industry.

Thus, this project is a very useful tool for any industry.

FUTURE DEVELOPMENTS

Future developments

The efficiency of the project can be further enhanced by using a microcontroller along with a serial port in the transmitter. This will further reduce the hardware and the whole system can be controlled by software.

The project can be applied in any particular industry like textiles, chemicals etc. or in hospitals for bio-medical telemetry. In this project only three sensors are used and upto a maximum of seven sensors can be used which will further improve the efficiency.

This project can be developed as a feedback control system for any industrial application.

As said by Neil Armstrong,

"One small step for a man, forms a giant leap for mankind"

this small step taken by us will pave a way for others.

BIBLIOGRAPHY

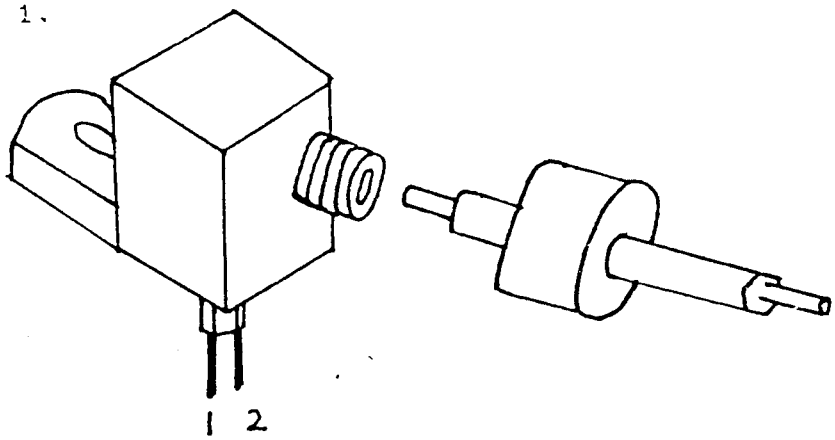
PHOTOGRAPHS

APPENDIX

TECHNICAL SPECIFICATIONS OF LED AND DETECTOR:

MFOE71 Plastic LED

Fig. 1.



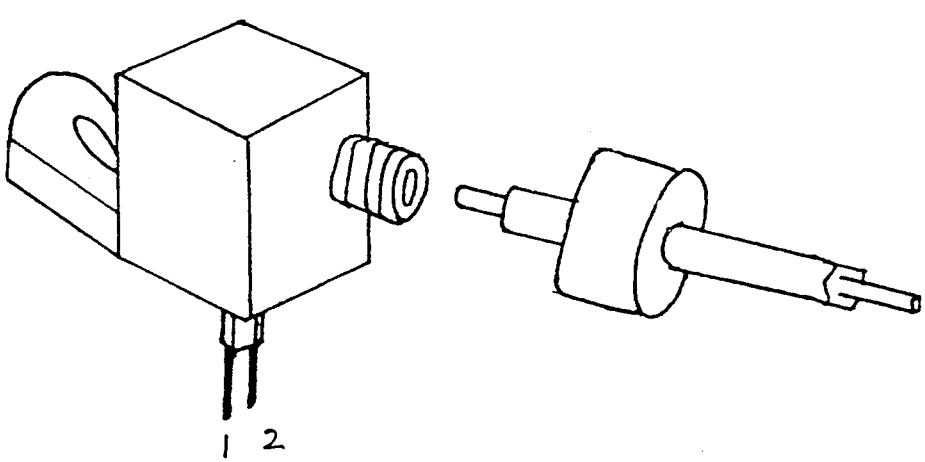
PIN 1 : ANODE

PIN 2 : CATHODE

Power output	=	3.5 mW
Forward current	=	100 mA
T_{on}/T_{off}	=	25 ns
Peak wavelength	=	820 nm

MFOD71 Plastic Detector

Fig. 2.



PIN 1 : CATHODE

PIN 2 : ANODE

Responsivity	=	0.2 μA/μW
Peak wavelength	=	820 nm
T_{on}/T_{off}	=	1.0 ns
VBR	=	100 V

SPECIFICATION SHEET

PLASTIC LED :

FOLK-PLED-01

This LED is designed as infrared source for fiber optic systems. The package houses the LED, has a molded lens which efficiently couples the light to and from the cable, has the fiber alignment with locking mechanism and the means for attaching to a board.

Specifications:

Power output	: 3.5 MW (at I_F = 100 mA)
Rise time & fall time	: 25 ns
Wavelength	: 820 nm
Package	: 2 pin PCB mountable package with fiber alignment & locking mechanism.

SPECIFICATION SHEET

PLASTIC DETECTOR :

FOLK-PDET-01

This detector is a low cost component designed for detection of infrared radiation in fiber optic systems.

Specifications:

Package	: T 046 Metal case with giass window
Responsivity	: 0.2 uA/uW
Peak wavelength	: 820 nm
Rise & Fall time	: 1 ns
VBR	: 100 volts
Package	: 2 pin PC mountable package with fiber alignment & locking mechanism.

SPECIFICATION SHEET

PLASTIC FIBER :

FOLK-PFIBER-01

1.0 mm x 1 fiber

The plastic fiber is super ESKA fiber which is a "total internal reflection type" (step index) fiber made of a core of high-purity polymethyl methacrylote with a thin layer of special transparent fluorine polymer clading. The clading has a lower refractive index than the core, resulting in total internal reflection and transmission of light rays.

The cable is made with black polyethylene jacket with the fiber inside. The cables are particularly suited for short-distance light data transmission cables.

Specifications:

- 1 mm Fiber dia
- 2.2mm Cable outer dia
- 1.2 kg/fiber breaking stress

CD4049UB, CD4050B Types

CMOS
Hex Buffer/Converters

High-Voltage Types (20-Volt Rating)

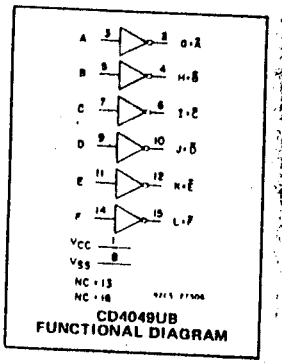
CD4049UB—Inverting Type
CD4050B—Non-Inverting Type

Features:

- High sink current for driving 2 TTL loads
- High-to-low level logic conversion
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- 5-, 10-, and 15-volt parametric ratings

Applications:

- CMOS to DTL/TTL hex converter
- CMOS current "sink" or "source" driver
- CMOS high-to-low logic-level converter

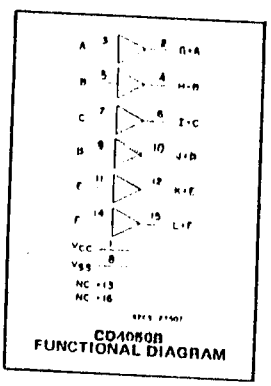


CD4049UB
FUNCTIONAL DIAGRAM

The RCA-CD4049UB and CD4050B are inverting and non-inverting hex buffers, respectively, and feature logic-level conversion using only one supply (voltage (V_{CC}). The input-signal high level (V_{IH}) can exceed the V_{CC} supply voltage when these devices are used for logic-level conversions. These devices are intended for use as CMOS to DTL/TTL converters and can drive directly two DTL/TTL loads. (V_{CC}=5 V, $V_{OL} \leq$ 0.4 V, and $I_{OL} \geq$ 3.3 mA.)

The CD4049UB and CD4050B are designated as replacements for CD4009UB and CD4010B, respectively. Because the CD4049UB and CD4050B require only one power supply, they are preferred over the CD4009UB and CD4010B and should be used in place of the CD4009UB and CD4010B in all inverter, current driver, or logic-level conversion applications. In these applications the CD4049UB and CD4050B are pin compatible with the CD4009UB and CD4010B respectively, and can be substituted for these devices in existing as well as in new designs. Terminal No. 16 is not connected internallyon the CD4049UB or CD4050B, therefore, connection to this terminal is of no consequence to circuit operation. For applications not requiring high sink-current or voltage conversion, the CD4069UB Hex Inverter is recommended.

The CD4049UB and CD4050B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).



CD4050B
FUNCTIONAL DIAGRAM

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{CC})
(Voltages referenced to V_{SS} Terminal) . . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to +20.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D, F, K) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range (V_{CC}) (For T_A=Full Package Temperature Range)	3	18	V
Input Voltage Range (V_{IN})	V_{CC}*	18	V

*The CD4049 and CD4050 have high-to-low level voltage conversion capability but not low-to-high-level; therefore it is recommended that $V_{IN} \geq V_{CC}$.

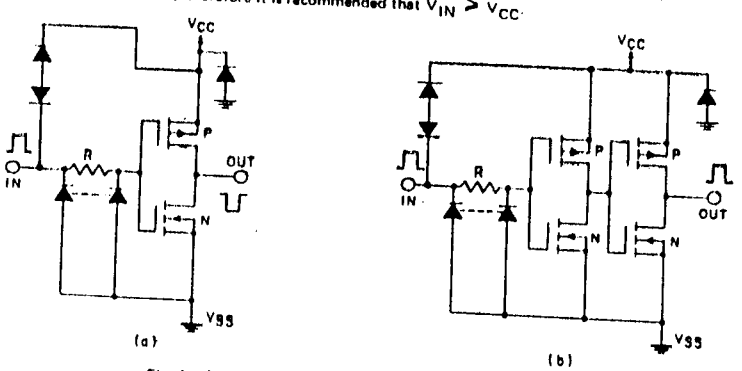


Fig. 1 – a) Schematic diagram of CD4049UB, 1 of 6 identical units; b) Schematic diagram of CD4050B, 1 of 6 identical units.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			Limits At Indicated Temperatures (°C) *Values at -55, +25, +125 Apply to D, F, K, H Pkgs. Values at 40,125,185 Apply to E Package*							UNITS
	V_O (V)	V_{IN} (V)	V_{CC} (V)	-55	-40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	1	1	30	30		0.02	1	μA
	–	0,10	10	2	2	60	60		0.02	2	
	–	0,15	15	4	4	120	120		0.02	4	
	–	0,20	20	20	20	600	600		0.04	20	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	3.3	3.1	2.1	1.8	2.0	4.2	–	mA
	0.4	0,5	5	4	3.8	2.9	2.4	3.2	6.4	–	
	0.5	0,10	10	10	9.6	6.6	5.6	8	16	–	
	1.5	0,15	15	26	26	20	18	24	48	–	
Output High (Source) Current I_{OH} Min.	4.6	0,5	5	-0.61	-0.73	-0.66	-0.48	-0.66	-1.2	–	
	2.5	0,5	5	-2.6	-2.4	-1.9	-1.55	-2.1	-3.9	–	
	9.5	0,10	10	-2.0	-1.8	-1.35	-1.18	-1.65	-3.0		
	13.5	0,15	15	-5.2	-4.8	-3.6	-3.1	-4.3	-8.0	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05					0	0.05	V
	–	0,10	10	0.05					0	0.05	
	–	0,15	15	0.05					0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10		
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage: V_{IL} Max. CD4049UB	4.5	–	5	1						1	V
	9		10	2						2	
	13.5		15	2.5						2.5	
Input Low Voltage: V_{IL} Max. CD4050B	0.5	–	5	1.5						1.5	
	1		10	3						3	
	1.5		15	4						4	
Input High Voltage: V_{IH} Min. CD4049UB	0.5	–	5	4				4	–	–	
	1	–	10	8				8	–	–	
	1.5	–	15	12.5				12.5	–	–	
Input High Voltage: V_{IH} Min. CD4050B	4.5	–	5	3.5				3.5	–	–	
	9	–	10	7				7	–	–	
	13.5	–	15	11				11	–	–	
Input Current, I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$±10^{-5}$	±0.1	μA

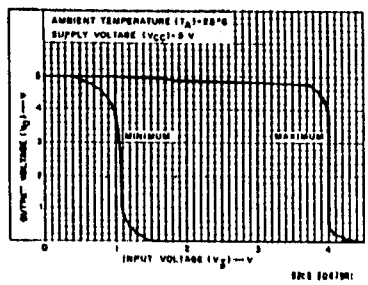


Fig. 2 – Minimum and maximum voltage transfer characteristics for CD4049UB.

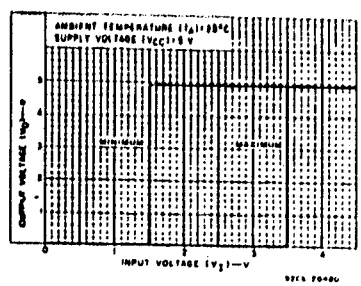


Fig. 3 – Minimum and maximum voltage transfer characteristics for CD4050B.

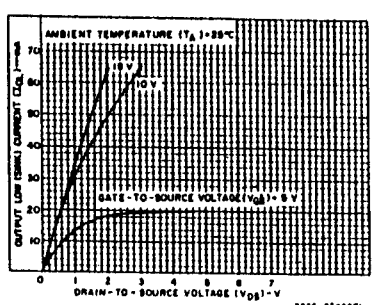


Fig. 4 – Typical output low (sink) current characteristics.

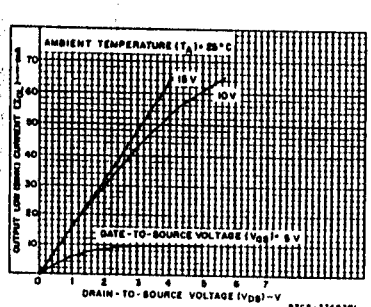


Fig. 5 – Minimum output low (sink) current drain characteristics.

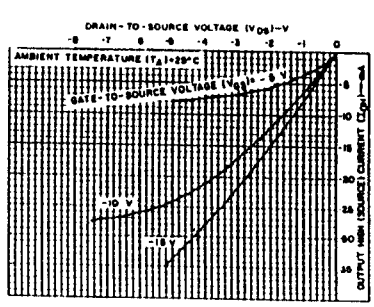


Fig. 6 – Typical output high (source) current characteristics.

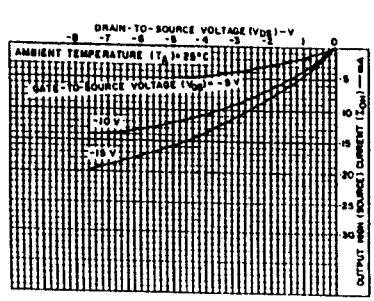


Fig. 7 – Minimum output high (source) current characteristics.

CD4049UB, CD4050B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A=25°C; Input t_r,t_f=20 ns, C_L=50 pF, R_L=200 kΩ

CHARACTERISTIC	CONDITIONS		LIMITS ALL PKGS.		UNITS
	V_{IN}	V_{CC}	Typ.	Max.	
Propagation Delay Time: Low-to-High, t_{PLH} CD4049UB	5	5	60	120	ns
	10	10	32	65	
	10	5	45	90	
	15	15	25	50	
	15	5	45	90	
CD4050B	5	5	70	140	
	10	10	40	80	
	10	5	45	90	
	15	15	30	60	
	15	5	40	80	
High-to-Low, t_{PHL} CD4049UB	5	5	32	65	ns
	10	10	20	40	
	10	5	15	30	
	15	15	15	30	
	15	5	10	20	
CD4050B	5	5	55	110	
	10	10	22	55	
	10	5	50	100	
	15	15	15	30	
	15	5	50	100	
Transition Time: Low-to-High, t_{TLH}	5	5	80	160	ns
	10	10	40	80	
	15	15	30	60	
High-to-Low, t_{THL}	5	5	30	60	
	10	10	20	40	
	15	15	15	30	
Input Capacitance, C_{IN} CD4049UB			15	22.5	pF
CD4050B			5	7.5	

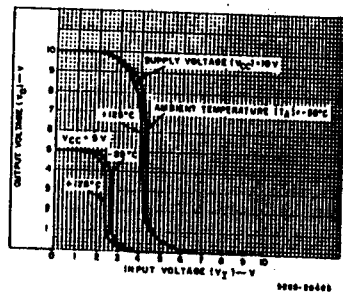


Fig. 8 – Typical voltage transfer characteristics as a function of temperature for CD4049UB.

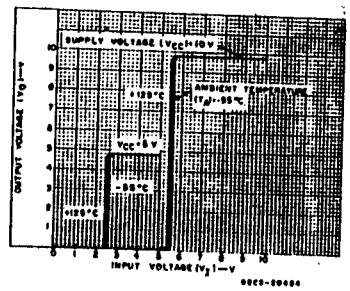


Fig. 9 – Typical voltage transfer characteristics as a function of temperature for CD4050B.

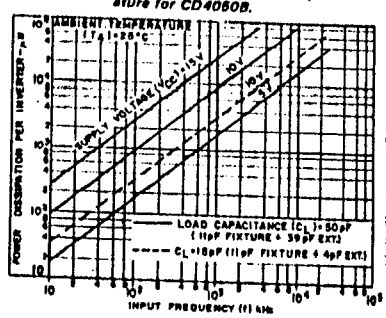


Fig. 10 – Typical power dissipation vs. frequency characteristics.

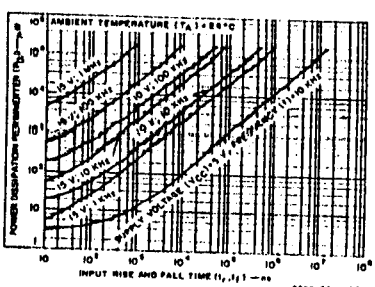


Fig. 11 – Typical power dissipation vs. input rise and fall times per inverter for CD4049UB.

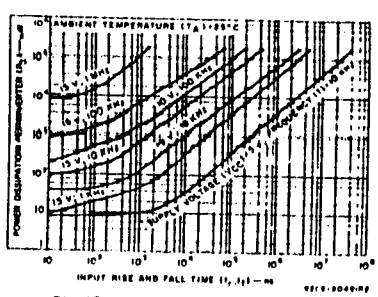


Fig. 12 – Typical power dissipation vs. input rise and fall times per inverter for CD4050B.

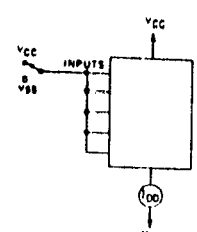


Fig. 13 – Quiescent device current test circuit.

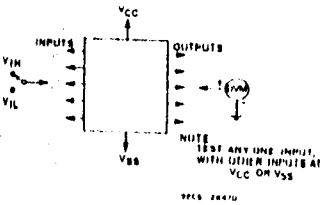


Fig. 14 – Input voltage test circuit.

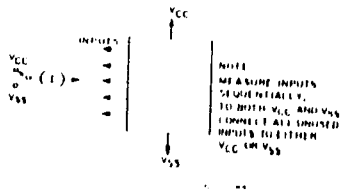


Fig. 15 – Input current test circuit.

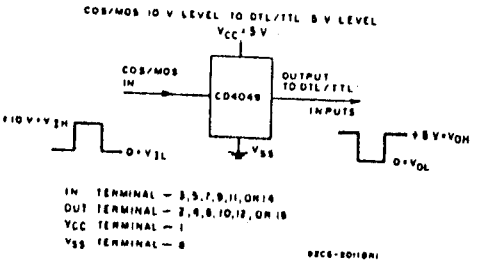
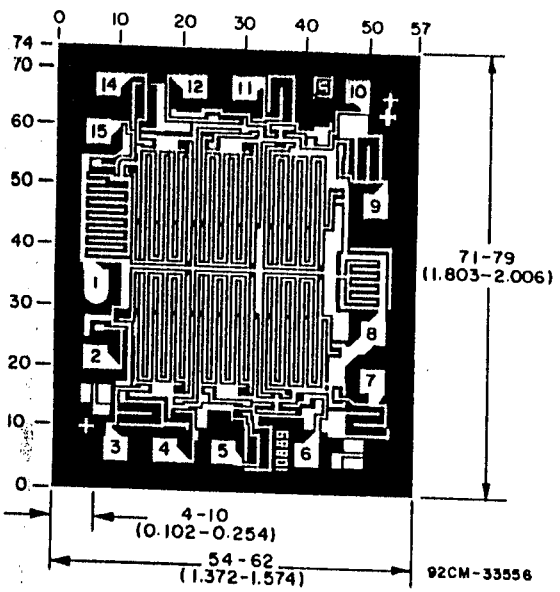
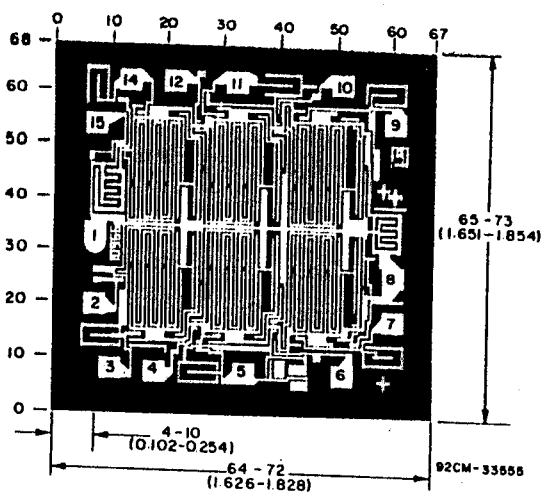


Fig. 16 – Logic-level conversion application.

CHIP PHOTOGRAPHS DIMENSIONS AND PAD LAYOUTS



CD4049UBH

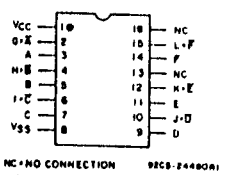


CD4050BH

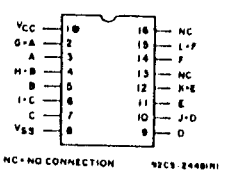
Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is separated into individual chips, the angle of cleavage may vary with respect to the chip face for different chips. The actual dimensions of the isolated chip, therefore, may differ slightly from the nominal dimensions shown. The user should consider a tolerance of −3 mils to +16 mils applicable to the nominal dimensions shown.

TERMINAL ASSIGNMENTS



CD4049UB



CD4050B

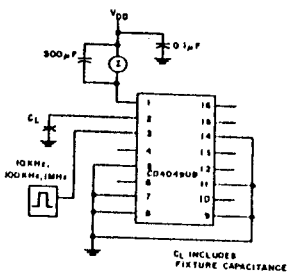


Fig. 17 – Dynamic power dissipation test circuit.

- '150 Selects One-of-Sixteen Data Sources
- Others Select One-of-Eight Data Sources
- Performs Parallel-to-Serial Conversion
- Permits Multiplexing from N Lines to One Line
- Also For Use as Boolean Function Generator
- Input-Clamping Diodes Simplify System Design
- Fully Compatible with Most TTL Circuits

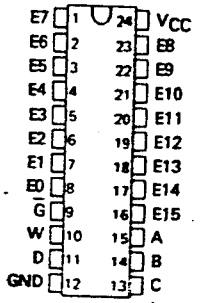
TYPE	TYPICAL AVERAGE PROPAGATION DELAY TIME DATA INPUT TO W OUTPUT	TYPICAL POWER DISSIPATION
'150	13 ns	200 mW
'151A	8 ns	145 mW
'LS151	8 ns	130 mW
'S151	13 ns	30 mW
'LS152	13 ns	28 mW
'S152	4.5 ns	225 mW

These monolithic data selectors/multiplexers contain full on-chip binary decoding to select the desired data source. The '150 selects one-of-sixteen data sources; the '151A, '152A, 'LS151, 'LS152, and 'S151 select one-of-eight data sources. The '150, '151A, 'LS151, and 'S151 have a strobe input which must be at a low logic level to enable these devices. A high level at the strobe forces the W output high, and the Y output (as applicable) low.

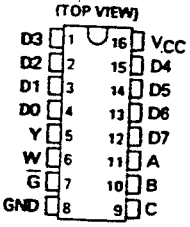
The '151A, 'LS151, and 'S151 feature complementary W and Y outputs whereas the '150, '152A, and 'LS152 have an inverted (W) output only.

The '151A and '152A incorporate address buffers which have symmetrical propagation delay times through complementary paths. This reduces the possibility of transients occurring at the output(s) when changes made at the select inputs, even when the '151A outputs are enabled (i.e., strobe low).

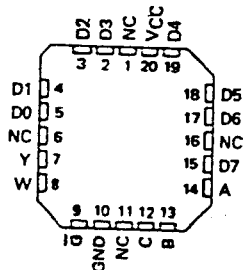
SN54150 . . . J OR W PACKAGE
SN74150 . . . J OR N PACKAGE
(TOP VIEW)



SN54151A, SN54LS151, SN54S151 . . . J OR W PACKAGE
SN74151A . . . J OR N PACKAGE
SN74LS151, SN74S151 . . . D, J OR N PACKAGE
(TOP VIEW)

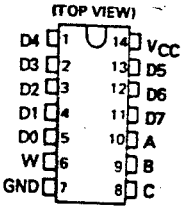


SN54LS151, SN54S151 . . . FK PACKAGE
SN74LS151, SN74S151 . . . FN PACKAGE
(TOP VIEW)



NC - No internal connection

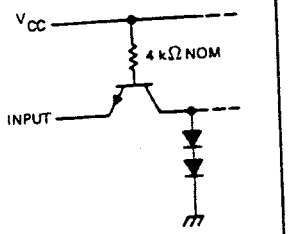
SN54152A, SN54LS152 . . . W PACKAGE
(TOP VIEW)



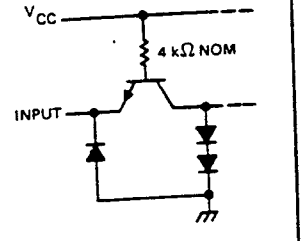
For SN54LS152 Chip Carrier Information, Contact The Factory.

schematics of inputs and outputs

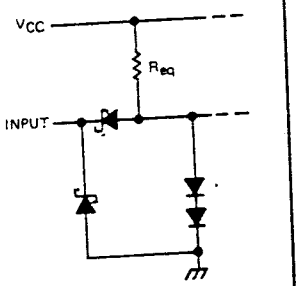
EQUIVALENT OF EACH INPUT OF '150



EQUIVALENT OF EACH INPUT OF '151A, '152A

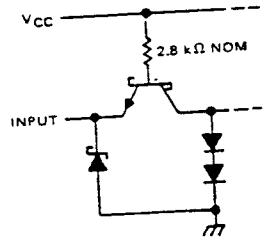


EQUIVALENT OF EACH INPUT OF 'LS151, 'LS152



Data select and strobe: R_{eq} = 20 kΩ NOM
Data inputs: R_{eq} = 17 kΩ NOM

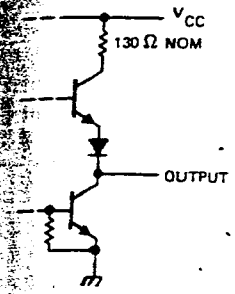
EQUIVALENT OF EACH INPUT OF 'S151



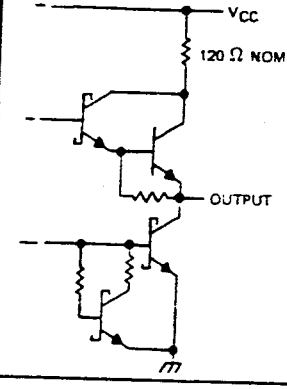
TYPES SN54150, SN54151A, SN54152A, SN54LS151, SN54LS152, SN54S151
SN74150, SN74151A, SN74LS151, SN74S151
DATA SELECTORS/MULTIPLEXERS

schematics of inputs and outputs

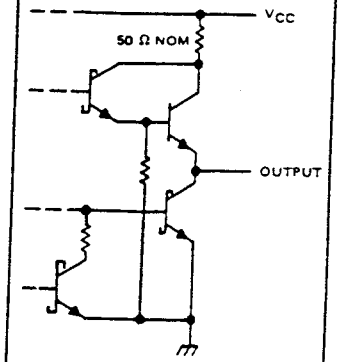
TYPICAL OF ALL OUTPUTS OF '150, '151A, '152A



TYPICAL OF ALL OUTPUTS OF 'LS151, 'LS152



TYPICAL OF ALL OUTPUTS OF 'S151



'150
FUNCTION TABLE

INPUTS					OUTPUT
SELECT				STROBE	
D	C	B	A	$\overline{G}$	W
X	X	X	X	H	H
L	L	L	L	L	$\overline{E0}$
L	L	L	H	L	$\overline{E1}$
L	L	H	L	L	$\overline{E2}$
L	L	H	H	L	$\overline{E3}$
L	H	L	L	L	$\overline{E4}$
L	H	L	H	L	$\overline{E5}$
L	H	H	L	L	$\overline{E6}$
L	H	H	H	L	$\overline{E7}$
H	L	L	L	L	$\overline{E8}$
H	L	L	H	L	$\overline{E9}$
H	L	H	L	L	$\overline{E10}$
H	L	H	H	L	$\overline{E11}$
H	H	L	L	L	$\overline{E12}$
H	H	L	H	L	$\overline{E13}$
H	H	H	L	L	$\overline{E14}$
H	H	H	H	L	$\overline{E15}$

'151A, 'LS151, 'S151
FUNCTION TABLE

INPUTS				OUTPUTS	
SELECT			STROBE		
C	B	A	$\overline{G}$	Y	W
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

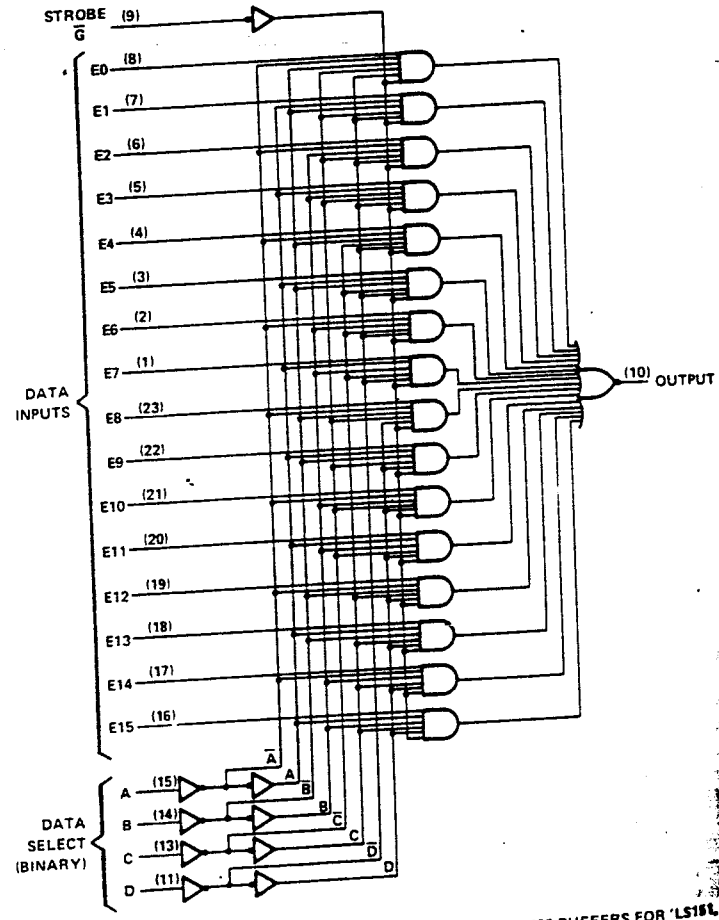
'152A, 'LS152
FUNCTION TABLE

SELECT INPUTS			OUTPUT
C	B	A	W
L	L	L	$\overline{D0}$
L	L	H	$\overline{D1}$
L	H	L	$\overline{D2}$
L	H	H	$\overline{D3}$
H	L	L	$\overline{D4}$
H	L	H	$\overline{D5}$
H	H	L	$\overline{D6}$
H	H	H	$\overline{D7}$

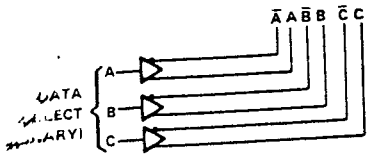
H = high level, L = low level, X = irrelevant
$\overline{E0}$, $\overline{E1}$ . . . $\overline{E15}$ = the complement of the level of the respective E inout
D0, D1 . . . D7 = the level of the D respective input

logic diagrams

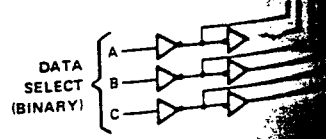
'150



ADDRESS BUFFERS FOR '151A, '152A

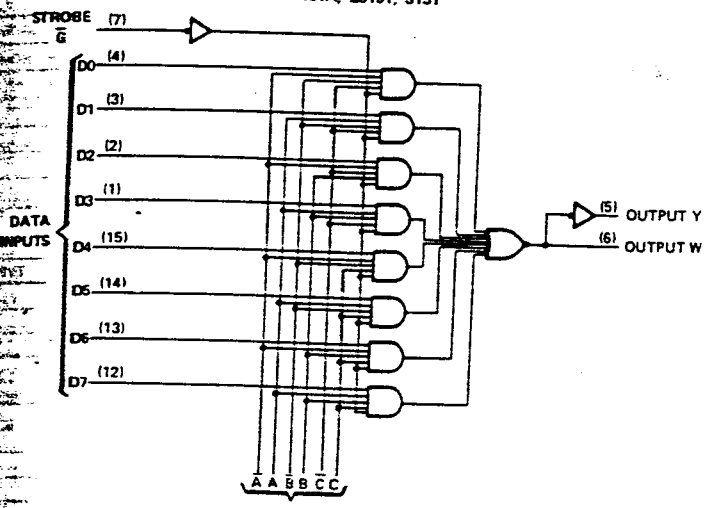


ADDRESS BUFFERS FOR 'LS151, 'S151



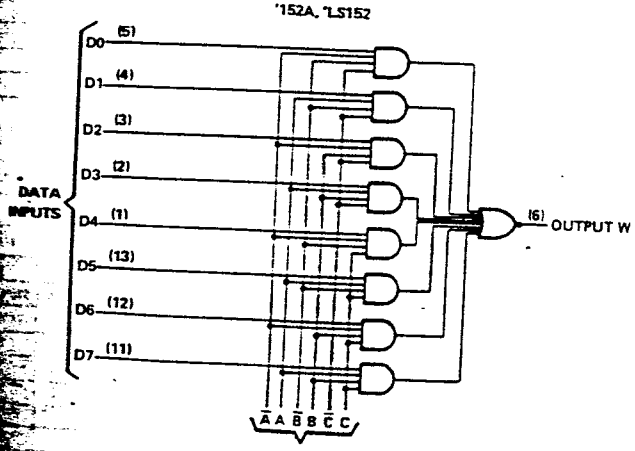
Pin numbers shown on logic notation are for D, J or N packages.

'151A, 'LS151, 'S151



TO ADDRESS BUFFERS

'152A, 'LS152



TO ADDRESS BUFFERS

Pin numbers shown on logic notation are for D, J or N packages.

ratings over operating free-air temperature range (unless otherwise noted)

CC (see Note 1) ..... 7 V
Note 2): '150, '151A, 'S151, '152A ..... 5.5 V
'LS151, 'LS152 ..... 7 V
temperature range: SN54' ..... −55°C to 125°C
SN74' ..... 0°C to 70°C
range ..... −65°C to 150°C
with respect to network ground terminal.
input voltages must be

recommended operating conditions

	SN54'			SN74'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−800			−800	μA
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		'150			'151A, '152A			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −8 mA							−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA		2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA			0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V				40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−1.6			−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	SN54'	−20		−55	−20		−55	mA
			SN74'	−18		−55	−18		−55	
I_{CC}	Supply current	V_{CC} = MAX, See Note 3	'150		40	68				mA
			'151A					29	48	
			'152A					26	43	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡ All typical values at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output of the '151A should be shorted at a time.
NOTE 3: I_{CC} is measured with the strobe and data select inputs at 4.5 V, all other inputs and outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'150			'151A, '152A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	A, B, or C (4 levels)	Y	C_L = 15 pF, R_L = 400 Ω, See Note 4					25	38	ns
t_{PHL}								25	38	
t_{PLH}	A, B, C, or D (3 levels)	W			23	35		17	26	ns
t_{PHL}					22	33		19	30	
t_{PLH}	Strobe $\overline{G}$	Y						21	33	ns
t_{PHL}								22	33	
t_{PLH}	Strobe $\overline{G}$	W			15.5	24		14	21	ns
t_{PHL}					21	30		15	23	
t_{PLH}	D0 thru D7	Y						13	20	ns
t_{PHL}								18	27	
t_{PLH}	E0 thru E15, or D0 thru D7	W			8.5	14		8	14	ns
t_{PHL}					13	20		8	14	

¶ t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output
See General Information Section for load circuits and voltage waveforms

recommended operating conditions

	SN54LS'			SN74LS'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†			SN54LS'			SN74LS'			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage				2			2			V
V_{IL} Low-level input voltage						0.7			0.8	V
V_{IK} Input clamp voltage	V_{CC} = MIN, I_I = −18 mA					−1.5			−1.5	V
V_{OH} High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max, I_{OH} = −400 μA			2.5	3.4		2.7	3.4		V
V_{OL} Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 4 mA			0.25	0.4		0.25	0.4	V
		I_{OL} = 8 mA						0.35	0.5	
I_I Input current at maximum input voltage	V_{CC} = MAX, V_I = 7 V					0.1			0.1	mA
I_{IH} High-level input current	V_{CC} = MAX, V_I = 2.7 V					20			20	μA
I_{IL} Low-level input current	V_{CC} = MAX, V_I = 0.4 V					−0.4			−0.4	mA
I_{OS} Short-circuit output current§	V_{CC} = MAX			−20		−100	−20		−100	mA
I_{CC} Supply current	V_{CC} = MAX, Outputs open, All inputs at 4.5 V	'LS151			6.0	10		6.0	10	mA
		'LS152			5.6	9				

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and duration of short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54LS', SN74LS'			UNIT
				MIN	TYP	MAX	
t_{PLH}	A, B, or C (4 levels)	Y	C_L = 15 pF, R_L = 2 kΩ, See Note 4		27	43	ns
t_{PHL}					18	30	
t_{PLH}	A, B, or C (3 levels)	W			14	23	ns
t_{PHL}					20	32	
t_{PLH}	Strobe $\overline{G}$	Y			26	42	ns
t_{PHL}					20	32	
t_{PLH}	Strobe $\overline{G}$	W			15	24	ns
t_{PHL}					18	30	
t_{PLH}	Any D	Y			20	32	ns
t_{PHL}					16	26	
t_{PLH}	Any D	W			13	21	ns
t_{PHL}					12	20	

¶ t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output
See General Information Section for load circuits and voltage waveforms

TTL DEVICES

recommended operating conditions

	SN54S151			SN74S151			Unit
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−1			−1	mA
Low-level output current, I_{OL}			20			20	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	Unit
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −1 mA	SN54S*	2.5	3.4		V
			SN74S*	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA				0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				50	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5 V				−2	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−40		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, All inputs at 4.5 V, All outputs open			45	70	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54S151, SN74S151			Unit
				MIN	TYP	MAX	
t_{PLH}	A, B, or C (4 levels)	Y	C_L = 15 pF, R_L = 280 Ω, See Note 4		12	18	ns
t_{PHL}					12	18	
t_{PLH}	A, B, or C (3 levels)	W			10	15	ns
t_{PHL}					9	13.5	
t_{PLH}	Any D	Y			8	12	ns
t_{PHL}					8	12	
t_{PLH}	Any D	W			4.5	7	ns
t_{PHL}					4.5	7	
t_{PLH}	Strobe $\overline{G}$	Y			11	16.5	ns
t_{PHL}					12	18	
t_{PLH}	Strobe $\overline{G}$	W			9	13	ns
t_{PHL}					8.5	12	

¶t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output

NOTE 4: See General Information Section for load circuits and voltage waveforms.

TEXAS INSTRUMENTS
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REVISED DECEMBER 1983

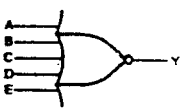
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

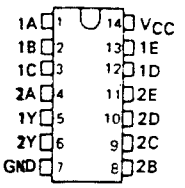
These devices contain two independent 5-input positive -NOR gates. They perform the Boolean function $Y = \overline{A+B+C+D+E}$ in positive logic.

The SN54S260 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74S260 is characterized for operation from 0°C to 70°C.

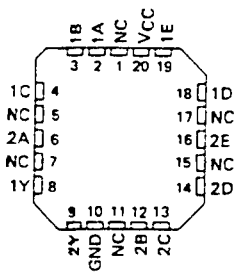
logic diagram (each gate)



SN54S260 . . . J OR W PACKAGE
SN74S260 . . . D, J OR N PACKAGE
(TOP VIEW)

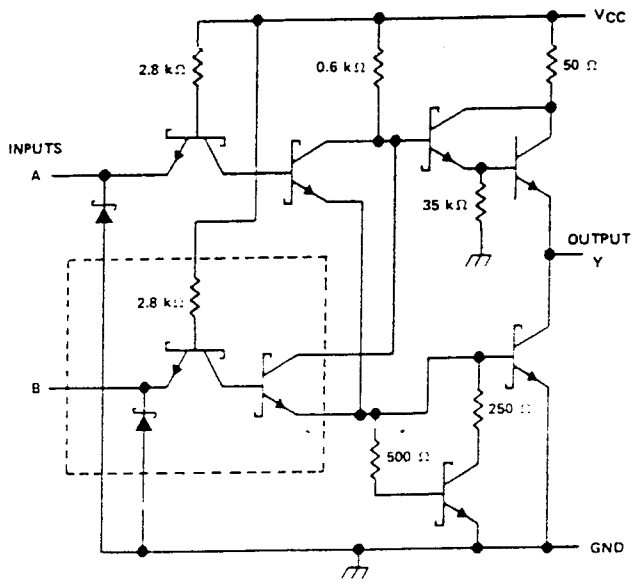


SN54S260 . . . FK PACKAGE
SN74S260 . . . FN PACKAGE
(TOP VIEW)



NC – No internal connection

schematic (each gate)



Resistor values shown are nominal.
The portion of the schematic within the dashed-line is repeated for each additional input.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 7 V
Input voltage ..... 5.5 V
Operating free-air temperature range: SN54' ..... −55°C to 125°C
SN74' ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54S260			SN74S260			UNIT
	MIN	TYP	MAX	MIN	TYP	MAX	
V_{CC} Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH} High-level input voltage	2			2			V
V_{IL} Low-level input voltage			0.8			0.8	V
I_{OH} High-level output current			−1			−1	mA
I_{OL} Low-level output current			20			20	mA
T_A Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN54S260			SN74S260			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN, I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OH} = −1 mA	2.5	3.4		2.7	3.4		V
V_{OL}	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 20 mA			0.5			0.5	V
I_I	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	V_{CC} = MAX, V_{IH} = 2.7 V			50			50	μA
I_{IL}	V_{CC} = MAX, V_{IL} = 0.5 V			−2			−2	mA
I_{OS} §	V_{CC} = MAX	−40		−100	−40		−100	mA
I_{CCH}	V_{CC} = MAX, V_I = 0 V		17	29		17	29	mA
I_{CCL}	V_{CC} = MAX, See Note 2		26	45		26	45	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.
NOTE 2: One input at 4.5 V, all others at GND.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Any	Y	R_L = 280 Ω, C_L = 15 pF		4	5.5	ns
t_{PHL}					4	6	ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

National Semiconductor

ADC0808, ADC0809 8-Bit μP Compatible A/D Converters With 8-Channel Multiplexer

General Description

The ADC0808, ADC0809 data acquisition component is a monolithic CMOS device with an 8-bit analog-to-digital converter, 8-channel multiplexer and microprocessor compatible control logic. The 8-bit A/D converter uses successive approximation as the conversion technique. The converter features a high impedance chopper stabilized comparator, a 256R voltage divider with analog switch tree and a successive approximation register. The 8-channel multiplexer can directly access any of 8-single-ended analog signals.

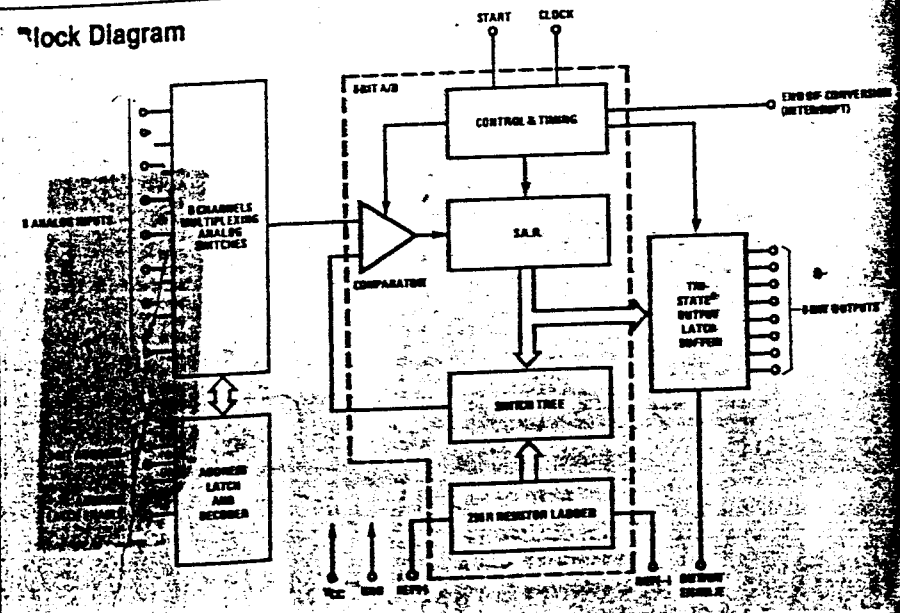
The device eliminates the need for external zero and full-scale adjustments. Easy interfacing to microprocessors is provided by the latched and decoded multiplexer address inputs and latched TTL TRI-STATE® outputs.

The design of the ADC0808, ADC0809 has been optimized by incorporating the most desirable aspects of several A/D conversion techniques. The ADC0808, ADC0809 offers high speed, high accuracy, minimal temperature dependence, excellent long-term accuracy and repeatability, and consumes minimal power. These features make this device ideally suited to applications from process and machine control to consumer and automotive applications. For 16-channel multiplexer with common output (sample/hold port) see ADC0816 data sheet. (See AN-247 for more information.

Features

- Resolution — 8-bits
- Total unadjusted error — ±1/2 LSB and ±1 LSB
- No missing codes
- Conversion time — 100 μs
- Single supply — 5 V_{DC}
- Operates ratiometrically or with 5 V_{DC} or analog span adjusted voltage reference
- 8-channel multiplexer with latched control logic
- Easy interface to all microprocessors, or operates "stand alone"
- Outputs meet T^2L voltage level specifications
- 0V to 5V analog input voltage range with single 5V supply
- No zero or full-scale adjust required
- Standard hermetic or molded 28-pin DIP package
- Temperature range −40°C to +85°C or −55°C to +125°C
- Low power consumption — 15 mW
- Latched TRI-STATE® output

Block Diagram



Absolute Maximum Ratings (Notes 1 and 2)

Supply Voltage (V_{CC}) (Note 3)	6.5V
Voltage at Any Pin Except Control Inputs	−0.3V to (V_{CC} + 0.3V)
Voltage at Control Inputs (START, OE, CLOCK, ALE, ADD A, ADD B, ADD C)	−0.3V to +15V
Storage Temperature Range	−65°C to +150°C
Package Dissipation at T_A = 25°C	875 mW
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Ratings (Notes 1 and 2)

Temperature Range (Note 1) ADC0808CJ	$T_{MIN} \le T_A \le T_{MAX}$ −55°C ≤ T_A ≤ +125°C
ADC0808CCJ, ADC0808CCN, ADC0809CCN	−40°C ≤ T_A ≤ +85°C
Range of V_{CC} (Note 1)	4.5 V_{DC} to 6.0 V_{DC}

Electrical Characteristics

Converter Specifications: V_{CC} = 5 V_{DC} = $V_{REF(+)}$, $V_{REF(-)}$ = GND, $T_{MIN} \le T_A \le T_{MAX}$ and f_{CLK} = 640 kHz unless otherwise stated.

	Parameter	Conditions	Min	Typ	Max	Units
	ADC0808					
	Total Unadjusted Error (Note 5)	25°C			±1/2	LSB
		T_{MIN} to T_{MAX}			±3/4	LSB
	ADC0809					
	Total Unadjusted Error (Note 5)	0°C to 70°C			±1	LSB
		T_{MIN} to T_{MAX}			±1 1/4	LSB
	Input Resistance	From Ref(+) to Ref(−)	1.0	2.5		kΩ
	Analog Input Voltage Range	(Note 4) V(+) or V(−)	GND−0.10		V_{CC}+0.10	V_{DC}
$V_{REF(+)}$	Voltage, Top of Ladder	Measured at Ref(+)		V_{CC}	V_{CC}+0.1	V
$\frac{V_{REF(+)}+V_{REF(-)}}{2}$	Voltage, Center of Ladder			V_{CC}/2−0.1	V_{CC}/2	V_{CC}/2+0.1	V
$V_{REF(-)}$	Voltage, Bottom of Ladder	Measured at Ref(−)		−0.1	0		V
	Comparator Input Current	f_c = 640 kHz, (Note 6)		−2	±0.5	2	μA

Electrical Characteristics

Digital Levels and DC Specifications: ADC0808CJ 4.5V ≤ V_{CC} ≤ 5.5V, −55°C ≤ T_A ≤ +125°C unless otherwise noted ADC0808CCJ, ADC0808CCN, and ADC0809CCN 4.75 ≤ V_{CC} ≤ 5.25V, −40°C ≤ T_A ≤ +85°C unless otherwise noted

	Parameter	Conditions	Min	Typ	Max	Units
ANALOG MULTIPLEXER						
$I_{OFF(+)}$	OFF Channel Leakage Current	V_{CC} = 5V, V_{IN} = 5V, T_A = 25°C		−10	200	nA
		T_{MIN} to T_{MAX}			1.0	μA
$I_{OFF(-)}$	OFF Channel Leakage Current	V_{CC} = 5V, V_{IN} = 0, T_A = 25°C	−200	−10		nA
		T_{MIN} to T_{MAX}	−1.0			μA
CONTROL INPUTS						
$V_{IN(1)}$	Logical "1" Input Voltage		V_{CC}−1.5			V
$V_{IN(0)}$	Logical "0" Input Voltage				1.5	V
$I_{IN(1)}$	Logical "1" Input Current (The Control Inputs)	V_{IN} = 15V			1.0	μA
$I_{IN(0)}$	Logical "0" Input Current (The Control Inputs)	V_{IN} = 0	−1.0			μA
I_{CC}	Supply Current	f_{CLK} = 640 kHz		0.3	3.0	mA

ADC0808, ADC0809

...acteristics (Continued)

Digital Levels and DC Specifications: ADC0808CJ $4.5V \le V_{CC} \le 5.5V$, $-55°C \le T_A \le +125°C$ unless otherwise noted
ADC0808CCJ, ADC0808CCN, and ADC0809CCN $4.75 \le V_{CC} \le 5.25V$, $-40°C \le T_A \le +85°C$ unless otherwise noted

Parameter		Conditions	Min	Typ	Max	Units
DATA OUTPUTS AND EOC (INTERRUPT)						
$V_{OUT(1)}$	Logical "1" Output Voltage	$I_O = -360\ \mu A$	$V_{CC}-0.4$			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$I_O = 1.6$ mA			0.45	V
$V_{OUT(0)}$	Logical "0" Output Voltage EOC	$I_O = 1.2$ mA			0.45	V
I_{OUT}	TRI-STATE® Output Current	$V_O = 5V$			3	μA
		$V_O = 0$	−3			μA

Electrical Characteristics

Timing Specifications: $V_{CC} = V_{REF(+)} = 5V$, $V_{REF(-)} = GND$, $t_r = t_f = 20$ ns and $T_A = 25°C$ unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{WS}	Minimum Start Pulse Width	*(Figure 5)*		100	200	ns
t_{WALE}	Minimum ALE Pulse Width	*(Figure 5)*		100	200	ns
t_s	Minimum Address Set-Up Time	*(Figure 5)*		25	50	ns
t_H	Minimum Address Hold Time	*(Figure 5)*		25	50	ns
t_D	Analog MUX Delay Time From ALE	$R_S = 0\Omega$ *(Figure 5)*		1	2.5	μs
t_{H1}, t_{H0}	OE Control to Q Logic State	$C_L = 50$ pF, $R_L = 10$k *(Figure 8)*		125	250	ns
t_{1H}, t_{0H}	OE Control to Hi-Z	$C_L = 10$ pF, $R_L = 10$k *(Figure 8)*		125	250	ns
t_c	Conversion Time	$f_c = 640$ kHz, *(Figure 5)* (Note 7)	90	100	116	μs
f_c	Clock Frequency		10	640	1280	kHz
t_{EOC}	EOC Delay Time	*(Figure 5)*	0		8 + 2 μs	Clock Periods
C_{IN}	Input Capacitance	At Control Inputs		10	15	pF
C_{OUT}	TRI-STATE® Output Capacitance	At TRI-STATE® Outputs, (Note 12)		10	15	pF

Note 1: Absolute maximum ratings are those values beyond which the life of the device may be impaired.

Note 2: All voltages are measured with respect to GND, unless otherwise specified.

Note 3: A zener diode exists, internally, from V_{CC} to GND and has a typical breakdown voltage of 7 V_{DC}.

Note 4: Two on-chip diodes are tied to each analog input which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. The spec allows 100 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 100 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.900 V_{DC} over temperature variations, initial tolerance and loading.

Note 5: Total unadjusted error includes offset, full-scale, linearity, and multiplexer errors. See *Figure 3*. None of these A/Ds requires a zero or full-scale adjust. However, if an all zero code is desired for an analog input other than 0.0V, or if a narrow full-scale span exists (for example: 0.5V to 4.5V full-scale) the reference voltages can be adjusted to achieve this. See *Figure 13*.

Note 6: Comparator input current is a bias current into or out of the chopper stabilized comparator. The bias current varies directly with clock frequency and has little temperature dependence *(Figure 6)*. See paragraph 4.0.

Note 7: The outputs of the data register are updated one clock cycle before the rising edge of EOC.

...ctional Description

...ice: The device contains an 8-channel single-...analog signal multiplexer. A particular input chan-...is selected by using the address decoder. Table I ...e input states for the address lines to select any ...nel. The address is latched into the decoder on the ...gh transition of the address latch enable signal.

TABLE I

SELECTED ANALOG CHANNEL	ADDRESS LINE C	B	A
IN0	L	L	L
IN1	L	L	H
IN2	L	H	L
IN3	L	H	H
IN4	H	L	L
IN5	H	L	H
IN6	H	H	L
IN7	H	H	H

...VERTER CHARACTERISTICS

...e Converter

...e heart of this single chip data acquisition system is its ...bit analog-to-digital converter. The converter is designed to give fast, accurate, and repeatable conversions over a wide range of temperatures. The converter is partitioned into 3 major sections: the 256R ladder network, the successive approximation register, and the comparator. The converter's digital outputs are positive true.

The 256R ladder network approach *(Figure 1)* was chosen over the conventional R/2R ladder because of its inherent monotonicity, which guarantees no missing digital codes. Monotonicity is particularly important in closed loop feedback control systems. A non-monotonic relationship can cause oscillations that will be catastrophic for the system. Additionally, the 256R network does not cause load variations on the reference voltage.

The bottom resistor and the top resistor of the ladder network in *Figure 1* are not the same value as the remainder of the network. The difference in these resistors causes the output characteristic to be symmetrical with the zero and full-scale points of the transfer curve. The first output transition occurs when the analog signal has reached +1/2 LSB and succeeding output transitions occur every 1 LSB later up to full-scale.

The successive approximation register (SAR) performs 8 iterations to approximate the input voltage. For any SAR type converter, n-iterations are required for an n-bit converter. *Figure 2* shows a typical example of a 3-bit converter. In the ADC0808, ADC0809, the approximation technique is extended to 8 bits using the 256R network.

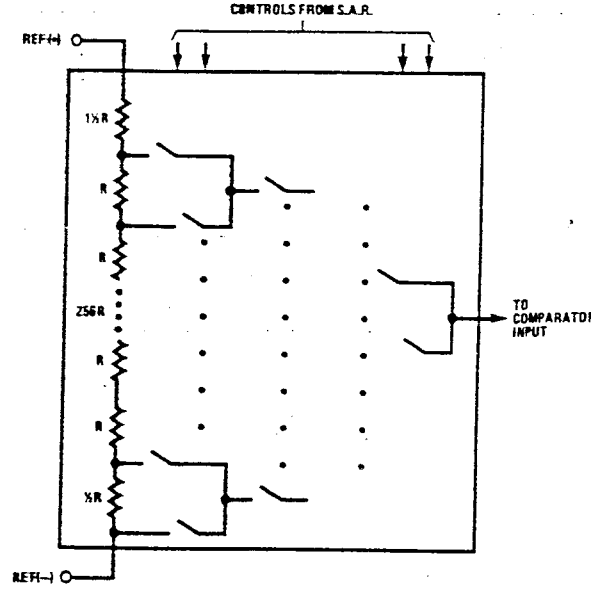


FIGURE 1. Resistor Ladder and Switch Tree

The A/D converter's successive approximation register (SAR) is reset on the positive edge of the start conversion (SC) pulse. The conversion is begun on the falling edge of the start conversion pulse. A conversion in process will be interrupted by receipt of a new start conversion pulse. Continuous conversion may be accomplished by tying the end-of-conversion (EOC) output to the SC input. If used in this mode, an external start conversion pulse should be applied after power up. End-of-conversion will go low between 0 and 8 clock pulses after the rising edge of start conversion.

The most important section of the A/D converter is the comparator. It is this section which is responsible for the ultimate accuracy of the entire converter. It is also the comparator drift which has the greatest influence on repeatability of the device. A chopper-stabilized comparator provides the most effective method of satisfying all the converter requirements.

The chopper-stabilized comparator converts the DC input signal into an AC signal. This signal is then fed through a high gain AC amplifier and has the DC level restored. This technique limits the drift component of the amplifier since the drift is a DC component which is not passed by the AC amplifier. This makes the entire A/D converter extremely insensitive to temperature, long term drift and input offset errors.

Figure 4 shows a typical error curve for the ADC0808 as measured using the procedures outlined in AN-179.

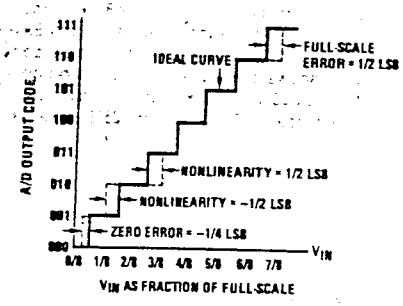


FIGURE 2. 3-Bit A/D Transfer Curve

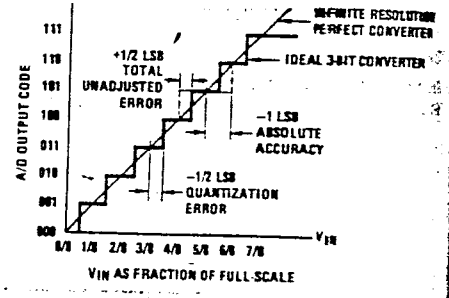


FIGURE 3. 3-Bit A/D Absolute Accuracy Curve

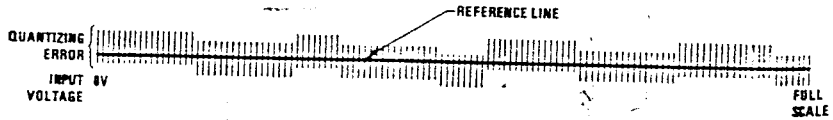
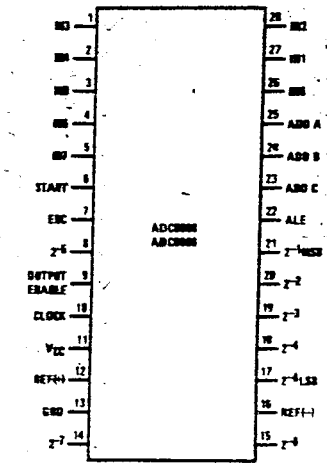


FIGURE 4. Typical Error Curve

Dual-In-Line Package



Timing Diagram

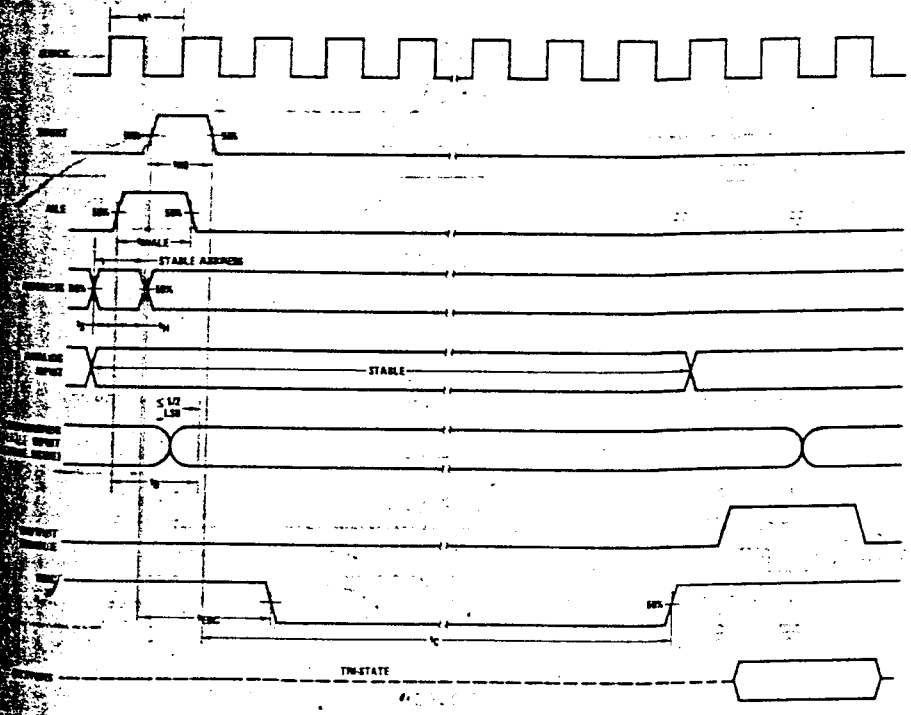


FIGURE 5

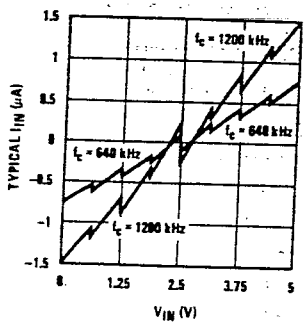


FIGURE 6. Comparator I_{IN} vs V_{IN} ($V_{CC} = V_{REF} = 5V$)

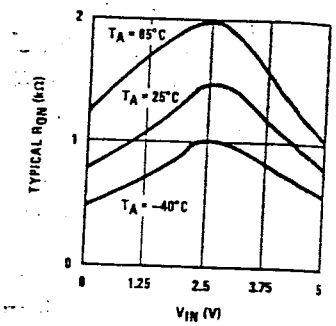


FIGURE 7. Multiplexer R_{ON} vs V_{IN} ($V_{CC} = V_{REF} = 5V$)

TRI-STATE® Test Circuits and Timing Diagrams

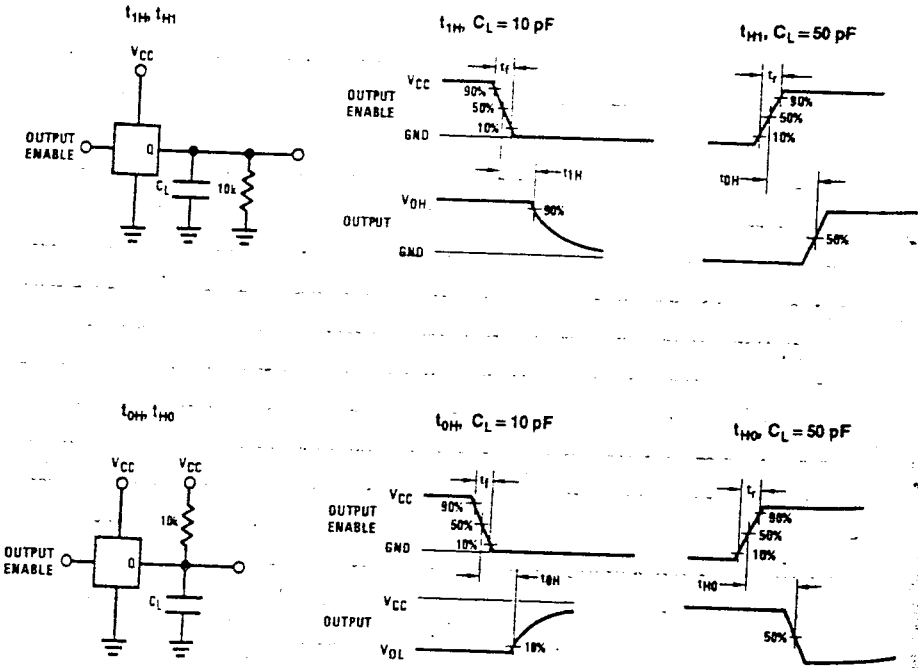


FIGURE 8

Ratiometric Conversion

ADC0808, ADC0809 is designed as a complete Data Acquisition System (DAS) for ratiometric conversion systems. In ratiometric systems, the physical variable measured is expressed as a percentage of full-scale and is not necessarily related to an absolute standard. The voltage input to the ADC0808 is expressed by the equation:

$$\frac{V_{IN} - V_Z}{V_{FS} - V_Z} = \frac{D_X}{D_{MAX} - D_{MIN}} \quad (1)$$

V_{IN} = Input voltage into the ADC0808
V_{FS} = Full-scale voltage
V_Z = Zero voltage
D_X = Data point being measured
D_{MAX} = Maximum data limit
D_{MIN} = Minimum data limit

A good example of a ratiometric transducer is a potentiometer used as a position sensor. The position of the wiper is directly proportional to the output voltage which is a ratio of the full-scale voltage across it. Since the data is represented as a proportion of full-scale, reference requirements are greatly reduced, eliminating a large source of error and cost for many applications. A major advantage of the ADC0808, ADC0809 is that the input voltage range is equal to the supply range so the transducers can be connected directly across the supply and their outputs connected directly into the multiplexer inputs. (*Figure 9*).

ratiometric transducers such as potentiometric, strain gauges, thermistor bridges, pressure transducers, etc., are suitable for measuring proportional relationships; however, many types of measurements must be referred to an absolute standard such as voltage or current. This means a system reference must be used which relates the full-scale voltage to the standard volt. For example, if $V_{CC} = V_{REF} = 5.12V$, then the full-scale range is divided into 256 standard steps. The smallest standard step is 1 LSB which is then 20 mV.

2.0 Resistor Ladder Limitations

The voltages from the resistor ladder are compared to the selected input 8 times in a conversion. These voltages are coupled to the comparator via an analog switch tree which is referenced to the supply. The voltages at the top, center and bottom of the ladder must be controlled to maintain proper operation.

The top of the ladder, Ref(+), should not be more positive than the supply, and the bottom of the ladder, Ref(−), should not be more negative than ground. The center of the ladder voltage must also be near the center of the supply because the analog switch tree changes from N-channel switches to P-channel switches. These limitations are automatically satisfied in ratiometric systems and can be easily met in ground referenced systems.

Figure 10 shows a ground referenced system with a separate supply and reference. In this system, the supply must be trimmed to match the reference voltage. For instance, if a 5.12V is used, the supply should be adjusted to the same voltage within 0.1V.

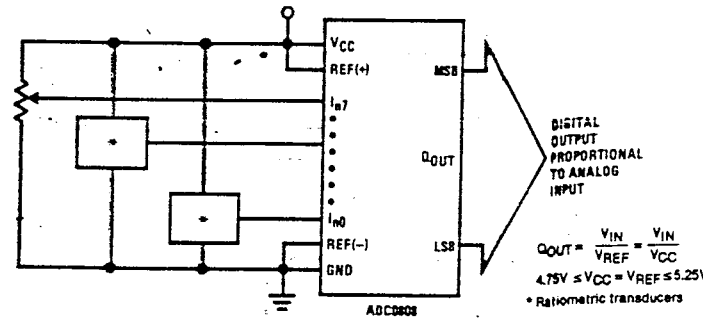


FIGURE 9. Ratiometric Conversion System

The ADC0808 needs less than a milliamp of supply current so developing the supply from the reference is readily accomplished. In *Figure 11* a ground referenced system is shown which generates the supply from the reference. The buffer shown can be an op amp of sufficient drive to supply the milliamp of supply current and the desired bus drive, or if a capacitive bus is driven by the outputs a large capacitor will supply the transient supply current as seen in *Figure 12*. The LM301 is overcompensated to insure stability when loaded by the 10 μF output capacitor.

The top and bottom ladder voltages cannot exce... and ground, respectively, but they can be symmet... less than V_{CC} and greater than ground. The center... ladder voltage should always be near the center o... supply. The sensitivity of the converter can be incre... (i.e., size of the LSB steps decreased) by using a ... metrical reference system. In *Figure 13*, a 2.5V ref... is symmetrically centered about $V_{CC}/2$ since the ... current flows in identical resistors. This system u... 2.5V reference allows the LSB bit to be half the si... 5V reference system.

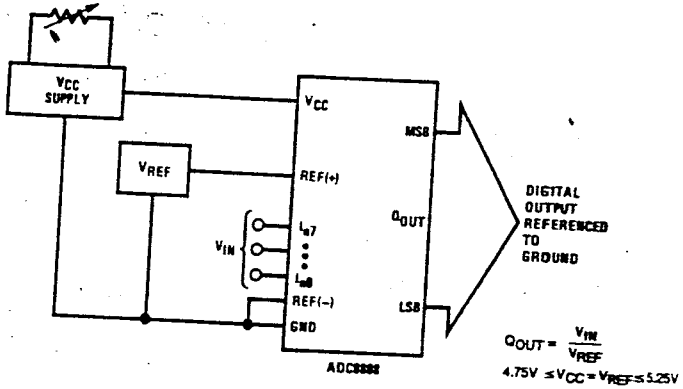


FIGURE 10. Ground Referenced Conversion System Using Trimmed Supply

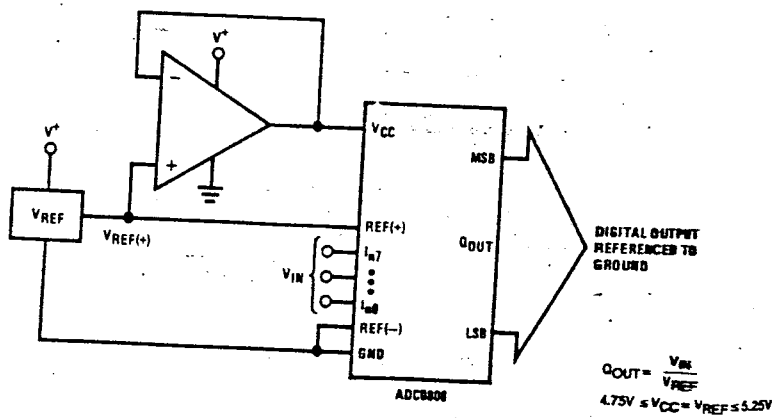


FIGURE 11. Ground Referenced Conversion System with Reference Generating V_{CC} Supply

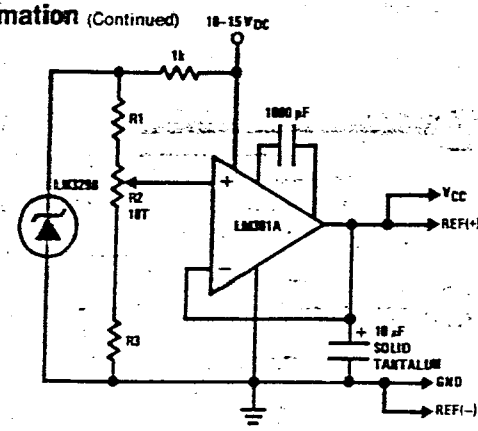


FIGURE 12. Typical Reference and Supply Circuit

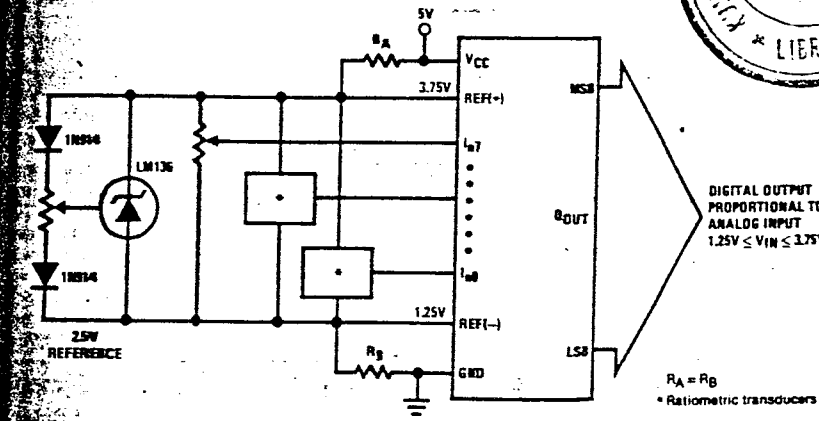


FIGURE 13. Symmetrically Centered Reference

...rter Equations

...ition between adjacent codes N and N+1 is

$$\left|(V_{REF(+)} - V_{REF(-)})\left[\frac{N}{256} + \frac{1}{512}\right] \pm V_{TUE}\right| + V_{REF(-)} \quad (2)$$

...e of an output code N is given by:

$$\left|(V_{REF(+)} - V_{REF(-)})\left[\frac{N}{256}\right] \pm V_{TUE}\right| + V_{REF(-)} \quad (3)$$

...ut code N for an arbitrary input are the integers ...the range:

$$\frac{V_{IN} - V_{REF(-)}}{V_{REF(+)} - V_{REF(-)}} \times 256 \pm \text{Absolute Accuracy} \quad (4)$$

V_{IN} = Voltage at comparator input
$V_{REF(+)}$ = Voltage at Ref(+)
$V_{REF(-)}$ = Voltage at Ref(−)
V_{TUE} = Total unadjusted error voltage (typically $V_{REF(+)} \div 512$)

4.0 Analog Comparator Inputs

The dynamic comparator input current is caused by the periodic switching of on-chip stray capacitances. These are connected alternately to the output of the resistor ladder/switch tree network and to the comparator input as part of the operation of the chopper stabilized comparator.

The average value of the comparator input current varies directly with clock frequency and with V_{IN} as shown in *Figure 6*.

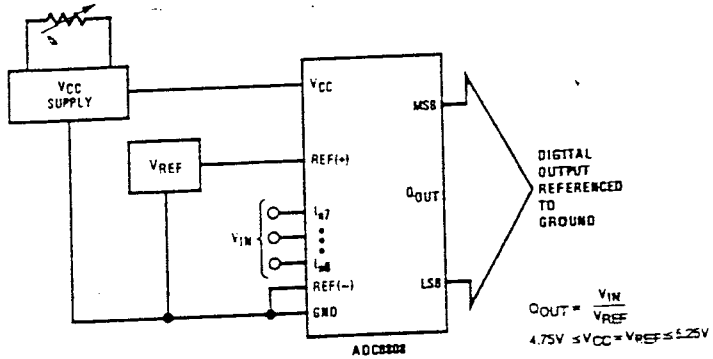
If no filter capacitors are used at the analog inputs and the signal source impedances are low, the comparator input current should not introduce converter errors, as the transient created by the capacitance discharge will die out before the comparator output is strobed.

If input filter capacitors are desired for noise reduction and signal conditioning they will tend to average out the dynamic comparator input current. It will then take on the characteristics of a DC bias current whose effect can be predicted conventionally.

Applications Information (Continued)

The ADC0808 needs less than a milliamp of supply current so developing the supply from the reference is readily accomplished. In *Figure 11* a ground referenced system is shown which generates the supply from the reference. The buffer shown can be an op amp of sufficient drive to supply the milliamp of supply current and the desired bus drive, or if a capacitive bus is driven by the outputs a large capacitor will supply the transient supply current as seen in *Figure 12*. The LM301 is overcompensated to insure stability when loaded by the 10 μF output capacitor.

The top and bottom ladder voltages cannot exceed V_{CC} and ground, respectively, but they can be symmetrical to less than V_{CC} and greater than ground. The center of the ladder voltage should always be near the center of the supply. The sensitivity of the converter can be increased (i.e., size of the LSB steps decreased) by using a symmetrical reference system. In *Figure 13*, a 2.5V reference is symmetrically centered about $V_{CC}/2$ since the same current flows in identical resistors. This system with a 2.5V reference allows the LSB bit to be half the size of a 5V reference system.



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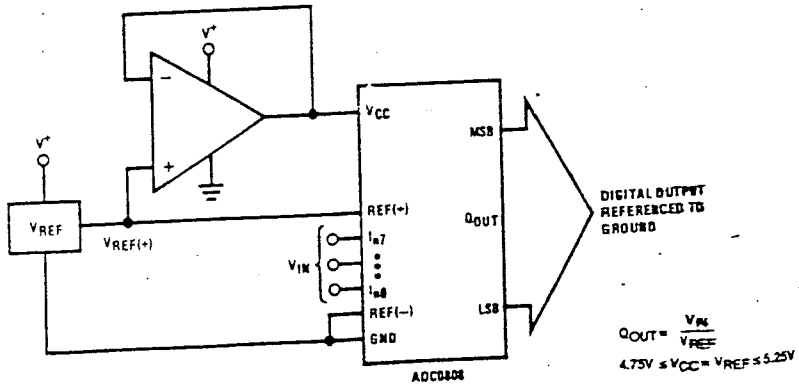
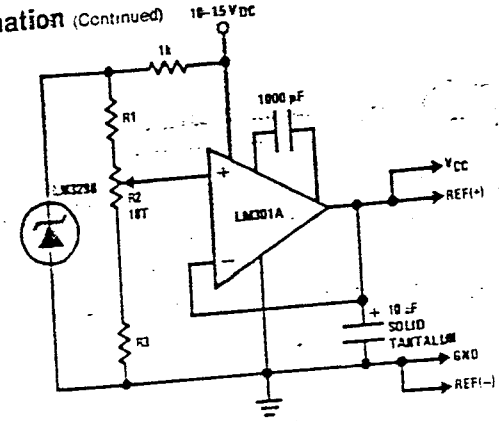


FIGURE 11. Ground Referenced Conversion System with Reference Generating V_{CC} Supply

...ons Information (Continued)



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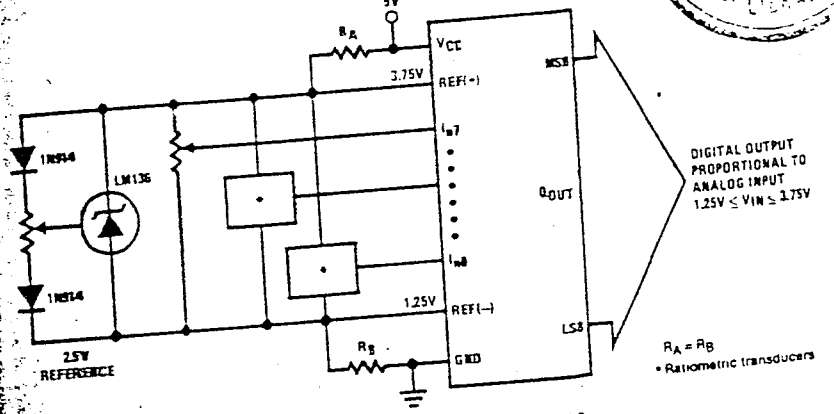

FIGURE 13. Symmetrically Centered Reference

...ll Converter Equations

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$$V_{IN} = (V_{REF(+)} - V_{REF(-)})\left[\frac{N}{256} + \frac{1}{512}\right] \pm V_{TUE} + V_{REF(-)} \quad (2)$$

The center of an output code N is given by:

$$V_{IN} = (V_{REF(+)} - V_{REF(-)})\left[\frac{N}{256}\right] \pm V_{TUE} + V_{REF(-)} \quad (3)$$

The output code N for an arbitrary input are the integers within the range:

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where:

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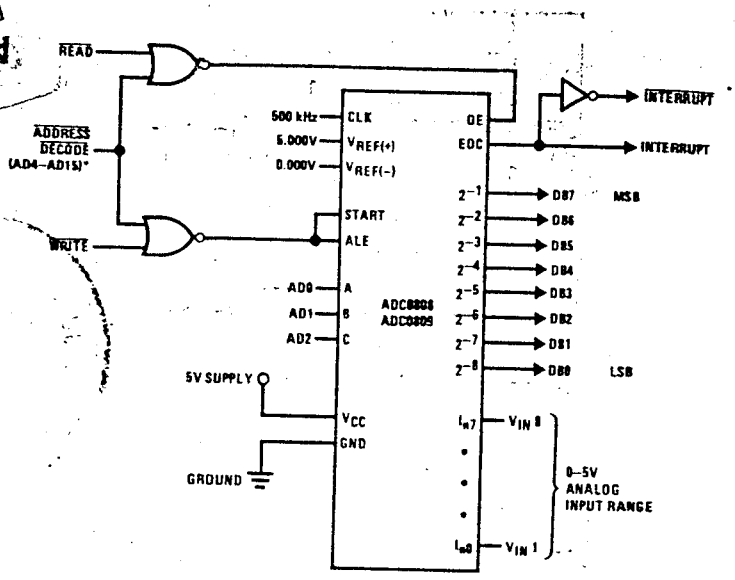
If input filter capacitors are desired for noise reduction and signal conditioning they will tend to average out the dynamic comparator input current. It will then take on the characteristics of a DC bias current whose effect can be predicted conventionally.

Application



* Address latches needed for 8085 and SC/MP interfacing the ADC0808 to a microprocessor

MICROPROCESSOR INTERFACE TABLE

PROCESSOR	$\overline{RD}$	$\overline{WRITE}$	INTERRUPT (COMMENT)
8080	$\overline{MEMR}$	$\overline{MEMW}$	INTR (Thru RST Circuit)
8085	$\overline{RD}$	$\overline{WR}$	INTR (Thru RST Circuit)
Z-80	$\overline{RD}$	$\overline{WR}$	$\overline{INT}$ (Thru RST Circuit, Mode 0)
SC/MP	NRDS	NWDS	SA (Thru Sense A)
6800	VMA·Φ2·R/W	VMA·Φ2·$\overline{R/W}$	$\overline{IRQA}$ or $\overline{IRQB}$ (Thru PIA)

Ordering Information

TEMPERATURE RANGE		−40°C to +85°C		−55°C to +125°C
Error	±1/2 Bit Unadjusted	ADC0808CCN	ADC0808CCJ	ADC0808CJ
	±1 Bit Unadjusted	ADC0809CCN		
Package Outline		N28A Molded DIP	J28A Hermetic DIP	J28A Hermetic DIP

National Semiconductor

Industrial Blocks

LM555/LM555C Timer

General Description

The LM555 is a highly stable device for generating accurate time delays or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and duty cycle are accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output circuit can source or sink up to 200 mA or drive TTL circuits.

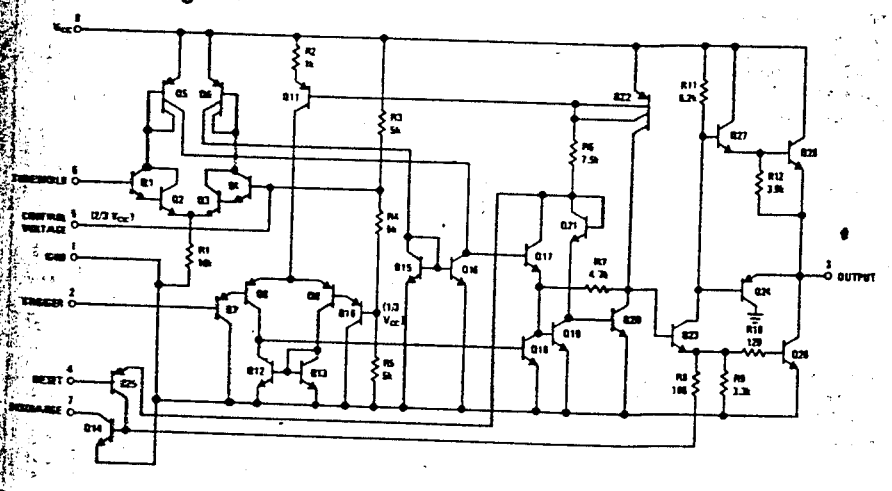
Features

- Direct replacement for SE555/NE555
- Timing from microseconds through hours
- Operates in both astable and monostable modes
- Adjustable duty cycle
- Output can source or sink 200 mA
- Output and supply TTL compatible
- Temperature stability better than 0.005% per °C
- Normally on and normally off output

Applications

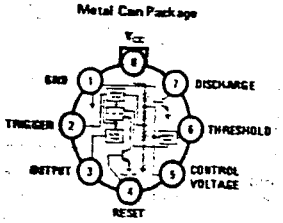
- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Linear ramp generator

Schematic Diagram



Connection Diagrams

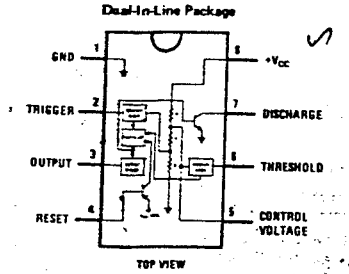
Metal Can Package



TOP VIEW

Order Number LM555H, LM555CH

Dual-In-Line Package



TOP VIEW

Order Number LM555CN
See NS Package N08B
Order Number LM555J or LM555CJ
See NS Package J08A

9

Supply Voltage	+18V
Power Dissipation (Note 1)	600 mW
Operating Temperature Ranges	
LM555C	0°C to +70°C
LM555	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics (T_A = 25°C, V_{CC} = +5V to +15V, unless otherwise specified)

PARAMETER	CONDITIONS	LIMITS						UNITS
		LM555			LM555C			
		MIN	TYP	MAX	MIN	TYP	MAX	
Supply Voltage		4.5		18	4.5		16	V
Supply Current	V_{CC} = 5V, R_L = ∞		3	5		3	6	mA
	V_{CC} = 15V, R_L = ∞ (Low State) (Note 2)		10	12		10	15	mA
Timing Error, Monostable								
Initial Accuracy			0.5			1		%
Drift with Temperature	R_A, R_B = 1k to 100 k, C = 0.1μF, (Note 3)		30			50		ppm/°C
Accuracy over Temperature			1.5			2.5		%
Drift with Supply			0.05			0.1		%/V
Timing Error, Astable								
Initial Accuracy			1.5			2.25		%
Drift with Temperature			90			150		ppm/°C
Accuracy over Temperature			2.5			3.0		%
Drift with Supply			0.15			0.30		%/V
Threshold Voltage			0.667			0.667		x V_{CC}
Trigger Voltage	V_{CC} = 15V	4.8	5	5.2		5		V
	V_{CC} = 5V	1.45	1.67	1.9		1.67		V
Trigger Current			0.01	0.5		0.5	0.9	μA
Reset Voltage		0.4	0.5	1	0.4	0.5	1	V
Reset Current			0.1	0.4		0.1	0.4	mA
Threshold Current	(Note 4)		0.1	0.25		0.1	0.25	μA
Control Voltage Level	V_{CC} = 15V	9.6	10	10.4	9	10	11	V
	V_{CC} = 5V	2.9	3.33	3.8	2.6	3.33	4	V
Pin 7 Leakage Output High			1	100		1	100	nA
Pin 7 Sat (Note 5)								
Output Low	V_{CC} = 15V, I_7 = 15 mA		150			180		mV
Output Low	V_{CC} = 4.5V, I_7 = 4.5 mA		70	100		80	200	mV
Output Voltage Drop (Low)	V_{CC} = 15V							
	I_{SINK} = 10 mA		0.1	0.15		0.1	0.25	V
	I_{SINK} = 50 mA		0.4	0.5		0.4	0.75	V
	I_{SINK} = 100 mA		2	2.2		2	2.5	V
	I_{SINK} = 200 mA		2.5			2.5		V
	V_{CC} = 5V							
	I_{SINK} = 8 mA		0.1	0.25				V
	I_{SINK} = 5 mA					0.25	0.35	V
Output Voltage Drop (High)	I_{SOURCE} = 200 mA, V_{CC} = 15V		12.5			12.5		V
	I_{SOURCE} = 100 mA, V_{CC} = 15V	13	13.3			13.3		V
	V_{CC} = 5V	3	3.3		12.75	3.3		V
Rise Time of Output			100		2.75	180		ns
Fall Time of Output			100			180		ns

Note 1: For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of +45°C/W junction to case for TO-5 and +150°C/W junction to ambient for both packages.

Note 2: Supply current when output high typically 1 mA less at V_{CC} = 5V.

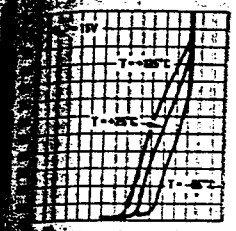
Note 3: Tested at V_{CC} = 5V and V_{CC} = 15V.

Note 4: This will determine the maximum value of $R_A + R_B$ for 15V operation. The maximum total ($R_A + R_B$) is 20 MΩ.

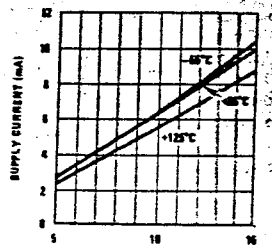
Note 5: No protection against excessive pin 7 current is necessary providing the package dissipation rating will not be exceeded.

Performance Characteristics

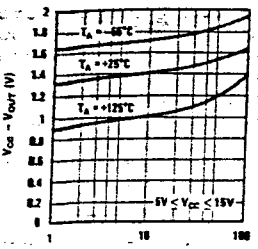
Minimum Pulse Width required for Triggering



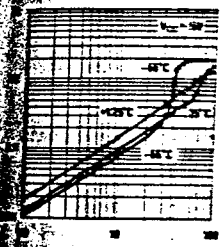
Supply Current vs Supply Voltage



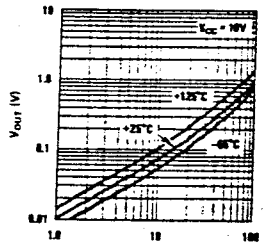
High Output Voltage vs Output Source Current



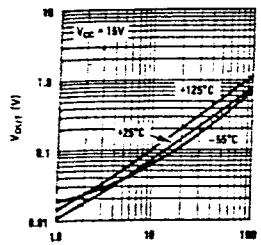
Low Output Voltage vs Output Sink Current



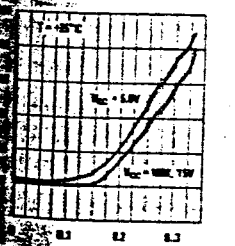
Low Output Voltage vs Output Sink Current



Low Output Voltage vs Output Sink Current



Output Propagation Delay vs Voltage Level of Trigger Pulse



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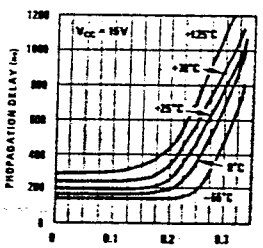
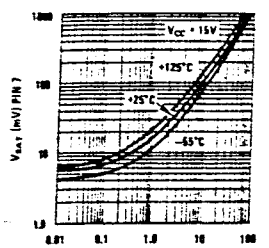
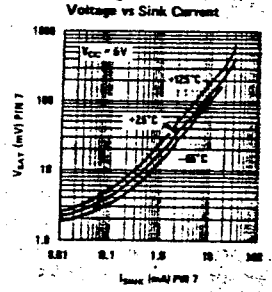


Discharge Transistor (Pin 7) Voltage vs Sink Current



Discharge Transistor (Pin 7) Voltage vs Sink Current



Applications Information

MONOSTABLE OPERATION

In this mode of operation, the timer functions as a one-shot (*Figure 1*). The external capacitor is initially held discharged by a transistor inside the timer. Upon application of a negative trigger pulse of less than 1/3 V_{CC} to pin 2, the flip-flop is set which both releases the short circuit across the capacitor and drives the output high.

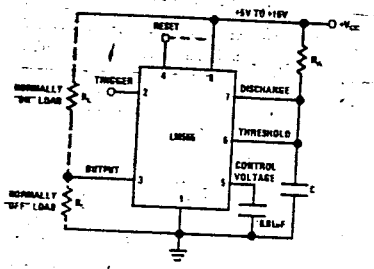


FIGURE 1. Monostable

The voltage across the capacitor then increases exponentially for a period of $t = 1.1\ R_A C$, at the end of which time the voltage equals 2/3 V_{CC}. The comparator then resets the flip-flop which in turn discharges the capacitor and drives the output to its low state. *Figure 2* shows the waveforms generated in this mode of operation. Since the charge and the threshold level of the comparator are both directly proportional to supply voltage, the timing internal is independent of supply.

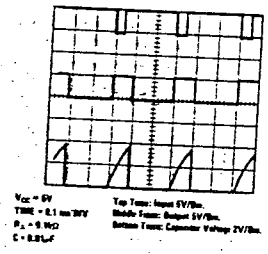


FIGURE 2. Monostable Waveforms

During the timing cycle when the output is high, the further application of a trigger pulse will not effect the circuit. However the circuit can be reset during this time by the application of a negative pulse to the reset terminal (pin 4). The output will then remain in the low state until a trigger pulse is again applied.

When the reset function is not in use, it is recommended that it be connected to V_{CC} to avoid any possibility of false triggering.

Figure 3 is a nomograph for easy determination of R, C values for various time delays.

NOTE: In monostable operation, the trigger should be driven high before the end of timing cycle.

ASTABLE OPERATION

If the circuit is connected as shown in *Figure 4* (pins 2 and 6 connected) it will trigger itself and free run as a multivibrator. The external capacitor charges through $R_A + R_B$ and discharges through R_B. Thus the duty cycle may be precisely set by the ratio of these two resistors.

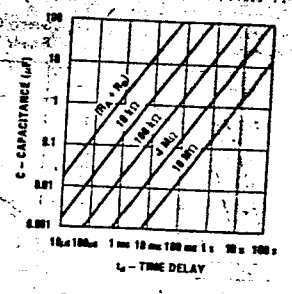


FIGURE 3. Time Delay

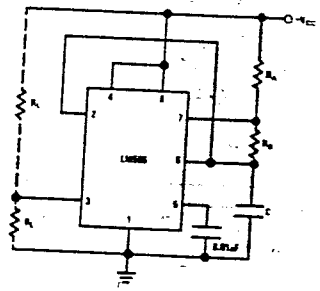


FIGURE 4. Astable

In this mode of operation, the capacitor charges and discharges between 1/3 V_{CC} and 2/3 V_{CC}. As in the triggered mode, the charge and discharge times, and therefore the frequency are independent of the supply voltage.

Figure 5 shows the waveforms generated in this mode of operation.

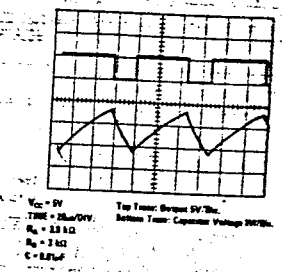


FIGURE 5. Astable Waveforms

The charge time (output high) is given by:

$$t_1 = 0.693\ (R_A + R_B)\ C$$

And the discharge time (output low) by:

$$t_2 = 0.693\ (R_B)\ C$$

Thus the total period is:

$$T = t_1 + t_2 = 0.693\ (R_A + 2R_B)\ C$$

Applications Information (Continued)

The frequency of oscillation is:

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B)\ C}$$

Figure 6 may be used for quick determination of these RC values.

The duty cycle is:

$$D = \frac{R_B}{R_A + 2R_B}$$

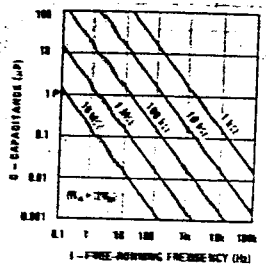


FIGURE 6. Free Running Frequency

FREQUENCY DIVIDER

The monostable circuit of *Figure 1* can be used as a frequency divider by adjusting the length of the timing cycle. *Figure 7* shows the waveforms generated in a divide by three circuit.

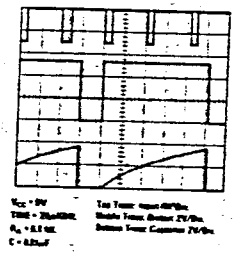


FIGURE 7. Frequency Divider

PULSE WIDTH MODULATOR

When the timer is connected in the monostable mode and triggered with a continuous pulse train, the output pulse width can be modulated by a signal applied to pin 5. *Figure 8* shows the circuit, and in *Figure 9* are some waveform examples.

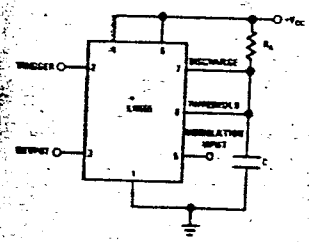


FIGURE 8. Pulse Width Modulator

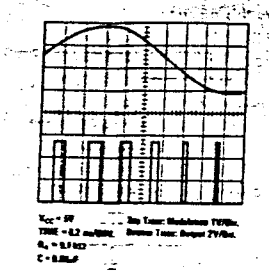


FIGURE 9. Pulse Width Modulator

PULSE POSITION MODULATOR

This application uses the timer connected for astable operation, as in *Figure 10*, with a modulating signal again applied to the control voltage terminal. The pulse position varies with the modulating signal, since the threshold voltage and hence the time delay is varied. *Figure 11* shows the waveforms generated for a triangle wave modulation signal.

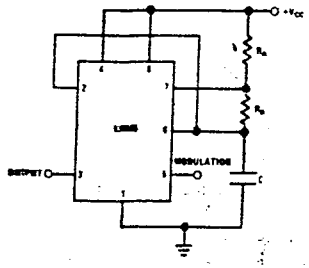


FIGURE 10. Pulse Position Modulator

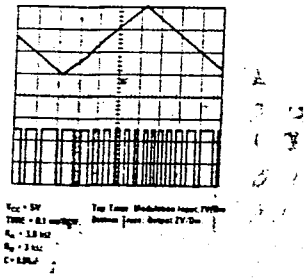


FIGURE 11. Pulse Position Modulator

LINEAR RAMP

When the pullup resistor, R_A, in the monostable circuit is replaced by a constant current source, a linear ramp is

Applications Information (Continued)

generated. *Figure 12* shows a circuit configuration that will perform this function.

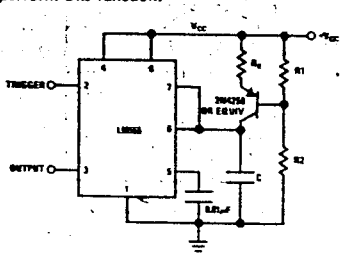


FIGURE 12.

Figure 13 shows waveforms generated by the linear ramp.

The time interval is given by:

$$T = \frac{2/3\ V_{CC}\ R_E\ (R_1 + R_2)\ C}{R_1\ V_{CC} - V_{BE}\ (R_1 + R_2)}$$

$V_{BE} \simeq 0.6V$

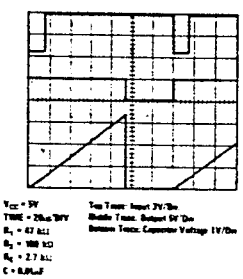


FIGURE 13. Linear Ramp

50% DUTY CYCLE OSCILLATOR

For a 50% duty cycle, the resistors R_A and R_B may be connected as in *Figure 14*. The time period for the output high is the same as previous, $t_1 = 0.693\ R_A\ C$. For the output low it is $t_2 =$

$$[(R_A\ R_B)/(R_A + R_B)]\ C \ln\left[\frac{R_B - 2R_A}{2R_B - R_A}\right]$$

Thus the frequency of oscillation is $f = \frac{1}{t_1 + t_2}$

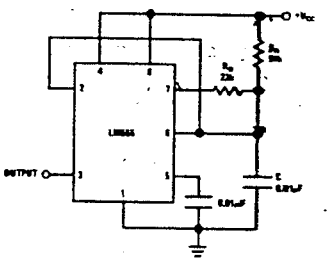


FIGURE 14. 50% Duty Cycle Oscillator

Note that this circuit will not oscillate if R_B is greater than 1/2 R_A because the junction of R_A and R_B cannot bring pin 2 down to 1/3 V_{CC} and trigger the lower comparator.

ADDITIONAL INFORMATION

Adequate power supply bypassing is necessary to protect associated circuitry. Minimum recommended is 0.1μF in parallel with 1μF electrolytic.

Lower comparator storage time can be as long as 10μs when pin 2 is driven fully to ground for triggering. This limits the monostable pulse width to 10μs minimum.

Delay time reset to output is 0.47μs typical. Minimum reset pulse width must be 0.3μs, typical.

Pin 7 current switches within 30 ns of the output (pin 3) voltage.

National Semiconductor

Operational Amplifiers/Buffers

LM741/LM741A/LM741C/LM741E Operational Amplifier

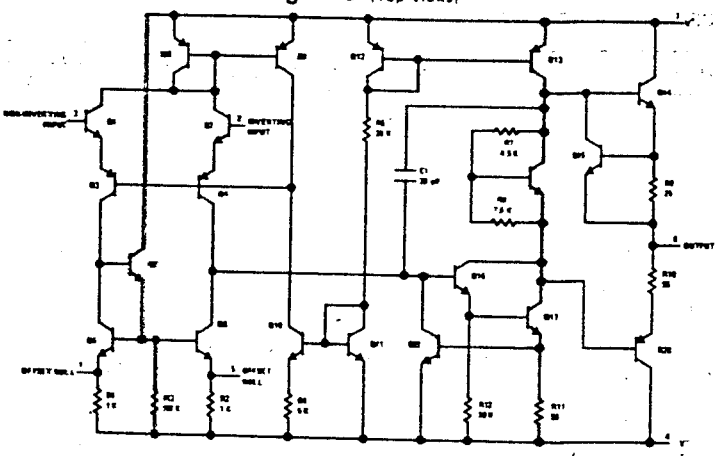
General Description

The LM741 series are general purpose operational amplifiers which feature improved performance over industry standards like the LM709. They are direct, plug-in replacements for the 709C, LM201, MC1439 and 748 in most applications.

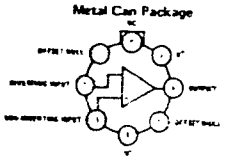
The amplifiers offer many features which make their application nearly foolproof: overload protection on the input and output, no latch-up when the common mode range is exceeded, as well as freedom from oscillations.

The LM741C/LM741E are identical to the LM741/LM741A except that the LM741C/LM741E have their performance guaranteed over a 0°C to +70°C temperature range, instead of −55°C to +125°C.

Schematic and Connection Diagrams (Top Views)

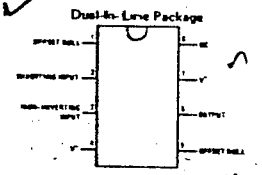


Metal Can Package



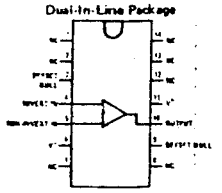
Order Number LM741H, LM741AH, LM741CH or LM741EH
See NS Package H08C

Dual-In-Line Package



Order Number LM741CN or LM741EN
See NS Package N08B
Order Number LM741CJ
See NS Package J08A

Dual-In-Line Package



Order Number LM741CN-14
See NS Package N14A
Order Number LM741J-14, LM741AJ-14 or LM741CJ-14

	LM741A	LM741E	LM741	LM741C
Supply Voltage	±22V	±22V	±22V	±18V
Power Dissipation (Note 1)	500 mW	500 mW	500 mW	500 mW
Differential Input Voltage	±30V	±30V	±30V	±30V
Input Voltage (Note 2)	±15V	±15V	±15V	±15V
Output Short Circuit Duration	Indefinite	Indefinite	Indefinite	Indefinite
Operating Temperature Range	−55°C to +125°C	0°C to +70°C	−55°C to +125°C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C	300°C	300°C	300°C

Electrical Characteristics (Note 3)

PARAMETER	CONDITIONS	LM741A/LM741E			LM741			LM741C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$T_A = 25°C$										
	$R_S \le 10\ k\Omega$					1.0	5.0		2.0	6.0	mV
	$R_S \le 50\Omega$		0.8	3.0							mV
	$T_{AMIN} \le T_A \le T_{AMAX}$										
	$R_S \le 50\Omega$			4.0							mV
	$R_S \le 10\ k\Omega$						6.0			7.5	mV
Average Input Offset Voltage Drift				15							µV/°C
Input Offset Voltage Adjustment Range	$T_A = 25°C$, $V_S = \pm 20V$	±10				±15			±15		mV
Input Offset Current	$T_A = 25°C$		3.0	30		20	200		20	200	nA
	$T_{AMIN} \le T_A \le T_{AMAX}$			70		85	500			300	nA
Average Input Offset Current Drift				0.5							nA/°C
Input Bias Current	$T_A = 25°C$		30	80		80	500		80	500	nA
	$T_{AMIN} \le T_A \le T_{AMAX}$			0.210			1.5			0.8	µA
Input Resistance	$T_A = 25°C$, $V_S = \pm 20V$	1.0	6.0		0.3	2.0		0.3	2.0		MΩ
	$T_{AMIN} \le T_A \le T_{AMAX}$, $V_S = \pm 20V$	0.5									MΩ
Input Voltage Range	$T_A = 25°C$										
	$T_{AMIN} \le T_A \le T_{AMAX}$				±12	±13		±12	±13		V
Large Signal Voltage Gain	$T_A = 25°C$, $R_L \ge 2\ k\Omega$										
	$V_S = \pm 20V$, $V_O = \pm 15V$	50									V/mV
	$V_S = \pm 15V$, $V_O = \pm 10V$				50	200		20	200		V/mV
	$T_{AMIN} \le T_A \le T_{AMAX}$, $R_L \ge 2\ k\Omega$,										
	$V_S = \pm 20V$, $V_O = \pm 15V$	32									V/mV
	$V_S = \pm 15V$, $V_O = \pm 10V$				25			15			V/mV
	$V_S = \pm 5V$, $V_O = \pm 2V$	10									V/mV
Output Voltage Swing	$V_S = \pm 20V$										
	$R_L \ge 10\ k\Omega$	±16									V
	$R_L \ge 2\ k\Omega$	±15									V
	$V_S = \pm 15V$										
	$R_L \ge 10\ k\Omega$				±12	±14		±12	±14		V
	$R_L \ge 2\ k\Omega$				±10	±13		±10	±13		V
Output Short Circuit Current	$T_A = 25°C$	10	25	35		25			25		mA
	$T_{AMIN} \le T_A \le T_{AMAX}$	10		40							mA
Common-Mode Rejection Ratio	$T_{AMIN} \le T_A \le T_{AMAX}$										
	$R_S \le 10\ k\Omega$, $V_{CM} = \pm 12V$				70	90		70	90		dB
	$R_S \le 50\ k\Omega$, $V_{CM} = \pm 12V$	80	95								dB

Electrical Characteristics (Continued)

PARAMETER	CONDITIONS	LM741A/LM741E			LM741			LM741C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Supply Voltage Rejection	$T_{AMIN} \le T_A \le T_{AMAX}$,										
	$V_S = \pm 20V$ to $V_S = \pm 5V$										
	$R_S \le 50\Omega$	86	96								dB
	$R_S \le 10\ k\Omega$				77	96		77	96		dB
Transient Response	$T_A = 25°C$, Unity Gain										
Rise Time			0.25	0.8		0.3			0.3		µs
Overshoot			6.0	20		5			5		%
Bandwidth (Note 4)	$T_A = 25°C$	0.437	1.5								MHz
Slew Rate	$T_A = 25°C$, Unity Gain	0.3	0.7			0.5			0.5		V/µs
Supply Current	$T_A = 25°C$					1.7	2.8		1.7	2.8	mA
Power Consumption	$T_A = 25°C$										
	$V_S = \pm 20V$		80	150							mW
LM741A	$V_S = \pm 15V$					50	85		50	85	mW
	$V_S = \pm 20V$										
	$T_A = T_{AMIN}$			165							mW
	$T_A = T_{AMAX}$			135							mW
LM741E	$V_S = \pm 20V$			150							mW
	$T_A = T_{AMIN}$			150							mW
	$T_A = T_{AMAX}$			150							mW
LM741	$V_S = \pm 15V$										
	$T_A = T_{AMIN}$					60	100				mW
	$T_A = T_{AMAX}$					45	75				mW

Note 1: The maximum junction temperature of the LM741/LM741A is 150°C, while that of the LM741C/LM741E is 100°C. For operation at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W junction to case. The thermal resistance of the dual-in-line package is 100°C/W junction to ambient.

Note 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 3: Unless otherwise specified, these specifications apply for $V_S = \pm 15V$, $-55°C \le T_A \le +125°C$ (LM741/LM741A). For the LM741C/LM741E, these specifications are limited to $0°C \le T_A \le +70°C$.

Note 4: Calculated value from: BW (MHz) = 0.35/Rise Time(µs).

Control word for 8255 Processor