Operator Console-An FPGA Approach with 'Scroll and Dial'

A Project Report
Submitted In partial fulfilment of the requirements
for the award of the Degree of
BACHELOR OF ENGINEERING IN
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of the Bharathiar University Coimbatore.

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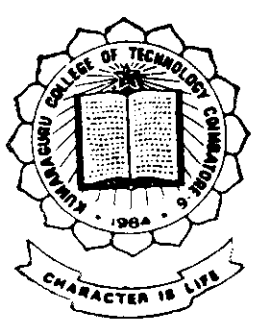

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of Kumaraguru College of Technology, Coimbatore have completed the project entitled '***OPERATOR CONSOLE - AN FPGA APPROACH WITH SCROLL AND DIAL***' at BPL Telecom Ltd during August '97 - March '98.

Their performance during the period was found to be Excellent. We wish them all success.

Place : Palakkad
Date : 31/03/98

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P-1342

We are extremely thankful to **Mr. R. G. K. PAI ,** **Asst. General Manager-R & D, BPL Telecom Ltd** *for having extended his kind cooperation and for having provided us all the facilities.*

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Last but not the least we thank all the faculty members and our friends for their help and support.

CONTENTS

SYNOPSIS

The designed Operator console incorporates Field Programmable Gate Arrays in its hardware design. Several discrete logic circuits have been integrated into a single chip, conserving hardware space , reducing the cost and improving the design flexibility. The Operator console is designed to work with a DPL designed EPABX by name PRODIGY.

The console operation is controlled by the 8031 micro-controller interfaced to external program and data memories. It communicates with the exchange through a RS-232 C interface. The status of the trunk and extension lines are indicated by LEDs placed beside their respective keys.

The console , apart from the normal features, presents the special features viz Conferencing, Serial call, Day/Night option, Call parking and a Fax port controlled by software written into the program memory. Apart from these, a LCD module has been interfaced to the console to provide a visual aid for the operator.

The normal LCD operation indicates the number dialed and displays a message when on-hook. The LCD, in specially programmed modes, can be used to Store, Search, Scroll and Dial. This provides the user with a digital memory to store up to 1000 numbers along with some additional information. The retrieval of these data is done by a 'Search and Scroll' software written into the micro-controller program memory. The number displayed in the LCD screen can, then, be dialed with a single touch option.

INTRODUCTION

" THE OLD ORDER CHANGETH
GIVING WAY TO THE NEW "

These very words of Lord Tennyson epitomises the present trend in the Telecommunications market. Gone are the days of bulky multimodular design . The advancements in Integration technology have given the designer a powerful tool for a fast and compact time-to-market solution with more user friendly features. Our project is a small step towards realising the advantages provided by the state-of-the-art technology.

The value-savvy user of today is swamped with products competing in technology, features and cost. The Operator Console - the sought after user-friendly equipment in any Private Exchange - that we have designed, is precisely aimed to satisfy the evergrowing needs of the modern user.

The user needs have framed our design objectives as

- Compactness
- Cost effectiveness
- Special Features
- Ease of use

The Multimodular design was upgraded to a single chip solution using the FPGA. Several Logical circuits were integrated on to a single chip using this technique. Then the basic console operations aside, several features for monitoring and controlling were crypted and wired. Besides the console was incorporated with an LCD module and sophisticated features like Store, Search and

Scroll were added through software to improve the user friendliness .

This report gives you a brief overview of the role of consoles followed by the detailed hardware description. Apart from the general interfacing details, a detailed section on FPGA and the circuits inside is provided. The LCD interfacing is dealt with in the next section followed by the Flowcharts and explanations on the software of the module.

OPERATOR CONSOLE - THE PRESENT AND THE FUTURE.

Necessity drives invention.

Resource handling is a key area of management to increase the efficacy and efficiency of the operation carried on. In communication parlance, this accounts to handling the available resources by constant and indicative management. Limited resources can be handled manually or by simple machines. But when it comes to industrial environment, the usage of the available resources is quite large and the task of monitoring becomes complex. Added to this is the onus of providing many features that could assist in eliminating much of the practical problems.

In this scenario enters the operator console - the trusted watch-dog and an intelligent slave that reduces the burden on its master. With the available high-speed electronic circuitry, it is possible to monitor many lines on a time division basis, without any loss of generality. Combined with this is the advantage that the information provided by this circuitry can be used to make electronic decisions , taking into account the user's choice and the status of the resources available. These decisions, when properly interpreted and integrated could improve the overall scenario of communication by providing many or all of the features the user could wish for.

The Present:

The present day operator consoles are equipped with rigid hardware, mostly in modules and hence less flexible in both hardware and software. Though they provide many features sought-for by the user, it still takes quite an amount of work from the user's side to store and retrieve the required information, mostly without any visual aid. Even if some visual aid is supported, it doesn't serve

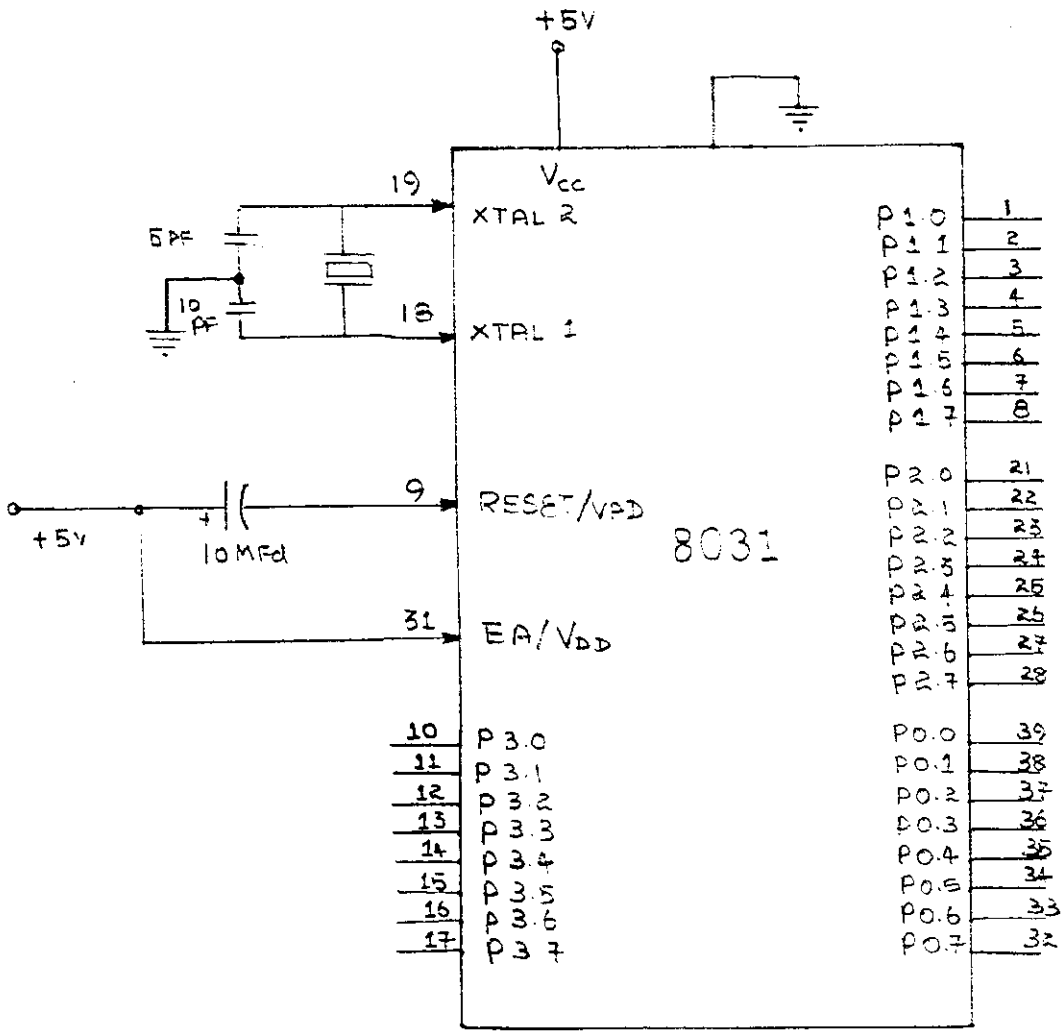
any purpose other than checking the numbers dialed or displaying date and time.

These visual aids can be exploited a little more in improving user-friendliness and the approach could be utilized as a stepping stone to design the intelligent console of the future.

The Future:

The present trend can be extended to have Operator consoles with a greater degree of intelligence incorporating Voice - recognized Search, Scroll and Dial, Automatic timed redial and callback and so on.

Our design is a step towards achieving the required degree of intelligence expected from an Operator console.



PIN DIAGRAM OF 8031 MICROCONTROLLER

FIG 3.0

8031 MICRO-CONTROLLER

FEATURES :

The designed Operator console uses a 8031 micro-controller as the heart of its operations. The said micro-controller was chosen based on the following features :

- 8-bit CPU
- 128 bytes of on-chip RAM
- 21 special function registers
- 32 I/O lines
- 64K address space for external program memory
- Two 16-bit timer/counter
- A 5 source interrupt structure with 2 priority levels
- Full duplex serial port
- Bit addressability for Boolean processing

INTERRUPTS :

The 8031 provides 5 interrupt sources each of which can be programmed to one of the two priority levels. The 5 interrupt sources are listed below

Source	**Description**
INT 0	External request from P3.2 pin
Timer 0	Overflow from Timer 0 activates interrupt request flag TFO
INT 1	External request from P3.3 pin
Timer 1	Overflow from Timer 1 activates interrupt request flag TF1
Serial port	Completion of transmission or reception of one signal frame activates request flag TF1 or R1

PIN DESCRIPTION :

Vss : Circuit ground potential

Vcc: Supply voltage during programming, verification and normal operation.

Port 0 : Port 0 is an 8-bit open drain bidirectional I/O port. It is also the multiplexed low order address and data bus during access to external memory. It also outputs instruction bytes during program verification. Port 0 can sink 8 LS -TTL inputs.

Port 1: Port 1 is an 8-bit bidirectional I/O port with internal pullups. It receives the lower order address byte during program verification. Port 1 can sink/source 3 LS-TTL inputs. It can drive MOS inputs without external pullups.

Port 2: Port 2 is an 8-bit directional I/O port with internal pullups. It emits the higher order address byte during accesses to external memory. It also receives the higher order address byte and control signals during program verification. Port 2 can sink/ source 3 LS-TTL inputs. It can drive MOS inputs without external pullups.

Port 3 : Port 3 is an 8-bit bidirectional I/O port with internal pullups. It also serves the functions of various special features of the MCS-51 family as listed below

Port pin	**Alternate function**
P 3.0	RXD(Serial input port)
P 3.1	TXD(Serial output port)
P 3.2	INT0(External interrupt)
P 3.3	INT1(External interrupt)

P 3.4	T0(Timer0 External input)
P 3.5	T1(Timer1 External input)
P 3.6	WR(External data memory write strobe)
P3.7	RD(External data memory read strobe)

Port 3 can sink/source 3LS-TTL inputs. It can drive MOS inputs without external pullups.

RST/VPD : A high level on this pin for 2 machine cycles while the oscillator is running resets the device. An internal pulldown permits power-on reset using only a capacitor connected to Vcc.

ALE/PROG : Address Latch Enable output for latching the lower byte if the address during accesses to external memory. ALE can also be used for external clocking or timing purposes. This pin is also a program pulse input during EPROM programming.

PSEN : Program Store Enable output is the read strobe for external program memory . PSEN is activated twice each machine cycle during fetches from external program memory. PSEN is not activated during fetches from internal program memory.

EA: When EA is held high the CPU executes out of internal program memory. When EA is held low the CPU executes out of external program memory. In the 8031, EA must be externally wired low.

XTAL1: Input to the inverting amplifier that forms the oscillator . It should be grounded when an external oscillator is used.

XTAL2: Output of the inverting amplifier that forms the oscillator, and input to the internal clock generator. It receives the external oscillator signal when an external oscillator is used.

PORT BIT ASSIGNMENT :

Port 0 :

P0.0 - P0.7 : Multiplexed Address/ Data Bus AD0-AD7

Port 1 :

P1.0 : LOOP
P1.1 : MUTE
P1.2 : H/S VOL1
P1.3 : H/S VOL2
P1.4 : H/M VOL1
P1.5 : H/M VOL2
P1.6 : SPK VOL1
P1.7 : SPK VOL2

Port 2:

P2.0-P2.7 : Higher order Address Bus A8-A15

Port3:

P3.0 : RX DATA
P3.1 : TX DATA
P3.2 : HF
P3.3 : ANTI LAR
P3.4 : IN S
P3.5 : H/F SPK CS

P3.6 : WRITE

P3.7 : READ

MEMORY ORGANISATION :

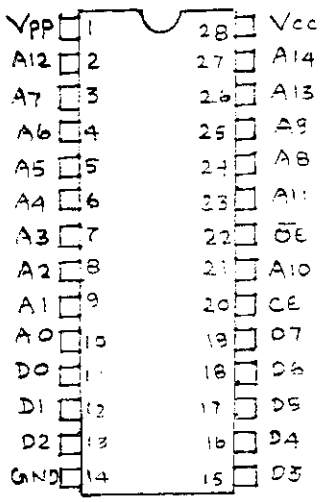
The 8031 maintains separate address spaces for program memory and data memory. The program memory can be up to 64KB long. The data memory consists of 128 bytes of on chip RAM, in addition to 21 Special Function Registers. The device is capable of accessing up to 64KB of external data memory.

The program memory uses 16-bit addresses. The external data memory can use either 8-bit or 16-bit addresses. The internal data memory uses 8-bit addresses, which provide a 256 location address space. The lower 128 addresses access the on-chip RAM. The special function registers occupy various locations in the upper 128 bytes of the same address space.

The lowest 32 bytes in the internal RAM are divided into four banks of registers, each bank consisting of 8 bytes. Any one of these banks can be selected to be the "working registers" of the CPU and can be accessed by a 3-bit address in the same byte as the opcode of an instruction.

The next higher 16 bytes of the internal RAM have individually addressable bits. These are provided for use as software flags or for 1 bit (Boolean) processing. This bit addressing capability is an important feature of the 8031. In addition to the 128 individually addressable bits in RAM, eleven of the special function registers also have individually addressable bits.

Pin Configuration Of IC 27256 EPROM



Pin Configuration Of IC6264 RAM

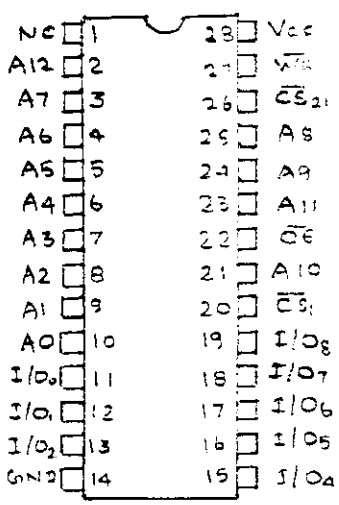


Fig 3.1

8031 INTERFACING WITH EXTERNAL PROGRAM AND DATA MEMORY

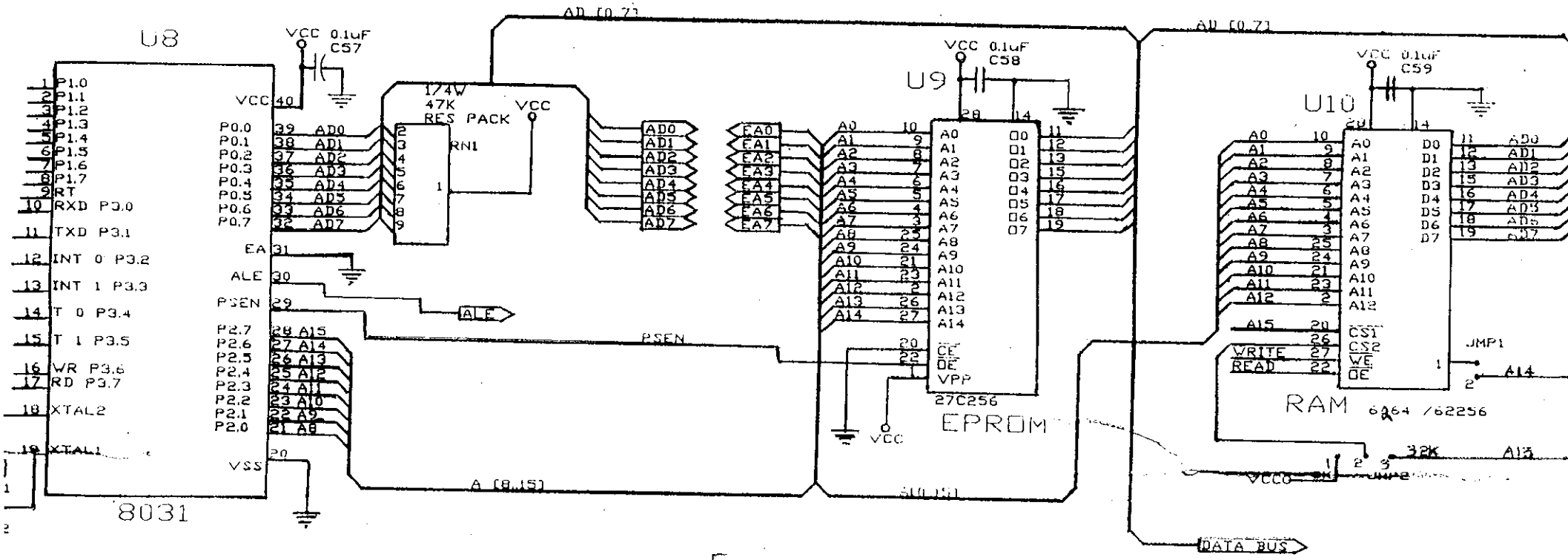


FIG. 3.2

8031 INTERFACING WITH EXTERNAL PROGRAM AND DATA MEMORY

Access to external memory is of two types : Access to external program memory and Access to external data memory. Access to external program memory the signal PSEN is used as the read strobe and to external data memory RD/WR is used as the strobe signal. Fetches from external program memory always uses a 16-bit address while to access the external data memory, either a 16-bit or an 8-bit address can be used.

The console is designed to work with a 32K external program memory (27C256) and a data memory(6264) with 8K or 32K memory space, depending on the user requirements it is shown in the figure 3.3. The pin diagrams of the program and data memories used are shown in figure 3.1.

The multiplexed address /data bus is fed into the FPGA chip for demultiplexing and the demultiplexed lower byte of address is taken out of it. The PSEN is connected to the EPROM Output Enable pin . The other enable pins are permanently enabled.

The WRITE and READ signals are provided to the RAM to enable respective operations. The Data Bus of EPROM, RAM are connected to the CPU data bus which is connected to Vcc via a 47K resistor pack. The data bus is also fed to the FPGA chip.

SERIAL PORT INTERFACE

The Serial Port of 8031 is full duplex. It consists of a serial buffer (SBUF) which is actually two separate registers. When data is moved to SBUF, it goes to the transmit buffer , where it is held for serial transmission. When data is moved from SBUF, it comes from the receiver buffer.

During serial reception, the incoming bits are checked into a separate shift register. When reception of a frame is complete and mandatory conditions satisfied, the received data bits are are transferred from the shift register to the receive buffer. The shift register is then ready to commence reception of a record frame, while the frame already received awaits servicing.

SERIAL PORT DATA REGISTERS :

In all serial modes a write to SBUF loads the same 9-bit shift register. The data byte goes into the first 8-bits, with the LSB at the output bit of the register. The write to SBUF also loads the 9^{th} bit of the shift register with either a 1 or TB8, depending on the mode, and it initializes the transmission.

The receive registers are an input shift register which is 8-bits wide in mode 0 and 9-bits wide in the other modes, plus SBUF itself, a read-only register which is loaded by the hardware with the data byte at the same time that R1 is activated. In the UART modes, the 9^{th} bit is loaded into RB8 in SCON at the same time that the data byte is loaded into SBUF. RB8 and SBUF are not changed if SM2 causes the received data to be ignored.

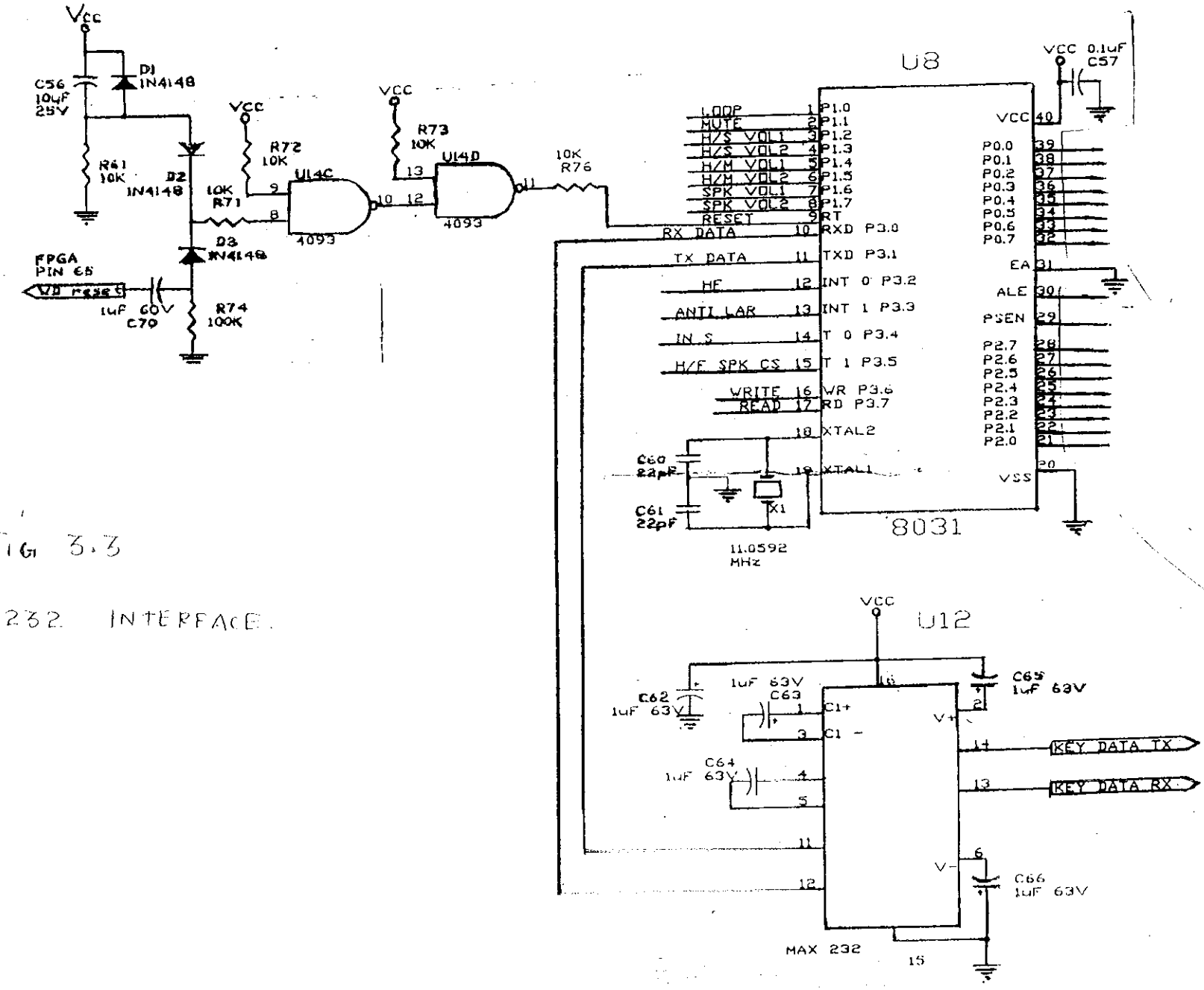


FIG 3.3

RS – 232 INTERFACE

RS-232 INTERFACE :

The data communication between the exchange and console is done through this circuit given in Fig 3.3.

The data to be transmitted from the console to the exchange is available at TXD pin of 8031. It is connected to T1in pin, a TTL/CMOS input of MAX232 IC. This signal will be available as an RS232 output at T1out of MAX232. T1out is connected to 25 pin D connector.

The signal coming through KEYDATA RX pins of 25 pin D connector are fed to R1in, one of the RS-232 input pins of MAX232. This will appear as a TTL/CMOS output at R1out pin.R1out is connected to RXD of 8031, from where the micro-controller will collect the data.

Capacitors C63, C64, C65 and C66 are part of charge pump voltage converters of U12 which converts +5V to +/-10V. The first charge pump voltage converter uses C63 to double +5V to +10V, storing the +10V on capacitor C65. The second charge pump voltage converter uses capacitor C64 to invert +10V to -10V, storing the -10V on capacitor C66. C62 is bypass capacitor.

RESET CIRCUITS

There are two reset circuits. Power-On Reset and Watchdog Reset also shown in Fig3.3 . The first one gives a reset to the system when it is switched ON. The second one gives reset when software goes out of control.

Power-On Reset :

The RC combination R61-C56 is used for Power-On Reset. Reset signal is taken across R61 and is active HIGH. The Schmitt

triggers(IC 4093) are used for conditioning the output of RC combination to a perfect pulse.

Watchdog Reset :

WD_RESET signal from FPGA is coming to an RC network consisting of C70 and R74. The voltage across R74 is the reset signal and is active HIGH. It is applied to a Schmitt trigger for conditioning.

The outputs from RC networks are connected to inputs of the Schmitt trigger through diodes D2 and D3. Thus a HIGH at the output of any of the reset circuits will make the input of Schmitt trigger HIGH. Hence pin9 of 8031 becomes HIGH. R72 and R73 are pullup resistors for the free ends of Schmitt triggers.

CIRCUITS IN FPGA

The following circuits where incorporated into the FPGA chip, the input and output lines of which are identified in the circuit diagram given in Fig.3.2.

- Address Latch
- Address Decoder
- Debounce Circuit with Buffered Outputs
- Multiplexed LED Drivers
- Tone Generator Circuit
- Watchdog Timer
- Clock Divider

The detailed description of the above mentioned circuit along with the circuit diagrams is given in the subsequent chapter.

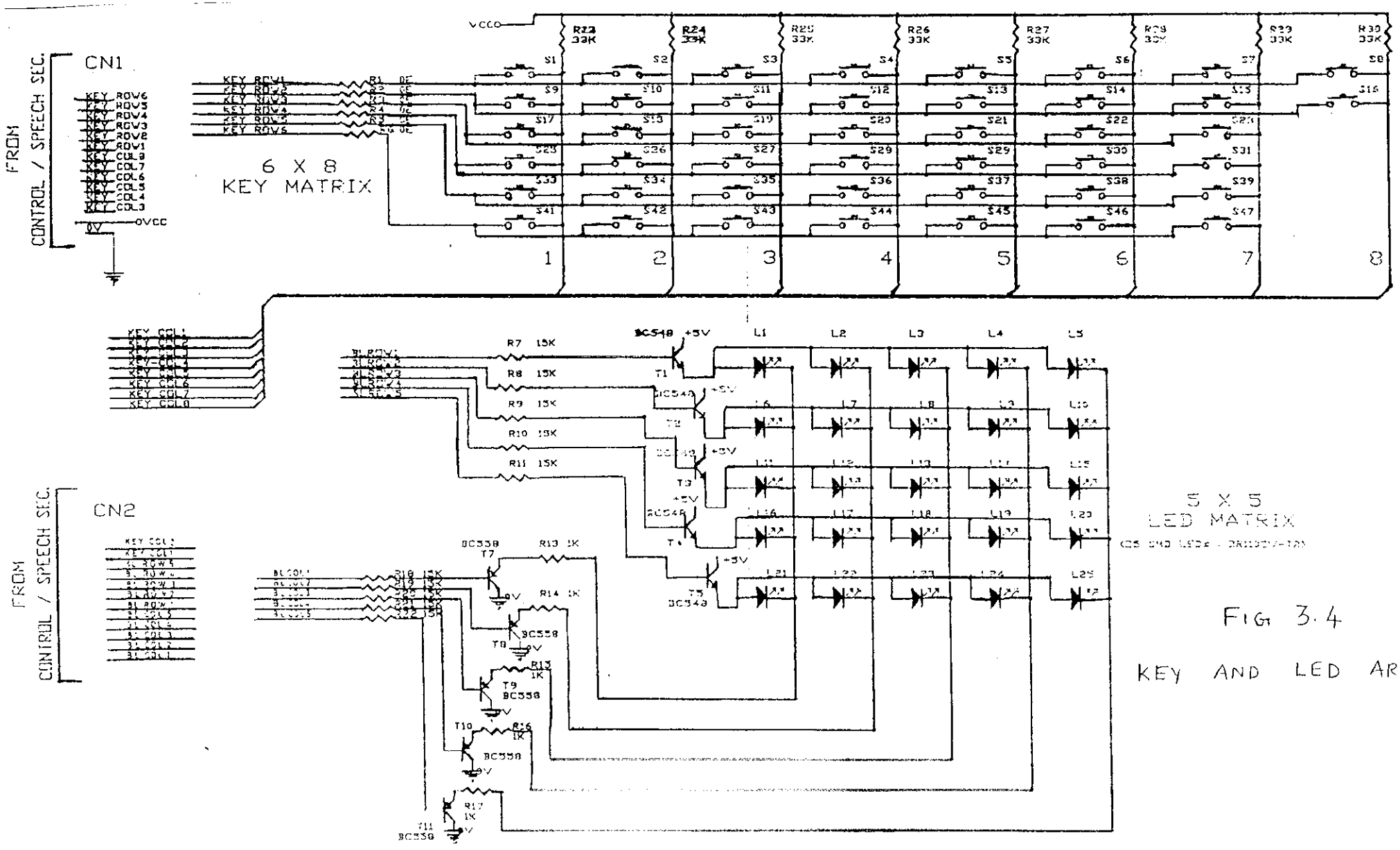


FIG 3.4

KEY AND LED ARRAY.

KEY AND LED ARRAYS

The circuit diagram of Key and LED arrays are shown in the Fig. 3.4.

KEY ARRAY :

The Total 44 keys are arranged into matrix with 6 rows and 8 columns, with eighth column having keys only in the first two rows.

One terminal each of all the keys in first column are tied together and fed with Vcc through resistor R23. This common point is taken out as KEY_ COL1 . Therefore KEY_COL1 is HIGH when keys are idle. The other point of each key in this column is takrn out as KEY_ROW1 to KEY_ROW6 and is also connected to corresponding points in other columns. The common point of keys in other columns are fed with Vcc through resistors R24 - R30 and is taken out as KEY_COL2 to KEY_COL8.

Using high speed scanning jey rows are fed with ground one by one. If (3,6) key is in the press state when row 3 is being scanned, the common point of the sixth column will become LOW Thus the code fed at KEY_ROW6 to KEY_ROW1 is 111011 and code read from KEY_COL8 to KEY_COL1 is 1101111. Using this information the micro-controller will detect the key which is pressed.

LED ARRAY :

25 LEDs are arranged in a 5 x 5 matrix. The cathodes of LEDs in each column are tied together and grounded through transistors T7 to T11. The anodes of LEDs in each are tied together and connected to +5V through switching transistors T1 to T5. The transistors T1 to T5 are controlled by signals BLROW1 to BLROW5. Transistors T7 to T11 are controlled by signals BLCOL1 to BLCOL5. If BLROW5 to BLROW1 is 00010 and BLCOL1 to

SPEECH COUPLING CIRCUIT

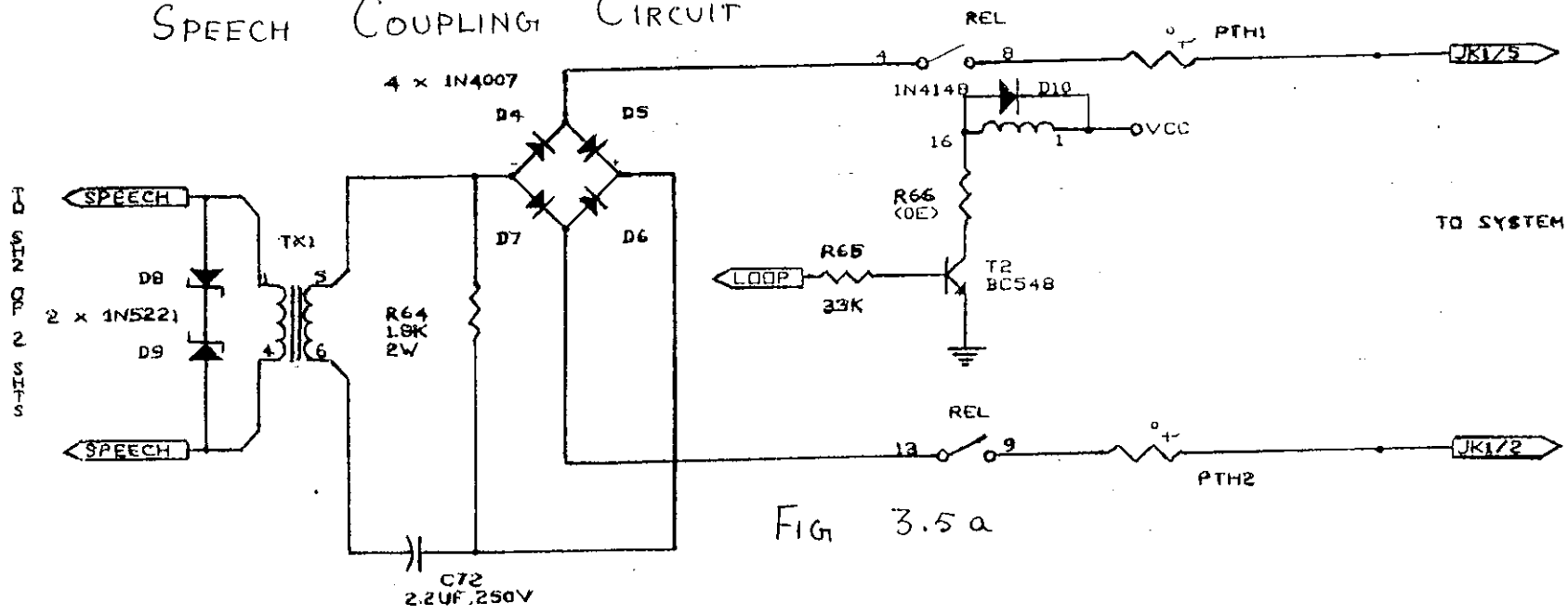


FIG 3.5a

12/5 VOLTAGE CONVERTER.

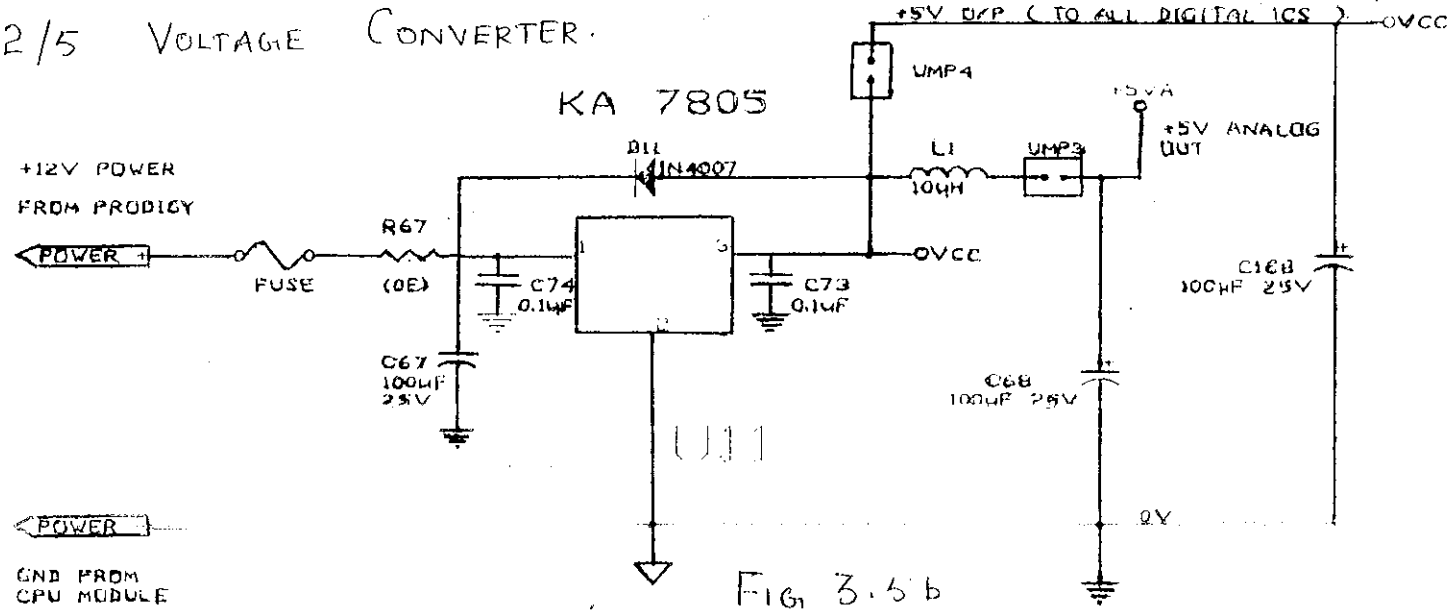


FIG 3.5b

BLCOL5 is 11110, then second row will get +5V and first column will get ground, hence L6 will glow.

BLROWn , BLCOLn, KEY_ROWn, and KEY_COLn are fed to the keyboard through cables and connectors (CN1 and CN2) from the control board. The first three are outputs from FPGA while KEY_COLn are inputs to the FPGA.

SPEECH COUPLING CIRCUIT

This circuit shown in Fig.3.5.a. couples the speech signals between the exchange and the speech processing circuit of the console. The speech signals from / to the exchange is coming through a jack JK1.

When handset is off-hooked the loop is offered by activating a relay REL. T2 is the driving transistor for the relay which is controlled

by the signal LOOP from P1.0 of 8031. Bridge rectifier comprising Diodes D4 - D7 is provided for loop offering independent of polarity. Resistor R64 is for offering DC to the loop. Matching transformer TX1 will pass only the speech signal, which is AC, to the speech processing circuit. Capacitor C72 will block most of the DC before it reaches the matching transformer . Zener diodes D8 and D9 will suppress any surges in speech part.

12 / 5 VOLTAGE CONVERTOR

This circuit shown in Fig 3.5b is for converting +12V supply to +5V. Separate supply is taken for digital and analog circuits. The +12V is fed to the console through a 25-pin connector from exchange.

The +12V from the exchange is coming through a fuse to the input of 7805. C67 and C74 are input filters. D11 is a protection

CONNECTORS

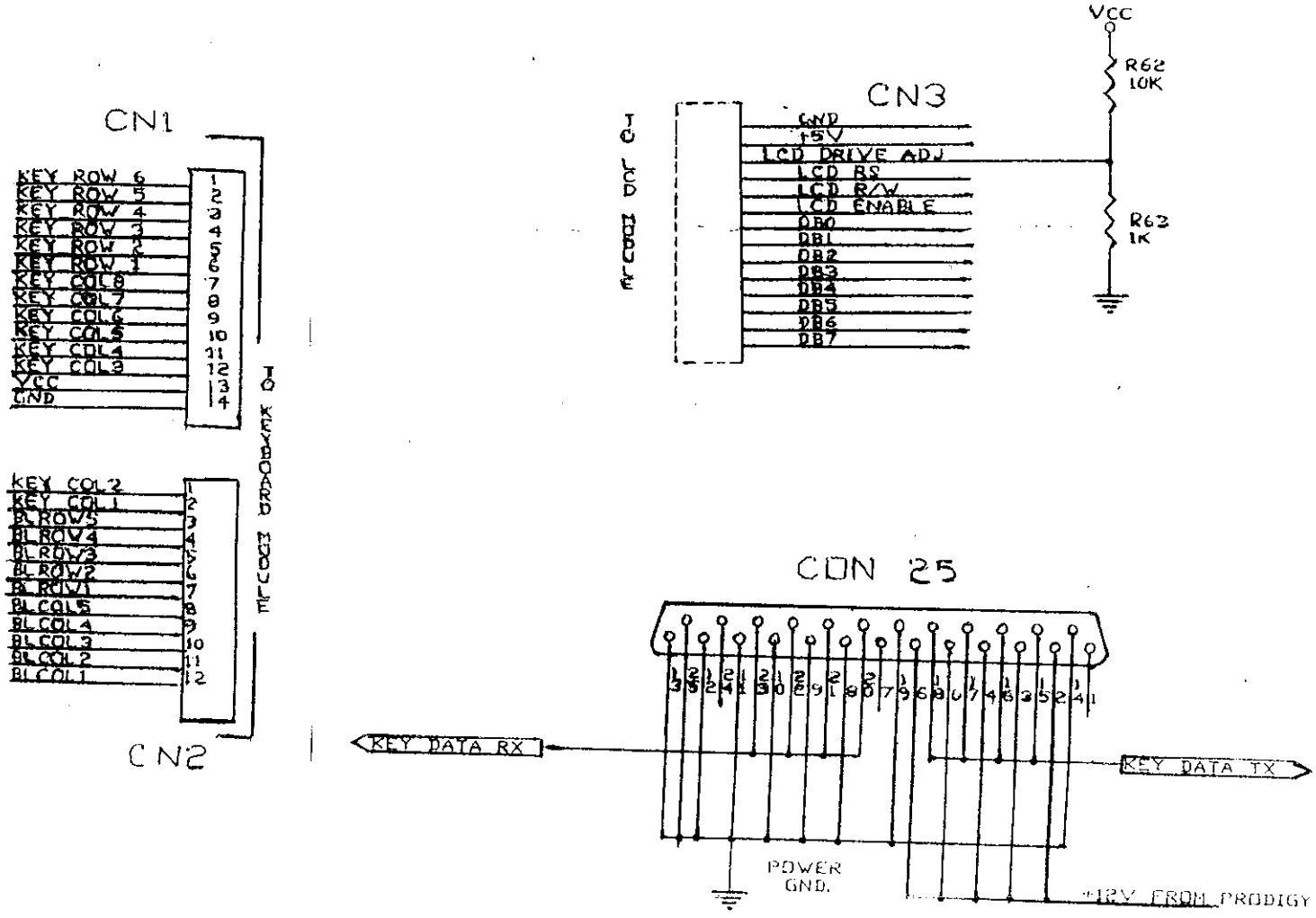


Fig 3.6

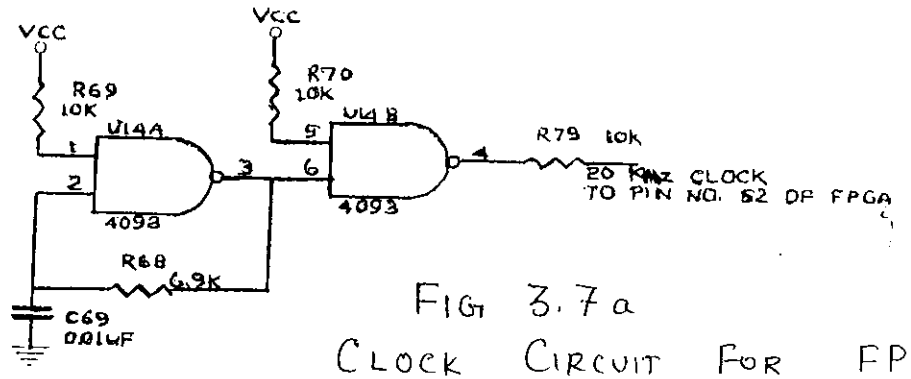
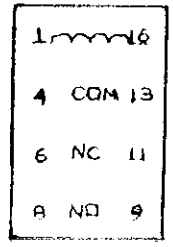


FIG 3.7a
CLOCK CIRCUIT FOR FPGA.

REL



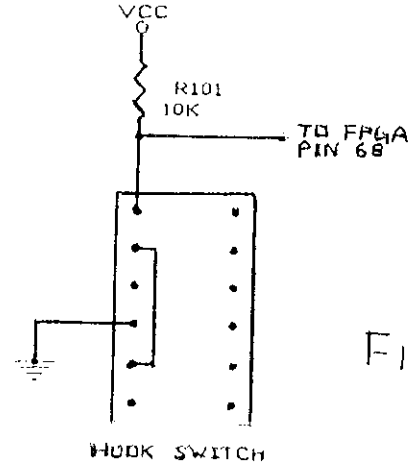
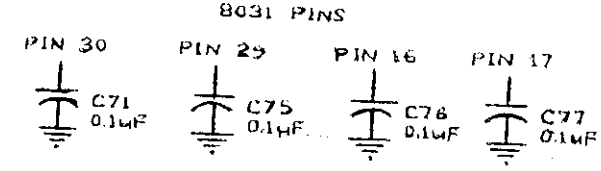


FIG 3.7b



diode. When 12V supply suddenly goes OFF, D11 gives an easy path for the output to discharge. C73 is output filter. L1 and C68 are the LC filter for analog +5V. C168 is the filter for digital +5V.

CONNECTORS

The connectors CN1,CN2,CN3 and the 25-pin D connector from the exchange are shown in Fig.3.6. Connectors CN1 and CN2 provide the signals to access the key and LED array. It also has a Vcc and a ground pin .

The connector CN3 is meant for the LCD module. It contains the data lines from the CPU along with the necessary control signals. It also has an adjustable LCD drive voltage. The ground and the +5V supply are also provided.

The 25-pin D connector indicated as CON 25 is primarily used for serial communication with the exchange. It is also used to derive the +12V supply from the exchange which is then converted to +5V locally as mentioned earlier. The unused pins are grounded.

CLOCK CIRCUIT FOR FPGA

The circuit shown in Fig.3.7a generates 20-KHz clock is used for ring pattern generation , key debouncing etc. Clock is generated using an astable multivibrator made out of a schmitt trigger(U14). R68-C69 is the RC combination used for generating clock. The clock is further conditioned by passing it through another schmitt trigger(gate B of U14). R69and R70 are pull-up resistors.

Clock is given to CLK_IN (pin 52) of FPGA through a resistor R75.

The hook switch, relay and pins 30,29,16 and 17 of the 8031 which are grounded through 0.1micro farad capacitors are shown in figure 3.7b.

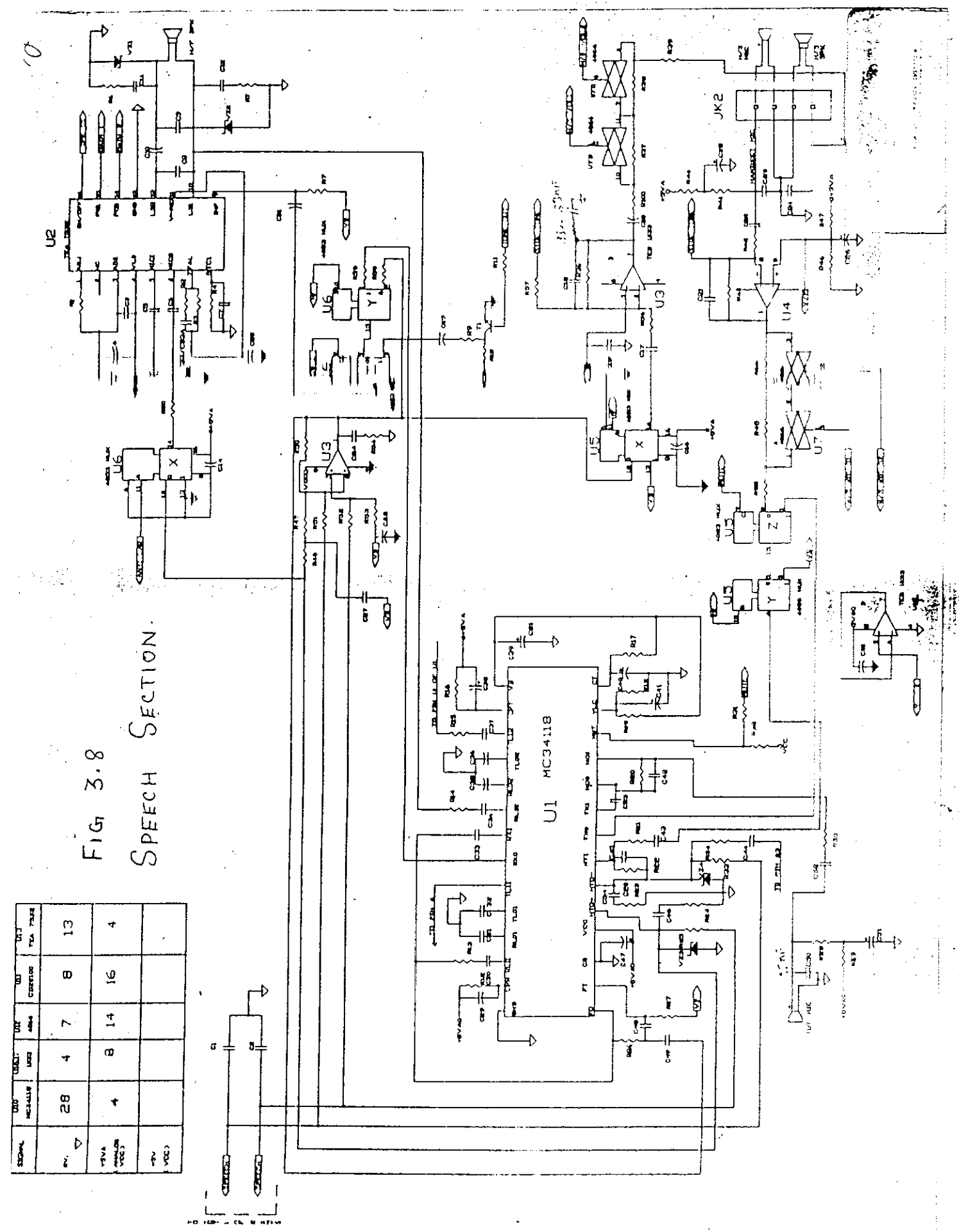


FIG 3.8 SPEECH SECTION.

SIGNAL		U10 MC34118	U11 4066	U12 CD4053	U13 TCA 7529
	PIN	28	7	8	13
	PIN	4	14	16	4
	PIN	4	8		

SPEECH SECTION

The speech section is divided into three parts namely :Handset transmission path, Handset receive path and Handsfree speaker circuit.

Handset Transmission Path :

The input to the circuit is speech signals from the handset mic. The output is fed to the speech coupling circuit so that it goes to the exchange. Handset mic. Is connected to the rest of the circuit through Hook switch such that the connection gets through only when handset is off-hooked. The speech signal is filtered and amplified using U4.

The Resistors R44 and R45 are connected across analog switch CD4066 determines the transmit level. These switches are controlled by signals from P1.4 and P1.5 of micro-controller. These signals determine the transmission level by inclusion/ omission of R44 and R45. P1.4 corresponds to R45 and P1.5 corresponds to R44.

Multiplexer U5B is used to select between handset mic. and handsfree mic. This is controlled by HF signal from 8031. U5C is used for muting of transmission. This is controlled by MUTE signal from 8031. The output of the multiplexer U5C is connected to hybrid amplifier input HT1 of speaker phone IC . The gain of hybrid amplifier depends on R22/R21. VZ4 will suppress any spikes. The same signal will appear at pin HT0+, but with a gain of -1 . For HT0+, zener diode VZ3 will act as spike suppresser. These signals are fed to the matching transformer through resistors R25 and R33. Pin 12 of U1 is mute input . By activating this pin, the handset transmission can be muted.

Handset Receive Path :

The input to this circuit is the speech signals from the speech coupling circuit. After processing the output is fed to the Handset speaker. The speech signal coming from matching transformer is fed to an amplifier U3. The output of the amplifier is fed to the multiplexer U5A. The multiplexer will select or deselect this signal according to the state of HF from micro-controller. The output of the multiplexer is given to a filter U3. The resistors R37 and R38 are connected across analog switches U7B and U7D. These switches are controlled by signals from P1.2 and P1.3 of micro-controller. These signals determine the Handset reception level by inclusion or omission of R37 and R38. P1.2 corresponds to R37 and P1.3 corresponds to R38.

Handsfree speaker circuit:

This circuit is used for

- Feeding dial tone to the Handsfree speaker if the system is in Handsfree mode.
- Feeding ring to the Handsfree speaker.

The amplified version of the signal coming from matching transformer is given to receive attenuator input of the speakerphone IC through an RC combination (R26and C49). The attenuator output is fed to the Multiplexer U6B. When HF signal is active this Multiplexer will pass the signal.

The next Multiplexer will select between speech and ring depending on the signal IN_S from 8031. The ring is coming from TONE_OUT of FPGA through a driving transistor T1.The level of ring is determined at this stage by the potential divider R9-R77.

The speech/ring is fed to the earphone input of the audio amplifier. The output pins 10 and 12 are connected to the loudspeaker. The RC combinations R6-C11 and R7-C12 will suppress any high frequency components present. The level of the

output is controlled by the signals PG1and PG0 which are connected to P1.6 and P1.7 of the micro-controller.

MIC1 and MIC2 inputs of 7532 are used for anti-larsen control.

MIC1 is connected to GND through a capacitor. Amplified transmit signal output of speakerphone IC, HT0+ is applied to MIC2 through a Multiplexer. Multiplexer is controlled by a signal ANTILAR from 8031. The level of the signal fed to MIC2 is controlled by potential divider R35-R5. The RC networks connected to pins 7 and 8 of 7532 are Anti larsen filters and they determine the gain and response of anti larsen system. For 7532 supply voltage is given at pin 4.Pin 3 is for AGC control and pin 1 is for voltage control.

For speaker phone IC,

Pin 13 is volume control input.

The RC combination at pin 14 determines the response time for the circuit to switch between modes (transmit and receive).

Vb (pin 15) is an output voltage =Vcc/2 and is a system A.C ground. C39 is the filter capacitor for Vb.

The RC combination R16-C38 at pin 16 sets the time constant for the transmit background monitor.

Pin 23 is the input to the transmit level detector inside speakerphone IC and is fed with a signal HTO- through RC combination R34-C44.

Pins 24 and 25 are the outputs of the transmit and receive level detector respectively and filter capacitors C32 and C31 are given at these pins.

Pin 26 is input to the receive level detector on line side and is fed with the filter output through RC combination R13-C30.

The RC combination R12-C29 at pin 27 sets the time constant for the receive background monitor.

Pin 4 is Vcc and Pin 28 is ground.

LCD MODULE

The LCD Module is the visual aid incorporated in the Operator Console that justifies the phrase " user-friendliness" associated with the Console. The important features that characterize this module are

- Compact, integrated display module
- Built-in controller IC
- Direct interface to four or eight bit CPUs
- Provided with various instruction functions

COMPOSITION :

Character font : 5 x 7 dot + cursor

Display format : 16 characters x 2 lines

Driving method : 1 / 16 duty multiplexed drive

SPECIFICATIONS:

Absolute maximum rating (Ta=25'C)

Item	*Symbol*	*Rat-min*	*Rat-max*	*Unit*
Logic power supply voltage	Vdd-Vss	0	7.0	V
I.C Driver supply voltage	Vdd-V0	0	7.0	V
Input voltage	Vi	Vss	Vdd	V
Operating temperature	Topr	0	50	C
Storage temperature	Tstg	-20	70	C

PIN ASSIGNMENTS:

Pin No.	*Signal*	*Level*	*Function*
1	GND	0 V	Power supply
2	Vdd	5V	Power Supply
3	Vo	Gnd to Vdd	Power Supply for LCD Drive
4	RS	H/L	H: Data Input L: Command Input
5	R/W	H/L	H: Data Read (Module to CPU) L: Data Write (CPU to Module)
6	E	H,H/L	Enable signal
7	DB0	H/L	Data bus
8	DB1	H/L	"
9	DB2	H/L	"
10	DB3	H/L	"
11	DB4	H/L	"
12	DB5	H/L	"
13	DB6	H/L	"
14	DB7	H/L	"

Function of registers:

1. **Instruction register and Data register**:

The LCD module built-in controller has two 8-bit registers, an instruction register (IR) and a data register (DR). IR stores instruction codes such as Display Clear and Cursor Shift, address information of DD RAM and CG RAM. IR can be written by CPU but CPU cannot read IR. DR temporarily stores data to be written into the DD RAM or the CG RAM. Data written into the DR is automatically sent to the DD RAM or the CG RAM as an internal operation. DR is also used for data storage for reading data from the DD RAM or the CG RAM. When address information is written into IR, data is transferred to DR from the DD RAM or the CG RAM as an internal operation. Then, CPU reads DR and data transfer is completed. After the CPU reads DR, data of the DD RAM or the CG RAM at the next address is sent to DR for the next reading. Register selector (RS) signals select these two registers.

Register Selection:

RS	*R/W*	*Functions*
L	L	IR Write
L	H	Read of a Busy flag and Address counter
H	L	DR Write
H	H	DR Read

2. **Busy flag (BF)**

When the busy flag is 'H', the LCD module is in the internal operation mode, and the next instruction is not accepted at this

time. The Busy flag is shown in DB7 when RS=L and R/W=H. The next instruction must be written after checking that busy flag is 'L'.

3. **Address counter (ADC)**

The ADC assigns DD and CG RAM addresses. When an instruction for address setting is written in IR, the address information is sent from IR to ADC. Selection of either DD or CG RAM is also determined by the instruction. After writing into (or reading from) DD or CG RAM display data, ADC is automatically incremented by 1.Data in ADC are in DB6 to DB0 when RS=L, BF=L and R/W=H.

4. **Display data RAM (DD RAM)**

The DD RAM stores display data represented in 8-bit character codes. The relationship between DD RAM addresses and display position on LCD display is shown in the table below.

Character Position	[1]	[2]	[3]	[4]	[5]	[6]	[7]	[8]	[9]	[10]	[11]	[12]	[13]	[14]	[15]	[16]
DD RAM Address	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
Character Position	[17]	[18]	[19]	[20]	[21]	[22]	[23]	[24]	[25]	[26]	[27]	[28]	[29]	[30]	[31]	[32]
DD RAM Address	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F

INSTRUCTION:

The instruction code refers to the signal through which LCD module is accessed through the CPU. The LCD module begins operation upon receipt of the code input. As the internal processing of the LCD module is started with the timing that does not affect the LCD display, the Busy status continues longer than the CPU cycle time.

Under the Busy status (when the Busy flag is set to 'H') the LCD module does not execute any instruction other than the Busy

flag read. For this reason , the CPU has to verify that the Busy flag is set to 'L' prior to the input of the instruction code.

The table given in the Appendix describes the different instructions.

INITIALIZATION OF THE LCD MODULE:

The LCD module is automatically initialized when the power is turned on. During initialization, the Busy flag holds 'H' and does not accept instructions (other than the BF read). The BF goes to 'H' for 15 ms after Vdd reaches 4.5 V or more. During initialization the LCD module executes the following instructions.

- Display Clear.
- Data length of interface with CPU = 8 bits.
- LCD 1 line display.
- Character font : 5 x 7 dots.
- ADC increment.
- No display shift.
- Display off.
- Cursor off.
- No blink.

The built-in reset circuit does not operate normally unless the required power supply conditions are not met. Otherwise the initialization is done through software.

FPGA

WHY FPGA ?

Aside from product differentiation, a top priority for every engineer is shorter design cycles. Since FPGAs offer the design flexibility and capacity of gate arrays, with the convenience and speed of desktop programming, they satisfy this Time-To-Market demand. In fact, FPGAs deliver the fastest Time-To-Market solution of all logic integration methodologies.

Today's design engineers must also deal with the relentless demand to make products that are both cheaper and smaller. Here again, FPGAs are the solution. By integrating thousands of gates of random logic onto a single chip, FPGAs let engineers simultaneously reduce board space, component count and power requirements.

The Anti-Fuse technology and unique segmented routing architecture, offers logic solutions that deliver significant advantages over competitive technologies. Actel Anti-Fuse FPGA technology is inherently fast, even at higher capacities. Currently, Actel FPGAs can give 250MHz counter and datapath designs with 7.5 nanosecond clock-to-out speeds in 4000 gate devices and 200MHz designs in 10000 gate devices.

With Actel FPGAs and design tools, all or some the system's logic can be shrunk onto a single programmable device. Also I/O pins can be fixed even before the design is finished. In addition Actel's automated design tools lets making changes in the logic design quickly, without affecting other parts of the design. As a result overall system design time is cut to a large extent.

Actel designer series tools automate many of the repetitious tasks in logic design, which makes them exceptionally easy to use. We get high performance, predictability and flexibility through automatic placement and routing-and automatic generation of counters, accumulators and other functional blocks. Designer series tools also support standard schematic capture and high level design through boolean and synthesis tool, as well as EDIF netlists.

The Actel Anti-Fuse is a nonvolatile, two terminal element that delivers a low "on" resistance when programmed. It provides the same wire-to-wire interconnect functions as "vias" do in mask-programmable gate arrays- and that transistor-based EPROM and RAM cells and metal fuse deliver in traditional programmable logic devices.

Actel 1010B gives up to 1200 gate arrays and lets integration up to 30 Transistor-Transistor-Logic devices or 12 Programmable Logic Devices on to a single device.

FEATURES OF ACTEL 1010B

- 3.3 Volt functionally fully compliant with JEDEC specifications
- Up to 2000 Gate Array Gates (6000 PLD equivalent gates)
- Replaces up to 50 TTL packages
- Replaces up to twenty 20-pin PAL packages
- Design Library with over 250 functions
- Gate Array architecture allows completely automatic place and route

FPGA Package Pin Assignments:-

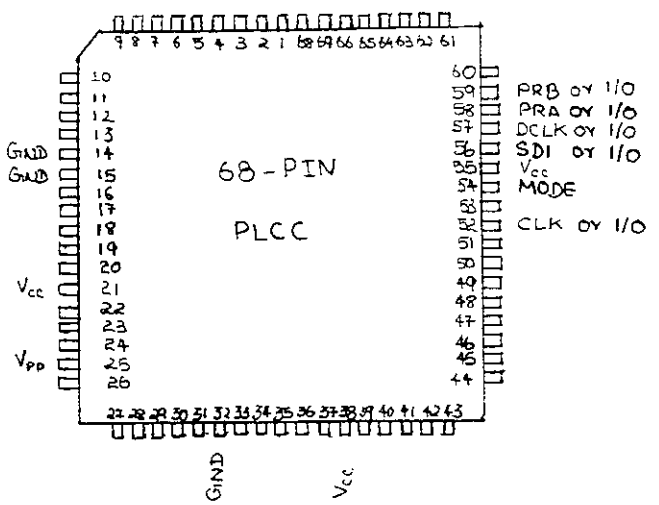


Fig 4.1

- Up to 547 Programmable Logic Modules
- Up to 273 Flip-Flops
- Flip-Flop toggle rates to 100MHz
- Two in circuit diagnostic probe pins support speed analysis to 15MHz
- Built-in high speed clock distribution network
- I/O drive to 6mA
- Non-volatile and User programmable
- Fabricated in 1.0 micron CMOS technology

Actel 3.3 Volt devices also provide system designers with unique on- chip diagnostic probe capabilities , allowing convenient testing and debugging. Additional features include an on-chip clock driver with a hardwired distribution network. The network provides efficient clock distribution with minimum skew. The user definable I/Os are capable of driving at both TTL and CMOS drive levels.

PIN DESCRIPTION :

CLK Clock (Input):

TTL clock input for global clock distribution network.The clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

DCLK Diagnostic Clock (Input) :

TTL clock input for diagnostic probe and device programming. DCLK is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

GND Ground :

Input LOW supply voltage.

I/O Input /Output (Input, Output) :

I/O pin functions as an input, output, three-state, or bidirectional buffer. Input and Output levels are compatible with standard TTL and CMOS specifications. Unused I/O pins are automatically driven LOW by the ALS software.

MODE Mode (Input) :

The MODE pin controls the use of multifunction pins (DCLK,PRA,PRB,SDI). When the MODE pin is HIGH, the special functions are active. When the MODE pin is LOW, the pins function as I/O.

NC No Connection :

This pin is not connected to circuitry within the device.

ACT 1 devices have two independent diagnostic probe pins. These pins allow the user to observe any two internal signals by entering the appropriate net name in the diagnostic software. Signals may be viewed on a logic analyzer using Actel's Actionprobe diagnostic tools. The probe pins can also be used as user-defined I/Os when debugging is finished. The two pins are described below;

PRA Probe A (Output) :

The Probe A pin is used to output data from any user-defined design node within the device. This independent diagnostic pin is used in conjunction with the Probe B pin to allow real-time

diagnostic output of any signal path within the device. The Probe A pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect the programmed design's confidentiality. PRA is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

PRB Probe B (Output) :

The Probe B pin is used to output data from any user-defined design node within the device. This independent diagnostic pin is used in conjunction with the Probe A pin to allow real time diagnostic output of any signal path within the device. The Probe B pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect the programmed design's confidentiality. PRB is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

SDI Serial Data Input (Input) :

Serial data input for diagnostic probe and device programming. SDI is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

Vcc Supply Voltage :

Input HIGH supply voltage.

Vpp Programming Voltage :

Input supply voltage used for device programming. This pin must be connected to Vcc during normal operation.

THE ACTEL DESIGNER AND DESIGNER ADVANTAGE SYSTEMS

The Actel Designer and Designer Advantage systems are high-productivity, computer-aided engineering environments for the Actel family of field programmable gate array(FPGA) devices. The Designer System can handle all Actel FPGA families up to 2500-gates, while the Designer Advantage System handles every Actel device, from the smallest to the largest.

Each Designer Series system gives you placement and routing, timing verification, and programming interface software, as well as interfaces to many popular CAE and electronic design automation platforms such as Cadence, Mentor Graphics, OrCAD, Synopsys and Viewlogic. In addition, both Designer Series systems support programming on data I/O's Unisite and 3900 series programmers.

The design can be entered by drawing a schematic with symbols generated by the ACTgen Macro Builder, or from the Actel Macro Library. This library has more than five hundred different hard and soft macro functions, including everything from simple gates to complex functions. For added design flexibility, application specific macros using the ACTgen Macro Builder can be created. Currently, the macro library and the ACTgen Macro Builder support most popular schematic capture and simulation systems like Viewlogic.

Automatic place and route software minimizes design delay by assigning macros to optimal locations on the chip. The software uses the netlist, critical net information, and I/O assignments to automatically place and route all the logic blocks within the blocks.

With Direct time, a powerful new design capability, the overall operating frequency can be specified and the pin-to-pin timing requirements as the design is created. Then during place and route, Direct time will use those requirements to create an FPGA that achieves the performance characteristics as specified.

The place and route software gives data on the direct interconnect delay. This information along with the along with the Direct time analyzer timing verification tool can be used for accurate post-routine timing simulations. The Designer series systems allows to analyze the functional and timing characteristics of the design in several different ways. For example static timing analysis can be performed, or back annotation capabilities can be used to give links to timing simulations.

Actel's static timing analyzer gives complete point-to-point timing information and allows to specify which signals are to be reported. Direct time analyzer is an interactive timing analysis tool that graphically displays the performance of all critical and non critical paths within a specified design. The Direct time analyzer will perform a static time analysis, using post-route delays extracted from the layout. Afterwards, it would give a spreadsheet view of the timing results, which can be used to optimize the design to meet timing specifications. When used with Direct time layout, the analyzer provides a system that implements the timing that is specified and allows the verification of the timing that is required.

After the completion of a final timing analysis, the designer series system produces device programming files that can be used by either data I/O or Actel Activator series programmers. Designer series software generates a fuse map for the specific device that is being programmed. This map specifies the programming of the PLICE Anti-Fuse and determines interconnections within the FPGA.

Actel's Designer and Designer Advantage system for the Viewlogic design environment is a low-cost field programmable gate array (FPGA) design, programming and verification software system.

SOFTWARE REQUIREMENTS :

- MS-DOS version 3.3 (or later)
- Windows version 3.1 (or later) optional
- Viewlogic Workview PLUS or PROseries 6.0
- Viewlogic Viewsim or PROsim

HARDWARE REQUIREMENTS :

- 24MB RAM (minimum)
- 40MB virtual disk
- Additional 50MB disk space for program and data files
- 1.44MB floppy disk drive
- CD-ROM drive (recommended)
- VGA, EGA, or monochrome graphics card

The figure shows how the Designer Advantage software works with Viewlogic's ViewDraw schematic capture and Viewsim simulation tools. A schematic description can be created by using ViewDraw. The ACTgen Macro Builder enhances schematic description by using ViewDraw. The ACTgen Macro Builder enhances schematic or synthesis based capture methods by creating macro functions that customized for your application. For the macro the macro type, bit width, control signals and so on have to be specified and the Macro Builder does the rest automatically. Custom, complex functions can be generated in minutes. The design files are then exported from Viewlogic directly in to the

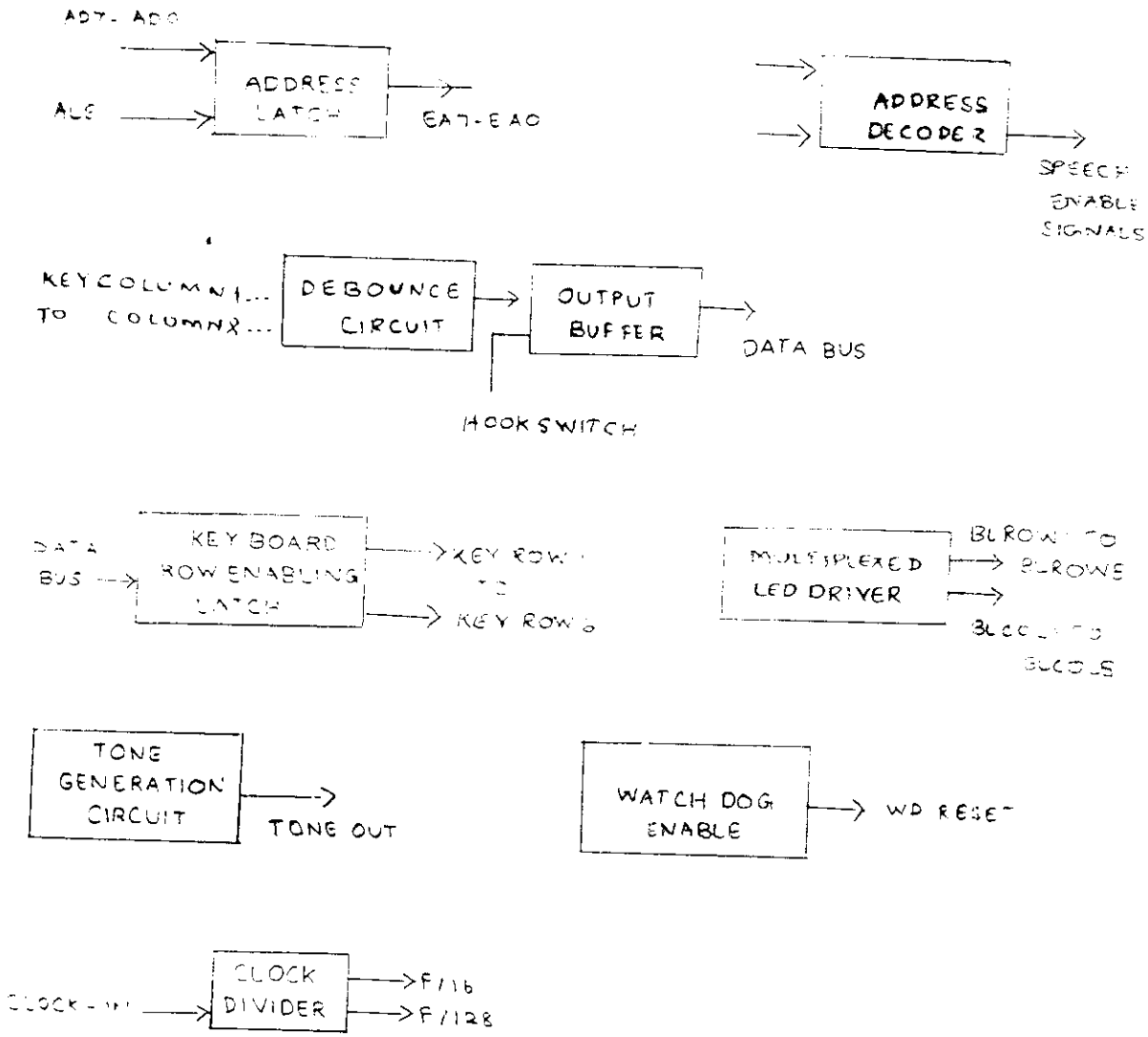


FIG 4.3

BLOCK DIAGRAM OF FPGA CIRCUITS

Designer or Designer Advantage environment, which runs under Microsoft Windows on PCs.

FPGA INTERNAL CIRCUITS

The block diagram of the circuits integrated into the FPGA chip is shown in Fig 4.3.

The circuits were designed using digital devices, calling macros from the ACTgen Macro Builder. These were placed using Automatic Place and Route and pin-edited, before being checked for timing and back-annotations. This was fed to the ViewLogic design environment to create the desired chip.

A brief description about the circuits along with their circuit diagrams is given in the following pages. The input and the output lines have been identified in the circuit diagrams given previously.

Address Latch:

It is a 8-bit latch with active high outputs and active low clock and clear. It is enabled by the POR and ALE signals. The outputs are buffered as shown in Fig 4.4.

Address Decoder:

This consists of two 3 to 8 decoders with enable and active low outputs along with a data latch as shown in Fig 4.5. The inputs viz READ and WRITE are buffered and then fed in. The various address combinations and the functions selected are given in the table in the next page.

The LCD_ENABLE _IN signal is buffered and provides the LCD_ENABLE signal. The LATCH_SELECT signal is NORed with WR signal to enable the latch. The contents from the accumulator, then , determine the output signals as shown in the figure.

ADDRESS LATCH:

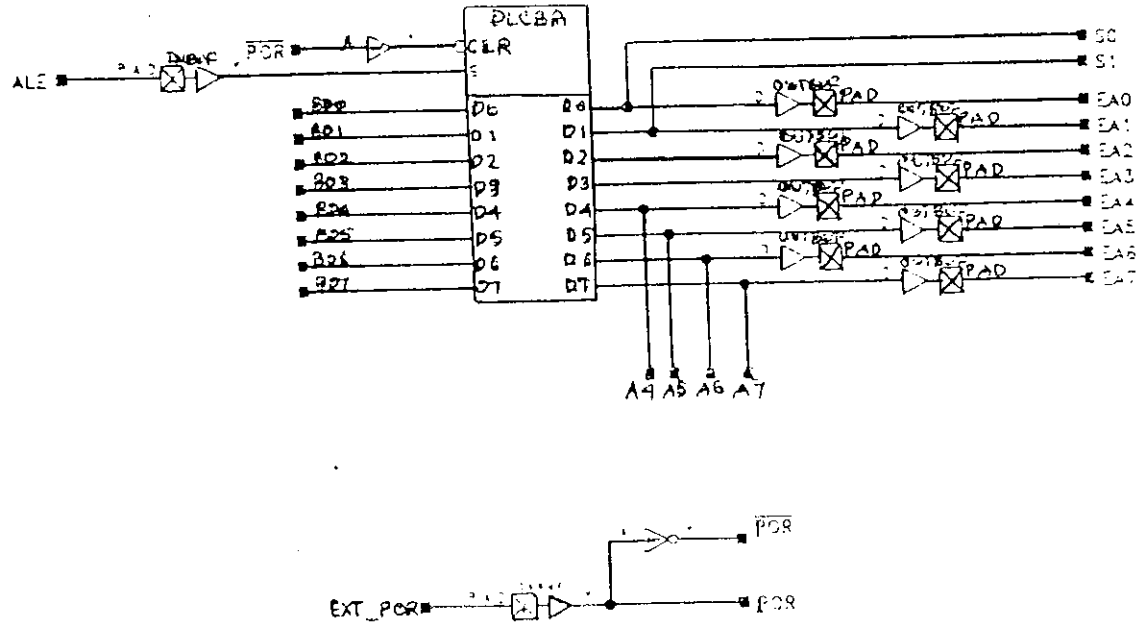
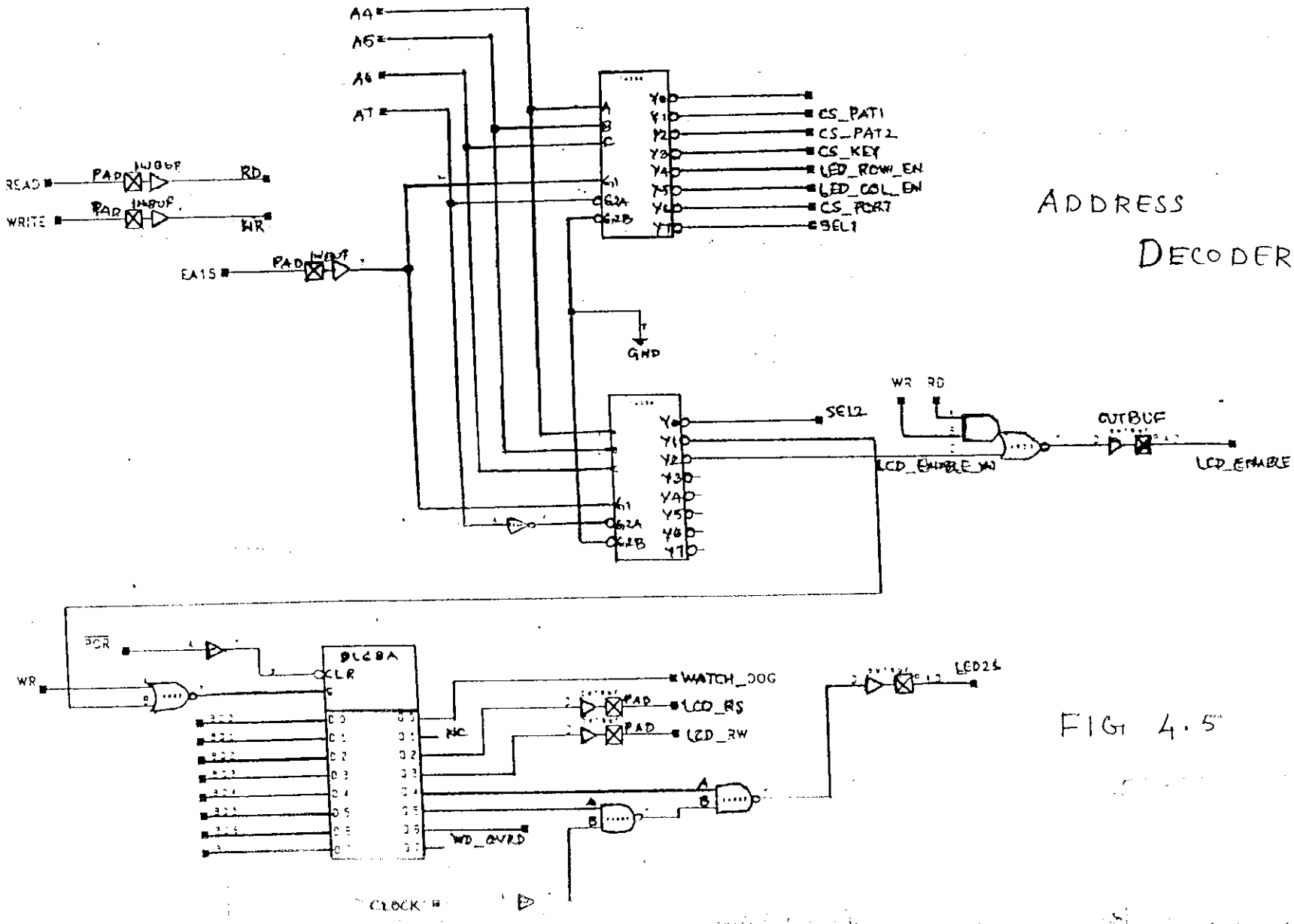


FIG. 4.4



ADDRESS DECODER

FIG 4.5

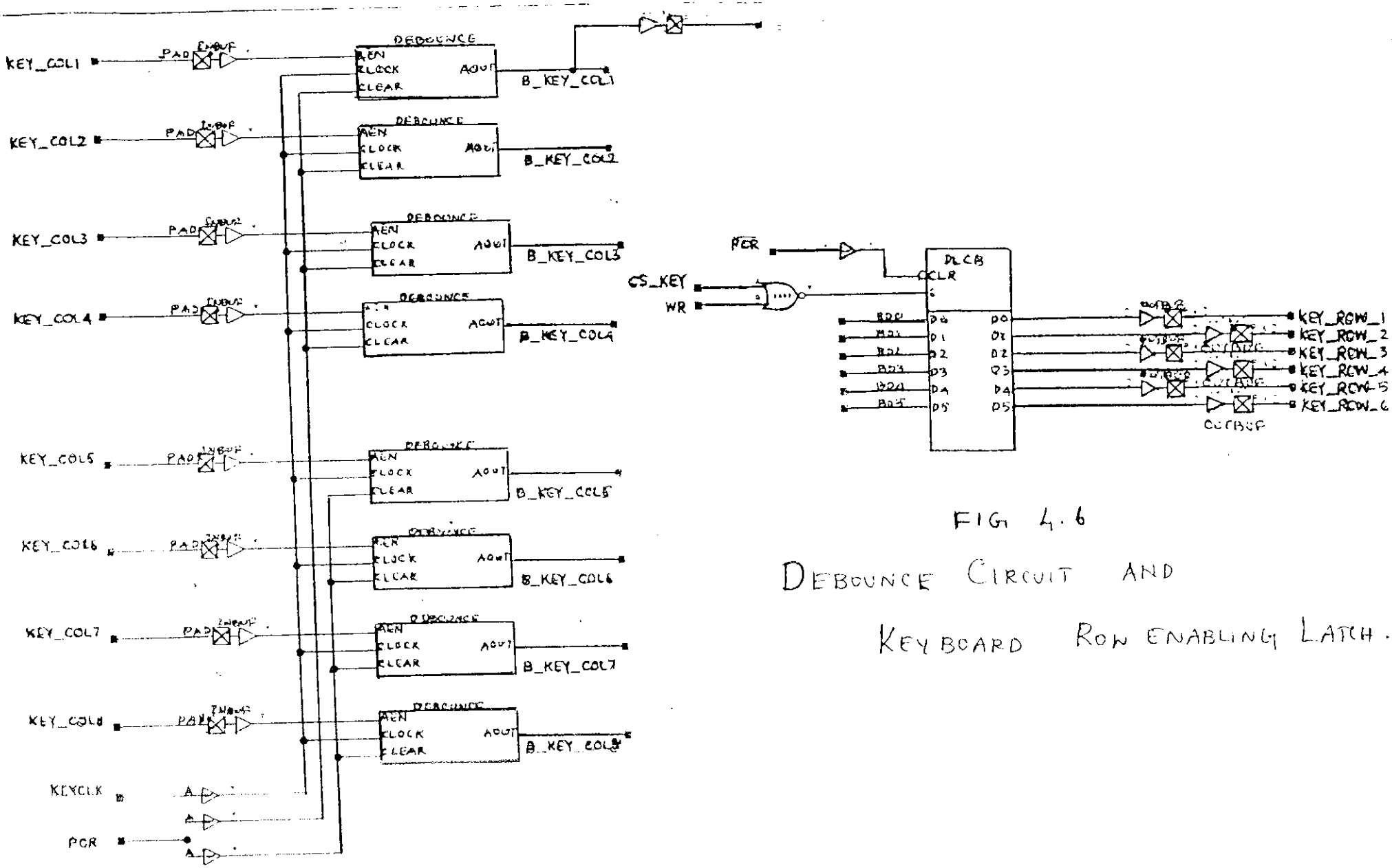


FIG 4.6

DEBOUNCE CIRCUIT AND

KEYBOARD ROW ENABLING LATCH.

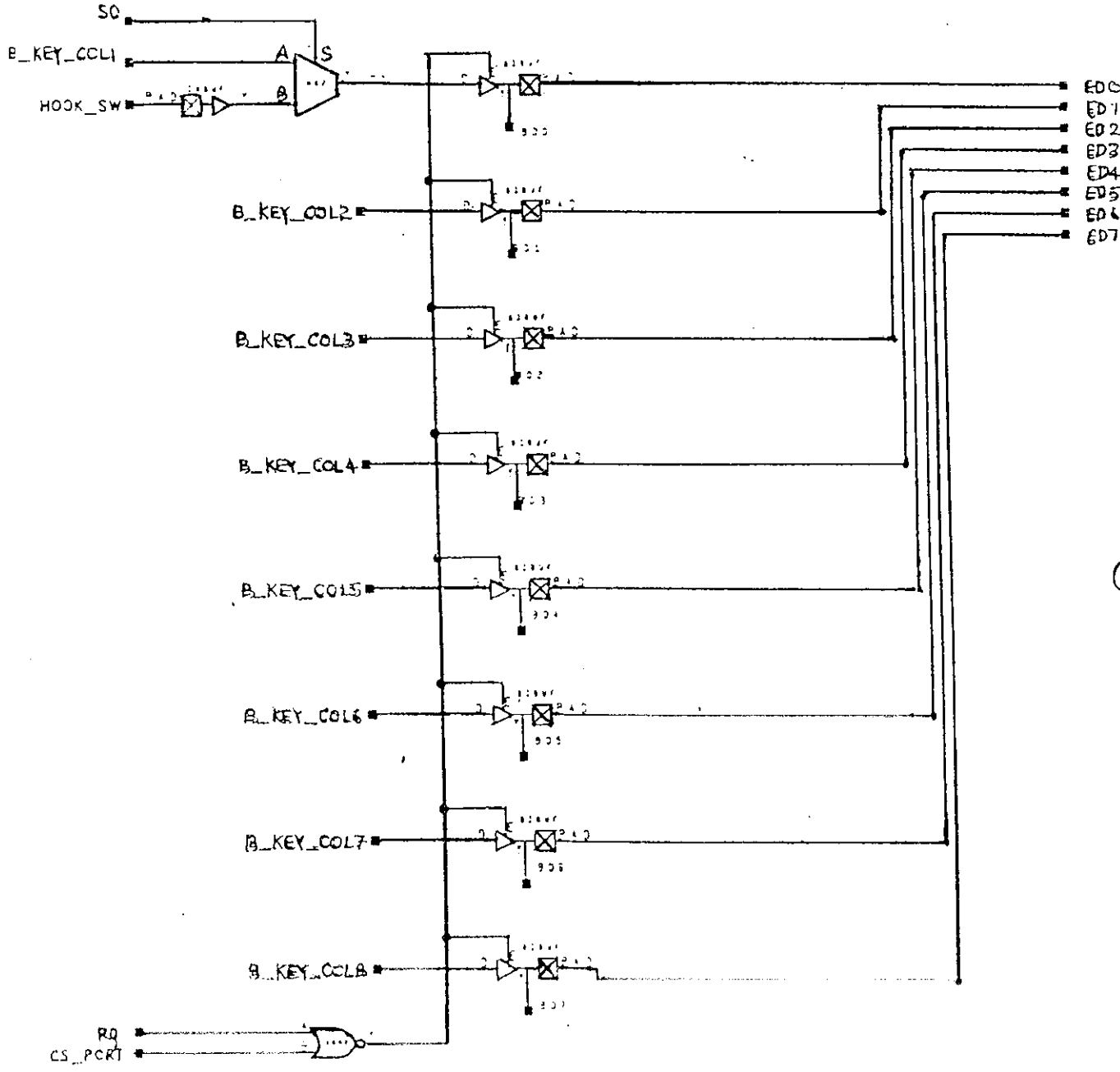


FIG 4.7

OUTPUT BUFFER FOR DEBOUNCE CIRCUIT.

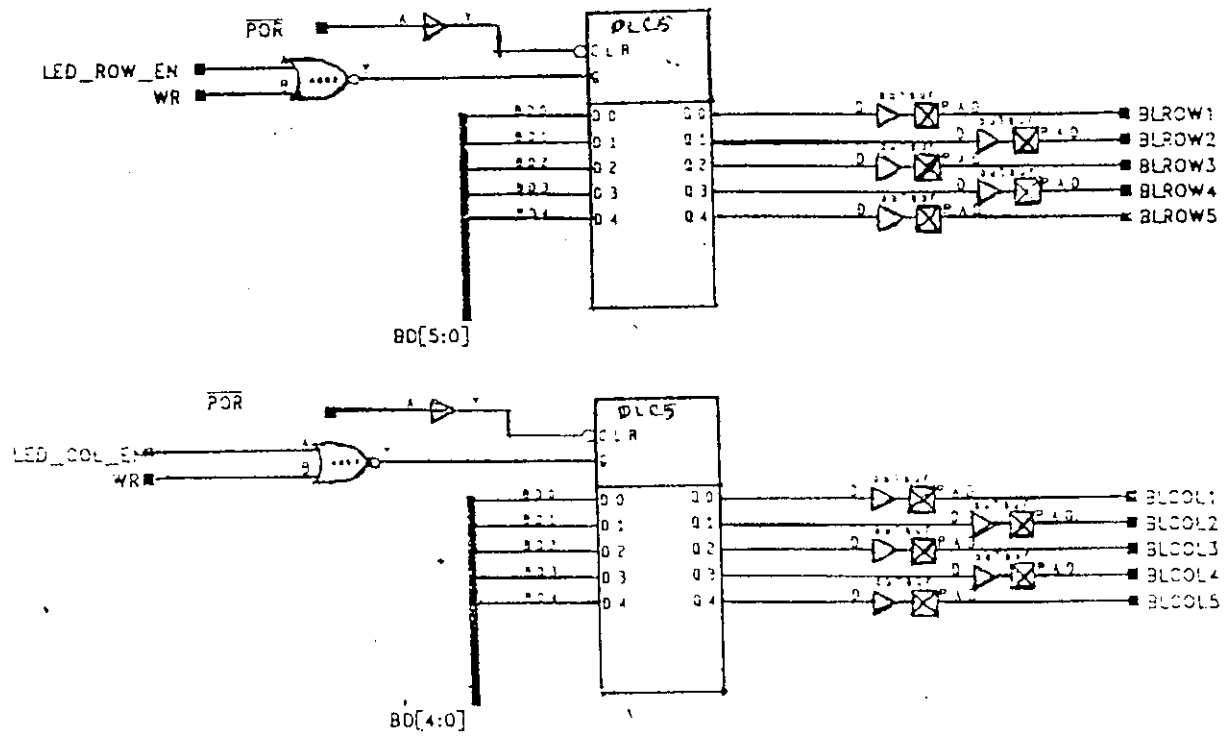


FIG 4.8

MULTIPLEXED LED DRIVERS.

Address	*Output of the Decoder.*
8010	CS_PAT1
8020	CS_PAT2
8030	CS_KEY
8040	LED_ROW ENABLE
8050	LED_COL ENABLE
8060	CS_PORT
8070	SEL1
8080	SEL2
8090	LATCH_SELECT
80A0	LCD_ENABLE

Debounce Circuit with Buffered output:

The debounce circuits along with buffered outputs are shown in Fig 4.6 & Fig 4.7. The KEY_COL inputs are taken , given a debounce time delay of 20ms and then sent as buffered outputs. The 6-bit latch is used to provide the KEY_ROW signals. Combined, they are used in the dynamic scanning procedure to detect the key pressed.

Multiplexed LED Drivers:

The Fig 4.8 shows the multiplexed LED drivers. The row and column enable signals are given to enable the latches and the input from the Accumulator, thus, determines the corresponding row or column to be selected. Combined, this amounts to selecting one LED from the 5x5 LED matrix.

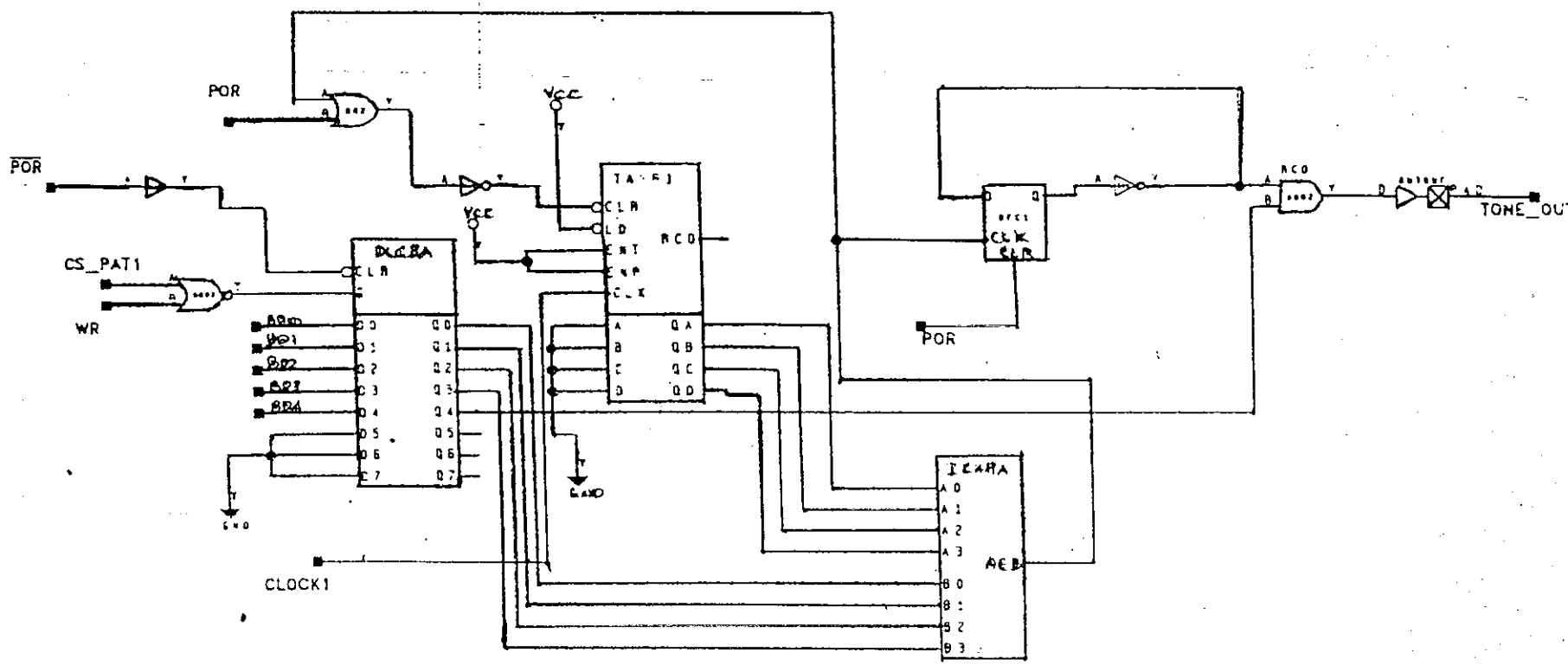


FIG 4.9.

TONE GENERATOR

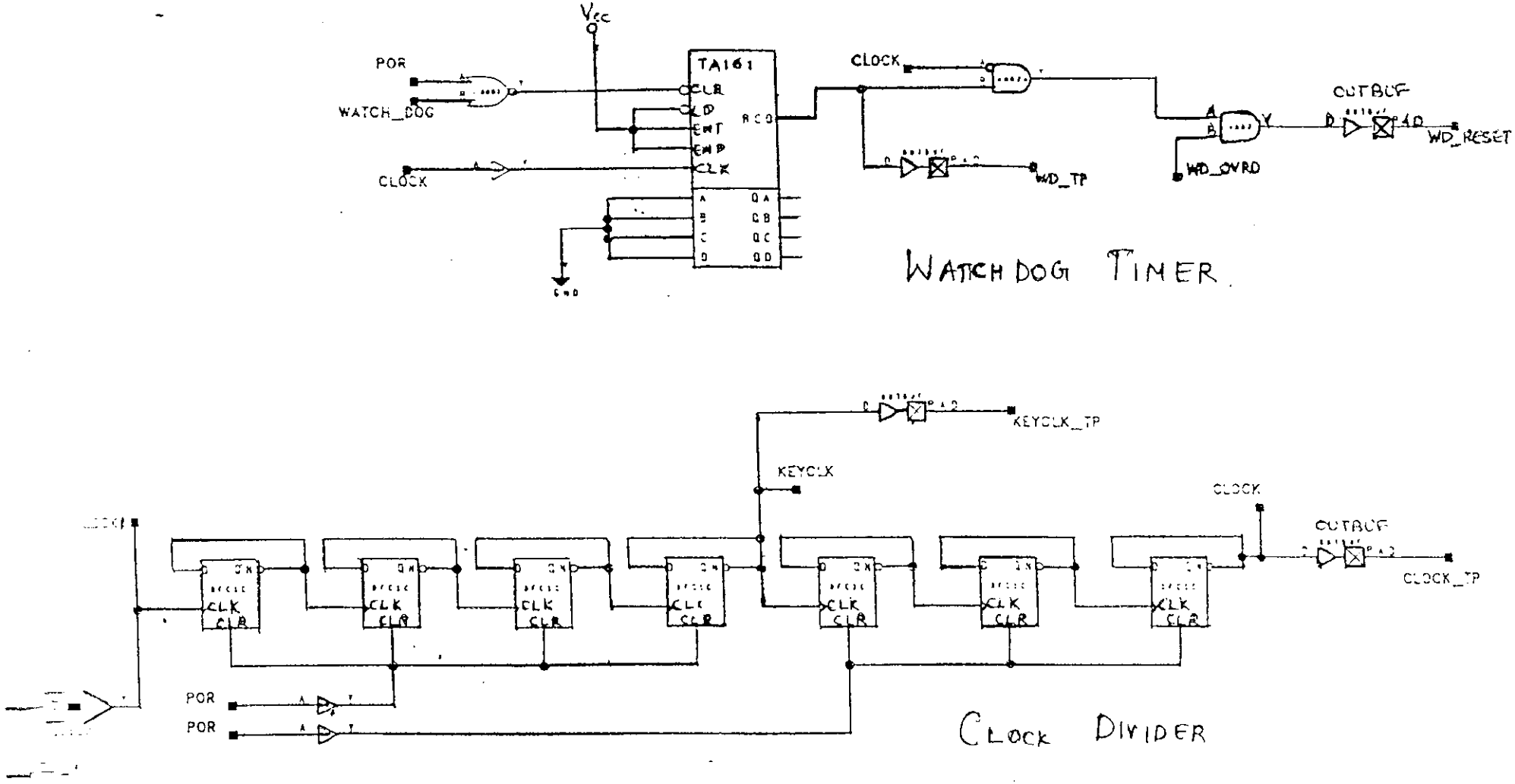

Vcc
POR
WATCH_DOG
CLOCK
74161
CLR
LD
ENT
ENP
CLK
RCO
QA
QB
QC
QD
GND
CLOCK
WD_TP
OUTBUF
WD_OVRD
WD_RESET
WATCH DOG TIMER
KEYCLK_TP
KEYCLK
CLOCK
OUTBUF
CLOCK_TP
POR
POR
CLOCK DIVIDER

FIG 4.10

Watchdog Timer and Clock Divider:

The Fig 4.10 shows the circuit for Watchdog timer and the divide by 16 / 128 clock divider. The WD_RESET output is used to provide a hardware reset to the general operation, if any failure occurs. This is overdriven by the software reset under normal conditions. When a fault occurs and the software reset is paralyzed, the Timer times out the Watchdog sending the system to a state of reset.

Tone Generator Circuit:

The Tone generator is a programmable ring tone generator. The CS_PAT signal input is used as an enable line for activating this tone generator circuit. This is programmed using the data bus of the 8031.Depending upon the bit combination this piece of circuitry generates different frequency ring tones.

FPGA PIN ASSIGNMENTS

1-AD0	18-EA6	35-BLCOL1	52-CLK_IN
2-AD1	19-EA7	36-BLCOL2	53-KEY_COL5
3-AD2	20-BOUNCE_KEY	37-BLCOL3	54-MODE
4-Vcc	21-Vcc	38-Vcc	55-Vcc
5-AD3	22-LCD_RW	39-BLCOL4	56-KEY_COL6
6-AD4	23-CLOCK_TP	40-BLCOL5	57-KEY_COL7
7-AD5	24-TONE_OUT	41-BLROW1	58-KEY_COL8
8-AD6	25-Vpp(Vcc)	42-BLROW2	59-KEY_ROW_1
9-AD7	26-EA15	43-BLROW3	60-KEY_ROW_2
10-EA0	27-READ	44-BLROW4	61-KEY_ROW_3
11-EA1	28-WRITE	45-BLROW5	62-KEY_ROW_4
12-EA2	29-ALE	46-LCD_RS	63-KEY_ROW_5
13-EA3	30-EXT_POR	47-KEY_COL1	64-KEY_ROW_6
14-GND	31-LED26	48-KEYCOL2	65-WD_RESET
15-GND	32-GND	49-GND	66-GND
16-EA4	33-WD_TP	50-KEY_COL3	67-LCD_ENABLE
17-EA5	34-KEYCLK_TP	51-KEY_COL4	68-HOOK_SW

FEATURES

FUNCTION KEYS - AT A GLANCE :

1. Extension / Trunk keys (S1 - S16)
2. Program
3. Fax
4. Serial Call
5. Release
6. CONF (conference)
7. Override
8. Day / Night
9. Flash
10. Speed Dial
11. Redial
12. Page
13. Park
14. Mute
15. H/S Vol (Handset receive volume control)
16. Tx-level (Handset transmission level control)
17. H/F Vol (Handsfree dialling / ring volume control)
18. Handsfree

EXTENSIONS / TRUNKS

When standard data entry is made, the function keys have following functions

KEYS	1606/803	1204	602
S1	1 Trunk	1 Trunk	1 Trunk
S2	2 Trunk	2 Trunk	2 Trunk
S3	3 Trunk	3 Trunk	Extn.31
S4	4 Trunk/Free	4 Trunk	Extn.34
S5	5 Trunk/Free	Extn.33	Extn.35
S6	6 Trunk/Free	Extn.34	Extn.36
S7	Extn.31	Extn.31	Extn.32
S8	Extn.32	Extn.32	Extn.33
S9	Extn.33	Extn.35	GMN 0
S10	Extn.34	Extn.36	GMN 1
S11	Extn.35	Extn.39	GMN 4
S12	Extn.36	Extn.40	GMN 5
S13	Extn.37	Extn.37	GMN 2
S14	Extn.38	Extn.38	GMN 3
S15	Extn.41/Free	Extn.41	GMN 6
S16	Extn.42/Free	Extn.42	GMN 7

Here GMN stands for Global Memory Numbers used in Speed Dialling.

PROGRAM

To enter in to the programming mode the Operator has to press this key followed by the corresponding password . Also to quit this programming mode the same operation can be performed.

FAX

This key transfers an incoming fax call to a fax machine connected to pre-programmed extension of the EPABX. The Fax machine can be connected to any extension of the exchange but that has to be programmed as Fax extension.

SERIAL CALL

This key allows the operator to transfer incoming calls to other extensions. The extension number is specified after pressing the **SERIAL CALL** key. Call transferred in this manner will, finally, comeback to the operator station. The **SERIAL CALL** LED will blink when this function is activated. Once the call returns , the LED stops blinking. When serial call returns to the operator, the ring cadence will be that of call back ring. If the extension to which call is transferred does not pick the call within thirty seconds call returns to the operator.

RELEASE

This key when pressed , will simulate the pressing of hook switch for release.

CONF

This key is used to up conference among internal/external parties. A conference is set up using the following procedure:

- Press the **CONF** key
- Dial tone would be heard
- Other party would be on music-on-hold
- Same procedure is continued till all mates have been put on music-on-hold
- The key is pressed to set up conference
- Maximum of eight parties can have conference at a time

OVERRIDE

If the calling extension is in conversation mode , then by pressing this key the operator can enter into conversation. The conversing extensions would be warned by piptone for five seconds. The facility can be used only if the extensions are override protected.

DAY / NIGHT

This feature allows the operator to switch to the night feature mode by pressing this key followed by the corresponding password . When the system is in this mode the corresponding LED would glow. The same way by pressing this key we can exit the mode.

FLASH

If the operator is in conversation , the present call will be terminated and the same trunk would be accessed once again , overriding call back of other extensions in this line.

SPEED CALL

Ten important numbers can be stored in memory and can be accessed by pressing this key and numbers from 0 to 9 .The number would be correspondingly dialled. A memory label is given in front for the help of the operator.

REDIAL

By pressing this key, the operator can redial the last external number pressed . For redial, system would use same trunk access code as the original dialling.

PAGE

By pressing this key, the operator would get connected to the customer provided paging system. Music will be heard for three seconds in the connecting speakers. Once the music stops operator can make announcements.

PARK

Operator can park the call by pressing this key, even while in conversation. The operator will get dial tone while the external party will get music. A maximum of three trunks can be parked by the operator. The following procedure is used for the operator to access the parked calls

- Press **PARK** twice to access the external party who has parked first.
- To access the external party who has parked his call, press **PARK** and the key of the corresponding trunk.

The LED corresponding to the **PARK** key would glow if any call is parked along with the corresponding trunk LED which would blink. The Trunk LED will stop blinking if the trunk is retrieved and that of the **PARK** will stop when all parked trunks are retrieved .

MUTE

To mute transmission through handset microphone this key is used . The corresponding status is indicated by the mute LED which glows when transmission is muted. To resume transmission the corresponding **MUTE** key has to be pressed again.

H/S VOL

The volume of the handset receiver can be adjusted using this key. The key can be pressed to maximize the volume which is indicated by glowing of the corresponding LED. To minimize the volume the same key is pressed again which takes to the minimum volume level .The LED goes off in this case. The LED glows only in the maximum volume condition.

H/F VOL

This key is used for handsfree dialling / ring volume adjustment. There are four different levels and volume adjustment can be done cyclically using this key. Maximum level of volume is indicated by the corresponding LED.

TX-LEVEL

By Using this key , the transmission level of handset microphone can be adjusted . The corresponding LED will glow in maximum level. There are four different levels of transmission which can be rotated by using this key.

HANDSFREE

This key is a mode changing key. We can change from handsfree to handset or from handset to handsfree . After handsfree dialling , for talking to the other party , lift the handset and press this key.

SOFTWARE OVERVIEW

The extensively written software controls the operation of the console. The software can be broadly divided into three parts viz. the backbone, the special features and the phonebook part.

Backbone Software:

The backbone software is structured to include Main and Interrupt. The Main consists of routines for initialization, transmission of keycode to the exchange, reception of bytes from the exchange(through the serial port), displaying the received information using the corresponding LEDs and the ringing routine.

The interrupt part handles the timing routine for LED display, dynamic key scanning routine to detect the key pressed, a routine to check the hook status and a timing routine for the ring.

The general flowchart for the backbone software is given in Fig 6.1.

Special Features :

The special features like conference, serial call, call parking etc. are provided through communication with the exchange. The console offers features that are performed by the exchange by transmitting corresponding bytes to indicate the exchange about the service to be rendered.

Phone Book :

The phone book software takes care of the operation of the LCD module in the normal and special program modes. In the normal mode, the software displays the dialled digits in the LCD screen. In the special program mode the console is made to operate in any one of the three modes given below

STORE MODE :

In this mode the user can store up to 1000 numbers along with some additional information like names. The numbers are stored according to the alphabetical order of the names.

SEARCH MODE :

This mode provides the user with a tool to search for a name or any other information depending on an optional one or two character search procedure. The Search can be done recursively and the searched number can then be dialled with a single-touch dial option.

SCROLL MODE :

This is again a search tool which allows the user to scroll the details starting with a desired alphabet. The single-touch dial can also be performed in this mode.

The flowcharts for the various software modules mentioned above are given in the subsequent pages.

BACK BONE FLOW CHART

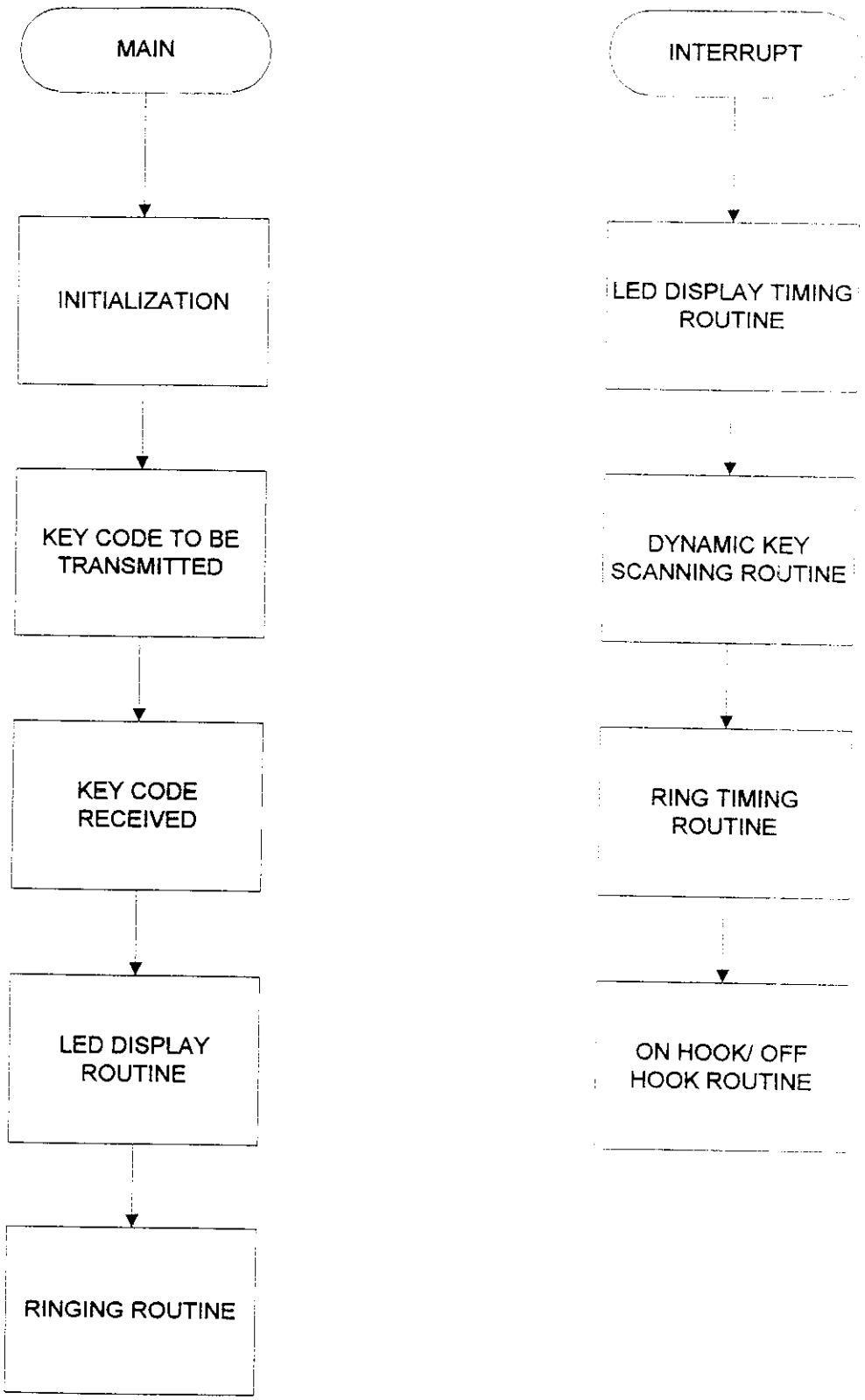


FIG : 6.1

MODE FLOW CHART

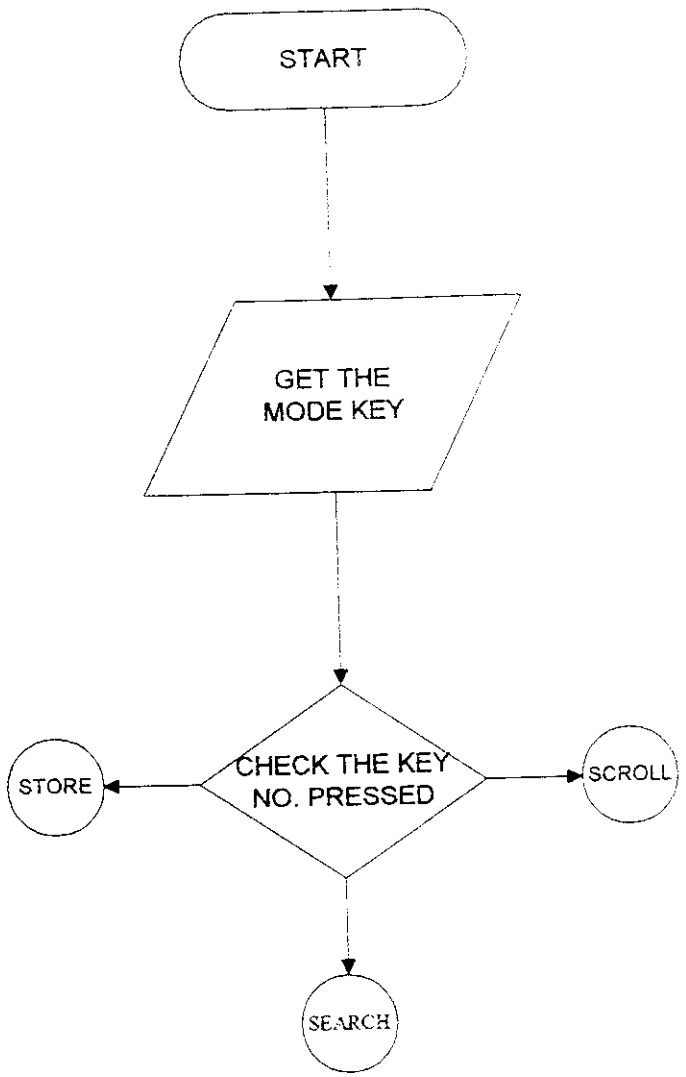
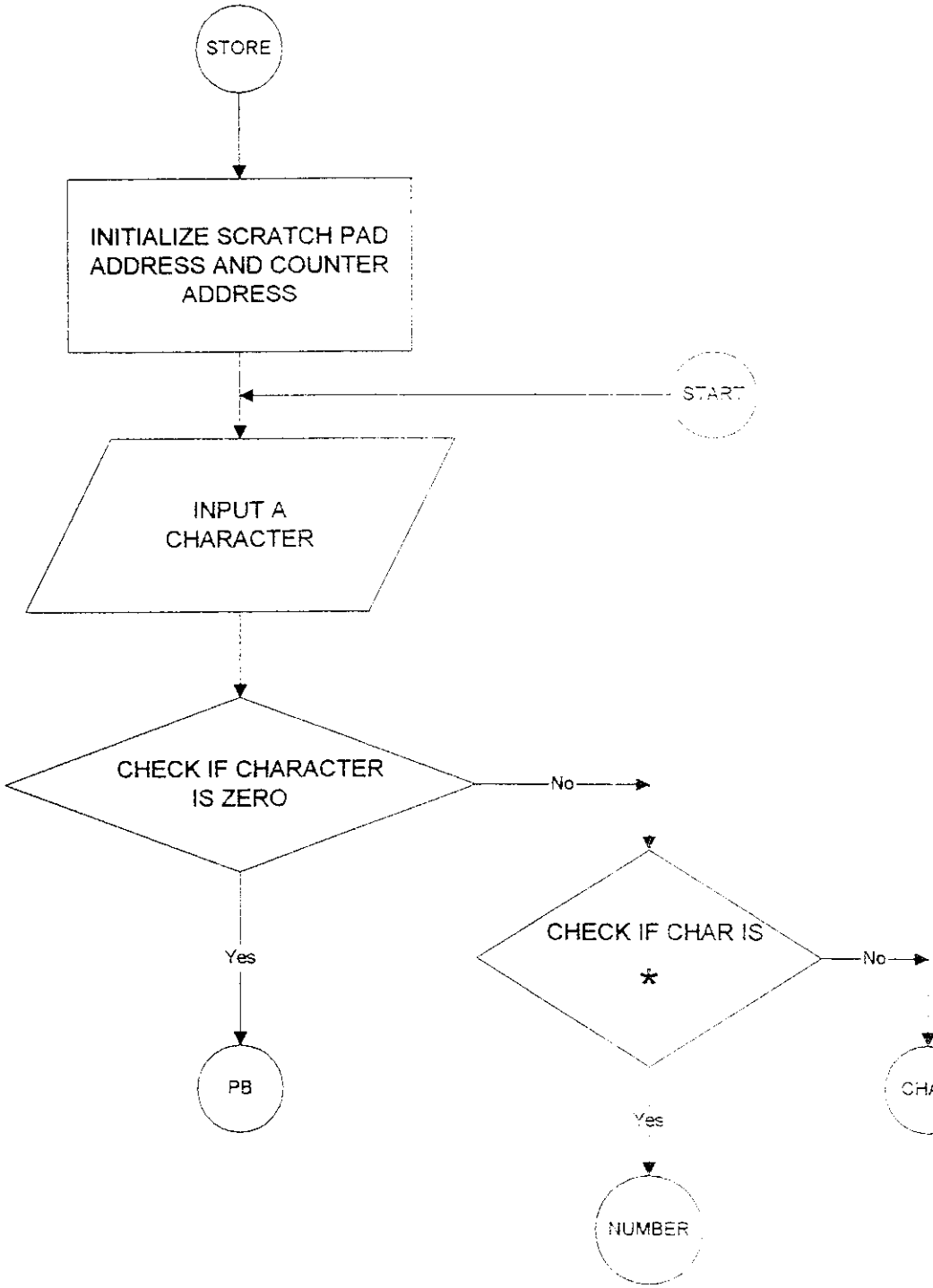
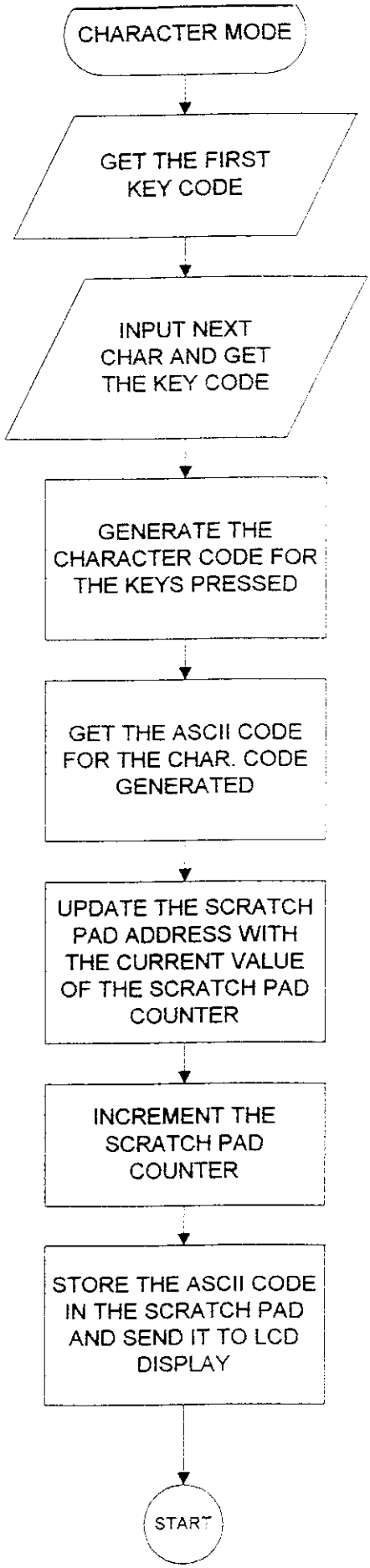
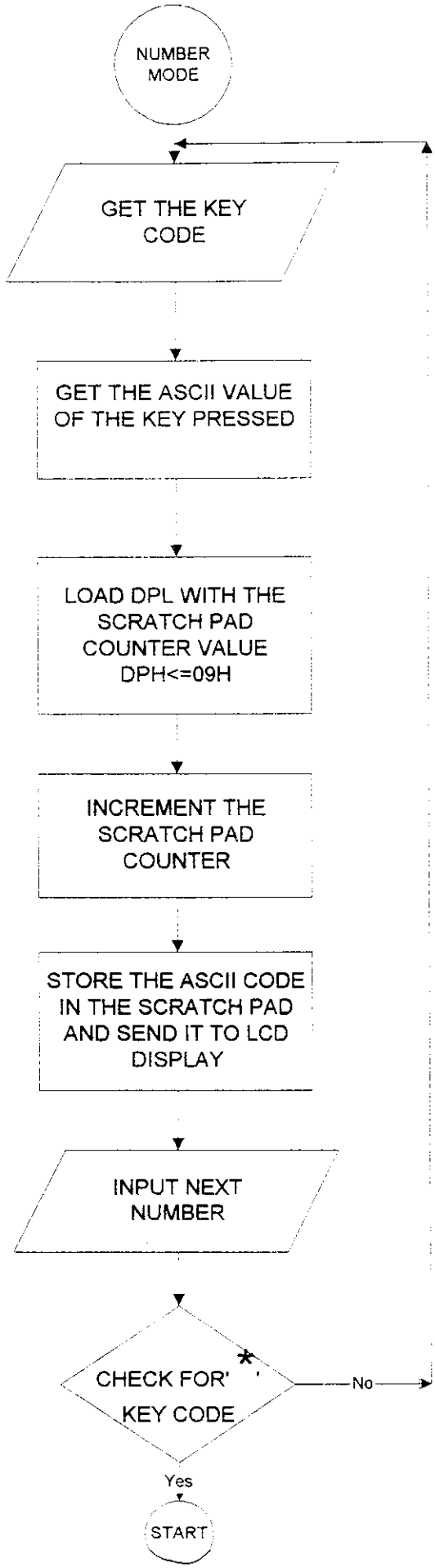


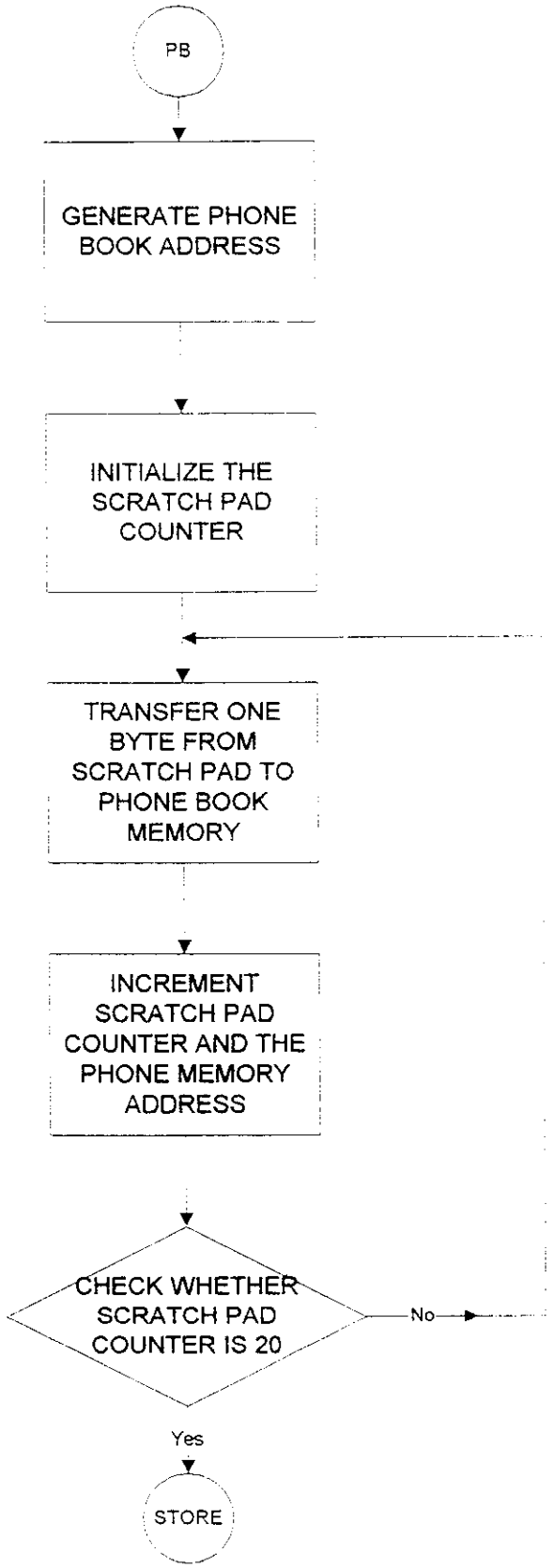
FIG: 6.2


STORE
INITIALIZE SCRATCH PAD ADDRESS AND COUNTER ADDRESS
START
INPUT A CHARACTER
CHECK IF CHARACTER IS ZERO
No
Yes
PB
CHECK IF CHAR IS
*
No
Yes
NUMBER

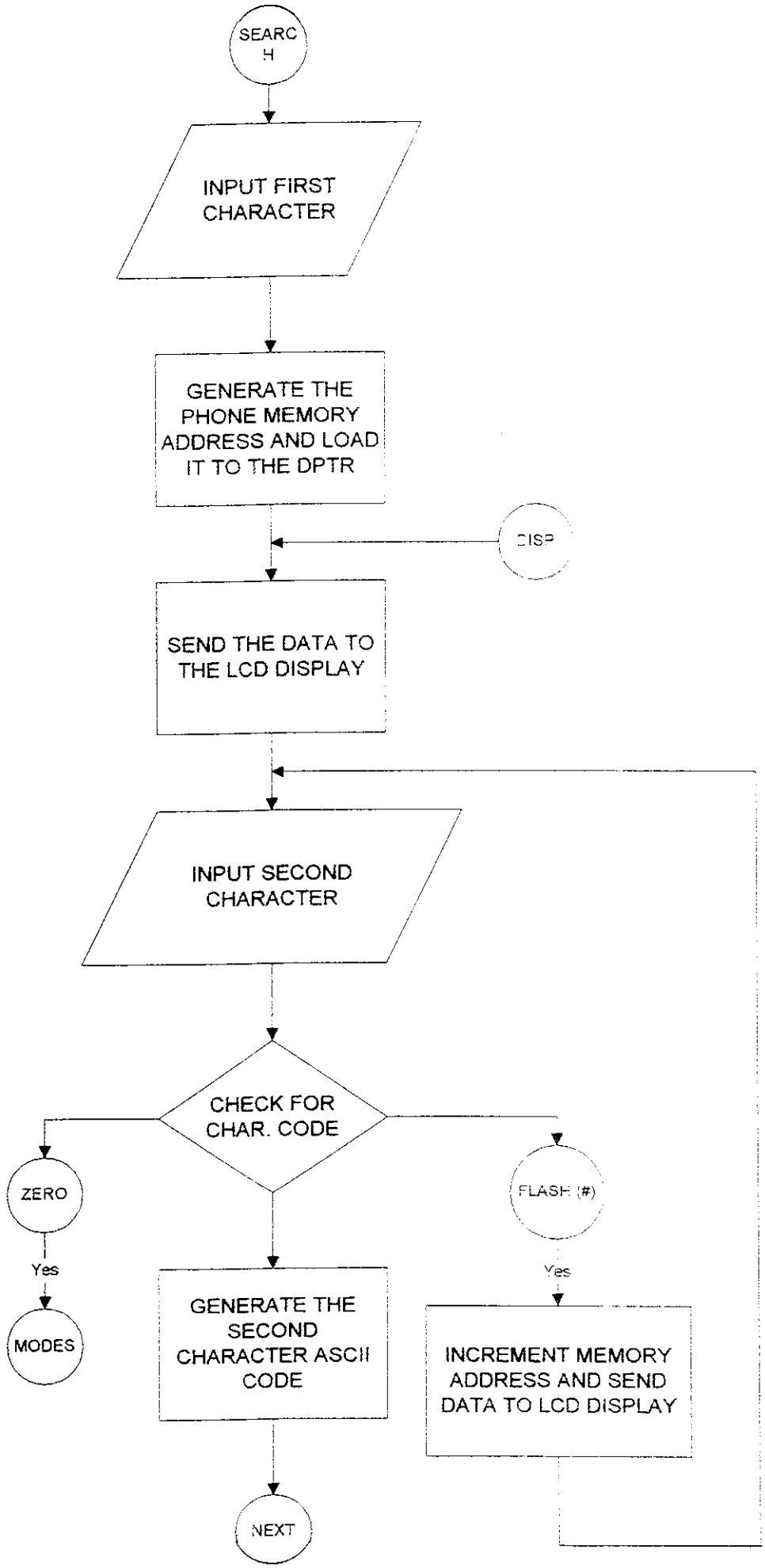
STORE MODE

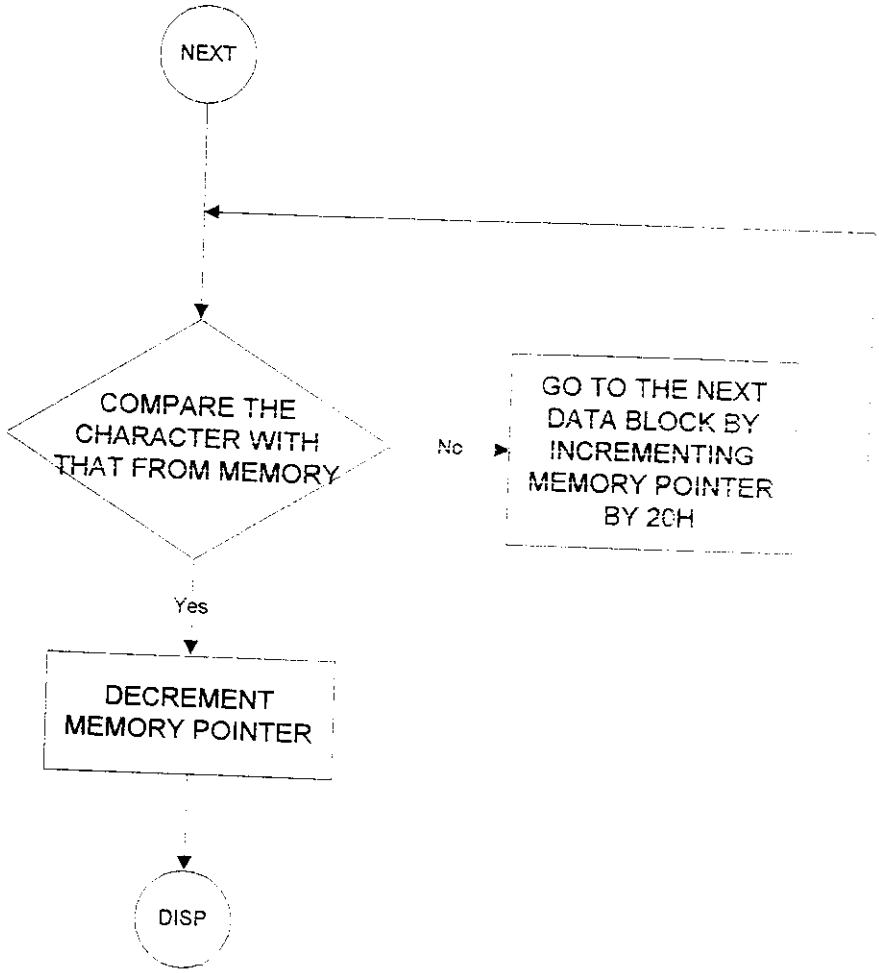

CHARACTER MODE
GET THE FIRST KEY CODE
INPUT NEXT CHAR AND GET THE KEY CODE
GENERATE THE CHARACTER CODE FOR THE KEYS PRESSED
GET THE ASCII CODE FOR THE CHAR. CODE GENERATED
UPDATE THE SCRATCH PAD ADDRESS WITH THE CURRENT VALUE OF THE SCRATCH PAD COUNTER
INCREMENT THE SCRATCH PAD COUNTER
STORE THE ASCII CODE IN THE SCRATCH PAD AND SEND IT TO LCD DISPLAY
START


NUMBER MODE
GET THE KEY CODE
GET THE ASCII VALUE OF THE KEY PRESSED
LOAD DPL WITH THE SCRATCH PAD COUNTER VALUE DPH<=09H
INCREMENT THE SCRATCH PAD COUNTER
STORE THE ASCII CODE IN THE SCRATCH PAD AND SEND IT TO LCD DISPLAY
INPUT NEXT NUMBER
CHECK FOR' * ' KEY CODE
No
Yes
START


PB
GENERATE PHONE BOOK ADDRESS
INITIALIZE THE SCRATCH PAD COUNTER
TRANSFER ONE BYTE FROM SCRATCH PAD TO PHONE BOOK MEMORY
INCREMENT SCRATCH PAD COUNTER AND THE PHONE MEMORY ADDRESS
CHECK WHETHER SCRATCH PAD COUNTER IS 20
No
Yes
STORE

SEARCH


SEARCH
INPUT FIRST CHARACTER
GENERATE THE PHONE MEMORY ADDRESS AND LOAD IT TO THE DPTR
DISP
SEND THE DATA TO THE LCD DISPLAY
INPUT SECOND CHARACTER
CHECK FOR CHAR. CODE
ZERO
Yes
MODES
GENERATE THE SECOND CHARACTER ASCII CODE
NEXT
FLASH (#)
Yes
INCREMENT MEMORY ADDRESS AND SEND DATA TO LCD DISPLAY


NEXT
COMPARE THE CHARACTER WITH THAT FROM MEMORY
No
GO TO THE NEXT DATA BLOCK BY INCREMENTING MEMORY POINTER BY 20H
Yes
DECREMENT MEMORY POINTER
DISP

HOW TO USE THE PHONE BOOK ?

To enter into the phone book mode press the PROGRAM key. The message B P L will now be displayed on the LCD screen. From here the User can select one of the two options given below,

- STORE
- SEARCH and SCROLL

STORE MODE:

The phone book memory has the capacity to store 32 names/numbers starting with each alphabets.

For entering this mode press '1' when B P L is displayed.

The symbol '?' will now be displayed in the LCD screen.

Enter the names using the key combination for various characters. This will be displayed in the first row of the display.

To enter the numbers Press '*' key.

Then enter the numbers. To terminate this Number mode again Press '*' key again.

To save the Data in the phone book memory press 'R' key.

Now to exit the mode press '0' key or else enter the next data to be stored.

The system will go back to the normal mode if the memory allocated for a specific alphabet is full.

Irrespective of whether the numbers or characters entered first they will be displayed in the second and first rows of the LCD screen respectively.

SEARCH AND SCROLL MODE:

To enter this mode press '2' when 'B P L' is displayed.

Now '#' will be displayed.

Press the key combination of the first character of the name to be searched. The LCD screen will now display the first name of the desired alphabet block.

To scroll down this block press the 'FLASH' key.

To search for the second character press the corresponding key combination.

To continue searching press the second character's key combination until the desired name is reached.

Once the desired name is reached press the 'SPEED DIAL' key to dial the number. The system will go into the normal console operation once dialing is performed.

To exit this mode, otherwise, press '0'.

KEY COMBINATION FOR CHARACTERS:

	1	2	3
1	**A**	**B**	**C**
2	**D**	**E**	**F**
3	**G**	**H**	**I**
4	**J**	**K**	**L**
5	**M**	**N**	**O**
6	**P**	**Q**	**R**
7	**S**	**T**	**U**
8	**V**	**W**	**X**
9	**Y**	**Z**	

For any other combination of keys the blank code 20H will be generated.

CONCLUSION

An important design objective was to develop an Operator Console that would comply with the high standards expected by the user. This was made possible by incorporating some of the latest trends in hardware design.

The addition of the novel Phonebook makes it more user-friendly and serves as a first step towards intelligence. This can be used as a platform for developing consoles of the future with Voice recognized operations and Automatic features.

The designed console will serve to its potential when used with the Prodigy small EPABXs and is found to conform to the design objectives and the industrial standards.

INSTRUCTIONS OF LCD MODULE

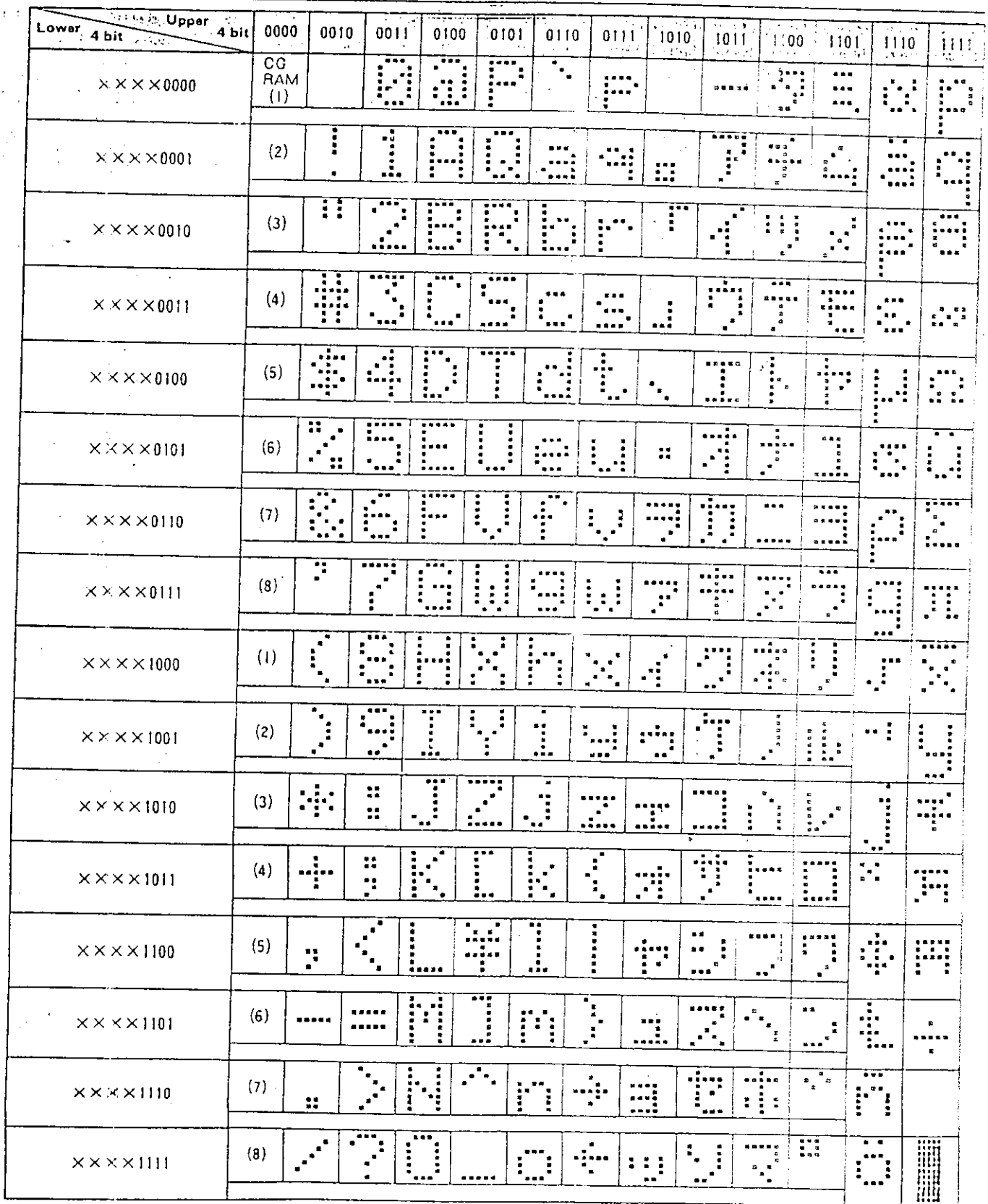
Instruction	Code										Description	Execute Time (max.)
	RS	R/W	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0		
Clear Display	0	0	0	0	0	0	0	0	0	1	Clears all display and returns the cursor to the home position (Address 0).	1.64mS
Cursor At Home	0	0	0	0	0	0	0	0	1	*	Returns the cursor to the home position (Address 0). Also returns the display being shifted to the original position. DD RAM contents remain unchanged.	1.64mS
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets the cursor move direction and specifies or not to shift the display. These operations are performed during data write and read.	40μS
Display On/Off Control	0	0	0	0	0	0	1	D	C	B	Sets ON/OFF of all display (D) cursor ON/OFF (C), and blink of cursor position character (B).	40μS
Cursor/Display Shift	0	0	0	0	0	1	S/C	R/L	*	*	Moves the cursor and shifts the display without changing DD RAM contents.	40μS
Function Set	0	0	0	0	1	DL	N	F	*	*	Sets interface data length (DL) number of display lines (L) and character font (F).	40μS
CG RAM Address Set	0	0	0	1	ACG						Sets the CG RAM address. CG RAM data is sent and received after this setting.	40μS
DD RAM Address Set	0	0	1	ADD							Sets the DD RAM address. DD RAM data is sent and received after this setting	40μS
Busy Flag/ Address Read	0	1	BF	AC							Reads Busy flag (BF) indicating internal operation is being performed and reads address counter contents.	40μS
CG RAM/DD RAM Data Write	1	0	WRITE DATA								Writes data into DD RAM or CG RAM.	40μS
CG RAM/DD RAM Data Read	1	1	READ DATA								Reads data from DD RAM or CG RAM.	40μS

■ NOTE:

Code	Description	Execute Time (max.)
I/D = 1: Increment I/D = 0: Decrement S = 1: With display shift S/C = 1: Display shift S/C = 0: Cursor movement R/L = 1: Shift to the right R/L = 0: Shift to the left DL = 1: 8-bit DL = 0: 4-bit N = 1: 2 lines N = 0: 1 line F = 1: 5 x 10 dots F = 0: 5 x 7 dots BF = 1: Internal operation is being performed. BF = 0: Instruction acceptable.	DD RAM: Display Data RAM CG RAM: Character Generator RAM ACG: CG RAM Address ADD: DD RAM Address Corresponds to cursor address. AC: Address Counter, used for both DD RAM and CG RAM * : Invalid	fcp or fosc = 250 kHz However, when frequency changes, execution time also changes. Ex. When fcp or fosc = 270 kHz, $40\mu S \times \frac{250}{270} = 37\mu S$

■ NOTE: For details in program, refer to the User's Manual which is separately provided.

CHARACTER FONT TABLE (Correspondence between Characters Codes and Character Pattern)



* CG RAM: Character pattern area which can freely be rewritten by program.

MC34118

Specifications and Applications Information

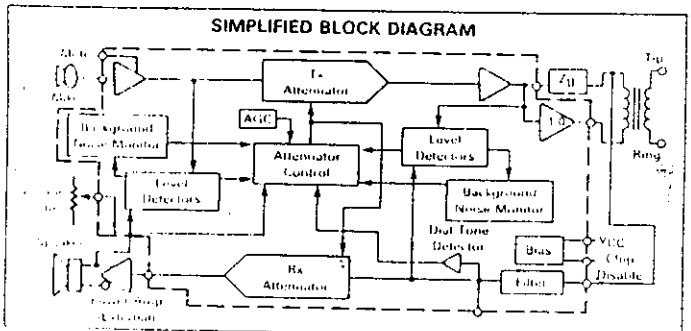
VOICE SWITCHED SPEAKERPHONE CIRCUIT

The MC34118 Voice Switched Speakerphone Circuit incorporates the necessary amplifiers, attenuators, level detectors, and control algorithm to form the heart of a high quality hands free speakerphone system. Included are a microphone amplifier with adjustable gain and MUTE control, Transmit and Receive attenuators which operate in a complementary manner, level detectors at both input and output of both attenuators, and background noise monitors for both the transmit and receive channels. A Dial Tone Detector prevents the dial tone from being attenuated by the Receive background noise monitor circuit. Also included are two line driver amplifiers which can be used to form a hybrid network in conjunction with an external coupling transformer. A high pass filter can be used to filter out 60 Hz noise in the receive channel, or for other filtering functions. A Chip Disable pin permits powering down the entire circuit to conserve power on long loops where loop current is at a minimum.

The MC34118 may be operated from a power supply, or it can be powered from the telephone line, requiring typically 5.0 mA. The MC34118 can be interfaced directly to Tip and Ring (through a coupling transformer) for stand-alone operation, or it can be used in conjunction with a handset speech network and/or other features of a feature phone.

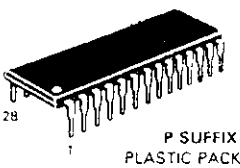
- Improved Attenuator Gain Range: 52 dB Between Transmit and Receive
- Low Voltage Operation for Line-Powered Applications (3.0 6.5 V)
- 4 Point Signal Sensing for Improved Sensitivity
- Background Noise Monitors for Both Transmit and Receive Paths
- Microphone Amplifier Gain Set by External Resistors — Mute Function Included
- Chip Disable for Active Standby Operation
- On Board Filter Pinned Out for User Defined Function
- Dial Tone Detector to Inhibit Receive Idle Mode During Dial Tone Presence
- Standard 28 Pin Plastic DIP Package and SOIC Package Available
- Compatible with MC34119 Speaker Amplifier

SIMPLIFIED BLOCK DIAGRAM



VOICE SWITCHED SPEAKERPHONE CIRCUIT

SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 710

DW SUFFIX
PLASTIC PACKAGE
CASE 751F

PIN CONNECTIONS

(Top View)

FO	1	28	GND
FI	2	27	CPR
CD	3	26	RLI1
VCC	4	25	RLO1
HTO	5	24	TLO1
HTO	6	23	TLI1
HTI	7	22	RXO
TXO	8	21	RXI
TXI	9	20	RLI2
MCO	10	19	RLO2
MCI	11	18	TLO2
MUT	12	17	TLI2
VLC	13	16	CPT
CT	14	15	VB

(Pin assignments same for both packages)

PIN DESCRIPTION

Pin	Name	Description
1	FO	Filter output. Output impedance is less than 50 ohms.
2	FI	Filter input. Input impedance is greater than 1.0 Mohm.
3	CD	Chip Disable. A logic low (< 0.8 V) sets normal operation. A logic high (>2.0 V) disables the IC to conserve power. Input impedance is nominally 90 kΩ.
4	V_{CC}	A supply voltage of + 2.8 to + 6.5 volts is required, at ≈ 5.0 mA. As V_{CC} falls from 3.5 to 2.8 volts, an AGC circuit reduces the receive attenuator gain by ≈ 25 dB (when in the receive mode).
5	HTO +	Output of the second hybrid amplifier. The gain is internally set at − 1.0 to provide a differential output, in conjunction with HTO −, to the hybrid transformer.
6	HTO −	Output of the first hybrid amplifier. The gain of the amp is set by external resistors.
7	HTI	Input and summing node for the first hybrid amplifier. DC level is ≈V_B.
8	TXO	Output of the transmit attenuator. DC level is approximately V_B.
9	TXI	Input to the transmit attenuator. Max. signal level is 350 mVrms. Input impedance is ≈10 kΩ.
10	MCO	Output of the microphone amplifier. The gain of the amplifier is set by external resistors.
11	MCI	Input and summing node of the microphone amplifier. DC level is ≈ V_B.
12	MUT	Mute input. A logic low (<0.8 V) sets normal operation. A logic high (>2.0 V) mutes the microphone amplifier without affecting the rest of the circuit. Input impedance is nominally 90 kΩ.

Pin	Name	Description
13	VLC	Volume control input. When VLC = V_B, the receive attenuator is at maximum gain when in the receive mode. When VLC = 0.3 V_B, the receive gain is down 35 dB. Does not affect the transmit mode.
14	C_T	An RC at this pin sets the response time for the circuit to switch modes.
15	V_B	An output voltage ≈V_{CC}/2. This voltage is a system ac ground, and biases the volume control. A filter cap is required.
16	CPT	An RC at this pin sets the time constant for the transmit background monitor.
17	TLI2	Input to the transmit level detector on the mike/speaker side.
18	TLO2	Output of the transmit level detector on the mike/speaker side, and input to the transmit background monitor.
19	RLO2	Output of the receive level detector on the mike/speaker side.
20	RLI2	Input to the receive level detector on the mike/speaker side.
21	RXI	Input to the receive attenuator and dial tone detector. Max input level is 350 mV RMS. Input impedance is ≈10 kΩ.
22	RXO	Output of the receive attenuetor. DC level is approximately V_B.
23	TLI1	Input to the transmit level detector on the line side.
24	TLO1	Output of the transmit level detector on the line side.
25	RLO1	Output of the receive level detector on the line side, and input to the receive background monitor.
26	RLI1	Input to the receive level detector on the line side.
27	CPR	An RC at this pin sets the time constant for the receive background monitor.
28	GND	Ground pin for the entire IC.

Note: Pin numbers are identical for the DIP package and the SOIC package.

CMOS Quad Bilateral Switch

For Transmission or Multiplexing of Analog or Digital Signals

High-Voltage Types (20-Volt Rating)

The RCA-CD4066B is a quad bilateral switch intended for the transmission or multiplexing of analog or digital signals. It is pin-for-pin compatible with RCA-CD4016B, but exhibits a much lower on-state resistance. In addition, the on-state resistance is relatively constant over the full input-signal range.

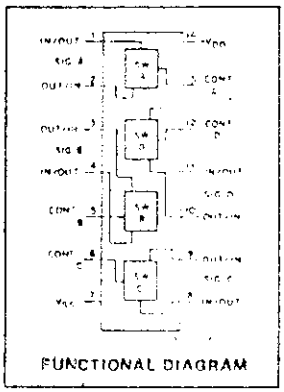
The CD4066B consists of four independent bilateral switches. A single control signal is required per switch. Both the p and the n device in a given switch are biased on or off simultaneously by the control signal. As shown in Fig.1, the well of the n-channel device on each switch is either tied to the input when the switch is on or to V_{SS} when the switch is off. This configuration eliminates the variation of the switch-transistor threshold voltage with input signal, and thus keeps the on-state resistance low over the full operating-signal range.

The advantages over single-channel switches include peak input-signal voltage swings equal to the full supply voltage, and more constant on-state impedance over the input-signal range. For sample-and-hold applications, however, the CD4016B is recommended.

The CD4066B is available in 14-lead ceramic dual-in-line packages (D and F suffixes), 14-lead plastic dual-in-line packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- 15-V digital or ±7.5-V peak-to-peak switching
- 125Ω typical on-state resistance for 15-V operation
- Switch on-state resistance matched to within 5 Ω over 15-V signal-input range
- On-state resistance flat over full peak-to-peak signal range
- High on/off output-voltage ratio: 80 dB typ. @ f_{is} = 10 kHz, R_L = 1 kΩ
- High degree of linearity: <0.5% distortion typ. @ f_{is} = 1 kHz, V_{is} = 5 Vp-p, $V_{DD} - V_{SS} \geq 10$ V, R_L = 10 kΩ
- Extremely low off-state switch leakage resulting in very low offset current and high effective off-state resistance: 10 pA typ. @ $V_{DD} - V_{SS}$ = 10 V, T_A = 25°C
- Extremely high control input impedance (control circuit isolated from signal circuit): 10^{12} Ω typ.
- Low crosstalk between switches: −50 dB typ. @ f_{is} = 8 MHz, R_L = 1 kΩ
- Matched control-input to signal-output capacitance: Reduces output signal transients
- Frequency response, switch on = 40 MHz (typ.)
- 100% tested for quiescent current at 20 V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No.13A, "Standard Specifications for Description of "B" Series CMOS Devices"



FUNCTIONAL DIAGRAM

Applications:

- Analog signal switching/multiplexing
  Signal gating — Modulator
  Squelch control — Demodulator
  Chopper — Commutating switch
- Digital signal switching/multiplexing
- Transmission-gate logic implementation
- Analog-to-digital & digital-to-analog conversion
- Digital control of frequency, impedance, phase, and analog-signal gain

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)	0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS	0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT (except for TRANSMISSION GATE which is 25 mA)	±10 mA
POWER DISSIPATION PER PACKAGE (P_D)	
For T_A = −40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D, F, K)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A)	
PACKAGE TYPES D, F, K, H	−55 to +125°C
PACKAGE TYPE E	−40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg})	−65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	3	18	V

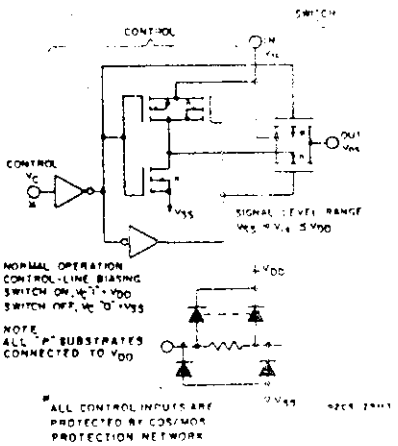


Fig.1 – Schematic diagram of 1 of 4 identical switches and its associated control circuitry.

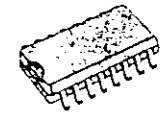
SGS-THOMSON MICROELECTRONICS

TEA7532

MONITOR AMPLIFIER

- PROGRAMMABLE GAIN IN STEPS OF 6 dB
- ON/OFF POSITION
- LOW VOLTAGE
- POWER : 100 mW AT 5 V

DIP16



SO16

ORDERING NUMBERS : TEA7532DP (DIP16)
TEA7532FP (SO16)

DESCRIPTION

This 16 pins IC is designed for monitor (loudspeaker) telephone set and provides :

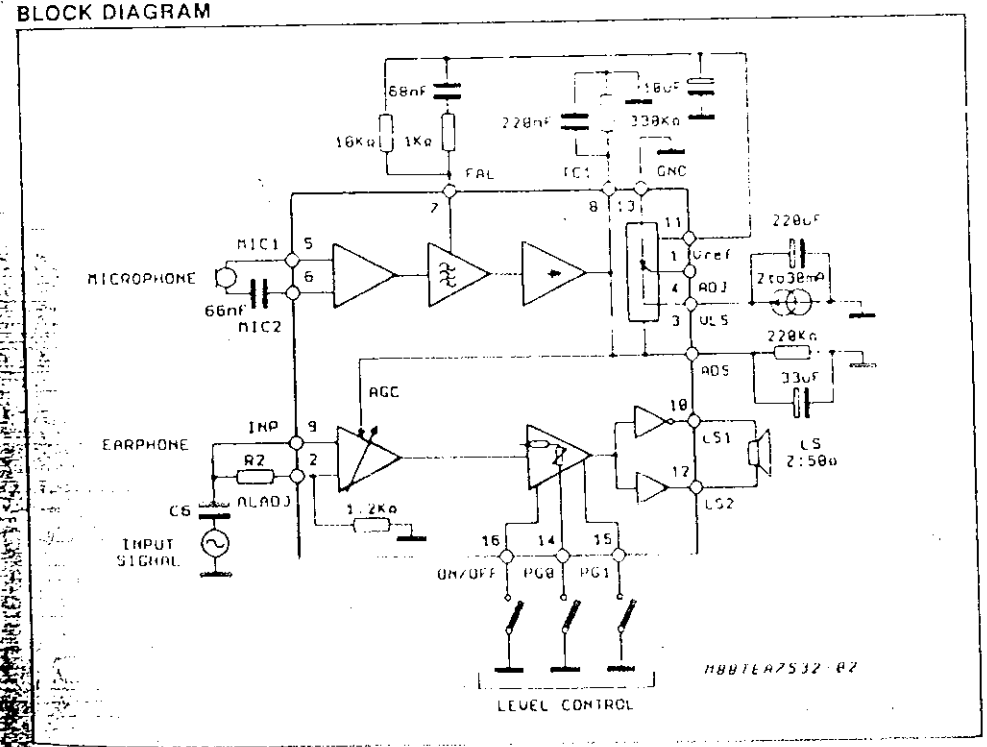
a) Signal amplification for monitoring (loudspeaker)

b) Antiacoustic feedback (antilarsen)

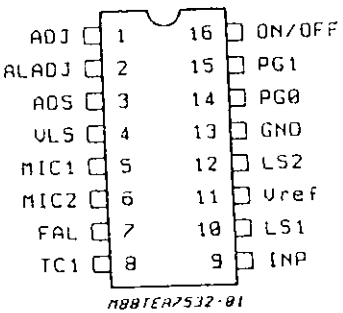
c) Antidistortion by automatic gain adaptation

d) Antilarsen adjustment (full duplex)

BLOCK DIAGRAM



N CONNECTION (Top view)



PIN CONNECTION (Top view)

PIN DESCRIPTION

N°	Symbol	Description
1	ADJ	Adjust Internal Reference V_{LS}
2	ALADJ	Antilarsen Adjustement
3	ADS	Antidistorsion
4	V_{LS}	Supply
5	MIC1	Microphone Input
6	MIC2	Microphone Input
7	FAL	Antilarsen Filter
8	TC1	Antilarsen Time Constant
9	INP	Input Signal
10	LS1	Output Loudspeaker 1
11	V_{REF}	Internal Resistance
12	LS2	Output Loudspeaker 2
13	GND	Ground
14	PG0	Inputs Program Level to Loudspeaker
15	PG1	
16	ON/OFF	

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
T_{op}	Temperature Range	-5 to + 45	°C
V_{LS}	Supply Voltage	6	V
I_{LS}	Supply Current for T > 300ms for T ≤ 300ms	30 150	mA mA
V_i	Voltage Level pins, PG0, PG1, on/off	-0.6 < V_S < 0.6	V

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, I_{LS} = 30mA unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{LS1}	V_{LS} Supply	I_{LS} = 2mA (fig. 7) I_{LS} = 30mA (fig. 7)	2.6	3.0 3.15	3.4 3.4	V V
V_{LSM}	V_{LS} Maximum	$I_{pin\ 1}$ = 50uA (fig. 7 ; So = closed)			5.5	V
V_{ADJ}	Voltage Pin 1	I_{LS} = 2mA to 30mA (fig. 7)	1.1	1.25	1.4	V
G	Loudspeaker Amplifier Gain = $\frac{V_{10} - V_{12}}{V_9}$	ON/OFF / PG0 / PG1				
G000		GND / GND / GND	12	14	16	dB
G001		GND / GND / V_{LS}	18	20	22	dB
G010		GND / V_{LS} / GND	24	26	28	dB
G011		GND / V_{LS} / V_{LS}	30	32	34	dB
G100		V_{LS} / X / X		- 30	- 20	dB
THD	Distortion	f = 300Hz to 2kHz, $V_{10} - V_{12}$ = 0.8V_{rms}, G = G011, (fig. 8)			2	%
G2	(V(10) – V(12))/V2	$P_{G0} = P_{G1} = V_{LS}$, V_9 = 0.8V (fig. 8)	30	32	34	dB
Z_{MICIN}	Microphone Input	Symetrical at (pins 5-6) Asymetrical at (pin 6) fig. 9		4.5		kΩ
Z_{INPIN}	Earphone Input	(fig. 9)	2.2	2.8	3.4	kΩ
Z_{IN2}	Antilarsen Adjustment Input		1	1.2	1.45	kΩ
V_{OFFS}	Ouput Offset $\lvert V_{(10)} - V_{(12)} \rvert$	G011 ; (fig. 8)	- 50		50	mV
$I_{ON/OFF}$ I_{PG0} I_{PG1}	Input Current ON State	V_{PG1} = 0V ; (fig. 8)	- 10 - 10 - 10	- 5 - 5 - 5		µA µA µA
$I_{ON/OFF}$ I_{PG0} I_{PG1}	Input Current OFF State	$V_{PG1} = V_{LS}$; (fig. 8)			1 1 1	µA µA µA
$V_{IL\ ON/OFF}$ $V_{IL\ PG0}$ $V_{IL\ PG1}$	Input Voltage ON State				0.45 0.45 0.45	V V V
$V_{IH\ ON/OFF}$ $V_{IH\ PG0}$ $V_{IH\ PG1}$	Input Voltage OFF State		1.5 1.5 1.5			V V V
G_{MIC}	Microphone Gain = $V_{(7)}/(V_{5} - V_{6})$	V_{MIC} = 10mV_{rms}, f = 2kHz (fig. 10)	22.5	23.5	24.5	dB
V_9	Voltage Pin 3		0.48	0.67	0.75	V
G_{ATT}	Loudspeaker Attenuated Gain = $\lvert V_{(10)} - V_{(12)} \rvert / V_{(9)}$	G011 ; V_9 = 0.6V ; (fig. 10) G011 ; V_9 = 0.4V ; (fig. 10)	20	- 30 30	- 20	dB dB

FUNCTIONAL DESCRIPTION

TEA7532 performs the following functions :

The circuit amplifies the incoming signal and feeds to the loudspeaker. PG0 and PG1 inputs are used to set the loudspeaker gain in a range of 32dB to 8dB in 6dB steps.

The TEA7532 inputs (PG0, PG1, ON/OFF) permit the loudspeaker to be cut-off thus ensuring privacy of communication.

- The antilarsen (antiacoustic feedback) system is incorporated.
- The maximum power available on a 50Ω impedance loudspeaker is 25mW at 3 volts and 100mW at 5V.

Limit values for external components :
R3 min = 5 kΩ (R3 adjust VLS), R7 max = 390 kΩ,
R6 min = R7/35
R max between pin 5 and 6 = 10kΩ - C min = 10nF