1. Over Head Cleaner Controller
2. Telemetry - Wireless Channel For Instrumentation

PROJECT REPORT

Submitted by

S. K. Santha Lakshmi
R. Kavitha Rani
V. Sudha Rani
S. Subha Lakshmi

Guided by

Ms. Latha B.E.,
Lecturer in ECE

Sponsored by

Mr. Aravind Venkatachalam M.D.
Freeway Electronics Pvt LTD.

IN PARTIAL FULFILMENT OF THE REQUIREMENTS
FOR THE AWARD OF THE DEGREE OF
BACHELOR OF ENGINEERING
IN ELECTRONICS AND COMMUNICATION ENGINEERING
OF THE BHARATHIAR UNIVERSITY

1998 - 1999

Department of Electronics and Communication Engineering

Kumaraguru College of Technology

Coimbatore-641 006

Department of Electronics and Communication Engineering

Kumaraguru College of Technology

Coimbatore 641 006

Certificate

This is to certify that the Report entitled

1. Over Head Cleaner Controller
2. Telemetry–Wireless Channel for Instrumentation

has been submitted by

R. KAVITHA RANI S. SUBHALAKSHMI

Mr./Ms. S.K. SANTHA LAKSHMI ..... A.SUDHA RAJ .....

In partial fulfillment for the award of Bachelor of Engineering in Electronics and Communication Branch of Bharathiar University, Coimbatore–641 006 During the academic year 1998–1999

R. Lave 16/3/99

Guide

Head of the department

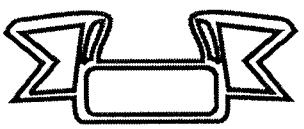
Date: 16.3.99

Certified that the candidate with University Registration No._____

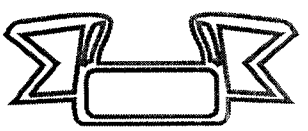
the project work viva–voce Examination held on _____

Internal Examiner 16/3

External Examiner



Certificate



Freeway Electronics Private Limited

Regd. Office : P. B. 1126, 507, D. B. Road, R. S. Puram, Coimbatore - 641 002. INDIA.
Phone : 0422 - 453109, 439726 Fax : 0422 - 450072 Grams : FREEWAY

Certificate

This is to certify that

V.Sudha Rani
S. Subhalakshmi
S.K.Santhalakshmi
R.Kavitha Rani

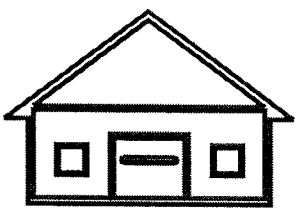
the students of **Kumaraguru College of Engineering,** E.C.E Branch have Completed their project works.

Telemetry - Wireless Channel for Instrumentation.
Overhead Cleaner Controller

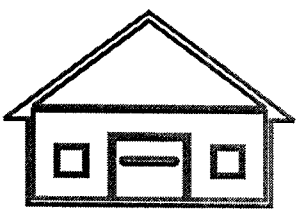
in our organisation on 08.03.99

We wish them all the best.

S.VENKATACHALAM
Director.



Dedicated to our
Beloved parents



ACKNOWLEDGEMENT

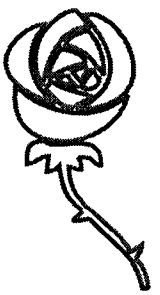
We thank our **Principal Dr. K.K. Padmanabhan B.sc. (Engg). , M.Tech. , Ph. D.** for his kind patronage and encouragement .

Our thanks to the **Head of the Department , Prof. M . Ramasamy M.E. , MEEE (USA) , M.I.E. , M.I.S.T.E. ,** for his support through out this project .

We express our sincere thanks to our beloved guide **Ms. R. Latha B.E. Lecturer , Department of Electronics and Communication Engineering** for her guidance and encouragement . We are very grateful to her for her technical ideas which made this project a success .

We extend our thanks to **Mr. Arvind Venkatachalam M.D. Freeway Electronics Pvt. Ltd., Coimbatore** for his valuable guidance during the course of our project .

This project was carried out under the overall guidance of **Mr. Balachandar , Freeway Electronics Pvt. Ltd.** we also acknowledge his help in the preparation of this project .



Synopsis

SYNOPSIS

In Textile industry , micro – controller based device used to suck the unwanted dust from the machine by blowing air . This improves the productivity and saves time .

The Over Head Cleaner is one such device designed around the versatile PIC16C54 micro – controller .

In Over Head Cleaner three relays are used , one for motor , one for blower and one for Forward / Reverse path .

The blower consists of a fan motor which blows the air and suck the unwanted cotton and dust . The motor starts travelling as soon as the unit is energized by three phase supply . The motor moves in the forward and reverse direction and this is sensed by proximity sensors . There are two proximity sensors and they are Discharge sensors & Reverse sensors .

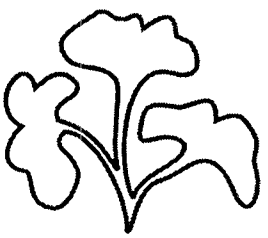
Discharge sensors is used to remove all the dust and unwanted cotton form the collection center .

Reverse sensor is used to sense when the motor wants to travel in the reverse direction .

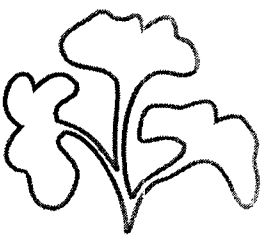
The microcontroller program written , automatically checks the sensor and work accordingly .

The motors , blower and forward / reverse path relay are controlled through contactors .

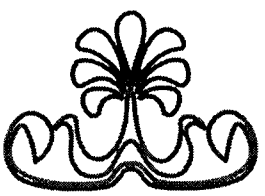
This Over Head Cleaner (OHC) improves the efficiency of mill due to its automatic working style .



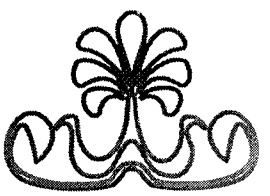
Contents



CONTENTS



Introduction



CHAPTER – 1

INTRODUCTION

Cotton , the raw material used by the textile industry is most variable in nature influenced by soil & climatic condition .

The development of series of instruments to specific properties of the same has been made long back & is being preferred by integrating latest innovations in electronics & measurements technologies today .

One of the problem faced by the spinning industry is the removal of cotton dusts produced after spinning .

The whole idea of developing a cleaning instrument & testing the same will help the textile industries , a lot .

Over head cleaner , as the name indicates is used for cleaning the cotton dusts by sucking it & also discharges the absorbed dust particles .

The micro controller , 16C54 is used for controlling the instrument .

Block diagram

CHAPTER - 2

BLOCK DIAGRAM OF OHC

2.1 DESCRIPTION OF BLOCK DIAGRAM

The important blocks are relays , contacts , controller box and switches .

MICROCONTROLLER (PICl6C54)

This is a low cost , high performance , 8 – bit , fully static CMOS microcontroller , PIC16C54 receives seven inputs which are

1. Start push button .
2. Stop push button .
3. Reverse push button .
4. Reverse delay .

5. Discharge delay .

6. Reverse sense .

7. Discharge sense .

Port B is input port and port A is output port . The output of the microcontroller drives three relays .

RELAYS

By installing relays at the operating points to do the heavy duty switching , the remote controls can be comparatively small and inexpensive since they handle light current for relay coils .

Three relays are installed here

1. For blower .
2. Travel ON or OFF .
3. Travel forward or reverse .

The relays drive a set of contacts which in turn control the motor operation .

DELAY FUNCTIONS

Reverse function has four delays

1. No delay .
2. 10 seconds .
3. 20 seconds .
4. 30 seconds .

The DCG function has four delays

1. 5 seconds .
2. 15 seconds .
3. 30 seconds .
4. 51 seconds .

2.2 OPERATION OF CIRCUIT DIAGRAM

The 440 volts AC supply is given to the primary of the transformer , this is step down to 12 volts by using a 12 volt step down transformer . This is given to a bridge rectifier to convert the AC to equivalent DC voltage . The output of the rectifier is fed to the

regulator IC7805 which provides a stable DC voltage for powering the microcontroller .

The output pins of the microcontroller 1, 18 and 17 are given to the driver IC ULN2003 which drives three relays one for Blower and the other two for Travel (one forward and the other reverse) . The relays in turn operate a setup contacts .

Two switches are provided in the controller box .

1. Reverse operation .
2. Discharge operation .

These switches have four positions each one of which corresponds to a particular delay .

The connections are made such that the following logic is obtained (refer fig. c) .

Logic		Reverse	Discharge
B_2	B_1		
0	0	No Delay	5 sec.
0	1	10 sec.	15 sec.
1	0	20 sec.	30 sec.
1	1	30 sec.	51 sec.

BLOCK DIAGRAM

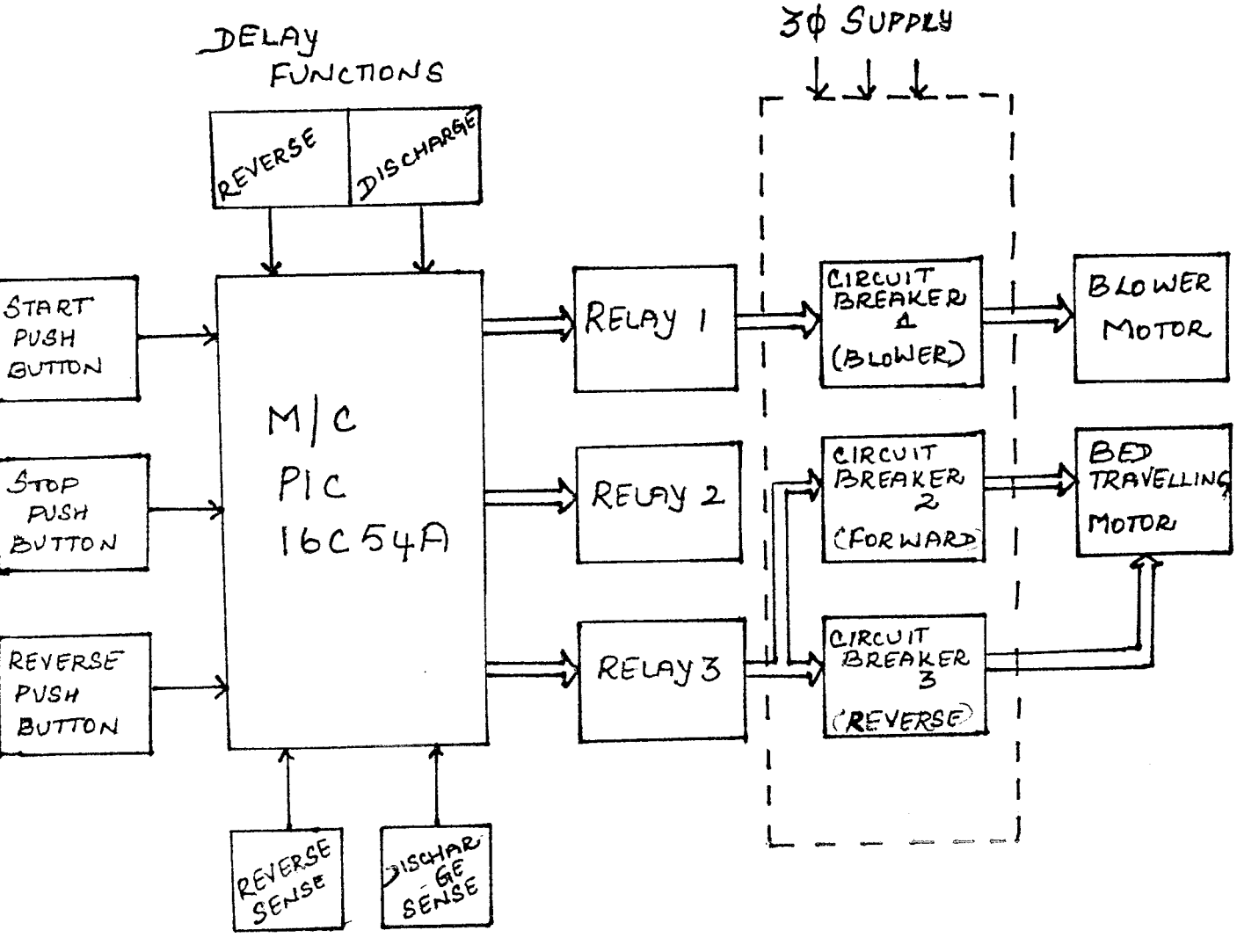
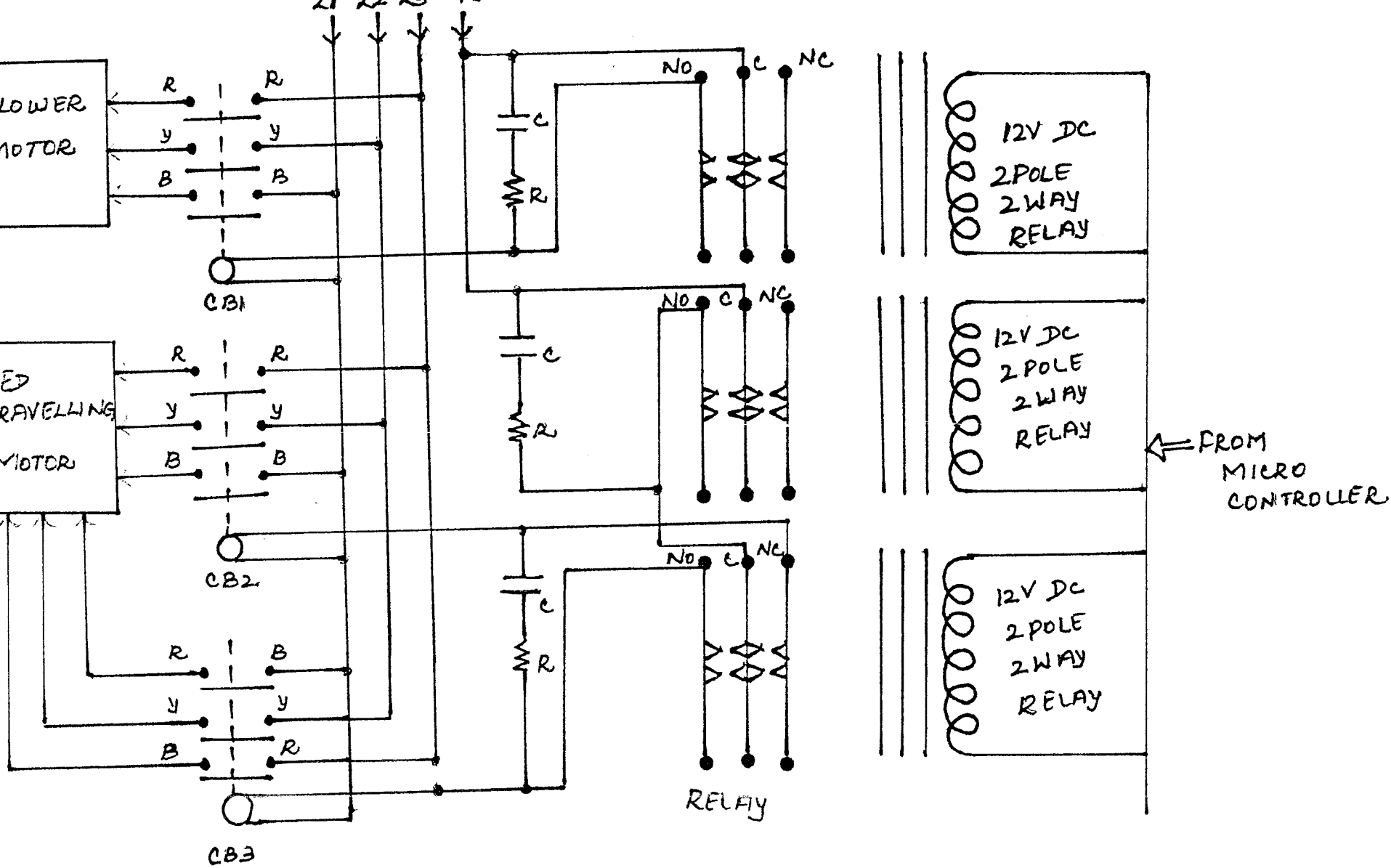


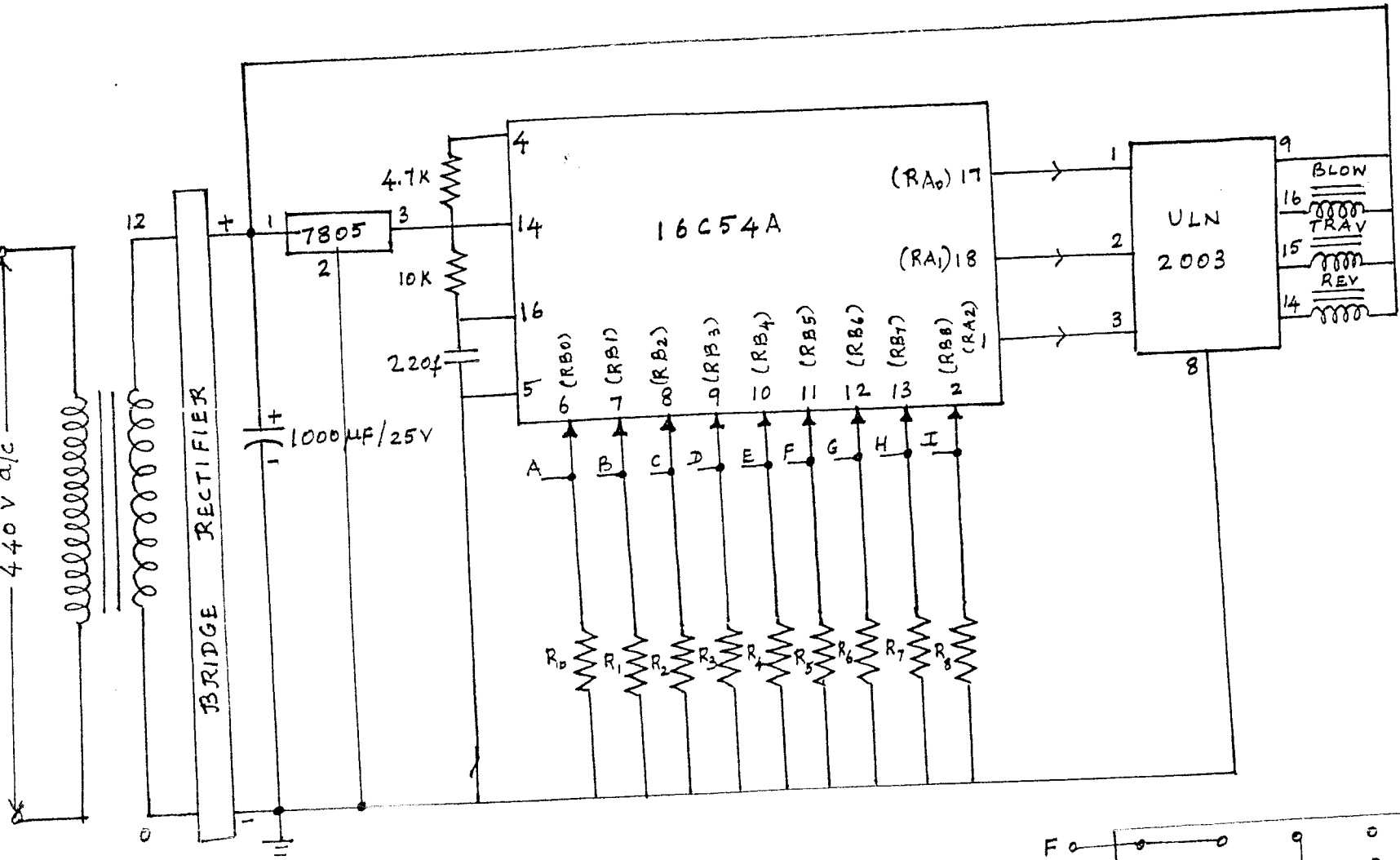
FIG:-(a)

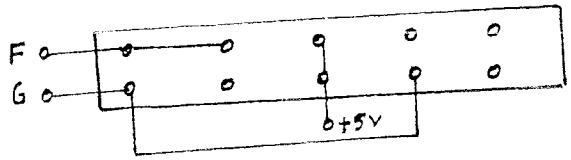


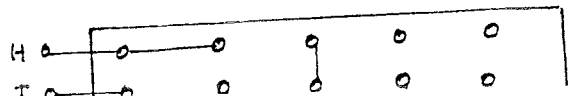
1, CB2 AND CB3 ARE CIRCUIT BREAKERS

FIG: (1)

CONTROLLER FIG:(c)



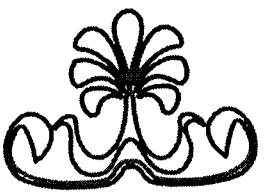




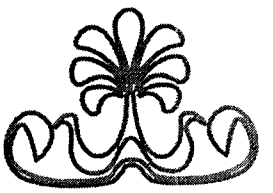
R0 - R8 - 470Ω /0.25W

A - START PB
B - STOP PB
C - REV PB

D - DCG SENSE
E - REV SENSE
F - REV DELAY (a)
G - REV DELAY (b)
H - DISCHARGE DELAY (a)



Micro controller



CHAPTER – 3

MICROCONTROLLER

3.1 DESCRIPTION OF MICROCONTROLLER (PIC16C54)

The enhanced PIC16C54 from a microchip technology is a family of low - cost , high performance , 8 – bit , fully static , EPROM / ROM based CMOS microcontrollers . This PIC16C54 is pin and software compatible with the family of devices in a new enhanced process technology . It employs a RISC architecture with only 33 single word / single cycle instructions . All the instructions are single cycle (200 ns) except for program branches which takes two cycles .

The PIC16C54 fits perfectly in application ranging from high speed automotive and appliance motor control to

lower power remote transmitters / receivers , pointing devices and telecom processors .

3.2 FEATURES

1. Pin compatible .
2. Only 33 single word instructions to learn .
3. All instructions are single cycle (200 ns) except for program branches which are two cycles .
4. Operating speed DC - 20 MHZ clock input
   DC - 200 ns instruction cycle .
5. 12 – bit wide instructions .
6. 8 – bit wide data path .
7. Seven (or) Eight special function hardware .
8. Addresses 512 x 12 program memory register .
9. Two level deep hardware stack .
10. Direct , indirect and relative addressing modes for data and instructions .
11. 12 I/O pins .
12. Low power consumption
    -< 2 mA typical @ 5 V , 4 MHZ .

13. Wide operating voltage range

    - ROM - 2.5 V to 6.25 V .

14. Maximum frequency of 20 MHZ .

15. Fully static design .

16. High speed CMOS EPROM / ROM technology .

    Peripheral features includes .

17. 8 – bit real time clock / counter with 8 – bit programmable prescaler .

18. Power – on – reset (POR) .

19. Device reset timer (DRT) .

20. Programmable watch dog timer (WDT) .

21. Programmable code - protection .

22. Power saving SLEEP MODE .

.3 PIN DESCRIPTION

PIC16C54A used in this system is a 18 – pin DIP package with V_{DD} = + 5 V . There are three I/O ports and they are

PORT A : pins 1 , 2 , 17 , & 18 .

PORT B : pins 6 to 13 .

PORT C : General Purpose Register

pin diagram of PIC16C54A is shown in fig .

PIN OUT DESCRIPTIONS

PORT PINS	NAMES	DESCRIPTION
17	RA0	
18	RA1	Bi – directional I/O port .
1	RA2	
2	RA3	
6	RB0	
7	RB1	
8	RB2	Bi – directional I/O port .
9	RB3	
10	RB4	
11	RB5	
12	RB6	

13	RB7	
3	TOCK1	Clock input to Timer 0, tied to V_{SS} or V_{DD} (or) used to reduce current consumption .
4	$\overline{MCLR}$ / V_{PP}	Master clear (reset) input / programming voltage input .
16	OSC1 / CLKIN	Oscillator crystal input / external clock source input .
15	OSC2 / CLKOUT	Oscillator crystal output / clock output .
14	V_{DD}	Positive supply for logic & I/O pins .
5	V_{SS}	Ground reference for logic & I/O pins .

3.4 ARCHITECTURE OF PIC16C54A

(Fig d).

ARITHMATIC AND LOGIC UNIT (ALU)

1. 8 – bit wide .
2. Capable of addition , subtraction , shift and logical operations .
3. Depending on the instructions executed , the ALU may effect the values of the carry (C) , Digit carry (DC) , and zero (Z) bits in the STATUS register .

WORKING REGISTER

1. 8 – bit working register used for ALU operations .
2. Not an addressable register .

GENERAL PURPOSE REGISTER

1. 25 general purpose register .
2. They are used for data and control information under command of the instructions .
3. Register file is accessed either directly or indirectly through file select register .

SPECIAL FUNCTION REGISTER

1. Seven special function register .
2. They include TMRO register , program counter (PC) , status register , I/O register and file select register .
3. Used to control the operations of the devices, used by CPU and peripheral functions .

STATUS REGISTER

1. This register contains the arithmetic status of the ALU and the RESET status and the page preselect bits

for program memories larger than 512 words .

OPTION REGISTER

1. It is a 6 – bit wide , write only register which contains various control bits to configure the Timer 0 / WDT prescaler .

PROGRAM COUNTER (PC)

1. It contains the address of the next program instructions to be executed .
2. 9 – bit register .

STACK

This device have a 9 – bit , 10 – bit or 11 – bit wide , two level hardware push / pop stack .

I / O PORTS

I/O register can be written and read under program control .

1. Port A
   i. 4 – bit I/O register .
   ii. RA3 – RA0 pins .
   iii. File address 05H
2. Port B
   i. 8 – bit I/O register .
   ii. RB0 – RB7 pins .
   iii. File address 06H .
3. Port C
   i. General purpose register .
   ii. File address 07H .
4. TRIS Register

   TRIS register are " write - only " and are set upon RESET .

MEMORY ORGANISATION

1. PIC16C54A memory is organized into program memory and data memory .
2. Program memory accessed using one or two STATUS register bits .
3. Data memory banks are accessed using FSR .

PROGRAM MEMORY ORGANISATION

PIC16C54A have a 9 – bit PC capable of addressing a 512 x 12 program memory space . The reset vector for this micro controller is at 1FFH .

DATA MEMORY ORGANISATION

Data memory is composed of registers are bytes of RAM . Therefore , data memory for a device is specified by its register file . The register file is divided into two functional groups .

1. Special function register .
2. General purpose register .

INDIRECT DATA ADDRESSING (INDF) & FSR REGISTER

1. INDF register is not a physical register .
2. Actually addresses the register whose address is contained in the FSR register .

TIMER0 MODULE AND TMR0 REGISTER

1. 8 – bit timer / counter register , TMR0 .
   - Readable and Writable .
2. 8 – bit software programmable scalar .
3. Internal or external clock select .
   - Edge select for external clock .

RESET

PIC16C54A may be reset in one of the following ways .

1. Power – ON – RESET (POR) .
2. $\overline{\text{MCLR}}$ reset (normal operation) .
3. $\overline{\text{MCLR}}$ wake-up reset (from SLEEP) .
4. WDT reset (normal operation) .
5. WDT wake-up reset (from SLEEP) .

POWER – ON – RESET

This provides an internal chip reset for most power – up situations . When the device starts normal operation , device operating parameters (voltage , frequency , temperature , etc.) must be met to ensure operation . If the condition are not met , the device must be held in reset until the operating conditions are met .

DEVICE RESET TIMER (DRT)

This provides a fixed 18 ms nominal time out on reset . The DRT operates on an internal RC oscillator .

WATCH DOG TIMER

It is a free running on – chip RC oscillator which does not require any external components . During normal operation or SLEEP , a WDT reset or wake-up reset generates a device RESET .

POWER – DOWN MODE (SLEEP)

A device may be powered down (SLEEP) and later powered up (wake-up from SLEEP) .

SLEEP

If enabled , the WDT will be cleared but keeps running , the $\overline{T_O}$ bit is set , $\overline{T_D}$ bit is cleared and oscillator a driver is turned off .

WAKE – UP FROM SLEEP

The device can wake-up from SLEEP through one of the following events .

1. An external reset input on $\overline{MCLR}$ / V_{PP} .
2. WDT time out reset .

The WDT is cleared when the device wakes from sleep , regardless of the wake-up source .

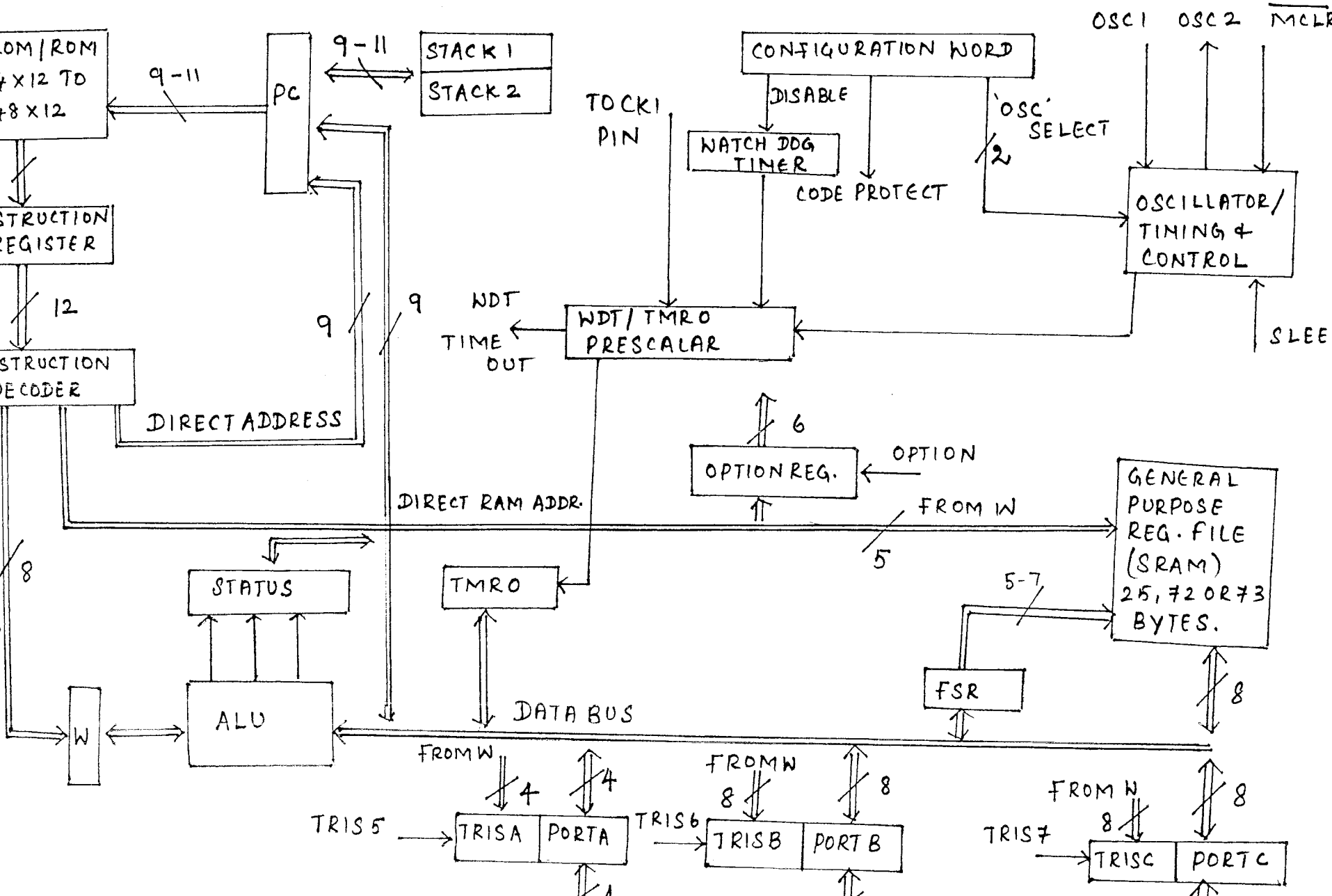
PIC16C5X COMPATIBILITY

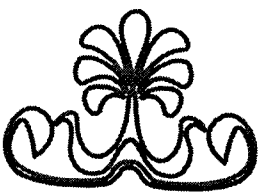
To convert code written for PIC16CXX to PIC16C54A , the user should take the following steps .

1. Check any CALL , GO TO instructions that modify the PC to determine if any program memory page select operations need to be made .
2. Revisit any computer jump operation to make sure page bits are set properly under the new scheme .
3. Eliminate any special function register page switching . Redefine data variables to reallocate them .
4. Verify all write to STATUS , OPTION and FSR segments

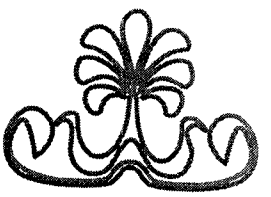
since these have changed .

5. Change reset vectors to proper for processor used .
6. Remove any use of ADDLW and SUBLW instructions .
7. Rewrite any code segment that use interrupts .


OSC1
OSC2
MCLR
CONFIGURATION WORD
DISABLE
'OSC' SELECT
2
OSCILLATOR/ TIMING & CONTROL
SLEE
TOCKI PIN
WATCH DOG TIMER
CODE PROTECT
PC
9-11
STACK 1
STACK 2
STRUCTION REGISTER
12
STRUCTION DECODER
DIRECT ADDRESS
9
WDT
TIME OUT
WDT/ TMR0 PRESCALAR
6
OPTION REG.
OPTION
DIRECT RAM ADDR.
FROM W
5
GENERAL PURPOSE REG. FILE (SRAM) 25, 72 OR 73 BYTES.
5-7
8
STATUS
TMR0
FSR
W
ALU
DATA BUS
FROM W
4
TRIS 5
TRISA
PORTA
TRIS 6
TRISB
PORT B
TRIS 7
TRISC
PORT C



Auxillary device



CHAPTER – 4

AUXILLARY DEVICES

4.1 RELAYS

A relay is a switch used to turn other circuits on or off . It is a transducer which changes an electrical signal to movement and then back to an electrical signal . It is useful if we want

1. a small current in one circuit to control another circuit containing a device such as a lamp or electric motor which needs a large current .
2. Several different switch contacts to be operated simultaneously .

The structure of a relay is shown in (fig e) with its symbol , the contacts may be normally open , normally closed or change over . When the controlling current flows through the coil , the soft iron core is temporarily magnetized and attracts the iron armature . This rocks on

its pivot and operates the contacts in the circuit being controlled . When the coil current stops , the armature is no longer attracted and the contacts return to their normal positions .

The current needed to operate a relay is called the pull – in – current , & the drop out current is the smaller current in the coil when the relay just stops working .

4.2 BRIDGE RECTIFIER

In a center tap full wave rectifier , only half of the secondary winding is used at any time and the transformer has to produce twice the voltage required . The problem does not arise if four diodes are arranged in a bridge network as in (fig f).

If A is positive with respect to B during the first half cycle . D_2 & D_4 conduct and current takes the path AD_2 R D_4B . On the next half cycle when B is positive , D_1 & D_3 are forward biased and current follows the path BD_3RD_1A . Once again the current through R is unidirectional during both half cycles of input and varying d.c output is obtained . This is a popular circuit because diodes are cheap .

All four diodes are available in one package , with two a.c input connections and two output connections .

4.3 VOLTAGE REGULATOR

The function of a voltage regulator is to provide a stable DC voltage for powering other electronic circuits . A voltage regulator is capable of providing substantial current . 7805 used here is a series regulator . Series regulators use a power transistor connected in series between the unregulated DC input and the load . The output voltage is controlled by the continuous voltage drop taking place across the series pass transistor . Since the transistor conducts in the active or linear region , these regulators are also called linear regulators . Linear regulators may have fixed or variable output voltage and could be positive or negative .

7805 is a three terminal , positive fixed voltage regulator . The last two numbers indicates the output voltage .

(Fig g) shows the standard representation of monolithic voltage regulator . A capacitor C_i (1 μF) is usually connected

between input terminal and ground to cancel the inductive effect due to long distribution leads . The output capacitor C_o (1 μF) improves the transient response .

BRIDGE RECTIFIER

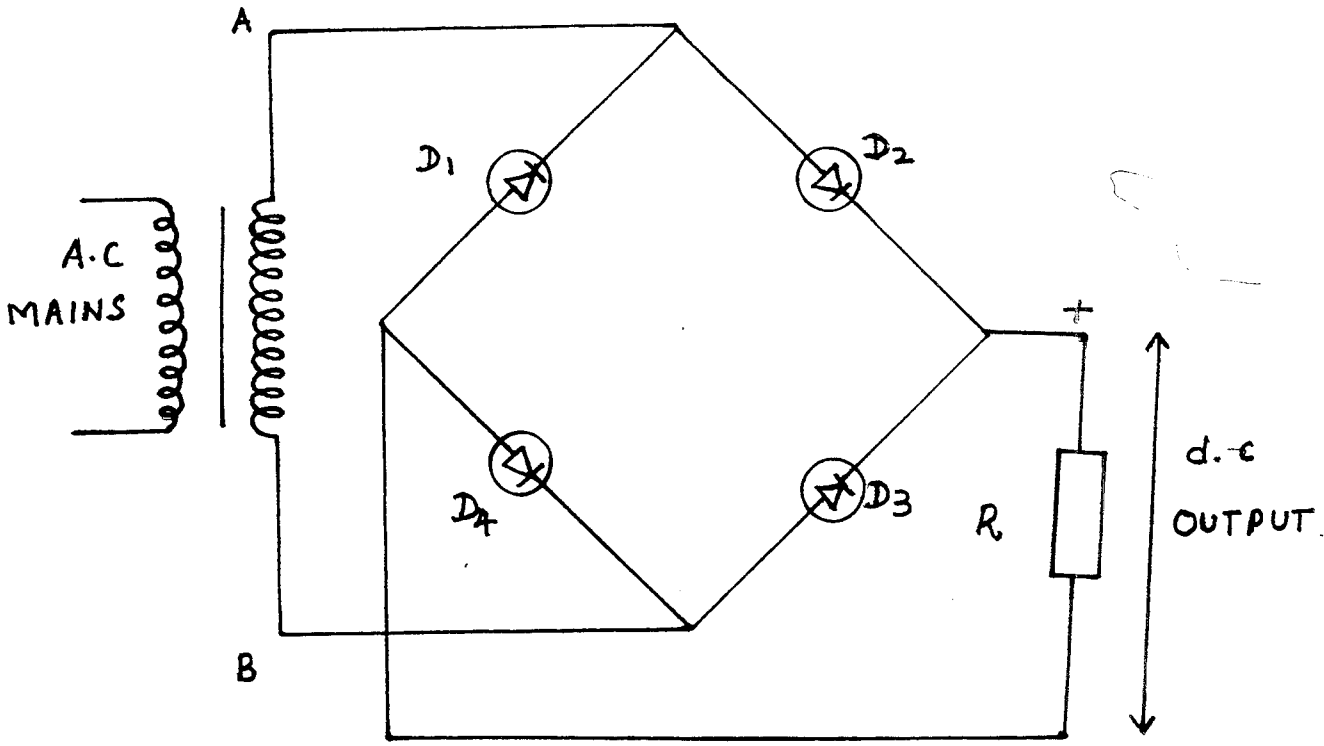
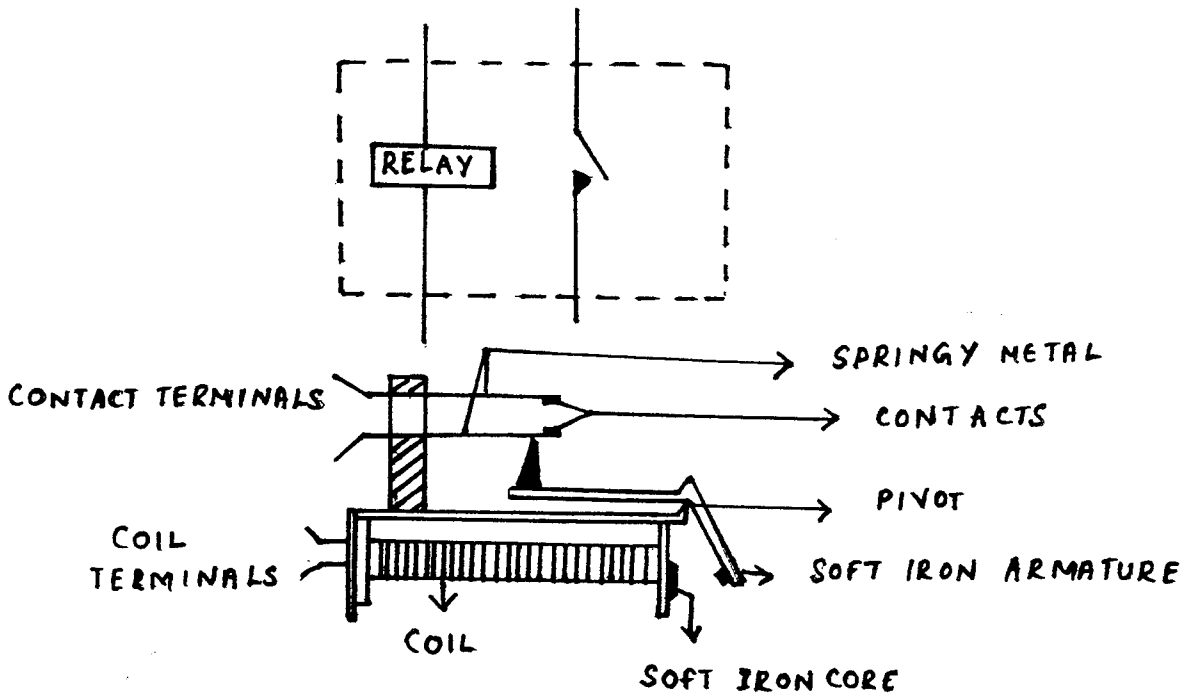
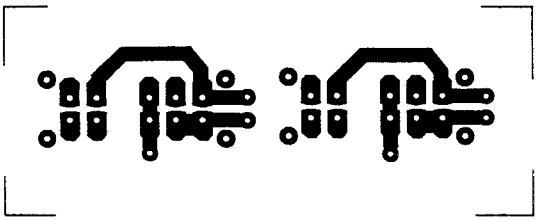
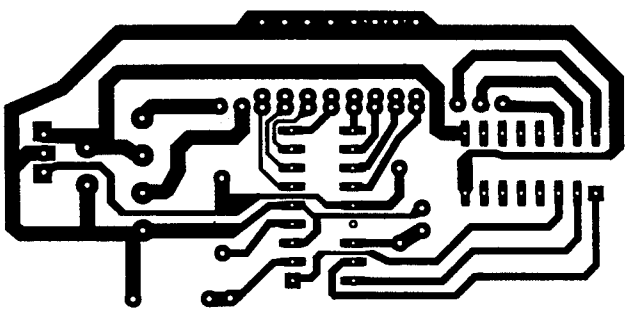


FIG :-(f)

RELAYS







ARVIND
DSGNOH10

FREEWAY ELECTRONICS (P) LTD.,		
TITLE: OVER HEAD CLEANER		REMARKS
NO:	SCALE: 1 : 1	
DATE :		
SIGN. :		Floppy & File Name:

SCHEMATIC OF A '3' TERMINAL POSITIVE REGULATOR

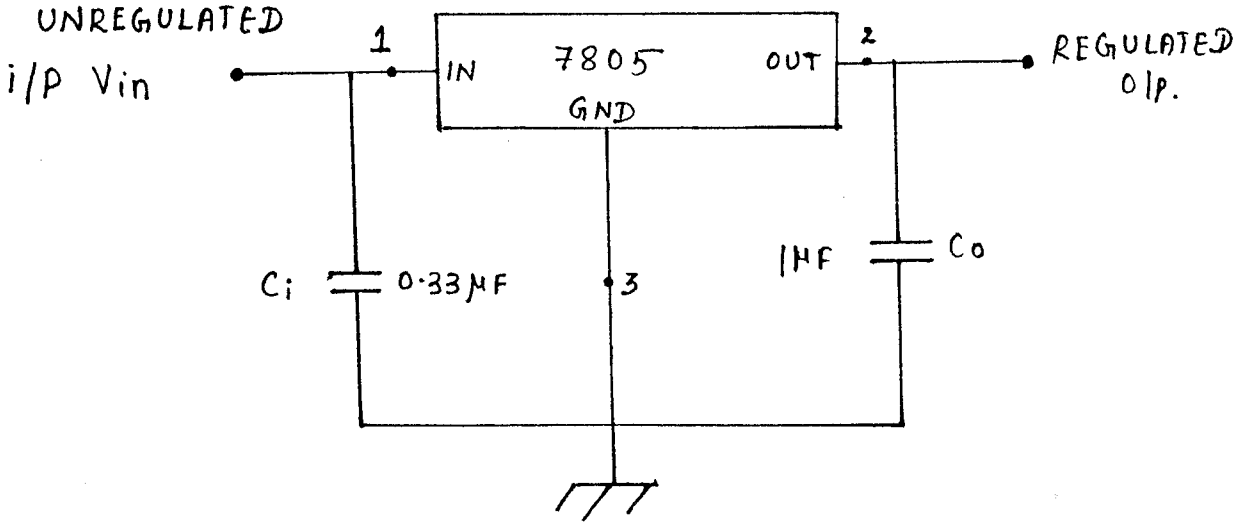
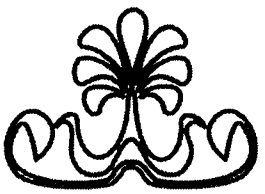
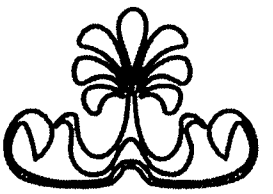


FIG:- (9)



Soft ware



CHAPTER – 5

SOFTWARE

5.1 ALGORITHM

1. Start by checking the start push button .
2. If the button in ON , the blower is started and the cleaner travels forward .
3. If it is not switched ON , then the control goes to the START push button .
4. check the stop push button .
5. The reverse push button is checked for
   If it is ON stop travel and call a delay .
6. Else go for the reverse sensor .
   If the reverse sensor is sensed stop travel , give a delay and then start the travel in the opposite direction .

7. If the reverse sensor is not sensed go for discharge sensor .
8. In the case of sensing it stop the travel , give the desired delay and then discharge .
9. Else go to the start .

5.2 PROGRAM

Hardware – OHC – 1 Board . PIC16C54 AT 4 MHz – RC OSC 10K / 22 PF

Switch Inputs :	6 – RB0 START PB	
	7 – RB1 STOP PB	
	8 – RB2 REV PB	
Sensor Inputs :	9 – RB3 REV SENS	
	10 – RB4 DCG SENS	TRIS 6 – PORT B
Revtime sw 1aB2 :	11 – RB5 RDLY 1a	" 1111 1111 " = FFH
1bB2	12 – RB6 RDLY 1b	
Distime sw 2aB2 :	13 – RB7 DCGDLY 2a	
Output	17 –RA0 BLO	
	18 – RA1 TRA	TRIS 5 – PORT A
	1 – RA2 REV	" 0000 1000 " = 08H

Input

Distime sw 2bB1 : 2 – RA3 DCGDLY 2b

```
        LIST    P = 16C54

        CBLOCK  0 x 10
                DLY1
                DLY2
                DLY3
                FRFLG

        ENDC

PORT A  EQU     5               ; DEFINE EQUATES
PORT B  EQU     6

        ORG     00

        MOVLW   08              ; INIT PORTS
        TRIS    PORT A
        MOVLW   0XFF
```

```
        TRIS        PORT B

        CLRF        PORT A      ;  PORTS  CLEAR
        CLRF        PORT B

        CLRF        FRFLG

MAIN    GOTO        START
```

```
MS200   MOVLW       0XFF        ;  DELAY  OF  200 MS
        MOVWF       DLY2

LP2
        MOVLW       0XFF
        MOVWF       DLY1
LP1
        DECFSZ      DLY1,1          GO TO  LP2
        GO TO LP1                   RETLW  0
        DECFSZ      DLY2,1

DEBOUNCE                        ; DEBOUNCE  DELAY
```

```
        MOVLW   0XFF
        MOVWF   DLY1

LPDB
        DECFSZ  DLY1,1
        GOTO    LPDB
        RETLW   0
```

```
START

SENSTRT
        BTFSS   PORT B , 0          ; SENSE START PB
        GOTO    SENSTRT             ; LOOP IF 0

        CALL    DEBOUNCE            ; DEBOUNCE
        BTFSS   PORT B , 0          ; SENSE START PB
        GOTO    SENSTRT             ; LOOP IF 0

        BSF     PORT A , 0          ; BLOWER ON
        BSF     PORT A , 1          ; TRAVEL ON
```

```
MAINSCAN

STPPB
        BTFSS   PORT B , 1      ;  SENSE  STOP  PB
        GOTO    REVPB           ;  GOTO  NEXTIF OFF

        CALL    DEBOUNCE        ;  DEBOUNCE
        BTFSS   PORT  B , 1     ;  SENSE  STOP  PB
        GOTO    REVPB           ;  GOTO NEXT IF OFF

        BCF     PORT  A , 1     ;  TRAVEL OFF

KEYOF
        BTFSC   PORT  B ,1      ;  SENSE  KEY  OFF
        GOTO    KEYOF
        GOTO    SENSTRT         ;  SENSE  START KEY

REVPB
        BTFSS   PORT  B , 2     ;  SENSE  REVPB
        GOTO    REVSENS         ;  GOTO NEXT IF OFF
```

```
        CALL    DEBOUNCE
        BTFSS   PORT B , 2          ; SENSE REVPB
        GOTO    REVSENS             ; GOTO NEXT IF OFF

        BCF     PORT A , 1          ; TRAVEL OFF
        CALL    MS200
        BTFSC   FRFLG , 0           ; CHECK REV STATUS
        GOTO    REVOFF              ; IF ON SWITCH OFF
        BSF     PORT A , 2          ; ELSE SWITCH OFF
        MOVLW   0XFF 0, FF
        MOVWF   FRFLG               ; SET FLAG ON
        GOTO    TRVON               ; AND TRAVEL ON

REVOFF
        BCF     PORT A , 2          ; SET REV IF OFF
        CLRF    FRFLG               ; CLEAR FLAG
TRVON
        CALL    MS200               ; CALL DELAY FOR
                                            TURN
        BSF     PORT A ,1           ; TRAVEL ON
```

```
KEYREL
        BTFSC   PORT B , 2
        GOTO    KEYREL

REVSENS
        BTFSS   PORT B , 3          ; SENSE REVSENS
        GOTO    DCGSENS

        CALL    DEBOUNCE

        BTFSS   PORT B , 3          ; SENSE REVSENS
        GOTO    DCGSENS

        BCF     PORT A , 1          ; TRAVEL OFF
        CALL    MS200

        BTFSC   FRFLG , 0           ; CHECK REV STATUS
        GOTO    REVOFF1             ; IF ON SWITCH OFF
        BSF     PORT A , 2          ; ELSE SWITCH ON
        MOVLW   0XFF
        MOVWF   FRFLG               ; SET FLAG  ON
```

```
        GOTO    TRVON1              ; AND TRAVEL ON

REVOFF1
        BCF     PORT A , 2          ; SET REV IF OFF
        CLRF    FRFLG               ; CLEAR FLAG
TRVON1
        CALL    MS200               ; CALL DELAY FOR
                                      TURN
        BSF     PORT A , 1          ; TRAVEL ON

        MOVLW   0X14                ; CALL 4 SEC DELAY
                                      D.20
        MOWF    DLY3
LP3     CALL    MS200               ; 200 MILLISECONDS
        DECFSZ  DLY3, 1
        GOTO    LP3

        BCF     PORT A , 1          ; TRAVEL OFF
```

DELAY FOR REVERSING

```
        BTFSS   PORT B , 5          ; TEST B2
        GOTO    REVSW1B             ; B2 = 0

        BTFSS   PORT B , 6          ; B2 = 1
                                    ; TEST B1
        GOTO    B10                 ; B2 = 1  B1 = 0

        MOVLW   96H                 ; B2 = 1  B1 = 1
        MOVWF   DLY3
LP30    CALL    MS200               ; DELAY FOR 30 SEC.
        DECFSZ  DLY3 , 1
        GOTO    LP30
        GOTO    TRON

B10                                 ; B2 = 1  B1 = 0
        MOVLW   64H
        MOVWF   DLY3
LP20    CALL    MS200               ; DELAY FOR 20 SEC.
        DECFSZ  DLY3 , 1
```

```
            GOTO    LP20
            GOTO    TRON

REVSW1B
            BTFSS   PORT B , 6      ; CHECK SW1
            GOTO    TRON            ; B2 = 0  B1 = 0
                                    ; B2 = 0  B1 = 1
            MOVLW   32H
            MOVWF   DLY3
LP10        CALL    MS200           ; DELAY FOR 10 SES.
            DECFZ   DLY3 , 1
            GOTO    LP10

TRON        BSF     PORT A , 1      ; TRAVEL ON
```

```
DCGSENS
            BTFSS   PORT B , 4      ; SENSE DISCHARGE
                                      SENS
            GOTO    AGAIN           ; SKIP IF 0
```

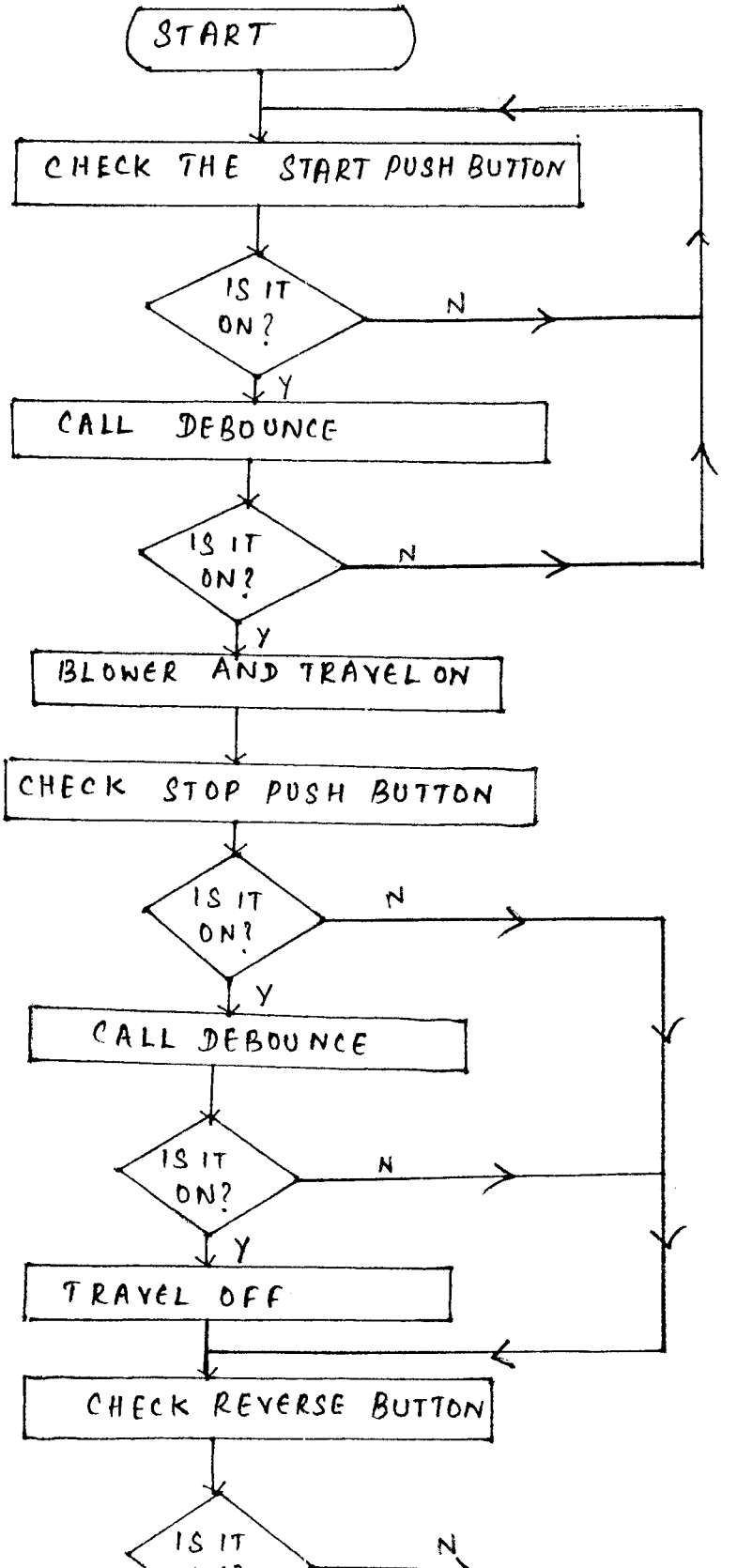
```
        BCF     PORT A , 1          ; TRAVEL OFF

DELAY FOR DISCHARGE

        BTFSS   PORT B , 7          ; TEST B2 GOTO DCG1B
        GOTO    DCG1B               ; B2 = 1

        BTFSS   PORT A , 3          ; TEST B1
        GOTO    BB10                ; B2 = 1  B1 = 0

        MOVLW   0XFE                ; B2 = 1  B1 = 1
        MOVWF   DLY3
P51     CALL    MS200               ; DELAY FOR 51 SEC.
        DECFSZ  DLY3 , 1
        GOTO    LP51
        GOTO    TRON3

BB10                                ; B2 = 1  B1 = 0
        MOVLW   96H
        MOVWF   DLY3
```

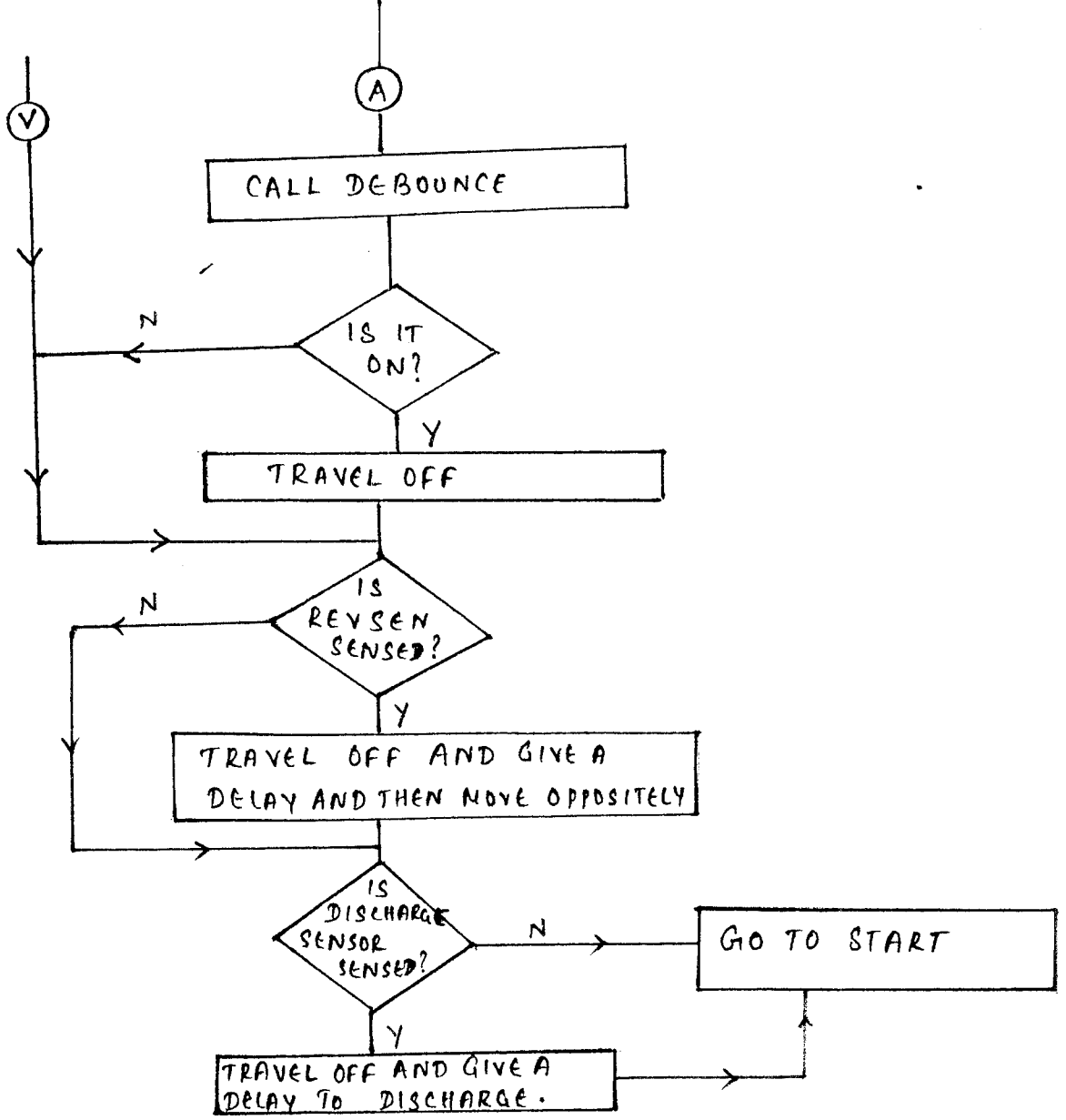
```
LOP30   CALL    MS200           ; DELAY FOR 30 SEC.
        DECFSZ  DLY3 , 1
        GOTO    LOP30
        GOTO    TON3

DCG1B
        BTFSS   PORT A , 3      ; CHECK SW1
        GOTO    TRON1           ; B2 = 0  B1 = 0
                                ; B2 = 0  B1 = 1

        MOVLW   4BH
        MOVWF   DLY3

LP15    CALL    MS200           ; DELAY FOR 15 SEC.
        DECFSZ  DLY3 , 1
        GOTO    LP15
        GOTO    TRON3

TRON1
        MOVLW   19H
        MOVWF   DLY3
```

```
LP05    CALL    MS200          ; DELAY FOR 05 SEC.
        DECFSZ  DLY3, 1
        GOTO    LP05

TRON3
        BSF     PORT A , 1     ; TRAVEL ON
```

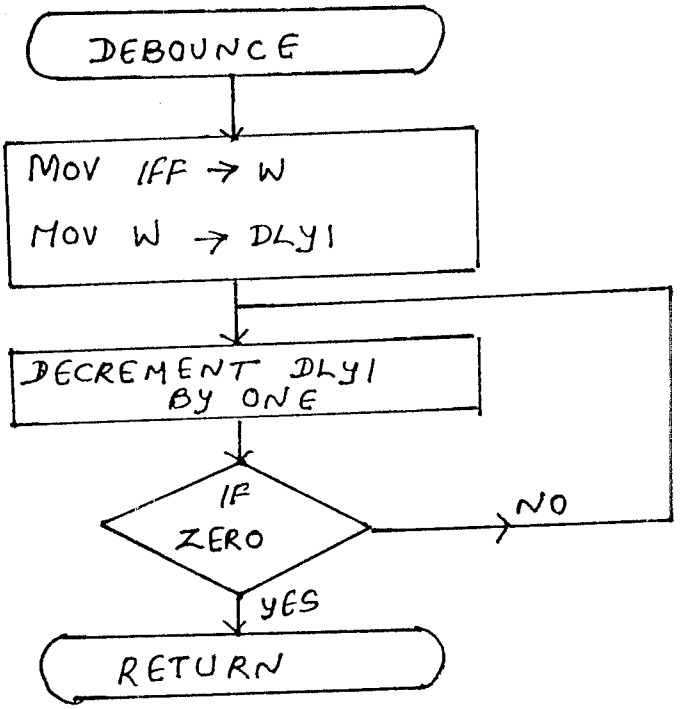
```
AGAIN   GOTO    MAINSCAN
        END
```

FLOWCHART

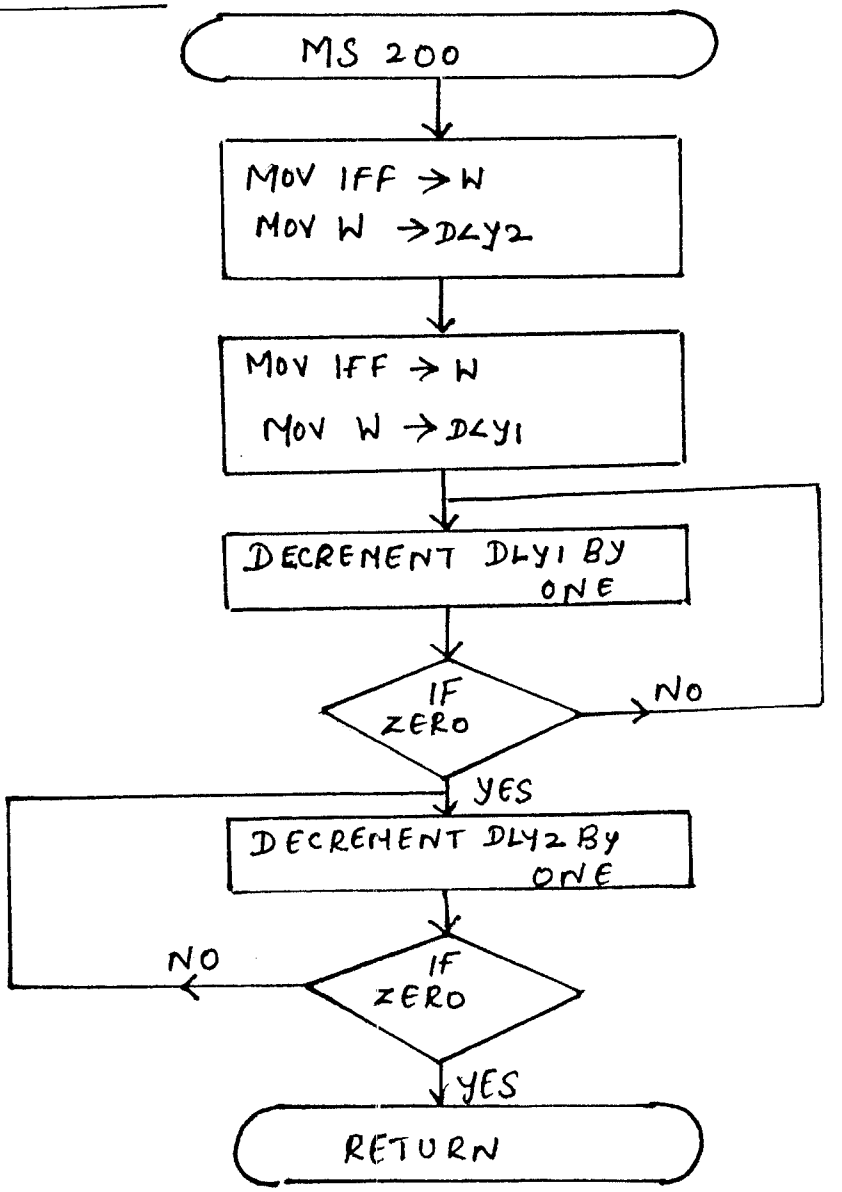

START
CHECK THE START PUSH BUTTON
IS IT ON?
N
Y
CALL DEBOUNCE
IS IT ON?
N
Y
BLOWER AND TRAVEL ON
CHECK STOP PUSH BUTTON
IS IT ON?
N
Y
CALL DEBOUNCE
IS IT ON?
N
Y
TRAVEL OFF
CHECK REVERSE BUTTON
IS IT
N

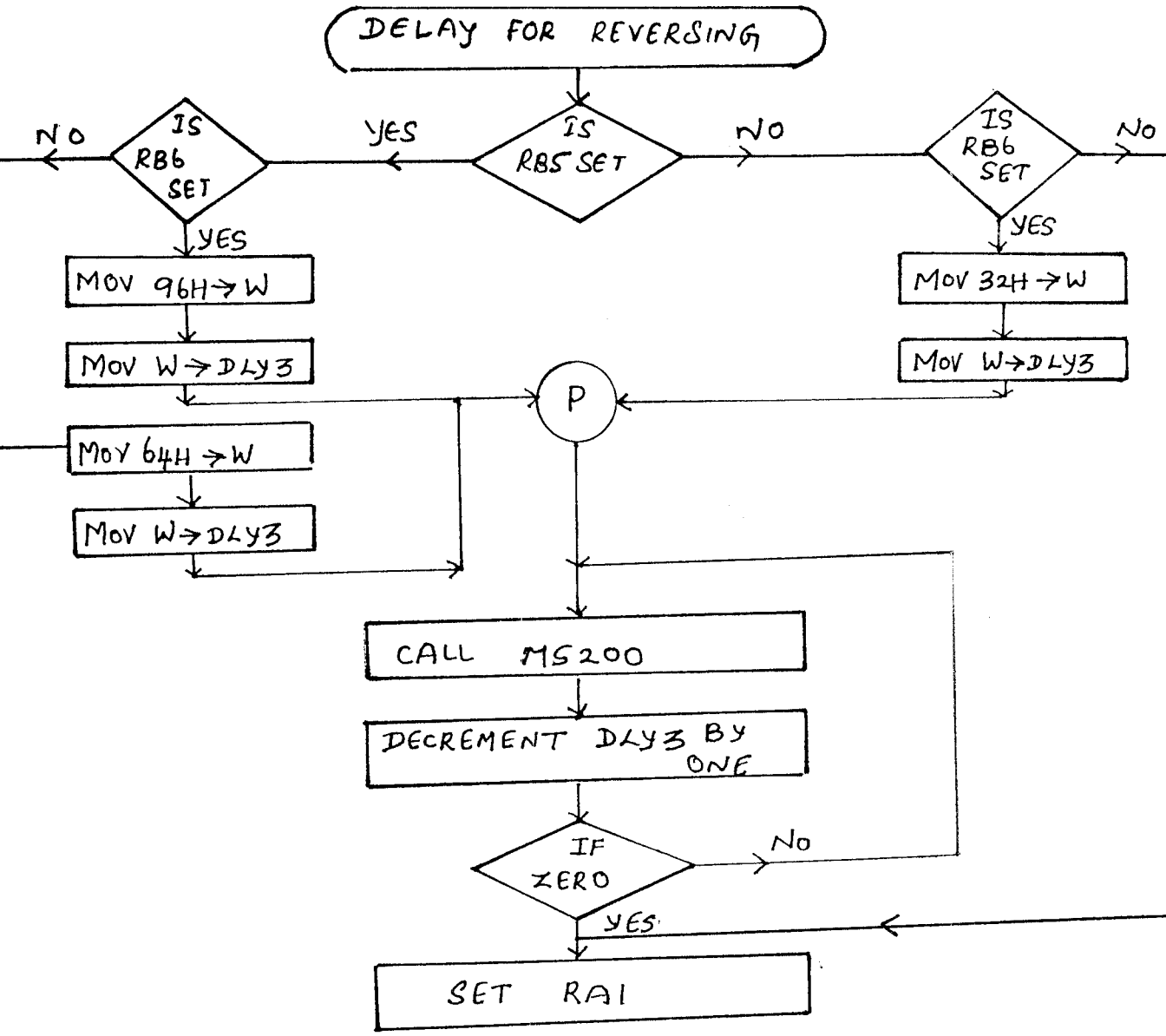

A
V
CALL DEBOUNCE
IS IT ON?
N
Y
TRAVEL OFF
IS REVSEN SENSED?
N
Y
TRAVEL OFF AND GIVE A DELAY AND THEN MOVE OPPOSITELY
IS DISCHARGE SENSOR SENSED?
N
GO TO START
Y
TRAVEL OFF AND GIVE A DELAY TO DISCHARGE.

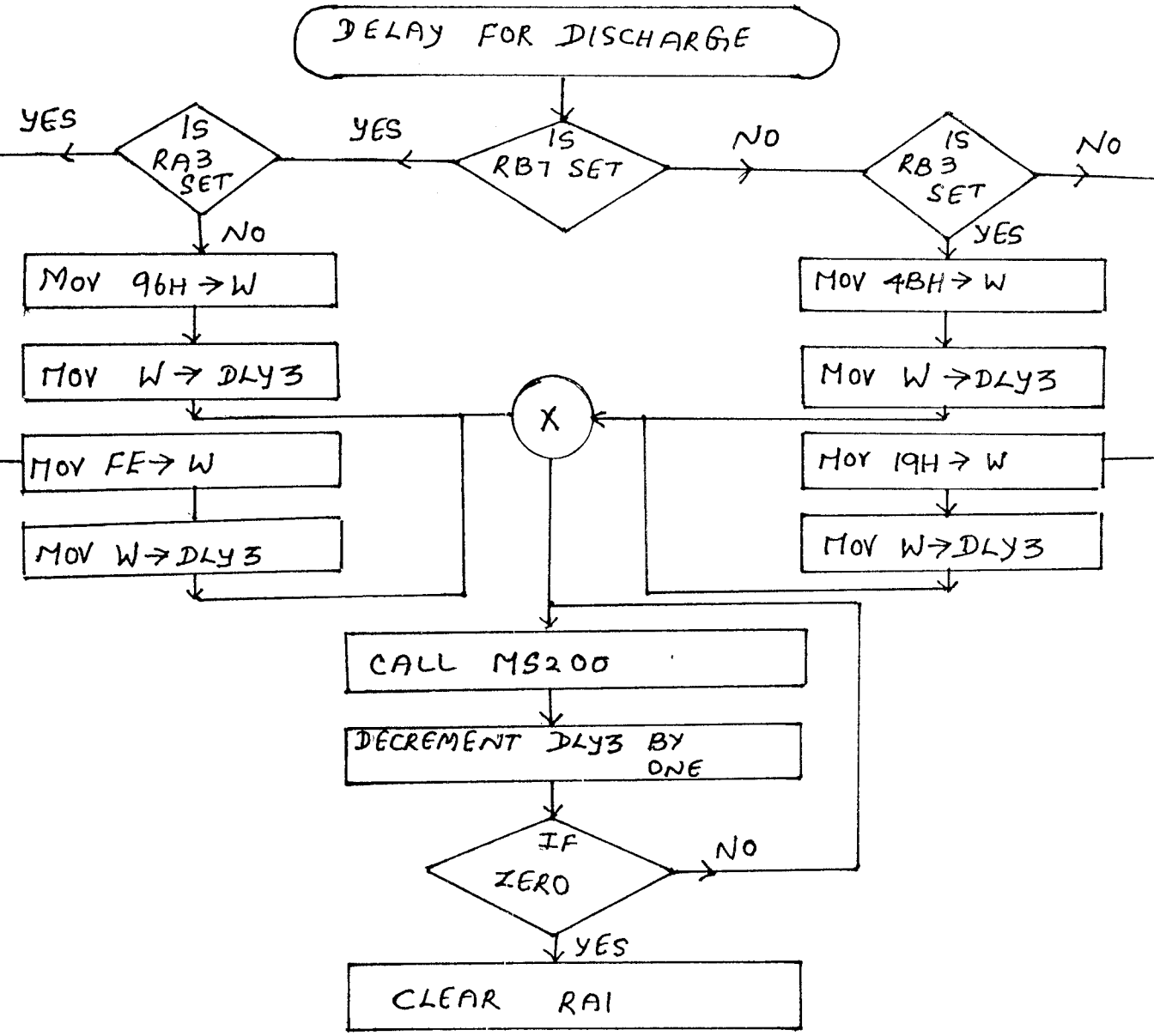
DEBOUNCE
DELAY

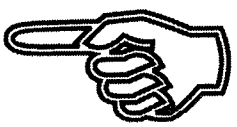


ELAY OF 200MS

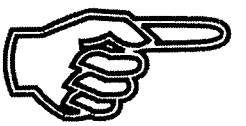



DELAY FOR REVERSING
IS RB5 SET
YES
NO
IS RB6 SET
NO
YES
MOV 96H→W
MOV W→DLY3
MOV 64H→W
MOV W→DLY3
IS RB6 SET
YES
NO
MOV 32H→W
MOV W→DLY3
P
CALL MS200
DECREMENT DLY3 BY ONE
IF ZERO
NO
YES
SET RA1


DELAY FOR DISCHARGE
IS RB7 SET
YES
NO
IS RA3 SET
YES
NO
IS RB3 SET
NO
YES
MOV 96H → W
MOV W → DLY3
MOV FE → W
MOV W → DLY3
MOV 4BH → W
MOV W → DLY3
MOV 19H → W
MOV W → DLY3
X
CALL MS200
DECREMENT DLY3 BY ONE
IF ZERO
NO
YES
CLEAR RA1



Conclusion



CONCLUSION

To conclude , our project would be economic method for removing the dust from the spinning industry .

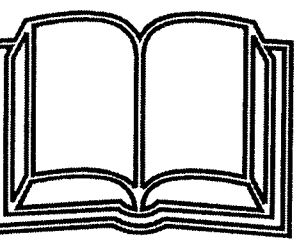
Removal of dust makes the environment of the textile industry , free from pollution . Accumulation of cotton dusts may cause breathing problem to the workers working in the industry . So Over Head Cleaner provides a better working condition .

The cotton dusts , if present in the industry , cuts the yarn and hence production is decreased . So by using this Over Head Cleaner quality of production can be increased .

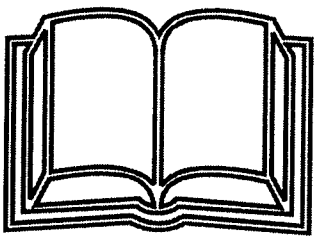
Our product will have good market because of its comparatively low cost .

FEATURE ADVANCEMENTS

An obstacle sensor can also be programmed such that , presence of any obstacle in the path of the travelling bed could be sensed and cleared .



Biblography



BIBILOGRAPHY

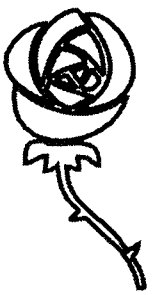
1. PIC 16 , 17 Microcontroller Data Book – Manual .

2. Intersil – Component Data Catalogue 1987 .

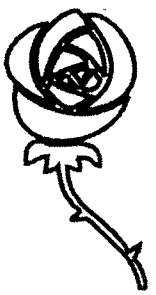
3. CMOS Cook Book – Second Edition – Don Lancaster Revised by Howard M . Berter .

4. Success in Electronics – Tom Duneon .

5. Electronics for Today and Tomorrow – Tom Duneon .



Synopsis



SYNOPSIS

The proposed system aims at the transmission of analog data over a distance as decided by the use of appropriate transmitter and receiver .

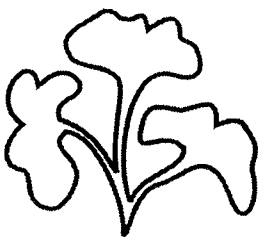
The system works under two module , the TRANSMITTER AND THE RECEIVER .

The transmitter uses the industry standard ICL7106 from Intersil . This chip is capable of converting an analog input voltage into a digital value . The digital data in parallel form is converted to a serial form by means of 4021 shift register . The clock for the serial data is provided by an oscillator which consist of a quartz crystal and a 4060 divider , which basically a ripple counter that counts in the up direction using positive logic . An 8 Hz signal which also happens to be available from the 4060 is used to load the shift register . With the output of the shift register , the start and stop bits are automatically added . Thus the output is converted into an RS232 compatible serial data stream and then fed to a PC RS232 port via

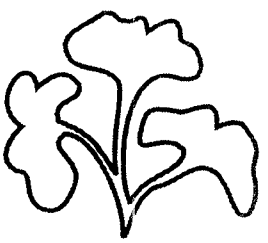
an opto – isolator . The main advantage of such a design is that an external power supply is not needed . The transmitted data stream could be viewed in the PC using the RS232 interface . Then the serial data is transmitted using a FM transmitter and received at the other end using a FM receiver .

The receiver section contains an UART IM6403 which converts the serial start , data , parity and stop bits to parallel data . This is essentially a low power device . The output of the UART goes to a 8 – bit digital to analog converter with a regulation of 3.9 ms. This gives an analog output which is the same as that transmitted .

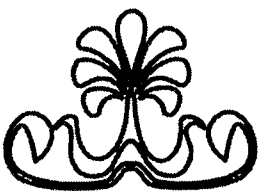
Thus wireless communication is achievable .



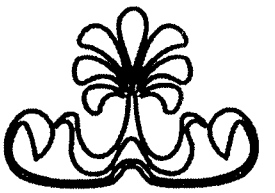
Contents



CONTENTS



Introduction



CHAPTER – 1

INTRODUCTION

1.1 TELEMETRY

Telemetry is a way of reducing the time involved in transferring the measured values to the required places . The measurements are almost real time .

1.2 NEED FOR TELEMETRY

Measurement of any kind plays a vital role in any industry . Measurement are of various kinds and the data measured are required by many people for processing . This leads to the evolution of 'Telemetry' which reduces the time involved in transferring the measured values to the required place and also made these measurements almost real time for many critical applications .

1.3 CLASSIFICATION OF TELEMETRY

Telemetry can be classified based on

Types of Modulation

1. Analog Telemetry System
2. Digital Telemetry System

1. ANALOG TELEMETRY SYSTEM

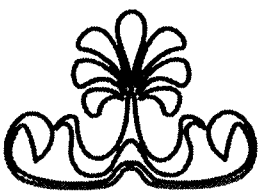
Analog Telemetry System are used for sending inherently analog information , such as voice , they can also be used for sending analog information which has been converted digital form . An analog communication system must accommodate many uses at the same time , in order to get the most use and efficiency from the equipment and circuitry at each end and the communication links between them . Basically an analog communication system is designed to handle a signal that can have any value within the total allowable range . Some of these includes standard amplitude modulated

(AM) and frequency modulated (FM) band ratio , telephone lines etc. With the growth of communication for computer and digital systems data is in digital form . Digital signals are really just a special case of analog signals .

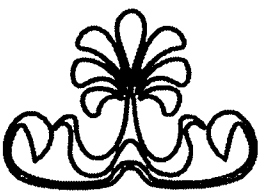
2. DIGITAL TELEMETRY SYSTEM

A digital system is designed to handle only digital signals , electrical signals which can take on only certain predefined values , instead of any value within a whole range . The entire communication system can be optimized to deal with these values . Digital communication systems are used to meet the needs of most new communication applications . A digital system that is handling signals which were originally analog must first sample the analog signal and convert it to digital format . Digital signals may also have to be encoded . Multiplexing and modulation of digital are related to the same operations on analog signals , but with some differences and simplifications .

There are two types of medium used . One is wireless communication which we use here and the other is fibre optic communications .



System overview



CHAPTER – 2

SYSTEM OVER VIEW

2.1 DESCRIPTION OF BLOCK DIAGRAM

The analog signal which is usually the output of any transducer is fed to Analog to Digital converter . The input signal is conditioned before feeding to Analog to Digital converter, shown (fig 1).

2.1.1 NEED FOR SIGNAL CONDITIONING

The process of modifying the transduced signal into a usable format for the final stage of measurement is known as signal conditioning .

The signal conditioning equipment may be required to do linear processes like amplification , attenuation , integration ,

differentiation , addition and subtraction . They are also required to do non – linear processes like modulation , demodulation , sampling , filtering , clipping & clamping , squaring , linearising or multiplication by another function etc .

The output of ADC which is in 8 – bit form is fed to a parallel to serial converter .

The 8 – bit binary data is converted to a serial format by a parallel to serial converter . This is fed by to a FM module for the purpose of transmission . The transmission is through atmosphere .

RECEIVER

The FM receiver receives the serial data stream , converts to an 8 – bit parallel one using the UART IC IM6403 . The parallel data is fed to a DAC to convert it to analog one .

2.3 TRANSMITTER SECTION

The circuit diagram shown in (fig 2) involves transmitter section . The circuit consists of a converter IC , 24 – bit shift register . The converter IC , ICL 7106 is an ADC and LCD driver (i.e) , this chip is capable of converting an analog input voltage into digital value and drive a 3.5 digit LCD . The display information , intended for a 3.5 digit 7 – segment readout with polarity indicated , converted into an RS232 compatible serial data stream including start and stop bits with the aid of a shift register , and then fed to PC's RS232 port via an opto – isolator .

The clock for the serial data is provided by an oscillator which consists of a quartz crystal of 32.768 KHz and a type of 4060 divider . Pin 7 of 4060 divider supplies the 2048 Hz shift register clock . An 8 HZ signal also available from 4060 divider is used to load the shift register .

A 24 – bit shift register is built form three numbers of IC 4021 . This converts the parallel data into serial format . The 18 data bits from ICL7106 is split into three bytes , each of which is headed

by a start bit and closed off by stop bit . The start bit is indicated by a low level and the stop bit is indicated by a high level .

On a high level at pin 9 of IC 4021 , the 24 bits are loaded into the shift register . A subsequent 'low' level causes the bits to be shifted out at the rate of clock applied to pin 10 of IC 4021 . Trailing stop bits are automatically added to the end of the serial word . The output of the shift register comes from pin 3 of IC4 which is the cascaded output . This output appears as a data stream with a length of 3 bytes of 10 / 2,048 secs = 4.9 ms each , at intervals of 125 ms .

The output of the shift register drives opto – isolator IC5 via resister R3 . At the PC side of the opto – isolator , the signal is amplified by T1 . The amplifier allows a relatively small drive current of 1mA to be used , while it has a positive effect on the current consumption of the opto – transister . To enable data to reach the PC , the computer must actuate the DTR line on its RS232 port (i,e) the line is made to + 12 v . An active low at the shift register output causes the LED in the opto – isolator to light , and T1 to conduct consequently , the R x D line is pulled to + 12 v . When T1 is switched

off , the internal pull – down resister of the interface pulls the line to - 12 v level .

At the converter side , the circuit uses the supply voltage pin of the ICL 7106 . This causes a few problem , though , because the 'low' level supplied by the outputs of the ICL 7106 is not 0 v , but approximately v_{cc}= -5v . Obviously , that level will not be recognized by the CMOS logic connected to the outputs . this problem is solved by raising the negative supply level of the circuit by about 2 v with the aid of diodes D1 , D2 , and D3 . At a typical supply voltage of 9v , that creates a ground voltage level of about 2v , while the threshold voltage of the shift register inputs lies at about 5.5v .

2.2.1 DISCRIPTION OF A TO D CONVERTOR

ANALOG SECTION

The (fig 3) shows the analog section of ICL7106 . Each measurement cycle is divided into three phase they are

a. Auto – Zero (A/Z)

b. Signal integrate (INT)

c. De – integrate (DE)

a. AUTO – ZERO PHASE

During auto – zero three things happen . First , input high and low are disconnected from the pins and internally shorted to analog common . Second , the reference capacitor is charged to the reference voltage . Third , the auto – zero capacitor C_{AZ} is charged to compensate for offset voltages in the buffer amplifier , integrator and comparator . Since the comparator is included in the loop , the A/Z accuracy is limited only by the noise of the system . In any case the offset referred to the input is less than 10 μv .

b. SIGNAL INTEGRATE PHASE

During this phase , the auto – zero loop is opened , the internal short is removed and the internal input high and low are

connected to the external pin . The convertor then integrates the differential voltage between INHI and INLO for a fixed time . This differential voltage can be with in a wide common mode range upto one volt from either supply . If , on the otherhand , the input signal has no return with respect to the convertor power supply , INLO can be tied to analog common to establish the correct common mode voltage . At the end of this phase , the polarity of the integrated signal is determine .

C. DE – INTERATE PHASE

The final phase is de – integrate (or) reference integrate . Input low is internally connected to analog common and input high is connected across the previously changed reference capacitor . Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero is proportional to the input signal . Specifically the digital readings displayed is $1000 (v_{in}/v_{REF})$.

DIFFERENTIAL INPUT

The input can accept differential voltage any where within the common mode range of the input amplifier , or specifically from 0.5 volts below the positive supply to 1.0 volt above the negative supply . In this range , the system has a CMRR of 86db typical . The integrator output can swing to within 0.3volts of either supply without loss of linearity .

DIFFERENTIAL REFERENCE

The reference voltage can be generated any where within the power supply voltage of the convertor . The difference in reference for + ve (or) - ve input voltage will give a roll – over error . This can be avoided by having the values of reference capacitor larger enough in comparison to the stray capacitance .

ANALOG COMMON

The common pin sets a voltage that is ≅ 2.8 v more(- ve) than the + ve supply . The common voltage will have a low voltage coefficient of 0.001% v , low output impedence of ≅ 15Ω and a temperature coefficient typically less than 80 ppm / °c . In 7106 , the internal heating which results from the LED drivers can cause some degradation in performance .

DIGITAL SECTION

The digital section of ICL7106 is shown in the (fig 4) . An internal digital ground in this IC is generated from a 6v zener diode and a large p channel source follower . It have a regulated supply and a back plane drive . The segment drive is from 2 to 8 mA , typical for instrument size common anode LCD displays .

The clock arrangement method in the 7106 are

a. An external oscillator connected to pin 40 .

b. A crystal between pins 39 and 40 .

c. An R – C oscillator using all three pins .

The clock circuit is shown in (fig 5)

The oscillator frequency is divided by four before it clocks the decade counters . For three readings / second , an oscillator frequency of 48KHZ would be used . Oscillator frequencies of 240KHZ , 120KHZ , 80KHZ , 60KHZ , 48KHZ , 40KHZ , 33 1/3KHZ , etc , should be selected for 60HZ rejection . For 50HZ rejection , oscillator frequencies of 200KHZ , 100KHZ , 66 2/3 KHZ , 50KHZ , 40KHZ , etc . are chosen .

The ICL 7106 are high performance , lower power 3 ½ digit A/D convertors containing all the necessary active devices on a single CMOS IC which also includes 7 segment decoders , display drivers , a reference , and a clock . The ICL 7106 will directly drive an instrument size light emitting diode displays .

8 STAGE SHIFT REGISTER (4021)

The pin details of shift register (4021) is shown in (fig 6)

This IC accepts a parallel input and gives serial output with the load at any time and it can be used also with serial input and serial output . This package can be used as a 6 , 7 or 8 stage shift right register . Stages may be cascaded for longer lengths which is used in this project .

As a serial – in serial – out register , the load input should be grounded . Data presented to the IN terminals gets shifted into the first stage on the ground – to – positive transition (+ve edge) of the clock input . In six successive clocking , this data appears at output 06 . Another clocking transfers to output 07 & yet another to 08 . Additional clocking will lose this bit of data unless stages are cascaded or data is recalculated .

To parallel load data , apply an 8 – bit word to the p1 through p8 terminals , having the p1 bit nearest the input of the register and the p8 bit nearest the output . The load terminal is made high , and the data immediately loads into the register . The load

terminal must return and stay grounded for normal register operation . The clock must be noise less and have only a single ground – to – positive transition per desired shifting . Clock rise and fall times should be faster than 5 μsec .

Maximum clock frequency is 5 megahertz at 10v and 2.5 megahertz at 5v . Total package current at a 1 megahertz clock rate is 2mA at 5v and 4mA at 10v .

BINARY RIPPLE COUNTER (4060)

The pin details of binary ripple counter (4060) is shown (fig 7) .

This is a binary ripple counter that counts in the up direction using positive logic . Feedback available at the clock input allows input conditioning (or)use of a reference – contained crystal (or)R – C oscillator .

The reset input is normally held at ground . Each time the clock changes from positive to ground , the counter advances one

count . The 4 output divides the input clock by $2^4 = 16$ up through the 14 output which divides by $2^{14} = 16{,}384$. No outputs are available for divisions of 2 , 4 , 8 and 2048 .

Since this is a ripple counter , the output changes in sequential order . In correct counts will briefly result during settling time .

The crystal oscillator connections are shown in the figure . When used as a divider only , the clock input must be bounceless and noise free , and have rise and fall times faster than 5μsecs . Bringing the reset Input positive for a minimum of half a μseconds resets all counter stages to zero .

Power supply current is 0.4 mA at 5v and 0.8 mA at 10v for a 1 mHZ clocking rate . An extra 2mA is needed by the clock is used in an astable (or) crystal mode . Maximum clock frequency is 1.75 megahertz at 5v and 4 megahertz at 10v .

OPTO – ISOLATOR

Opto – isolator is a small circuit which combines a LED and a photo – sensitive device inside a light proof chamber . The commercial opto – isolators are now made by foreign concerns , such as Texas , GE , Monsanto and RCA . Texas Til III is an opto – isolator containing a LED and a phototranistor in one envelop using dual – in – line (DIL) package . (fig 8).

Texas opto – isolator type Til – III is shown in figure . There is no electrical connection between the LED and the photo – transister . The opto – isolators are used to couple hot or live chassis of main operated equipment . The opto – isolator can be used to enable logic circuits to switch on mains equipment using SCR or triacs . The opto – isolators provides safe hazardless coupling to live main circuit , which does not use isolating transformer .

2.4 RECEIVER SECTION

The transmitted data in serial form is received by an FM receiver. The serial data is converted to a parallel one using the UART IC IM 6403. The output of the UART is given to DAC 0808 which converts the digital data to give an analog output.

2.4.1. DAC (DIGITAL TO ANALOG CONVERTER)

The DAC 0808 series is an 8 – bit monolithic digital to analog converter, featuring a full scale output current settling time of 150 ns while dissipating only 33 mw with ± 5 v supplies. No reference current (I_{ref}) trimming is required for most applications since the full-scale output current is typically ± 1 LSB of 255 I_{ref} / 256. Relative accuracies of better than ± 0.19 % assure, 8 – bit monotonocity and linearity while zero level, output current of less than 4 μA provides 8 – bit zero accuracy for $I_{ref} \geq 2$ mA. The power supply current of the DAC 0808 series are independent of bit codes, and exhibits essentially constant device characteristics over

the entire supply voltage range . The DAC 0808 will interface directly with popular TTL , DTL or CMOS logic levels .

The most important characteristics of a DAC converter is resolution . This is determined number of bits in the input binary word . For a converter with 8 binary inputs resolution in one part in 256 (2^8) .

2.4.2 UART (UNIVERSAL ANSYCHRONOUS RECEIVER TRANSMITTER)

The IM6403 is CMOS / LSI UART for interfacing computers or microprocessors to Asynchronous data channels . The receiver converts serial start , data , parity and stop bits to parallel data verifying proper code transmission , parity and stop bits . The transmitter converts parallel data into serial form and automatically adds start , parity and stop bits . The data word length can be 5, 6, 7, or 8 bits . Parity may be odd or even . The stop bits may be 1 or 2 (or 1 ½ and 1 when transmitting 5 – bit code) . The IM6403 can

be used in a wide range of applications including modems , printers , peripherals and remote data acquisition systems .

FEATURES

1. Low power - less than 10 mw typically at 2 MHz .
2. Operation upto 4 MHz clock .
3. Programmable word length , stop bits and parity .
4. Automatic data formatting and status generation .
5. Compatible with industry standard UART 's .
6. On - chip oscillator with external crystal .
7. Operating voltage - IM6402 / 6403 : 5 v .

With the proposed system reception of the transmitted data is achievable within 60 feet .

BLOCK DIAGRAM

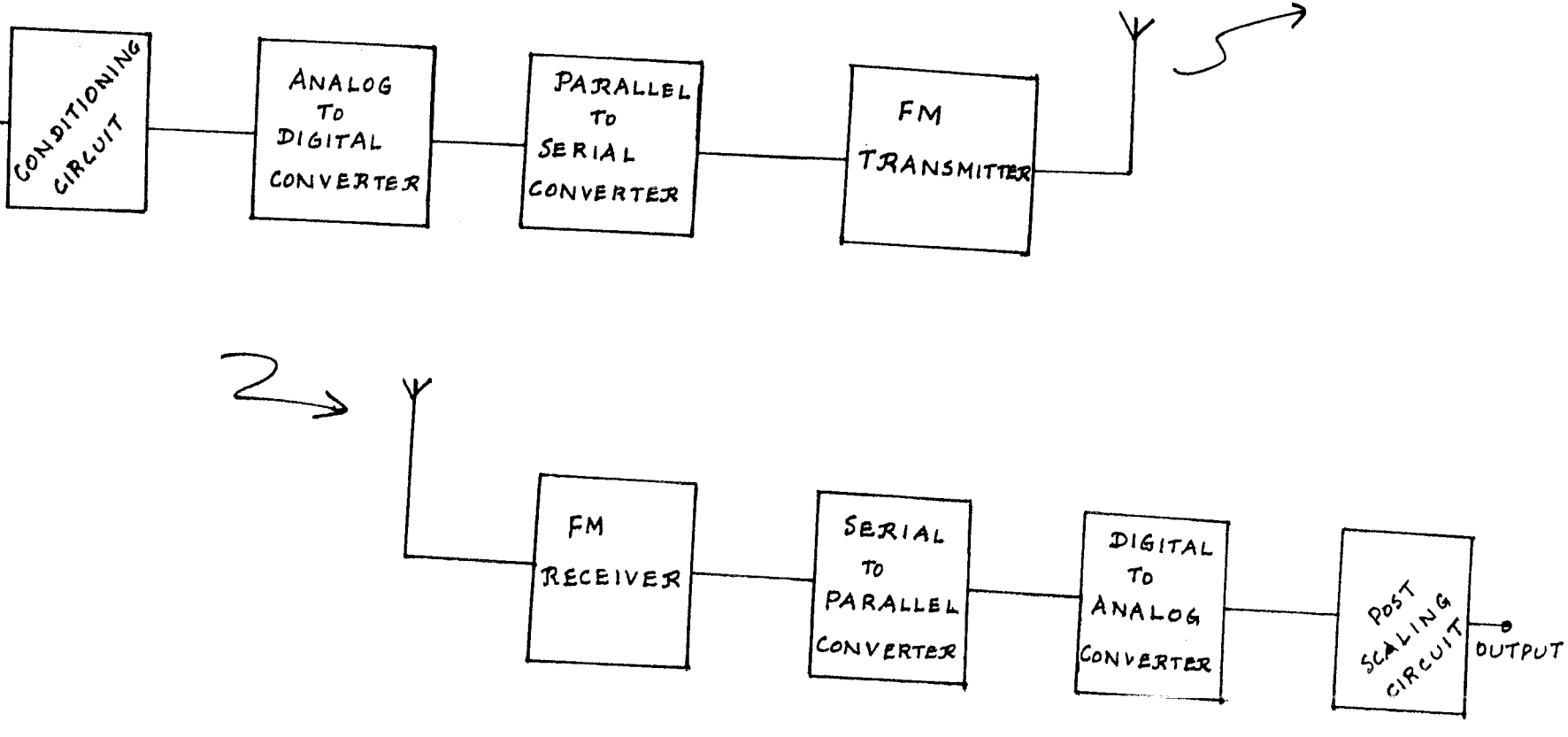
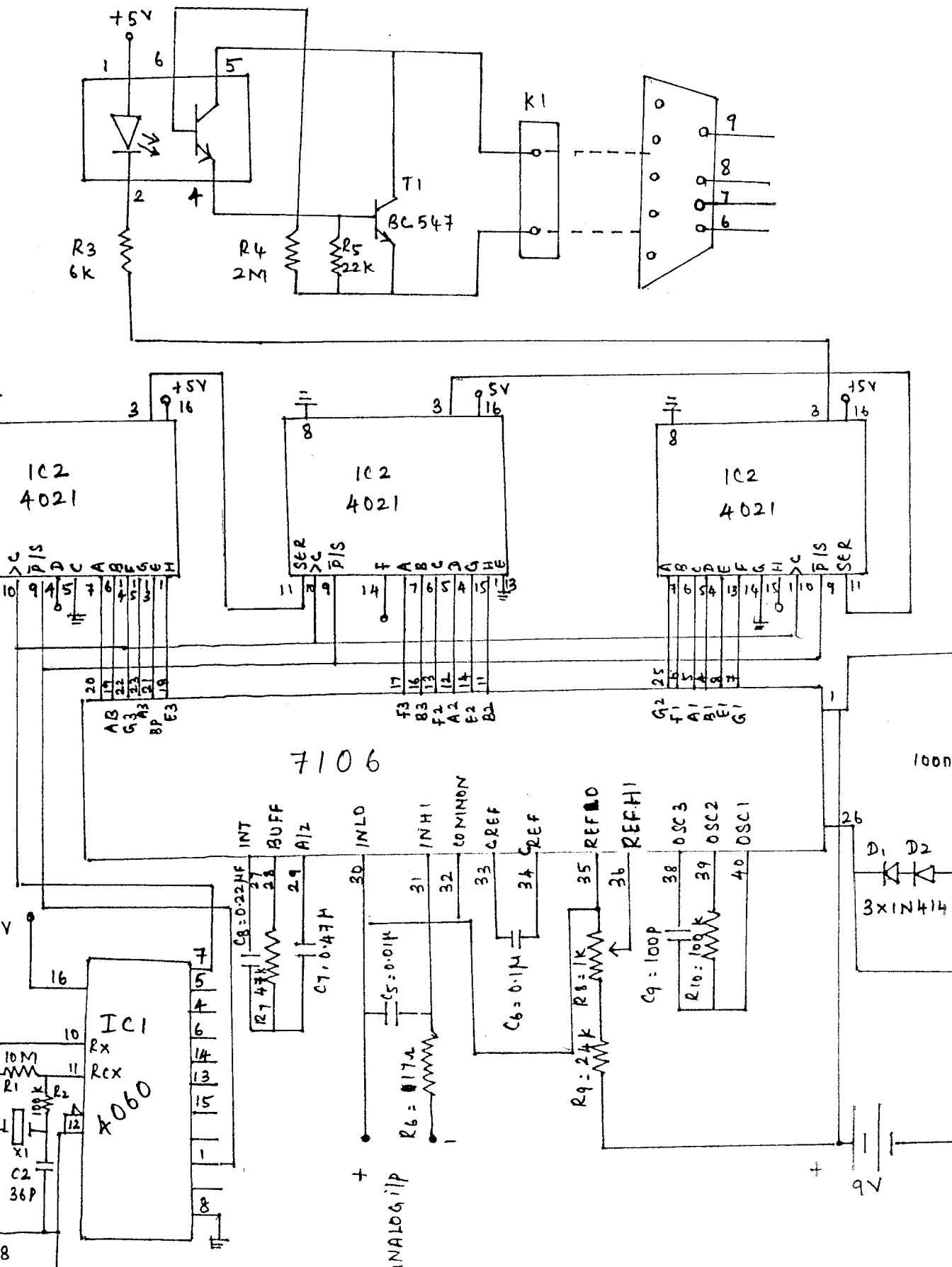
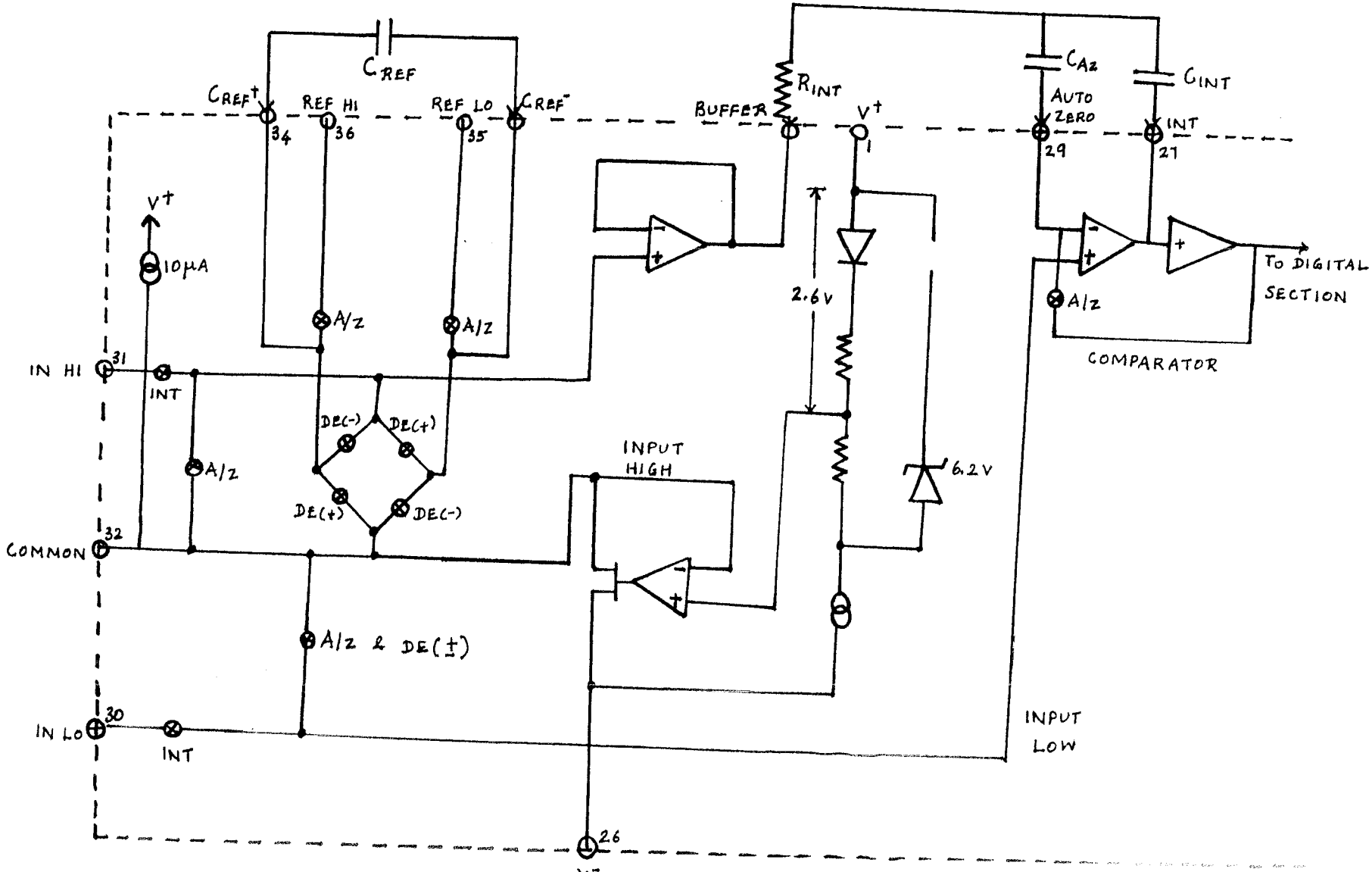


FIG:-(1)

TRANSMITTER CIRCUIT



ANALOG SECTION OF 7107/7106



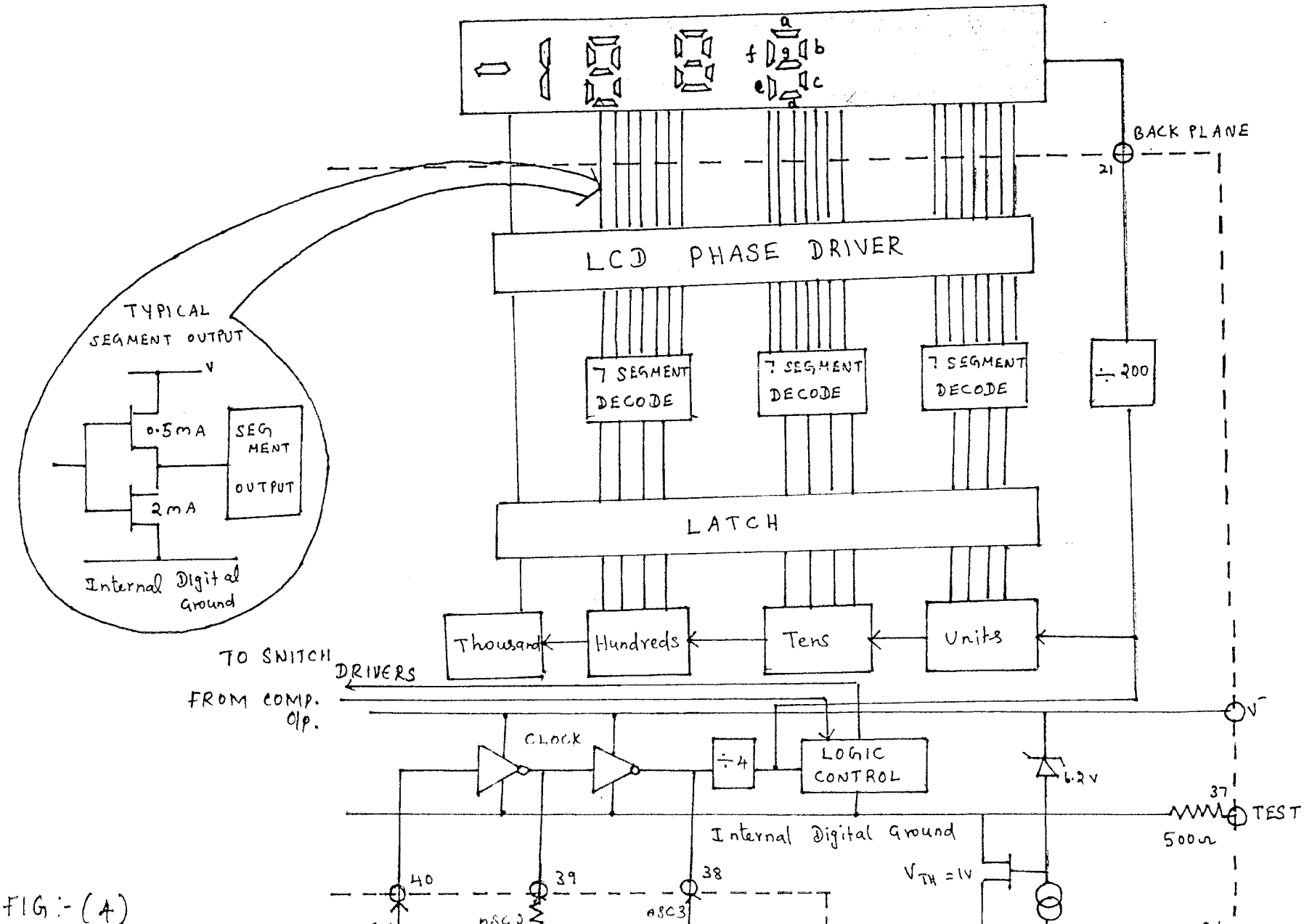

a
f
g
b
e
c
d
BACK PLANE
21
LCD PHASE DRIVER
7 SEGMENT DECODE
7 SEGMENT DECODE
7 SEGMENT DECODE
÷ 200
LATCH
Thousand
Hundreds
Tens
Units
TO SWITCH DRIVERS
FROM COMP. O/P.
V⁻
CLOCK
÷4
LOGIC CONTROL
6.2 V
37
TEST
500Ω
Internal Digital Ground
40
39
38
OSC2
OSC3
V_{TH} = 1V
TYPICAL SEGMENT OUTPUT
V
0.5mA
2mA
SEGMENT OUTPUT
Internal Digital Ground

FIG :- (A)

CLOCK CIRCUITS

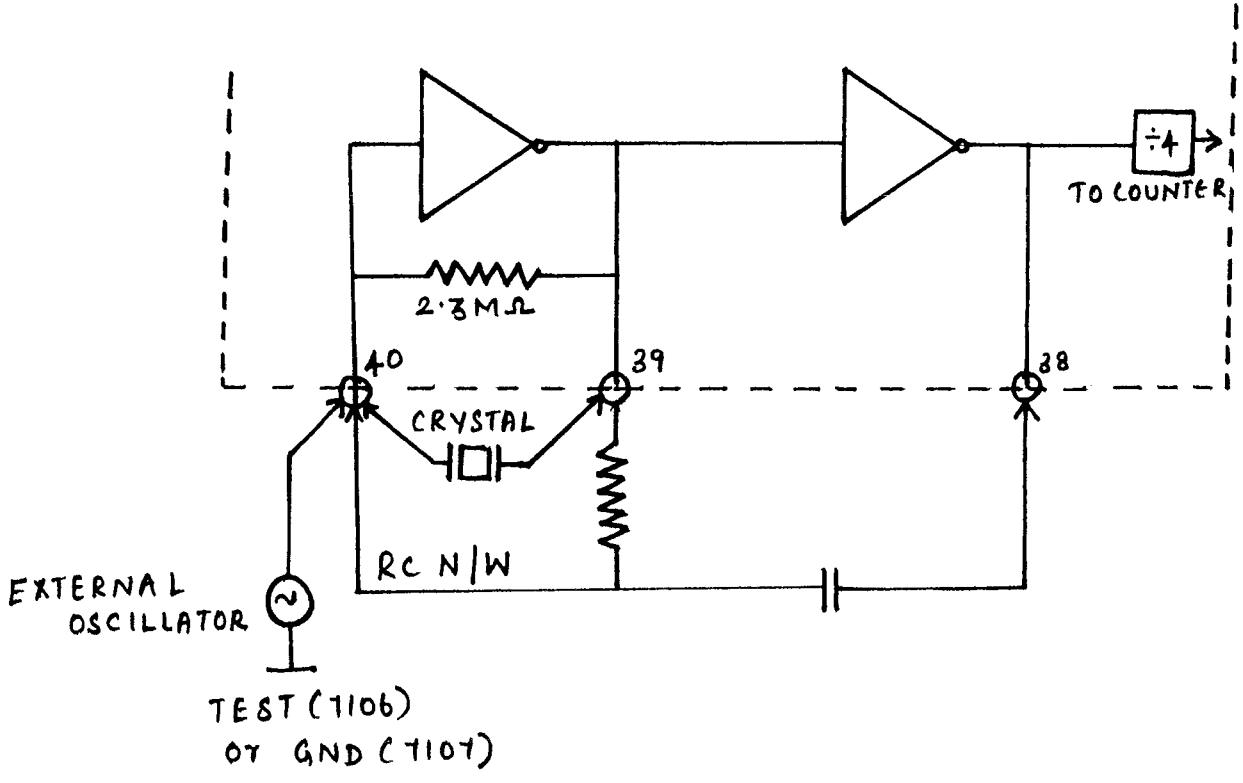


FIG:(5)

8-STAGE SHIFT REGISTER (4021)

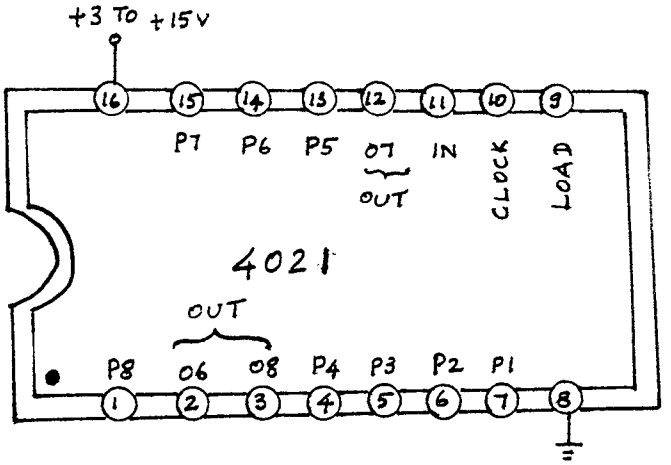
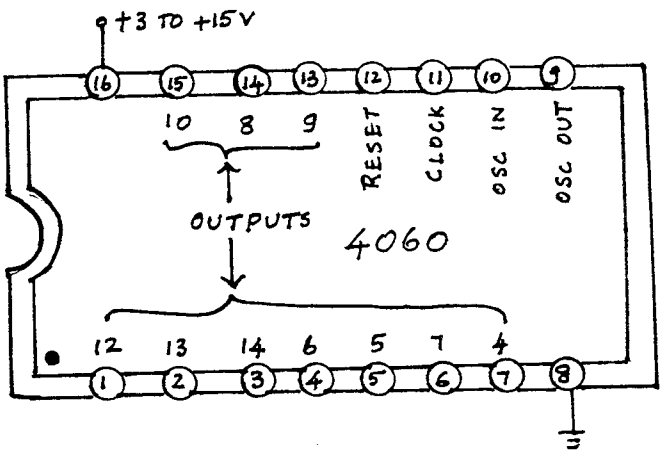
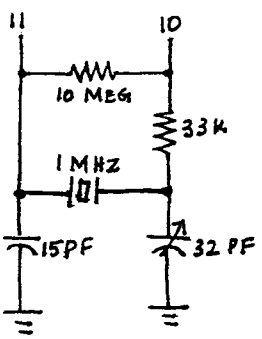


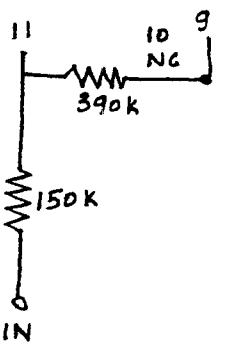
FIG:-(6)

BINARY RIPPLE COUNTER (4060)

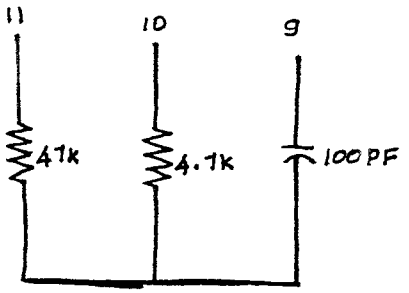




(XTAL OSCILLATOR)



(SCHMITT TRIGGER)



(RC OSCILLATOR)

OPTO - ISOLATOR

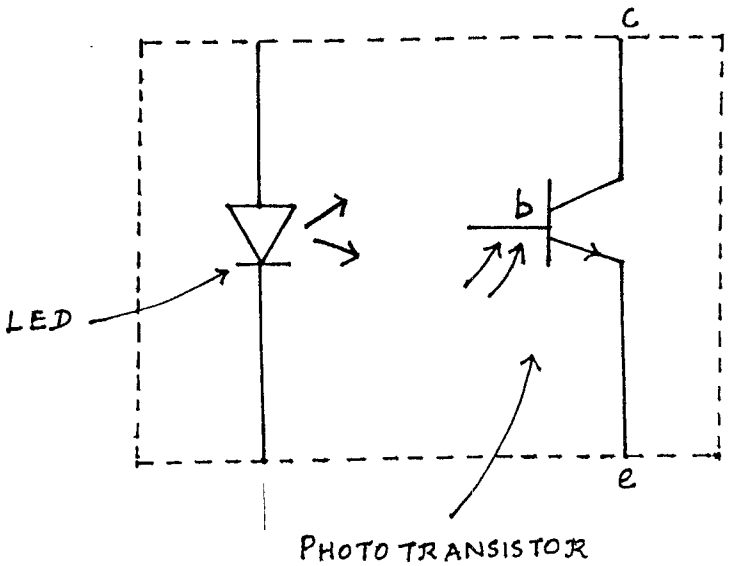
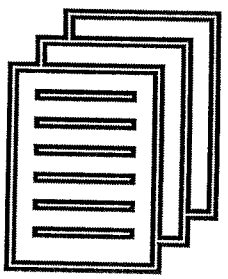
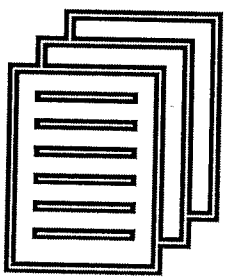


FIG:- (8)



Appendix



11.0 ELECTRICAL CHARACTERISTICS - PIC16C58A

Absolute Maximum Ratings†

Ambient Temperature under bias ..... -55°C to +125°C
Storage Temperature ..... - 65°C to +150°C
Voltage on V_{DD} with respect to V_{SS} ..... 0 to +7.5V
Voltage on $\overline{MCLR}$ with respect to V_{SS} (2) ..... 0 to +14V
Voltage on all other pins with respect to V_{SS} ..... -0.6V to (V_{DD} + 0.6V)
Total Power Dissipation(1) ..... 800 mW
Max. Current out of V_{SS} pin ..... 150 mA
Max. Current into V_{DD} pin ..... 100 mA
Max. Current into an input pin (T0CKI only) ..... ±500 µA
Input Clamp Current, I_{IK} (V_I < 0 or V_I > V_{DD}) ..... ±20 mA
Output Clamp Current, I_{OK} (V_O < 0 or V_O > V_{DD}) ..... ±20 mA
Max. Output Current sunk by any I/O pin ..... 25 mA
Max. Output Current sourced by any I/O pin ..... 20 mA
Max. Output Current sourced by a single I/O port ..... 50 mA
  PORTA ..... 100 mA
  PORTB
Max. Output Current sunk by a single I/O port ..... 50 mA
  PORTA ..... 100 mA
  PORTB

Note 1: Power Dissipation is calculated as follows: $P_{dis} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD}-V_{OH}) \times I_{OH}\} + \sum(V_{OL} \times I_{OL})$

Note 2: Voltage spikes below V_{SS} at the $\overline{MCLR}$ pin, inducing currents greater than 80mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low" level to the $\overline{MCLR}$ pin rather than pulling this pin directly to V_{SS}

† NOTICE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

5

Table. 6.1. Electrical characteristics of 7805 voltage regulator

Absolute Maximum Ratings

Input Voltage (5 V through 18 V)	35 V
(24 V)	40 V
Internal Power Dissipation	internally limited
Storage Temperature Range	−65°C to + 150°C
Operating Junction Temperature Range	
μA7800	− 55°C to + 150°C
μA7800C	0°C to + 125°C

7805C

Electrical Characteristics V_{IN} = 10 V, I_{OUT} = 500 mA, 0°C ≤ T_J ≤ 125°C, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF, unless otherwise specified.

Characteristic	Condition	Min	Typ	Max	Unit
Output Voltage	T_J = 25°C	4.8	5.0	5.2	V
Line Regulation	T_J = 25° C, 7 V ≤ V_{IN} ≤ V		3	100	mV
	8 V ≤ V_{IN} ≤ 12 V		1	50	mV
Load Regulation	T_J = 25°C, 5 mA ≤ I_{OUT} ≤ 1.5 A		15	100	mV
	250 mA ≤ I_{OUT} ≤ 750 mA		5	50	mV
Output voltage	7 V ≤ V_{IN} ≤ 20 V, 5 mA ≤ I_{OUT} ≤ 1.0 A, P ≤ 15 W	4.75		5.25	V
Quiescent Current	T_J = 25°C		4.2	8.0	mA
Quiescent Current Change with line	7 V ≤ V_{IN} ≤ 25 V			1.3	mA
with load	5 mA ≤ I_{OUT} ≤ 1.0 A			0.5	mA
Output Noise Voltage	T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz		40		μV
Ripple Rejection	f = 120 Hz, 8 V ≤ V_{IN} ≤ 18 V	62	78		dB
Dropout Voltage	I_{OUT} = 1.0 A, T_J = 25°C		2.0		V
Output Resistance	f = 1 kHz		17		mΩ
Short-Circuit Current	T_J = 25°C, V_{IN} = 35 V		750		mA
Peak Output Current	T_J = 25°C		2.2		A
Average Temperature Coefficient of output voltage	I_{OUT} = 5 mA, 0°C ≤ T_J ≤ 125°C		1.1		mV/°C

Metal Can Package — Aluminum

Plastic Package

MICROCHIP

ENHANCED PIC16C5X

EPROM/ROM-Based 8-Bit CMOS Microcontroller Series

Devices Included in this Data Sheet:

- PIC16C52
- PIC16C54A
- PIC16CR57B
- PIC16C58A
- PIC16CR58A

High-Performance RISC CPU:

- Only 33 single word instructions to learn
- All instructions are single cycle (200 ns) except for program branches which are two-cycle
- Operating speed: DC - 20 MHz clock input
  DC - 200 ns instruction cycle

Device	Pins	I/O	EPROM/ ROM	RAM
PIC16C52	18	12	384	25
PIC16C54A	18	12	512	25
PIC16CR57B	28	20	2K	72
PIC16C58A	18	12	2K	73
PIC16CR58A	18	12	2K	73

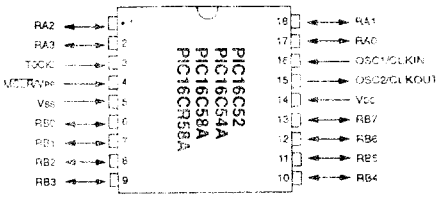
- 12-bit wide instructions
- 8-bit wide data path
- Seven or eight special function hardware registers
- Two-level deep hardware stack
- Direct, indirect and relative addressing modes for data and instructions

Peripheral Features:

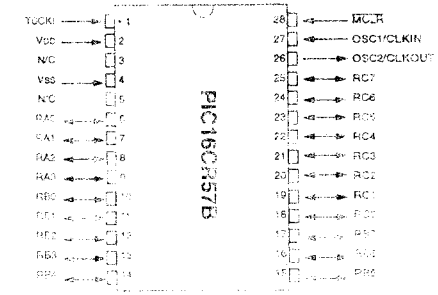
- 8-bit real time clock/counter (TMR0) with 8 bit programmable prescaler
- Power-On Reset (POR)
- Device Reset Timer (DRT)
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- Programmable code-protection
- Power saving SLEEP mode
- Selectable oscillator options:
  - RC: Low-cost RC oscillator
  - XT: Standard crystal/resonator
  - HS: High-speed crystal/resonator
  - LP: Power saving, low frequency crystal

Pin Diagrams

PDIP, SOIC, Windowed CERDIP

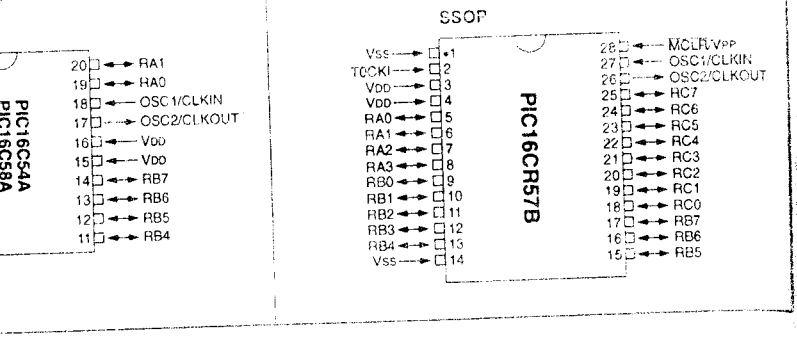


PDIP, SOIC



CMOS Technology:

- Low-power, high-speed CMOS EPROM/ROM technology
- Fully static design
- Wide-operating voltage range:
  - EPROM Commercial/Industrial 2.5V to 6.25V
  - ROM Commercial/Industrial 2.5V to 6.25V
  - EPROM Automotive 2.5V to 6.0V
- Low-power consumption:
  - < 2 mA typical @ 5V, 4 MHz
  - 15 µA typical @ 3V, 32 kHz
  - < 0.6 µA typical standby current (with WDT disabled) @ 3V, 0°C to 70°C



To Our Valued Customers

...e to improve the quality of all our products and documentation. We have spent an exceptio...
...ensure that these documents are correct. However, we realize that we may have missed a...
...any information that is missing or appears in error, please use the reader response form in...
...to inform us. We appreciate your assistance in making this a better document.

...amily of low-cost, high performance, 8-bit, fully ...atic, EPROM/ROM-based CMOS microcontrollers. ...s family is pin and software compatible with the ...C16C5X family of devices in a new enhanced ...ocess technology. It employs a RISC architecture ...h only 33 single word/single cycle instructions. All ...structions are single cycle (200 ns) except for ...gram branches which take two cycles. The ...nanced PIC16C5X delivers performance an order of ...gnitude higher than its competitors in the same ...r category. The 12-bit wide instructions are highly ...metrical resulting in 2:1 code compression over ...-bit microcontrollers in its class. The easy to use ...easy to remember instruction set reduces ...opment time significantly.

...Enhanced PIC16C5X products are equipped with ...features that reduce system cost and power ...rements. The Power-On Reset (POR) and Device ... Timer (DRT) eliminate the need for external ... circuitry. There are four oscillator configurations ...oose from, including the power-saving LP (Low ...er) oscillator and cost saving RC oscillator. Power ...g SLEEP mode, Watchdog Timer and code ...tion features improve system cost, power and ...ty.

...V erasable CERDIP packaged versions are ideal ...de development, while the cost-effective One ... Programmable (OTP) versions are suitable for ...tion in any volume. The customer can take full ...ge of Microchip's price leadership in OTP ...rollers while benefiting from the OTP's ...

...C16C5X products are supported by a ...ed macro assembler, a software simulator, an ...mulator, a 'C' compiler, fuzzy logic support ...w-cost development programmer, and a full ... programmer. All the tools are supported on ... and compatible machines.

...ranging from high-speed automotive and appliance motor control to low-power remote transmitters/receivers, pointing devices and telecom processors. The EPROM technology makes customizing application programs (transmitter codes, motor speeds, receiver frequencies, etc.) extremely fast and convenient. The small footprint packages, for through hole or surface mounting, make this microcontroller series perfect for applications with space limitations. Low-cost, low-power, high performance, ease of use and I/O flexibility make the PIC16C5X series very versatile even in areas where no microcontroller use has been considered before (e.g., timer functions, replacement of "glue" logic in larger systems, coprocessor applications).

Maximum Frequency of Operation (MHz)	Program Memory (14K words)	Program Memory (Bytes)	Timer Module(s)	I/O Pins	Voltage Range (Volts)	Number of Instructions	Packages
PIC16C62	4	384	—	25	TMR0	12	2.5-6.25	33	18-pin DIP, SOIC
PIC16C64	20	512	—	33	TMR0	12	2.5-6.25	33	**18-pin DIP, SOIC; 20-pin SSOP**
PIC16C64A	20	512	—	33	TMR0	12	2.0-6.25	33	18-pin DIP, SOIC; 20-pin SSOP
PIC16CR64A	20	—	512	25	TMR0	12	2.0-6.25	33	**18-pin DIP, SOIC; 20-pin SSOP**
PIC16C65	20	512	—	24	TMR0	20	2.5-6.25	33	**28-pin DIP, SOIC, SSOP**
PIC16C66	20	1K	—	25	TMR0	12	2.5-6.25	33	**18-pin DIP, SOIC; 20-pin SSOP**
PIC16C67	20	2K	—	72	TMR0	20	2.5-6.25	33	**28-pin DIP, SOIC, SSOP**
PIC16CR67B	20	—	2K	72	TMR0	20	2.5-6.25	33	28-pin DIP, SOIC, SSOP
PIC16C58A	20	2K	—	73	TMR0	12	2.0-6.25	33	18-pin DIP, SOIC; 20-pin SSOP
PIC16CR58A	20	—	2K	73	TMR0	12	2.5-6.25	33	18-pin DIP, SOIC; 20-pin SSOP

Legend: Grayed boxes: devices NOT covered in this data sheet.
All PIC16/17 Family devices have Power-On Reset, selectable Watchdog Timer, selectable code protect and high I/O current capability.

A variety of frequency ranges and packaging options are available. Depending on application and production requirements, the proper device option can be selected using the information in this section. When placing orders, please use the Enhanced PIC16C5X Product Identification System at the back of this data sheet to specify the correct part number.

For the Enhanced PIC16C5X family of devices, there are four device types, as indicated in the device number:

- **C**, as in PIC16C54A. These devices have EPROM program memory and operate over the standard voltage range.
- **LC**, as in PIC16LC54A. These devices have EPROM program memory and operate over an extended voltage range.
- **CR**, as in PIC16CR54A. These devices have ROM program memory and operate over the standard voltage range.
- **LCR**, as in PIC16LCR54A. These devices have ROM program memory and operate over an extended voltage range.

2.1 UV Erasable Devices

The UV erasable versions, offered in CERDIP packages, are optimal for prototype development and pilot programs.

UV erasable devices can be programmed for any of the four oscillator configurations. Microchip's PICSTART® and PRO MATE™ programmers both support programming of the Enhanced PIC16C5X. Third party programmers also are available; refer to the Third Party Guide for a list of sources.

2.2 One-Time-Programmable (OTP) Devices

The availability of OTP devices is especially useful for customers expecting frequent code changes and updates.

The OTP devices, packaged in plastic packages, permit the user to program them once. In addition to this program memory, the configuration bits must be programmed.

Microchip offers a QTP Programming Service for factory production orders. This service is made available for users who choose not to program a medium to high quantity of units and whose code patterns have stabilized. The devices are identical to the OTP devices but with all EPROM locations and configuration bit options already programmed by the factory. Certain code and prototype verification procedures apply before production shipments are available. Please contact your Microchip Technology sales office for more details.

2.4 Serialized Quick-Turnaround-Production (SQTP℠) Devices

Microchip offers the unique programming service where a few user-defined locations in each device are programmed with different serial numbers. The serial numbers may be random, pseudo-random or sequential.

Serial programming allows each device to have a unique number which can serve as an entry code, password or ID number.

2.5 Read Only Memory (ROM) Devices

Microchip offers masked ROM versions of several of the highest volume parts, giving the customer a low cost option for high volume, mature products.

The high performance of the PIC16C5X family can be attributed to a number of architectural features commonly found in RISC microprocessors. To begin with, the PIC16C5X uses a Harvard architecture in which program and data are accessed on separate buses. This improves bandwidth over traditional von Neumann architecture where program and data are fetched on the same bus. Separating program and data memory further allows instructions to be sized differently than the 8-bit wide data word. Instruction opcodes are 12-bits wide making it possible to have all single word instructions. A 12-bit wide program memory access bus fetches a 12-bit instruction in a single cycle. A two-stage pipeline overlaps fetch and execution of instructions. Consequently, all instructions (33) execute in a single cycle (200ns @ 20MHz) except for program branches.

The PIC16C52 address 384 x 12 of program memory, the PIC16C54A address 512 x 12 of program memory, and the PIC16CR57B and PIC16C58A/CR58A address 2K x 12 of program memory. All program memory is internal.

The PIC16C5X can directly or indirectly address its register files and data memory. All special function registers including the program counter are mapped in the data memory. The PIC16C5X has a highly orthogonal (symmetrical) instruction set that makes it possible to carry out any operation on any register using any addressing mode. This symmetrical nature and lack of 'special optimal situations' make programming with the PIC16C5X simple yet efficient. In addition, the learning curve is reduced significantly.

working register. The ALU is a general purpo arithmetic unit. It performs arithmetic and Boole functions between data in the working register and a register file.

The ALU is 8-bits wide and capable of additio subtraction, shift and logical operations. Unles otherwise mentioned, arithmetic operations are two complement in nature. In two-operand instruction typically one operand is the W (working) register. Th other operand is either a file register or an immedia constant. In single operand instructions, the operan is either the W register or a file register.

The W register is an 8-bit working register used fo ALU operations. It is not an addressable register.

Depending on the instruction executed, the ALU ma affect the values of the Carry (C), Digit Carry (DC) and Zero (Z) bits in the STATUS register. The C an DC bits operate as a $\overline{\text{borrow}}$ and $\overline{\text{digit borrow}}$ out bi respectively, in subtraction. See the SUBWF and ADDW instructions for examples.

A simplified block diagram is shown in Figure 3-1, with the corresponding device pins described in Table 3-1 and Table 3-2.

IC	SSOP No.	I/O/P Type	Input Levels	Description
	5	I/O	TTL	Bi-directional I/O port
	6	I/O	TTL	
	7	I/O	TTL	
	8	I/O	TTL	
	9	I/O	TTL	Bi-directional I/O port
	10	I/O	TTL	
	11	I/O	TTL	
	12	I/O	TTL	
	13	I/O	TTL	
	15	I/O	TTL	
	16	I/O	TTL	
	17	I/O	TTL	
	18	I/O	TTL	Bi-directional I/O port
	19	I/O	TTL	
	20	I/O	TTL	
	21	I/O	TTL	
	22	I/O	TTL	
	23	I/O	TTL	
	24	I/O	TTL	
	25	I/O	TTL	
	2	I	ST	Clock input to Timer0. Must be tied to Vss or VDD if not in use to reduce current consumption.
	28	I	ST	Master clear (reset) input. This pin is an active low reset to the device.
	27	I	ST	Oscillator crystal input/external clock source input.
	26	O	--	Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, OSC2 pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.
	3,4	P	-	Positive supply for logic and I/O pins.
	1,14	P	--	Ground reference for logic and I/O pins.
	--	--	--	Unused, do not connect

out, I/O = input/output,
Not Used,
ST = Schmitt Trigger input

The clock input (OSC1/CLKIN pin) is internally divided by four to generate four non-overlapping quadrature clocks namely Q1, Q2, Q3 and Q4. Internally, the program counter is incremented every Q1, and the instruction is fetched from program memory and latched into instruction register in Q4. It is decoded and executed during the following Q1 through Q4. The clocks and instruction execution flow is shown in Figure 3-2 and Example 3-1.

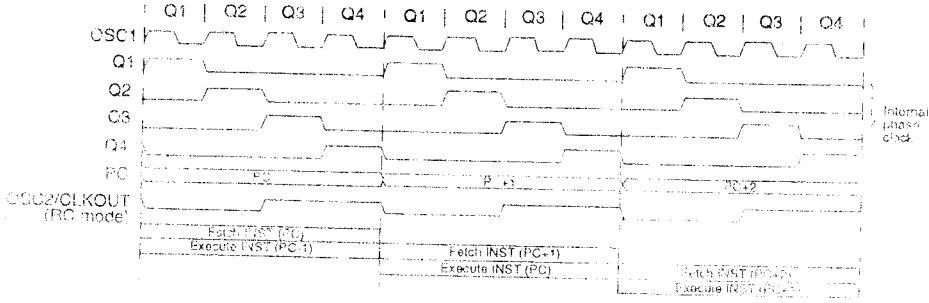
3.2 Instruction Flow/Pipelining

An Instruction Cycle consists of four Q cycles (Q1, Q2, Q3 and Q4). The instruction fetch and execute are pipelined such that fetch takes one instruction cycle while decode and execute takes another instruction cycle. However, due to the pipelining, each instruction effectively executes in one cycle. If an instruction causes the program counter to change (e.g., GOTO) then two cycles are required to complete the instruction (Example 3-1).

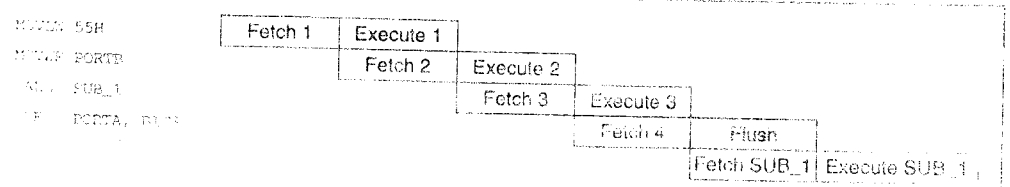
A fetch cycle begins with the program counter (PC) incrementing in Q1.

In the execution cycle, the fetched instruction is latched into the Instruction Register (IR) in cycle Q1. This instruction is then decoded and executed during the Q2, Q3, and Q4 cycles. Data memory is read during Q2 (operand read) and written during Q4 (destination write).

FIGURE 3-2: CLOCK/INSTRUCTION CYCLE



EXAMPLE 3-1: INSTRUCTION PIPELINE FLOW



All instructions are single cycle, except for any program branches. These take two cycles since the fetch instruction is "flushed" from the pipeline while the new instruction is being fetched and then executed.

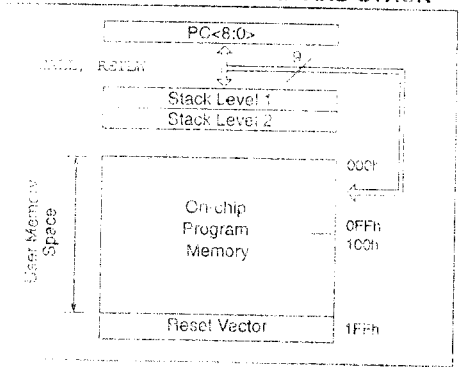
PIC16C5X memory is organized into program memory and data memory. For devices with more than 512 bytes of program memory, a paging scheme is used. Program memory pages are accessed using one or two STATUS register bits. For devices with a data memory register file of more than 32 registers, a banking scheme is used. Data memory banks are accessed using the File Selection Register (FSR).

4.1 Program Memory Organization

The PIC16C52 has a 9-bit Program Counter (PC) capable of addressing a 384 x 12 program memory space (Figure 4-2). The PIC16C54A has a 9-bit Program Counter (PC) capable of addressing a 512 x 12 program memory space (Figure 4-1). The PIC16CR57B, PIC16C58A, and PIC16CR58A have an 11-bit Program Counter capable of addressing a 2K x 12 program memory space (Figure 4-3). Accessing a location above the physically implemented address will cause a wraparound.

The reset vector for the PIC16C52 is at 17FL. A NOP at the reset vector location will cause a restart at location 000h. The reset vector for the PIC16C54A is at 1FFh, for the PIC16CR57B, PIC16C58A, and PIC16CR58A at 7FFh.

FIGURE 4-1: PIC16C54A PROGRAM MEMORY MAP AND STACK



MEMORY MAP AND STACK

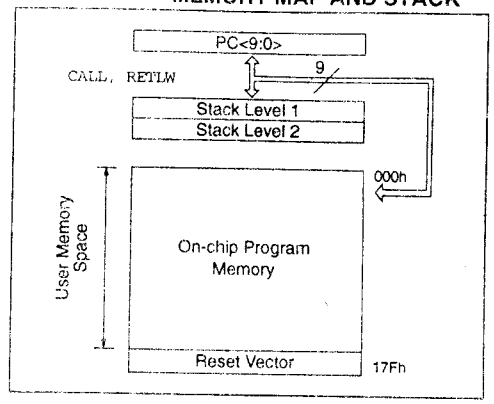
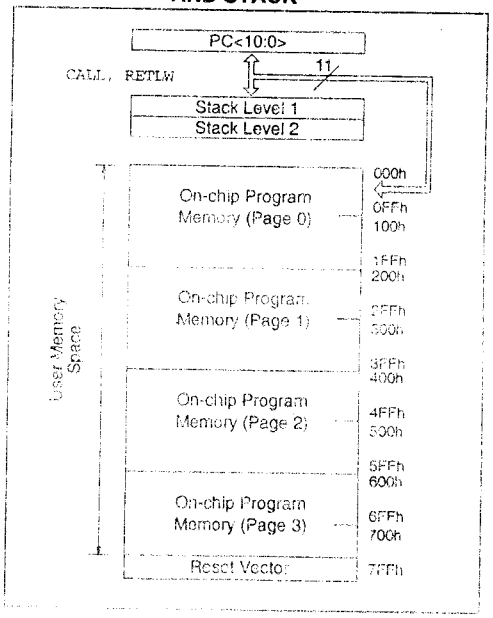


FIGURE 4-3: PIC16CR57B/C58A/CR58A PROGRAM MEMORY MAP AND STACK



...osed of registers, or bytes of ...emory for a device is specified ... register file is divided into two ...ecial function registers and ...ers.

... registers include the TMR0 ... Counter (PC), the Status ...ers (ports), and the File Select ...ition, special purpose registers ...he I/O port configuration and ...

...egisters are used for data and ...er command of the instructions.

... PIC16C54A, the register file is ...ial function registers and 25 ...ers (Figure 4-4).

... the register file is composed of ...egisters, 24 general purpose ...48 additional general purpose ...e addressed using a banking ...

...d PIC16CR58A, the register file ...ial function registers, 25 general ...d up to 48 additional general ...i may be addressed using a ...re 4-6).

...URPOSE REGISTER FILE

...essed either directly or indirectly ... register FSR (Section 4.7).

REGISTER FILE MAP

File Address		
00h	INDF(1)	
01h	TMR0	
02h	PCL	
03h	STATUS	
04h	FSR	
05h	PORTA	
06h	PORTB	
07h		
0Fh	General Purpose Registers	
10h		
1Fh		

Note 1: Not a physical register. See Section 4.7

FSR<6:5> →	00	01	10	11
File Address				
00h	INDF(1)	20h	40h	60h
01h	TMR0			
02h	PCL			
03h	STATUS			
04h	FSR			
05h	PORTA	Addresses map back to addresses in Bank 0.		
06h	PORTB			
07h	PORTC			
08h	General Purpose Registers			
0Fh		2Fh	4Fh	6Fh
10h	General Purpose Registers	30h	50h	70h
1Fh		3Fh	5Fh	7Fh
	Bank 0	Bank 1	Bank 2	Bank 3

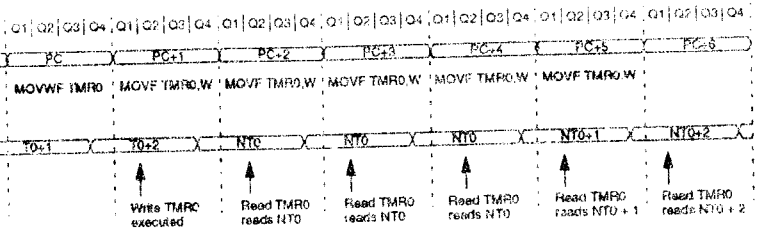
Note 1: Not a physical register. See Section 4.7

FIGURE 4-6: PIC16C58A/CR58A REGISTER FILE MAP

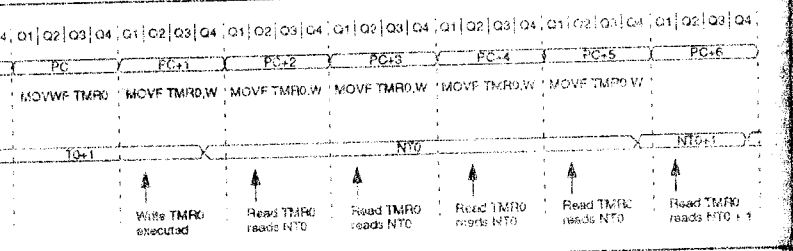
FSR<6:5> →	00	01	10	11
File Address				
00h	INDF(1)	20h	40h	60h
01h	TMR0			
02h	PCL			
03h	STATUS			
04h	FSR			
05h	PORTA	Addresses map back to addresses in Bank 0.		
06h	PORTB			
07h	General Purpose Registers			
0Fh		2Fh	4Fh	6Fh
10h	General Purpose Registers	30h	50h	70h
1Fh		3Fh	5Fh	7Fh
	Bank 0	Bank 1	Bank 2	Bank 3

Note 1: Not a physical register. See Section 4.7

NAL CLOCK/NO PRESCALE



0 TIMING:
NAL CLOCK/PRESCALE 1:2



STERS ASSOCIATED WITH TIMER0

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset	Value on MCLR and WDT Reset
Timer0 - 8-bit real-time clock/counter								xxxx xxxx	uuuu uuuu
—	—	T0CS	T0SE	PSA	PS2	PS1	PS0	--11 1111	--11 1111

Unimplemented bits,
nted, x = unknown, u = unchanged,

When an external clock input is used for Timer0, it must meet certain requirements. The external clock requirement is due to internal phase clock (Tosc) synchronization. Also, there is a delay in the actual incrementing of Timer0 after synchronization.

6.1.1 EXTERNAL CLOCK SYNCHRONIZATION

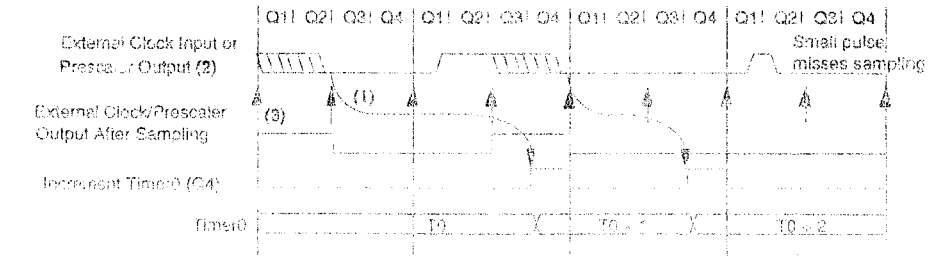
When no prescaler is used, the external clock input is the same as the prescaler output. The synchronization of T0CKI with the internal phase clocks is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks (Figure 6-5). Therefore, it is necessary for T0CKI to be high for at least 2Tosc (and a small RC delay of 20 ns) and low for at least 2Tosc (and a small RC delay of 20 ns). Refer to the electrical specification of the desired device.

divided by the asynchronous ripple counter-type prescaler so that the prescaler output is symmetrical. For the external clock to meet the sampling requirement, the ripple counter must be taken into account. Therefore, it is necessary for T0CKI to have a period of at least 4Tosc (and a small RC delay of 40 ns) divided by the prescaler value. The only requirement on T0CKI high and low time is that they do not violate the minimum pulse width requirement of 10 ns. Refer to parameters 40, 41 and 42 in the electrical specification of the desired device.

6.1.2 TIMER0 INCREMENT DELAY

Since the prescaler output is synchronized with the internal clocks, there is a small delay from the time the external clock edge occurs to the time the Timer0 module is actually incremented. Figure 6-5 shows the delay from the external clock edge to the timer incrementing.

FIGURE 6-6: TIMER0 TIMING WITH EXTERNAL CLOCK



Note 1: Delay from clock input change to Timer0 increment is 3Tosc to 7Tosc. (Duration of Q = Tosc). Therefore, the error in measuring the interval between two edges on Timer0 input = ±4Tosc max.
2: External clock if no prescaler selected, Prescaler output otherwise.
3: The arrows indicate the points in time where sampling occurs.

...mplemented on

...ble as a prescaler for the ...ostscaler for the Watchdog ...vely (Section 6.1.2). For ...is being referred to as ...s data sheet. Note that the ...either the Timer0 module or ...us, a prescaler assignment ... means that there is no ...d vice-versa.

...PS0 bits (OPTION<3:0>) ...nment and prescale ratio.

...mer0 module, all instructions ...er (e.g., CLRF 1, MOVWF 1, ...ear the prescaler. When ...WDT instruction will clear the ...WDT. The prescaler is neither ...en a RESET, the prescaler

...ESCALER ASSIGNMENT

...is fully under software control ..."on the fly" during program ...intended device RESET, the

following instruction sequence (Example 6-1) must be executed when changing the prescaler assignment from Timer0 to the WDT.

EXAMPLE 6-1: CHANGING PRESCALER (TIMER0→WDT)

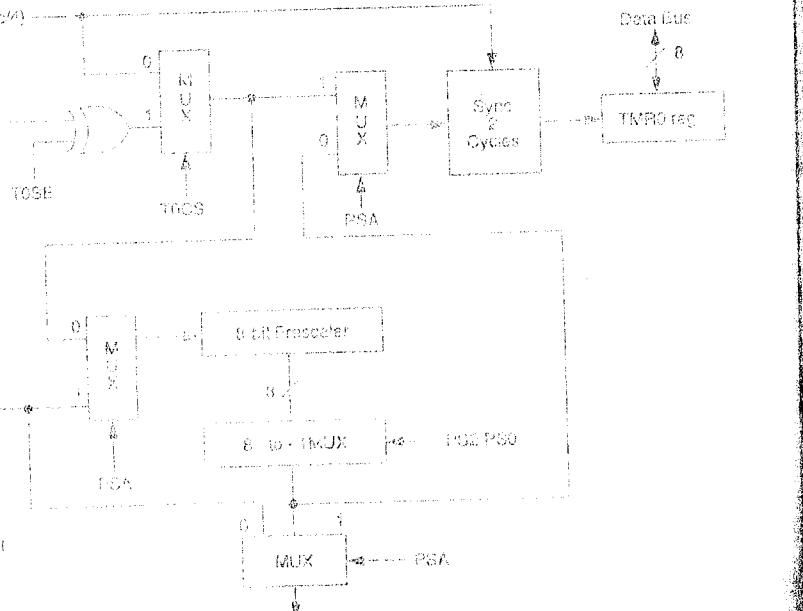
```
1. CLRWDT                    ;Clear WDT
2. CLRF   TMR0               ;Clear TMR0 & Prescaler
3. MOVLW  '00xx1111'b;       ;These 3 lines (5, 6, 7)
4. OPTION                    ; are required only if
                             ; desired
5. CLRWDT                    ;PS<2:0> are 000 or 001
6. MOVLW  '00xx1xxx'b        ;Set Postscaler to
7. OPTION                    ; desired WDT rate
```

To change prescaler from the WDT to the Timer0 module, use the sequence shown in Example 6-2. This sequence must be used even if the WDT is disabled. A CLRWDT instruction should be executed before switching the prescaler.

EXAMPLE 6-2: CHANGING PRESCALER (WDT→TIMER0)

```
CLRWDT                       ;Clear WDT and
                             ;prescaler
MOVLW   'xxxx0xxx'           ;Select TMR0, new
                             ;prescale value and
                             ;clock source
OPTION
```

...K DIAGRAM OF THE TIMER0/WDT PRESCALER



CPU

What sets a microcontroller apart from other processors are special circuits to deal with the needs of real-time applications. The PIC16C5X family of microcontrollers has a host of such features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving operating modes and offer code protection. These features are:

- Oscillator selection
- Reset
- Power-On Reset (POR)
- Device Reset Timer (DRT)
- Watchdog Timer (WDT) (not implemented on PIC16C52)
- SLEEP
- Code protection
- ID locations

Most PIC16C5X's have a Watchdog Timer which can be shut off only through configuration bit WDTE. It runs off of its own RC oscillator for added reliability. There is an 18 ms delay provided by the Device Reset Timer (DRT), intended to keep the chip in reset until the crystal oscillator is stable. With this timer on-chip, most applications need no external reset circuitry.

current power-down mode. The user can wake up from SLEEP through external reset or through a Watchdog Timer time-out. Several oscillator options are also made available to allow the part to fit the application. The RC oscillator option saves system cost while the LP crystal option saves power. A set of configuration bits are used to select various options.

7.1 Configuration Bits

The PIC16C5X configuration word consists of 4 or 12 bits, depending on device configuration. Configuration bits can be programmed to select various device configurations. Two bits are for the selection of the oscillator type and one bit is the Watchdog Timer enable bit. One bit is the code protection bit (Figure 7-1) for the PIC16C54A or PIC16C58A devices. Nine bits are code protection bits (Figure 7-2) for the PIC16CR57B or PIC16CR58B devices.

QTP or ROM devices have the oscillator configuration programmed at the factory and these parts are tested accordingly (see "Product Identification System" or the inside back cover).

...IGURE 7-1: CONFIGURATION WORD FOR PIC16C52/C54A/C58A

—	—	—	—	—	—	—	CP	WDTE	FOSC1	FOSC0		Register:	CONFIG
11	10	9	8	7	6	5	4	3	2	1	bit0	Address(1)	FFFh

...-11:4 Unimplemented: Read as '1'

...4 CP: Code protection bit
1 = Code protection off
0 = Code protection on

...3 WDTE: Watchdog Timer enable bit (Not implemented on PIC16C52)
1 = WDT enabled
0 = WDT disabled

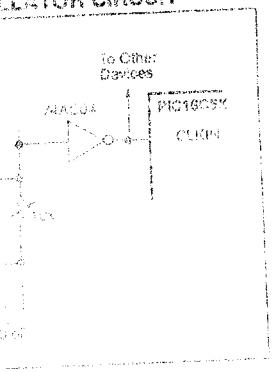
...2:1 FOSC1:FOSC0: Oscillator selection bits
11 = RC oscillator
10 = HS oscillator
01 = XT oscillator
00 = LP oscillator

...Refer to the PIC16C5X Programming Specifications (literature number DS30190) to determine how to access the configuration word.

illator or a simple oscillator
n be used as an external
Prepackaged oscillators
range and better stability. A
cillator will provide good
ates. Two types of crystal
e used: one with parallel
ries resonance.

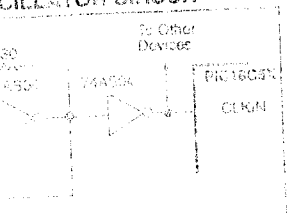
ementation of a parallel
. The circuit is designed to
quency of the crystal. The
e the 180-degree phase shift
equires. The 4.7 kΩ resistor
dback for stability. The 10 kΩ
74AS04 in the linear region.
used for external oscillator

RNAL PARALLEL
NANT CRYSTAL
LLATOR CIRCUIT



eries resonant oscillator circuit.
signed to use the fundamental
otal. The inverter performs a
t in a series resonant oscillator
esistors provide the negative
verters in their linear region.

TERNAL SERIES
SONANT CRYSTAL
CILLATOR CIRCUIT



For timing insensitive applications, the RC device option offers additional cost savings. The RC oscillator frequency is a function of the supply voltage, the resistor (Rext) and capacitor (Cext) values, and the operating temperature. In addition to this, the oscillator frequency will vary from unit to unit due to normal process parameter variation. Furthermore, the difference in lead frame capacitance between package types will also affect the oscillation frequency, especially for low Cext values. The user also needs to take into account variation due to tolerance of external R and C components used.

Figure 7-7 shows how the R/C combination is connected to the PIC16C5X. For Rext values below 2.2 kΩ, the oscillator operation may become unstable, or stop completely. For very high Rext values (e.g., 1 MΩ) the oscillator becomes sensitive to noise, humidity and leakage. Thus, we recommend keeping Rext between 3 kΩ and 100 kΩ.

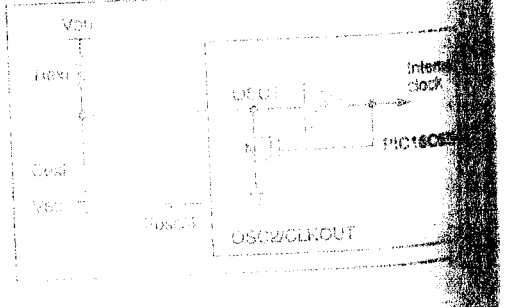
Although the oscillator will operate with no external capacitor (Cext = 0 pF), we recommend using values above 20 pF for noise and stability reasons. With no or small external capacitance, the oscillation frequency can vary dramatically due to changes in external capacitances, such as PCB trace capacitance or package lead frame capacitance.

The Electrical Specifications sections show RC frequency variation from part to part due to normal process variation. The variation is larger for larger R (since leakage current variation will affect RC frequency more) and for smaller C (since variation of input capacitance will affect RC frequency more).

Also, see the Electrical Specifications sections for variation of oscillator frequency due to VDD for given Rext/Cext values as well as frequency variation due to operating temperature for given R, C, and VDD values.

The oscillator frequency, divided by 4, is available on the OSC2/CLKOUT pin, and can be used for test purposes or to synchronize other logic.

FIGURE 7-7: RC OSCILLATOR MODE



following ways.

- Power-On Reset (POR)
- $\overline{MCLR}$ reset (normal operation)
- $\overline{MCLR}$ wake-up reset (from SLEEP)
- WDT reset (normal operation)
- WDT wake-up reset (from SLEEP)

WDT not implemented on PIC16C52

Table 7-5 shows these reset conditions for the PCL and STATUS registers.

"reset state" on Power-On Reset (POR), $\overline{MCLR}$ or WDT reset. A $\overline{MCLR}$ or WDT wake-up from SLEEP also results in a device reset, and not a continuation of operation before SLEEP.

The $\overline{TO}$ and $\overline{PD}$ bits (STATUS <4:3>) are set or cleared depending on the different reset conditions (Section 7.7). These bits may be used to determine the nature of the reset.

Table 7-6 lists a full description of reset states of all registers. Figure 7-8 shows a simplified block diagram of the on-chip reset circuit.

TABLE 7-5: RESET CONDITIONS FOR SPECIAL REGISTERS

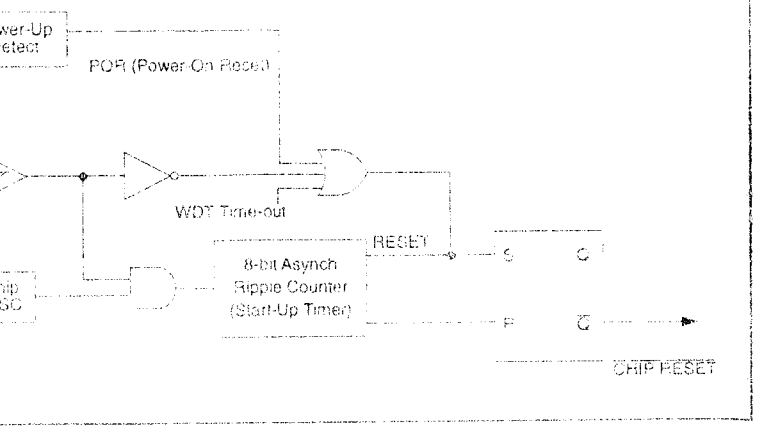
Condition	PCL Addr: 02h	STATUS Addr: 03h
Power-On Reset	1111 1111	0001 1xxx
$\overline{MCLR}$ reset (normal operation)	1111 1111	000u uuuu(1)
$\overline{MCLR}$ wake-up (from SLEEP)	1111 1111	0001 0uuu
WDT reset (normal operation)	1111 1111	0000 1uuu(2)
WDT wake-up (from SLEEP)	1111 1111	0000 0uuu

Legend: u = unchanged, x = unknown, - = unimplemented read as '0'.
Note 1: $\overline{TO}$ and $\overline{PD}$ bits retain their last value until one of the other reset conditions occur.
2. The CLRWDT instruction will set the $\overline{TO}$ and $\overline{PD}$ bits.

TABLE 7-6: RESET CONDITIONS FOR ALL REGISTERS

Register	Address	Power-On Reset	$\overline{MCLR}$ or WDT Reset
W	N/A	xxxx xxxx	uuuu uuuu
TRIS	N/A	1111 1111	1111 1111
OPTION	N/A	--11 1111	--uu uuuu
INDF	00h	xxxx xxxx	uuuu uuuu
TMR0	01h	xxxx xxxx	uuuu uuuu
PCL(1)	02h	1111 1111	1111 1111
STATUS(2)	03h	0001 1xxx	000q quuu
FSR	04h	1xxx xxxx	uuuu uuuu
PORTA	05h	---- xxxx	---- uuuu
PORTB	06h	xxxx xxxx	uuuu uuuu
PORTC(2)	07h	xxxx xxxx	uuuu uuuu
General Purpose Register files	08-7Fh	xxxx xxxx	uuuu uuuu

Legend: u = unchanged, x = unknown, - = unimplemented, q = value depends on condition
Note 1: See Table 7-5 for reset value for specific conditions.
2: General purpose register file on the PIC16C52/C54/C56.



...) circuitry which provides an internal chip ... most power-up situations. To use this feature, ... merely ties the MCLR/VPP pin (Figure 7-9) to ... A simplified block diagram of the on-chip ...-On Reset circuit is shown in Figure 7-8.

... Power-On Reset circuit and the Device Reset ... (Section 7.5) circuit are closely related. On ...-up, the reset latch is set and the DRT is reset. ... DRT timer begins counting once it detects MCLR ... high. After the time-out period, which is typically ..., it will reset the reset latch and thus end the ... reset signal.

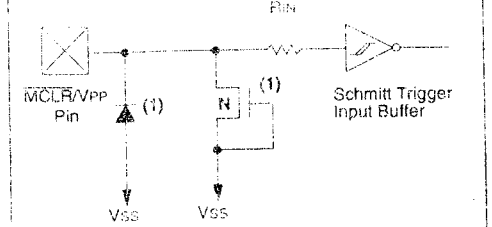
... example where MCLR is not tied to VDD is ... Figure 7-11. VDD is allowed to rise and ... before bringing MCLR high. The chip will ... come out of reset TDRT msec after MCLR ... high.

... 7-12, the on-chip Power-On Reset feature is ... used (MCLR and VDD are tied together). The ... is stable before the start-up timer times out and ... no problem in getting a proper reset. However, ... 7-13 depicts a problem situation where VDD ... too slowly. The time between when the DRT ... sees a high on the MCLR/VPP pin, and when the ... VPP pin (and VDD) actually reach their full ... is too long. In this situation, when the start-up ... times out, VDD has not reached the VDD (min) ... and the chip is, therefore, not guaranteed to ... correctly. For such situations, we recommend ... external RC circuits be used to achieve longer ... times (Figure 7-10).

When the device starts normal operation (exits the reset condition), device operating parameters (voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not met, the device must be held in reset until the operating conditions are met.

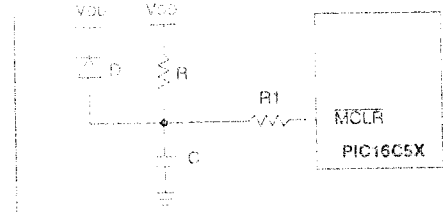
... information on PIC16C5X POR, see ... Considerations - AN522 in the Embedded ... Handbook.

... circuit does not produce an internal reset ... voltages.

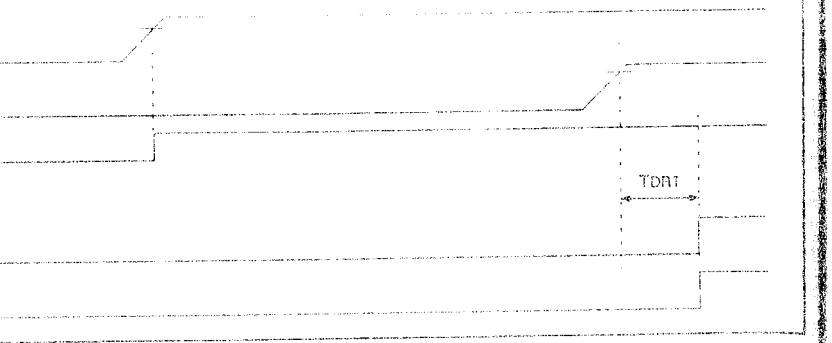


Note 1: ESD protection circuits

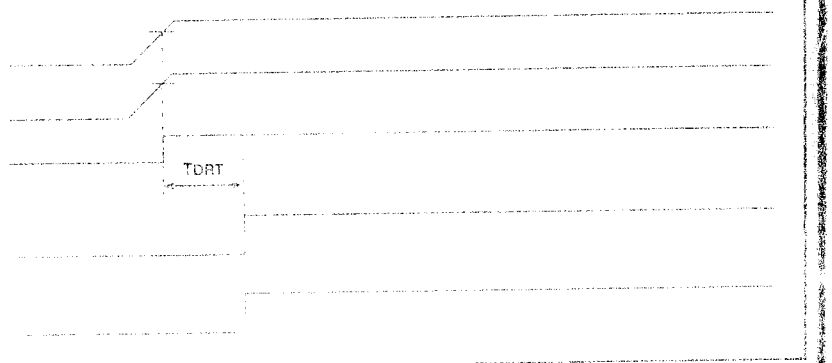
FIGURE 7-10: EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW VDD POWER-UP)



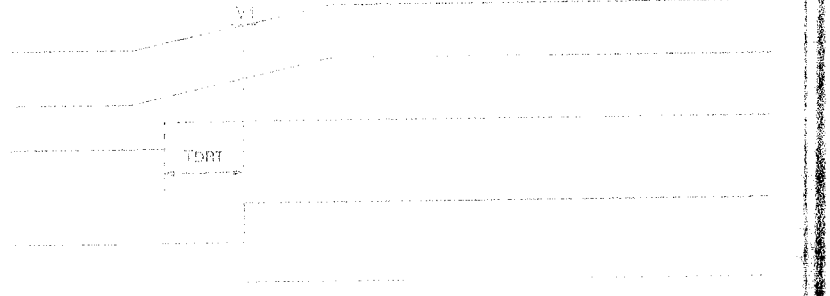
- External Power-On Reset circuit is required only if VDD power-up is too slow. The diode D helps discharge the capacitor quickly when VDD powers down.
- R < 40 kΩ is recommended to make sure that voltage drop across R does not violate the device electrical specification.
- R1 = 100Ω to 1 kΩ will limit any current flowing into MCLR from external capacitor C in the event of MCLR pin breakdown due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS).



-OUT SEQUENCE ON POWER-UP (MCLR TIED TO VDD): FAST VDD RISE TIME



-OUT SEQUENCE ON POWER-UP (MCLR TIED TO VDD): SLOW VDD RISE TIME



...DD rises slowly, the Time-out expires long before VDD has reached its final value. In ... example, the chip will reset properly if, and only if, VDD ...

...e Device Reset Timer (DRT) provides a fixed ... ...nal time-out on reset. The DRT operates on an ...ternal RC oscillator. The processor is kept in RESET ...s long as the DRT is active. The DRT delay allows ...DD to rise above VDD min., and for the oscillator to ...abilize.

...Oscillator circuits based on crystals or ceramic ...esonators require a certain time after power-up to ...stablish a stable oscillation. The on-chip DRT keeps ...e device in a RESET condition for approximately 18 ...s after the voltage on the MCLR/VPP pin has ...ched a logic high (VIHMC) level. Thus, external RC ...mponents connected to the MCLR input are not ...ired in most cases, allowing for savings in ...st-sensitive and/or space restricted applications.

...e Device Reset time delay will vary from chip to chip ...e to VDD, temperature, and process variation. See ...C parameters for details.

...e DRT will also be triggered upon a Watchdog ...er time-out. This is particularly important for ...plications using the WDT to wake the PIC16C5X ...m SLEEP mode automatically.

The Watchdog Timer (WDT) is a free running on-chip RC oscillator which does not require any external components. This RC oscillator is separate from the RC oscillator of the OSC1/CLKIN pin. That means that the WDT will run even if the clock on the OSC1/CLKIN and OSC2/CLKOUT pins have been stopped, for example, by execution of a SLEEP instruction. During normal operation or SLEEP, a WDT reset or wake-up reset generates a device RESET.

The $\overline{TO}$ bit (STATUS<4>) will be cleared upon a Watchdog Timer reset.

The WDT can be permanently disabled by programming the configuration bit WDTE as a '0' (Section 7.1). Refer to the PIC16C5X Programming Specifications (literature number DS30190) to determine how to access the configuration word.

7.6.1 WDT PERIOD

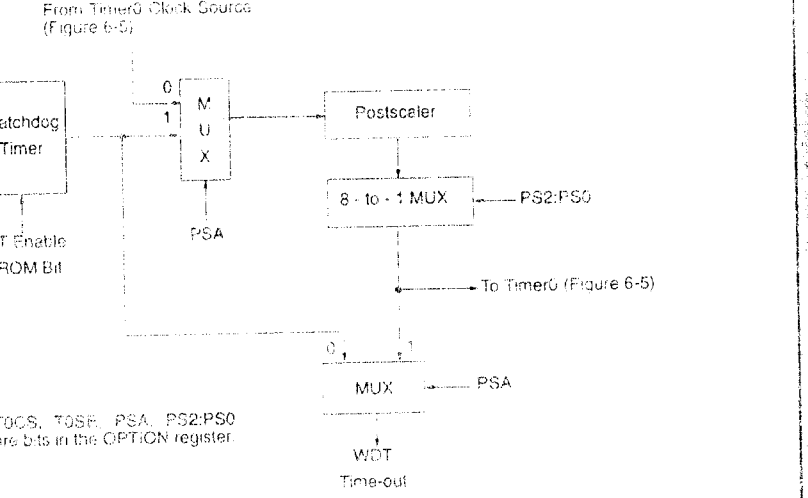
The WDT has a nominal time-out period of 18 ms, (with no prescaler). If a longer time-out period is desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT (under software control) by writing to the OPTION register. Thus, time-out a period of a nominal 2.3 seconds can be realized. These periods vary with temperature, VDD and part-to-part process variations (see DC specs).

Under worst case conditions (VDD = Min., Temperature = Max., max. WDT prescaler), it may take several seconds before a WDT time-out occurs.

7.6.2 WDT PROGRAMMING CONSIDERATIONS

The CLRWDT instruction clears the WDT and the prescaler, if assigned to the WDT, and prevents it from timing out and generating a device RESET.

The SLEEP instruction resets the WDT and the prescaler, if assigned to the WDT. This gives the maximum SLEEP time before a WDT wake-up reset.



T0CS, T0SE, PSA, PS2:PS0
are bits in the OPTION register.

MARY OF REGISTERS ASSOCIATED WITH THE WATCHDOG TIMER

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset	Value on MCLR and WDT Reset
	--	--	T0CS	T0SE	PSA	PS2	PS1	PS0	--11 1111	--11 1111

Not reset by Watchdog Timer.
ted, read as '0'. = unchanged

and $\overline{PD}$ bits in the STATUS register can be used to determine if a RESET condition has been caused by a power-up condition, a $\overline{MCLR}$ or Watchdog Timer (WDT) reset, or a $\overline{MCLR}$ or WDT wake-up reset.

TABLE 7-8: $\overline{TO}/\overline{PD}$ STATUS AFTER RESET

$\overline{TO}$	$\overline{PD}$	RESET was caused by
1	1	Power-up (POR)
1	u	$\overline{MCLR}$ reset (normal operation)(1)
1	0	$\overline{MCLR}$ wake-up reset (from SLEEP)
0	1	WDT reset (normal operation)
0	0	WDT wake-up reset (from SLEEP)

= unchanged
The $\overline{TO}$ and $\overline{PD}$ bits maintain their status (u) until a reset occurs. A low-pulse on the $\overline{MCLR}$ input does not change the $\overline{TO}$ and $\overline{PD}$ status bits.

The STATUS bits are only affected by events listed in Table 7-9.

TABLE 7-9: EVENTS AFFECTING $\overline{TO}/\overline{PD}$ STATUS BITS

Event	$\overline{TO}$	$\overline{PD}$	Remarks
Power-up	1	1	
Time-out	0	u	No effect on $\overline{PD}$
SLEEP instruction	1	0	
CLRWDT instruction	1	1	
= unchanged			

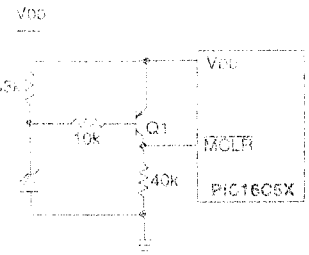
Time-out will occur regardless of the status of the $\overline{TO}$ bit. The SLEEP instruction will be executed regardless of the status of the $\overline{PD}$ bit. Table 7-8 reflects the state of $\overline{TO}$ and $\overline{PD}$ after the corresponding event.

Table 7-8 lists the reset conditions for the special function registers, while Table 7-6 lists the reset conditions for all the registers.

dips below its minimum value, but not to zero, and then recovers. The device should be reset in the event of a brown-out.

To reset PIC16C5X devices when a brown-out occurs, external brown-out protection circuits may be built, as shown in Figure 7-15 and Figure 7-16.

FIGURE 7-15: BROWN-OUT PROTECTION CIRCUIT 1



This circuit will activate reset when VDD goes below Vz + 0.7V (where Vz = Zener voltage).

FIGURE 7-16: BROWN-OUT PROTECTION CIRCUIT 2

This brown-out circuit is less expensive, although less accurate. Transistor Q1 turns off when VDD is below a certain level such that:

$$V_{DD} = \frac{R1}{R1 + R2} \cdot 0.7V$$

If the code protection bit(s) have not been programmed, the on-chip program memory can be read out for verification purposes.

Note: Microchip does not recommend code protecting windowed devices.

7.11 ID Locations

Four memory locations are designated as ID locations where the user can store checksum or other code-identification numbers. These locations are not accessible during normal execution but are readable and writable during program/verify.

Use only the lower 4 bits of the ID locations and always program the upper 8 bits as '1's.

Note: Microchip will assign a unique pattern number for QTP and SQTP requests and for ROM devices. This pattern number will be unique and traceable to the submitted code.

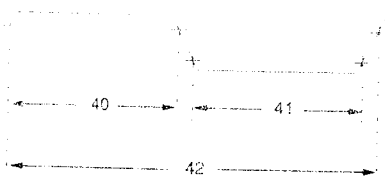
Absolute Maximum Ratings†

Ambient Temperature under bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on VDD with respect to VSS	0 V to +7.5 V
Voltage on MCLR with respect to VSS(2)	0 V to +14 V
Voltage on all other pins with respect to VSS	-0.6 V to (VDD + 0.6 V)
Total Power Dissipation(1)	800 mW
Max. Current out of VSS pin	150 mA
Max. Current into VDD pin	50 mA
Max. Current into an input pin (T0CKI only)	±500 µA
Input Clamp Current, IIK (VI < 0 or VI > VDD)	±20 mA
Output Clamp Current, IOK (VO < 0 or VO > VDD)	±20 mA
Max. Output Current sunk by any I/O pin	10 mA
Max. Output Current sourced by any I/O pin	10 mA
Max. Output Current sourced by a single I/O port (PORTA, B or C)	10 mA
Max. Output Current sunk by a single I/O port (PORTA, B or C)	10 mA

Note 1: Power Dissipation is calculated as follows: $P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum (V_{OL} \times I_{OL})$

Note 2: Voltage spikes below VSS at the MCLR pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50 to 100 Ω should be used when applying a "low" level to the MCLR pin rather than pulling this pin directly to VSS.

†NOTICE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.



...ER0 CLOCK REQUIREMENTS - PIC16C52

...eristics

Standard Operating Conditions (unless otherwise specified)
Operating Temperature 0°C ≤ TA ≤ +70°C (commercial),
-40°C ≤ TA ≤ +85°C (industrial).
Operating Voltage VDD range is described in Section 8.1.

...haracteristic		Min	Typ(1)	Max	Units	Conditions
...CKI High Pulse Width	- No Prescaler	0.5 TCY + 20*	---	---	ns	
	- With Prescaler	10*	---	---	ns	
...CKI Low Pulse Width	- No Prescaler	0.5 TCY + 20*	---	---	ns	
	- With Prescaler	10*	---	---	ns	
...CKI Period		20 or $\frac{T_{CY} + 40^*}{N}$	---	---	ns	Whichever is greater. N = Prescale Value (1, 2, 4, ..., 256)

...are characterized but not tested.
...Typ" columns at 5V, 25°C unless otherwise stated. These parameters are for design guidance only.

...lute Maximum Ratings†

...ent temperature under bias	-55°C to +125°C
...ge temperature	-65°C to +150°C
...age on VDD with respect to VSS	0 to +7.5V
...age on MCLR with respect to VSS(2)	0 to +14V
...age on all other pins with respect to VSS	-0.6V to (VDD + 0.6V)
...power dissipation(1)	800 mW
...current out of VSS pin	150 mA
...current into VDD pin	100 mA
...current into an input pin (T0CKI only)	±500 µA
...clamp current, IIK (VI < 0 or VI > VDD)	±20 mA
...clamp current, IOK (VO < 0 or VO > VDD)	±20 mA
...output current sunk by any I/O pin	25 mA
...output current sourced by any I/O pin	20 mA
...output current sourced by a single I/O port (PORTA or B)	40 mA
...output current sunk by a single I/O port (PORTA or B)	50 mA

Note 1: Power dissipation is calculated as follows: Pdis = VDD x {IDD - Σ IOH} + Σ ((VDD-VOH) x IOH) + Σ(VOL x IOL)

Note 2: Voltage spikes below VSS at the MCLR pin, inducing currents greater than 80mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low" level to the MCLR pin rather than pulling this pin directly to VSS.

† NOTICE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. ...s is a stress rating only and functional operation of the device at those or any other conditions above those ...dicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for ...tended periods may affect device reliability.

PIC16C5X Instruction Set

1.0 INSTRUCTION SET SUMMARY

Each PIC16C5X instruction is a 12-bit word divided into an OPCODE, which specifies the instruction type, and one or more operands which further specify the operation of the instruction. The PIC16C5X instruction set summary in Table 1-2 groups the instructions into byte-oriented, bit-oriented, and literal and control operations. Table 1-1 shows the opcode field descriptions.

For **byte-oriented** instructions, 'f' represents a file register designator and 'd' represents a destination designator. The file register designator is used to specify which one of the 32 file registers is to be used by the instruction.

The destination designator specifies where the result of the operation is to be placed. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed in the file register specified in the instruction.

For **bit-oriented** instructions, 'b' represents a bit field designator which selects the number of the bit affected by the operation, while 'f' represents the number of the file in which the bit is located.

For **literal and control** operations, 'k' represents an eight or nine bit constant or literal value.

TABLE 1-1: OPCODE FIELD DESCRIPTIONS

Field	Description
f	Register file address (0x00 to 0x7F)
W	Working register (accumulator)
b	Bit address within an 8-bit file register
k	Literal field, constant data or label
x	Don't care location (= 0 or 1) The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all Microchip software tools.
d	Destination select; d = 0 (store result in W) d = 1 (store result in file register f) Default is d = 1
label	Label name
TOS	Top of Stack
PC	Program Counter
WDT	Watchdog Timer Counter
TO	Time Out bit
PD	Power Down bit
dest	Destination either the W register or the specified register file location

Field	Description
→	Assigned to
< >	Register bit field
∈	In the set of
italics	User defined term (font is courier)

All instructions are executed within one single instruction cycle, unless a conditional test is true or the program counter is changed as a result of an instruction. In this case, the execution takes two instruction cycles. One instruction cycle consists of four oscillator periods. Thus, for an oscillator frequency of 4 MHz, the normal instruction execution time is 1 µs. If a conditional test is true or the program counter is changed as a result of an instruction, the instruction execution time is 2 µs.

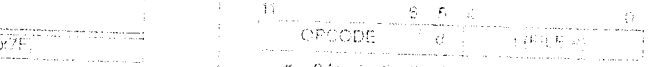
Figure 1-1 shows the three general formats that the instructions can have. All examples in the figure use the following format to represent a hexadecimal number:

0xhhh

where 'h' signifies a hexadecimal digit.

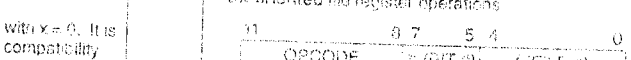
FIGURE 1-1: GENERAL FORMAT FOR INSTRUCTIONS

Byte-oriented file register operations



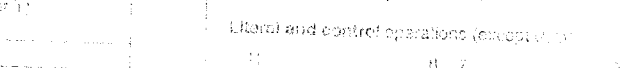
d = 0 for destination W
d = 1 for destination f
f = 5-bit file register address

Bit-oriented file register operations



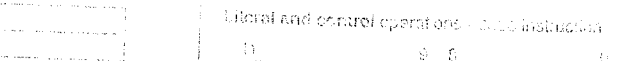
b = 3-bit bit address
f = 5-bit file register address

Literal and control operations (except GOTO)



k = 8-bit immediate value

Literal and control operations - GOTO instruction



Description	Cycles	12-Bit Opcode MSb		LSb	Status Affected	Notes
d f	1	0001	11df	ffff	C,DC,Z	1,2,4
ith f	1	0001	01df	ffff	Z	2,4
	1	0000	011f	ffff	Z	4
	1	0000	0100	0000	Z	
ent f	1	0010	01df	ffff	Z	
t f	1	0000	11df	ffff	Z	2,4
t f, Skip if 0	1(2)	0010	11df	ffff	None	2,4
f	1	0010	10df	ffff	Z	2,4
f, Skip if 0	1(2)	0011	11df	ffff	None	2,4
OR W with f	1	0001	00df	ffff	Z	2,4
	1	0010	00df	ffff	Z	2,4
f	1	0000	001f	ffff	None	1,4
tion	1	0000	0000	0000	None	
f through Carry	1	0011	01df	ffff	C	2,4
nt f through Carry	1	0011	00df	ffff	C	2,4
W from f	1	0000	10df	ffff	C,DC,Z	1,2,4
	1	0011	10df	ffff	None	2,4
OR W with f	1	0001	10df	ffff	Z	2,4
ER OPERATIONS						
	1	0100	bbbf	ffff	None	2,4
	1	0101	bbbf	ffff	None	2,4
Skip if Clear	1 (2)	0110	bbbf	ffff	None	
Skip if Set	1 (2)	0111	bbbf	ffff	None	
ERATIONS						
with W	1	1111	kkkk	kkkk	Z	
utine	2	1001	kkkk	kkkk	None	1
ndog Timer	1	0000	0000	0011	TO, PD	
nal operation	1	0000	0000	0000	None	
OR Literal with W	1	1101	kkkk	kkkk	Z	
ral to W	1	1100	kkkk	kkkk	None	
ION register	1	0000	0000	0010	None	
ace Literal to W	1	1110	kkkk	kkkk	None	
Standby mode	1	0000	0000	0011	TO, PD	
D register	1	0000	0001	ffff	None	3
OR Literal to W	1	1111	kkkk	kkkk	Z	

...on counter will be forced to a '0' by any instruction that writes to the PC except for GOTO...
...data sheets: Memory Section/Indirect Data Addressing, INDF and FSR Registers)
... modified as a function of itself (e.g. MOVF PORTB, 1), the value used will be that value ...
...mselves. For example, if the data latch is '1' for a pin configured as input and is driven ...
...ce, the data will be written back with a '0'.
..., where f = 5, 6, or 7 causes the contents of the W register to be written to the instate...
...C, respectively. A '1' forces the pin to a high-impedance state and disables the output buf...

...Zed in the TMR0 register (and when applicable, bits 5-3 in the prescaler) will be cleared

ADDWF Add W and f

Syntax: [*label*] ADDWF f,d

Operands: 0 ≤ f ≤ 31
d ∈ [0,1]

Operation: (W) + (f) → (dest)

Status Affected: C, DC, Z

Encoding: 0001 | 11df | ffff

Description: Add the contents of the W register and register f. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register f.

Words: 1

Cycles: 1

Example: ADDWF FSR, 0

Before Instruction
W = 0x17
FSR = 0xC2

After Instruction
W = 0xD9
FSR = 0xC2

ANDLW And literal with W

Syntax: [*label*] ANDLW k

Operands: 0 ≤ k ≤ 255

Operation: (W) .AND. (k) → (W)

Status Affected: Z

Encoding: 1111 | kkkk | kkkk

Description: The contents of W register are AND'ed with 8-bit literal 'k'. The result is placed in the W register.

Words: 1

Cycles: 1

Example: ANDLW 0x5F

Before Instruction
W = 0xA3

After Instruction
W = 0x03

ANDWF AND W with f

Syntax: [*label*] ANDWF f,d

Operands: 0 ≤ f ≤ 31
d ∈ [0,1]

Operation: (W) .AND. (f) → (dest)

Status Affected: Z

Encoding: 0001 | 01df | ffff

Description: The contents of the W register are AND'ed with register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example: ANDWF FSR, 1

Before Instruction
W = 0x17
FSR = 0xC2

After Instruction
W = 0x17
FSR = 0x02

BCF Bit Clear f

Syntax: [*label*] BCF f,b

Operands: 0 ≤ f ≤ 31
0 ≤ b ≤ 7

Operation: 0 → (f<b>)

Status Affected: None

Encoding: 0100 | bbbf | ffff

Description: Bit 'b' in register 'f' is cleared.

Words: 1

Cycles: 1

Example: BCF FLAG_REG, 7

Before Instruction
FLAG_REG = 0xC7

After Instruction
FLAG_REG = 0x47

Single Chip A/D Converters

GENERAL DESCRIPTION

The Intersil ICL7106 and 7107 are high performance, low power 3½-digit A/D converters containing all the necessary active devices on a single CMOS I.C. Included are seven-segment decoders, display drivers, a reference, and a clock. The 7106 is designed to interface with a liquid crystal display (LCD) and includes a backplane drive; the 7107 will directly drive an instrument-size light emitting diode (LED) display.

The 7106 and 7107 bring together an unprecedented combination of high accuracy, versatility, and true economy. It features auto-zero to less than 10μV, zero drift of less than 1μV/°C, input bias current of 10 pA max., and rollover error of less than one count. True differential inputs and reference are useful in all systems, but give the designer an uncommon advantage when measuring load cells, strain gauges and other bridge-type transducers. Finally, the true economy of single power supply operation (7106), enables a high performance panel meter to be built with the addition of only 10 passive components and a display.

FEATURES

- **Guaranteed Zero Reading for 0 Volts Input on All Scales**
- **True Polarity at Zero for Precise Null Detection**
- **1pA Typical Input Current**
- **True Differential Input and Reference**
- **Direct Display Drive — No External Components Required — LCD ICL7106**
  — LED ICL7107
- **Low Noise – Less Than 15μV p-p**
- **On-Chip Clock and Reference**
- **Low Power Dissipation – Typically Less Than 10mW**
- **No Additional Active Circuits Required**
- **New Small Outline Surface Mount Package Available**
- **Evaluation Kit Available**

ORDERING INFORMATION

Part Number	Temperature Range	Package
ICL7106CPL	0°C to +70°C	40 pin plastic DIP
ICL7106CJL	0°C to +70°C	40 pin CERDIP
ICL7106CM44	0°C to +70°C	44 pin Surface Mount
ICL7107CJL	0°C to +70°C	40 pin CERDIP
ICL7107CPL	0°C to +70°C	40 pin plastic DIP
ICL7106EV/Kit ICL7107EV/Kit	Evaluation kits contain IC, display, circuit board, passive components and hardware	

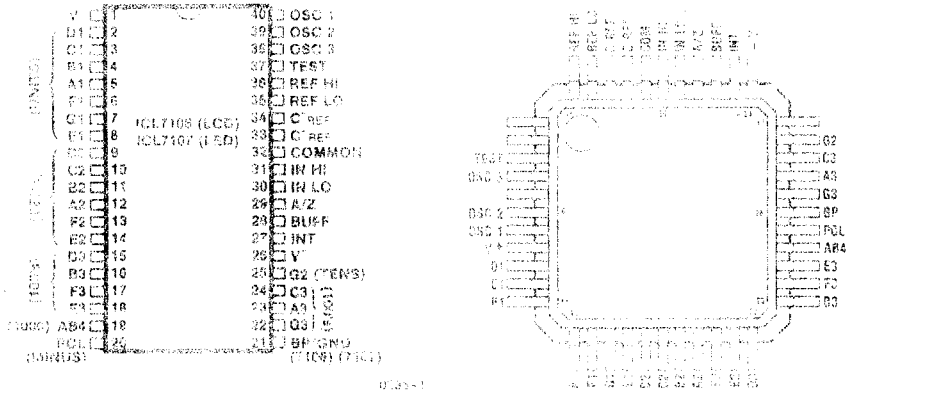


Figure 1. Pin Configurations

ATINGS

	15V
	+ 6V
	− 9V
e 1)	V + to V −
	V − to V

	TEST to V −
	GND to V +

Power Dissipation (Note 2)

Ceramic Package	1000mW
Plastic Package	800mW
Operating Temperature	0°C to + 70°C
Storage Temperature	− 65°C to + 150°C
Lead Temperature (Soldering, 10sec)	300°C

olute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional onditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute s may affect device reliability.

voltages provided the input current is limited to ± 100μA.

ounted with all leads soldered to printed circuit board.

ERISTICS (Note 3)

Test Conditions	Min	Typ	Max	Unit
V_{IN} = 0.0V Full Scale = 200.0mV	− 000.0	± 000.0	+ 000.0	Digital Reading
V_{IN} = V_{REF} V_{REF} = 100mV	999	999/1000	1000	Digital Reading
− V_{IN} = + V_{IN} = 200.0mV	− 1	± 2	+ 1	Counts
Full scale = 200.0mV or full scale = 2.000V (Note 6)	− 1	± 2	+ 1	Counts
V_{CM} = ± 1V, V_{IN} = 0V Full Scale = 200.0mV		50		μV/V
V_{IN} = 0V Full Scale = 200.0mV		15		μV
V_{IN} = 0 (Note 6)		1	10	pA
V_{IN} = 0 0°C ≤ T_A ≤ 70°C (Note 6)		0.2	1	μV/°C
V_{REF} = 100mV 0°C ≤ T_A ≤ 70°C (Ext. Ref. Applied To Pin 36) (Note 6)		1	5	ppm/°C
V_{IN} = 0		0.8	1.8	mA
		0.6	1.6	mA
9kΩ between Common & Positive Supply	2.4	2.8	3.2	V
25kΩ between Common & Positive Supply		50		ppm/°C

Characteristics	Test Conditions	Min	Typ	Max	Unit
7106 ONLY Pk-Pk Segment Drive Voltage Pk-Pk Backplane Drive Voltage (Note 5)	V + to V − = 9V	4	5	6	V
7107 ONLY Segment Sinking Current (Except Pin 19 & 20)	V + = 5.0V Segment voltage = 3V	5	8.0		mA
(Pin 19 only)		10	16		mA
(Pin 20 only)		4	7		

NOTES: 3. Unless otherwise noted, specifications apply to both the 7106 and 7107 at T_A = 25°C, f_{CLOCK} = 48kHz. 7106 is tested in the circuit of Figure 2. 7107 is tested in the circuit of Figure 3.

4. Refer to "Differential Input" discussion.

5. Back plane drive is in phase with segment drive for "off" segment. 180° out of phase for "on" segment. Frequency is 20 times conversion rate. Average DC component is less than 50mV.

6. Not tested, guaranteed by design.

TEST CIRCUITS

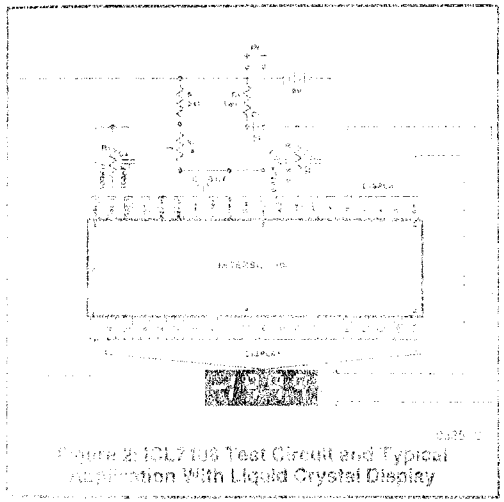


Figure 2. ICL7106 Test Circuit and Typical Application With Liquid Crystal Display

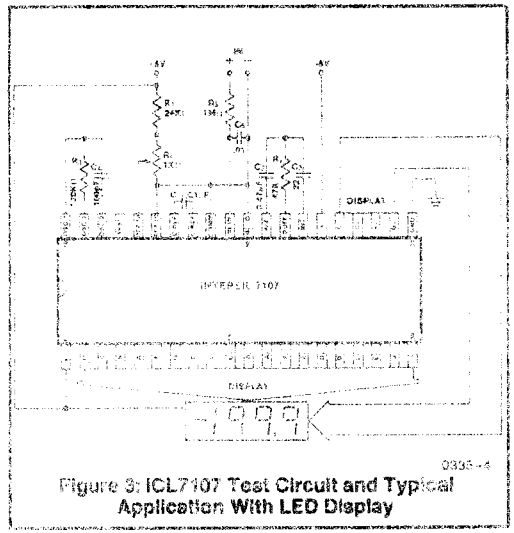


Figure 3. ICL7107 Test Circuit and Typical Application With LED Display

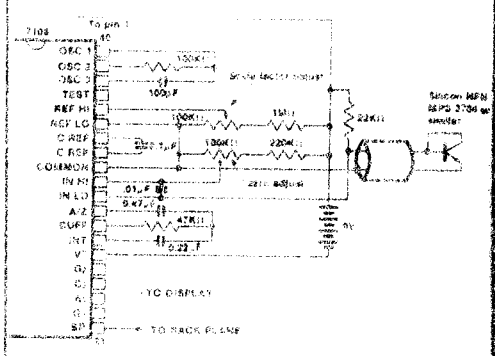


Figure 19: 7106 used as a digital centigrade thermometer. A silicon diode-connected transistor has a temperature coefficient of about −2mV/°C. Calibration is achieved by placing the sensing transistor in ice water and adjusting the zeroing potentiometer for a 000.0 reading. The sensor should then be placed in boiling water and the scale-factor potentiometer adjusted for 100.0 reading.

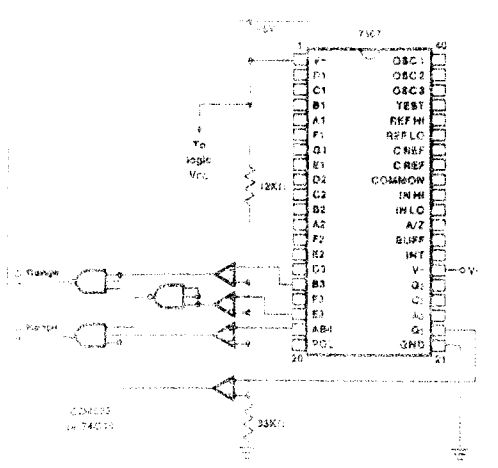


Figure 21: Circuit for developing Underrange and Overrange signals from 7107 outputs. The LM339 is required to ensure logic compatibility with heavy display loading.

7106/7107 EVALUATION KITS

After purchasing a sample of the 7106 or the 7107, the majority of users will want to build a simple voltmeter. This circuit can then be evaluated against the data sheet specifications and tried out in the intended application. However, before purchasing even the small number of additional

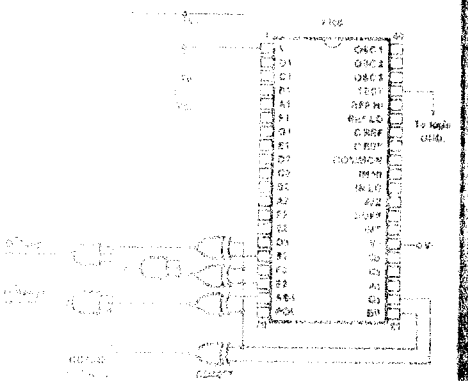


Figure 20: Circuit for developing Underrange and Overrange signals from 7106 outputs.

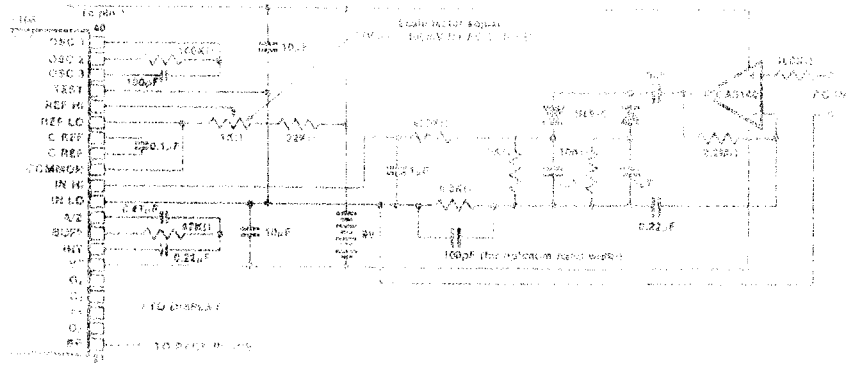


Figure 22: AC to DC Converter with 7106. TEST is used as a common-mode voltage level to ensure compatibility with most op-amps.

problem and facilitate evaluation of these unique circuits, Intersil is offering a kit which contains all the necessary components to build a 3½-digit panel meter. With the help of this kit, an engineer or technician can have the system "up and running" in about half an hour.

Two kits are offered, the ICL7106EV/KIT and the ICL7107EV/KIT. Both contain the appropriate IC, a circuit board, a display (LCD for 7106EV/KIT, LEDs for 7107EV/KIT), passive components, and miscellaneous hardware.

APPLICATION NOTES

A016 "Selecting A/D Converters", by David Fullagar

A017 "The Integrating A/D Converter", By Lee Evans.

A018 "Do's and Don'ts of Applying A/D Converters", by Peter Stubshaw and Skip Osgood.

A023 "Low Cost Digital Panel Meter Designs", by David Fullagar and Michael Dufort.

A032 "Understanding the Auto-Zero and Common Mode Performance of the ICL7106/7/9 Family", by Peter Bradshaw.

A040 "Building a Battery-Operated Auto Ranging DVM with the ICL7106", by Larry Goll.

A052 "Tips for Using Single-Chip 3½-Digit A/D Converters", by Dan Sheridan.