Control Module for Digital Cross- Connect Switch

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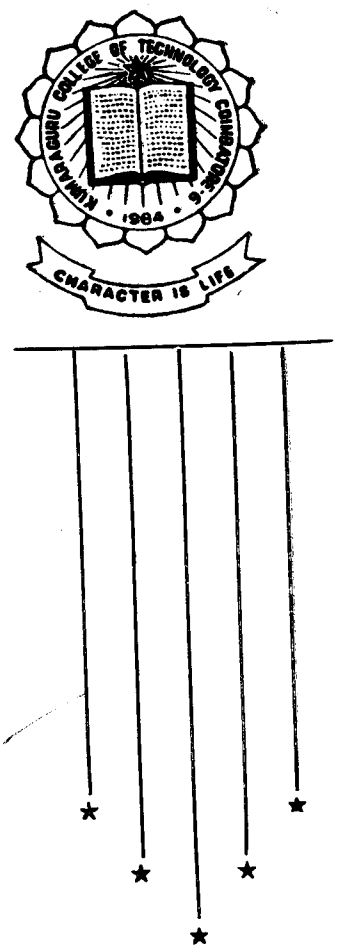
Project Report 1998-99



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IN PARTIAL FULFILMENT OF THE REQUIREMENTS FOR THE AWARD OF THE DEGREE OF **BACHELOR OF ENGINEERING IN ELECTRONICS & COMMUNICATION ENGINEERING** OF THE BHARATHIAR UNIVERSITY COIMBATORE

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Certificate

This is to certify that the project entitled

CONTROL MODULE FOR DIGITAL CROSS-CONNECT SWITCH

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in partial fulfilment of the requirements for the award of Degree of Bachelor of Engineering in the Electronics and Communication Engineering Branch of the Bharathiyar University, Coimbatore-641006 during the academic year

1998 – 99

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(Head of Department)

Certified that the candidate was examined by us in the Project Work, Viva – Voce Examination held on 15-03-99 *and the University Register Number is* _____.

(Internal Examiner) 15/3

15/3/99

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title of the Project was "**Control Module for Digital Cross-Connect Switch**". ing this period, their attendance and conduct were found to be very good.

wish them the very best for a bright future.

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SYNOPSIS

The advent of the criteria to reduce the cost of the existing telecommunication switching networks which use back-to-back multiplexer for add/drop of channels and the inflexibility due to fixed physical wiring for mapping has lead to the evolution of DIGITAL CROSS-CONNECT SWITCHING SYSTEM (DCS) .

Digital Cross Connection involves software controlled mapping by interchanging the timeslots belonging to the input and output streams. The channel mapping may be single or multiple and this can be temporary or permanent. All these are programmable and is controlled by the user. Adding and dropping of channels in a long distance transmission network is possible by selecting the free time slots at the output and the input stream respectively.

A network of Digital Cross-Connect switch can be installed and the entire network can be controlled by a single Network Management System(NMS) terminal, thus supporting the centralized switching network concept.

This project involves the study of Digital Cross-Connect Switch, design of its control module and the development of assembly level programs for intialization of various intergrated circuits in the control card

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INTRODUCTION

Telecommunication is the most rapidly developing field in correspondance with the necessities and amenities required by the mankind. A most important requisite of any telecommunication system, whether used for voice, data or other forms of electrical communication is its interconnection capability.

The system must be able to connect quickly and accurately between any station or terminal with any other in the communication network. As a first phase in reducing the cost of the analog switching equipment and the inflexibility in switching, we step in for digital switching which favours dynamically varying traffic, flexibility in switching and pre-determined or desired channel switching of the user.

Chapter I explains about the PCM and voice communication through multiplexing techniques. The European standards for telecommunication and Plesiochronous Digital Hierarchy (PDH) is explained in this chapter. It gives a brief explanation about the present communication system for add/drop of channels and its drawbacks.

Chapter II gives an introduction for the Digital Cross-Connect Switch. The concept of Digital Cross-Connect system is explained. The general DCS architecture model and its operating principle is discussed in

this chapter. Finally the over-view of 16-port Digital Cross-Connect Switch along with its salient features is given.

Chapter III gives a brief description about the Digital Cross-Connect Switch equipment. The cards used in Digital Cross-Connect Switch are described here and it gives a general idea about the arrangement of these cards in the product. The function of each card and various devices used in these cards are explained.

Chapter IV highlights on the control module. It gives the architecture of the 80186 processor, which is the main unit in the control circuitry. It explains about various ICs used in the control card. It gives an explanation about the working and the various signals in the circuit.

Chapter V explains about the software. The source code for intialization of various integrated circuits used in the control card and voice mapping, along with the algorithm and flowchart is given. It also briefly explains about the assembler used.

Thus an overview of what each chapter is going to deal with has been briefly introduced.

CHAPTER I

PRESENT TECHNOLOGY

In this chapter the basics of telecommunication such as PCM techniques and voice communication by multiplexing techniques are discussed. This chapter explains about the present technology of using conventional multiplexers used for add/drop of channels and its drawbacks.

1.1 Voice Communication By Multiplexing Techniques

1.1.1 Time Division Multiplexing

Communication may involve transmission of voice signals or data. In voice communication, the signals are coded in binary form and each channel is given an exclusive access to the tranmission line during periodic slices of time known as TIME SLOTS. This technique is called TIME DIVISION MULTIPLEXING.

1.1.2 Pulse Code Modulation

Pulse code modulation (PCM) is a technique for converting analog speech signal into digital format. The speech signal is first filtered to remove all frequencies outside the range of 300-3400Hz. Speech signal is then sampled at a rate of 8000 times per second. Each sample is then converted into an 8-bit digital code word using a process called ENCODING.

The process of pulse code modulation is described in fig1.1. The net result of the pulse code modulation process is that each conversation requires 64 Kbps.

1.2 Multiplexer (MUX)

A multiplexer takes the data from a number of different devices, combines it and sends it over one common line. This eliminates the need for many separate circuits and allows significant reduction in overall cost. The basic multiplexer is illustrated in fig 1.2.

1.3 European Telecommunication Standards

In India we are following the European telecommunication standards. The TDM frame format using European transmission and switching system is illustrated in fig 1.3.

Each frame consists of 32 time slots out of which 30 is used for PCM streams. TS0 denotes the sync. details and TS16 denotes the signalling details.

1.4 Plesiochronous Digital Hierarchy (PDH)

Transmission multiplex hierarchy has been developed for digital transmission using PCM. At present the standard used in public telecom network (PTN) is plesiochronous digital hierarchy.

European Plesiochronous Digital Hierarchy (PDH) till E5 level is shown in the Table T.1.1. and fig 1.4.

1.5 Tranmission Network Using Conventional Multiplexers

At present, to drop/insert channels, back-to-back multiplexers are used. A typical long distance tranmission network involving switching/transmisson equipment is illustrated in fig 1.5 . The long distance digital radio network connecting number of places and the typical channel multiplexing/demultiplexing equipment hierarchy for E2 level is shown in the figure. In order to drop/insert service channels, say between station 1 and station M to carry Subscriber Trunk Dialling (STD) calls, two numbers each of second order and primary multiplexers are required to accomplish the task. This situation becomes still worse if the transmission network carries 34 or 140 Mbps data.

1.6 Drawbacks Of Using Conventional Multiplexers

When we use back-to-back multiplexers in order to add/drop some specific channels in between two stations, the drawbacks are:

(i) When there are more number of subscribers, then the order of multiplexer used is more, then corresponding order of back to back multiplexers must be used in the add/drop circuit which will increase the cost.

(ii) To satisfy service requierments along facility routes, blocks of channels must be dropped, blocked and then added

Herewith, we have seen about the multiplexing techniques and transmission network using conventional multiplexer. Bacause of the demerits of using conventional multiplexer in tranmission network we go in for Digital Cross-Connect Switch.

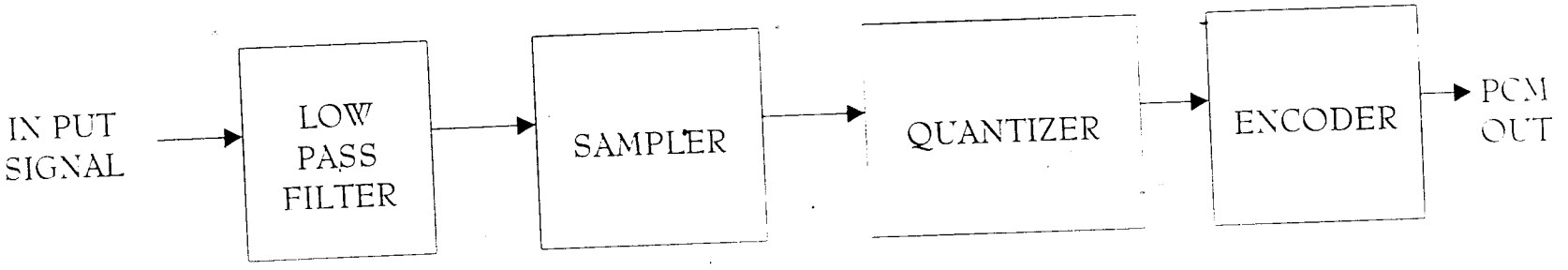


FIG. 1.1 PULSE CODE MODULATION

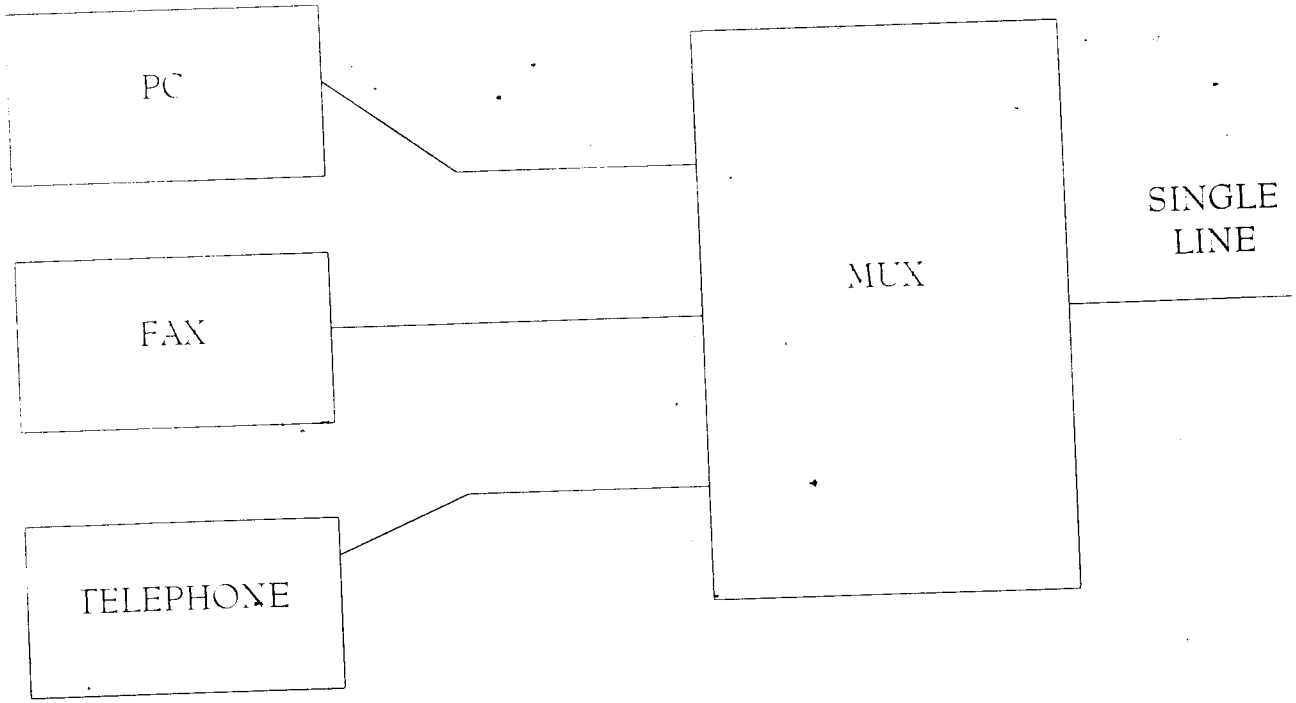


FIG. 1.2 BASIC MULTIPLEXER

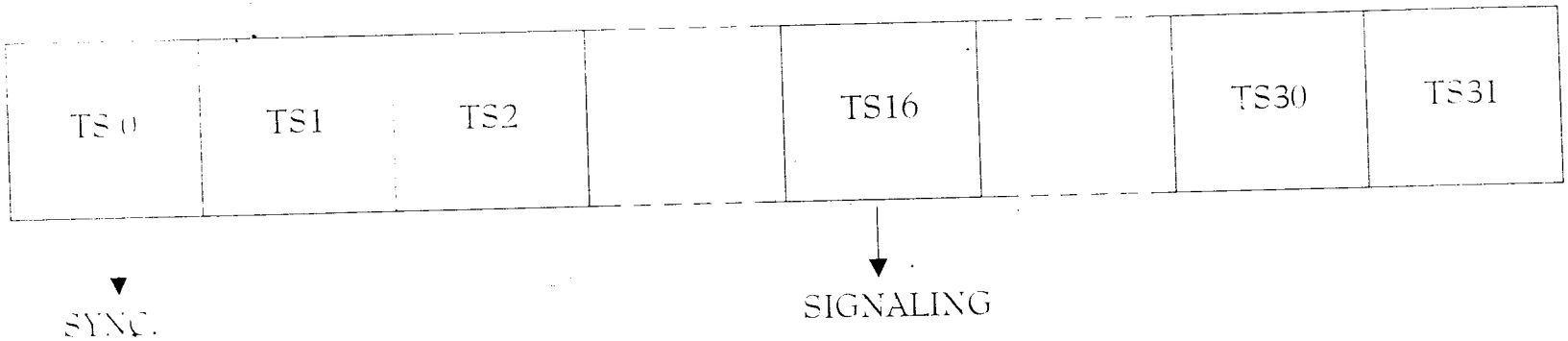


Fig. 1.3 TDM Frame Format

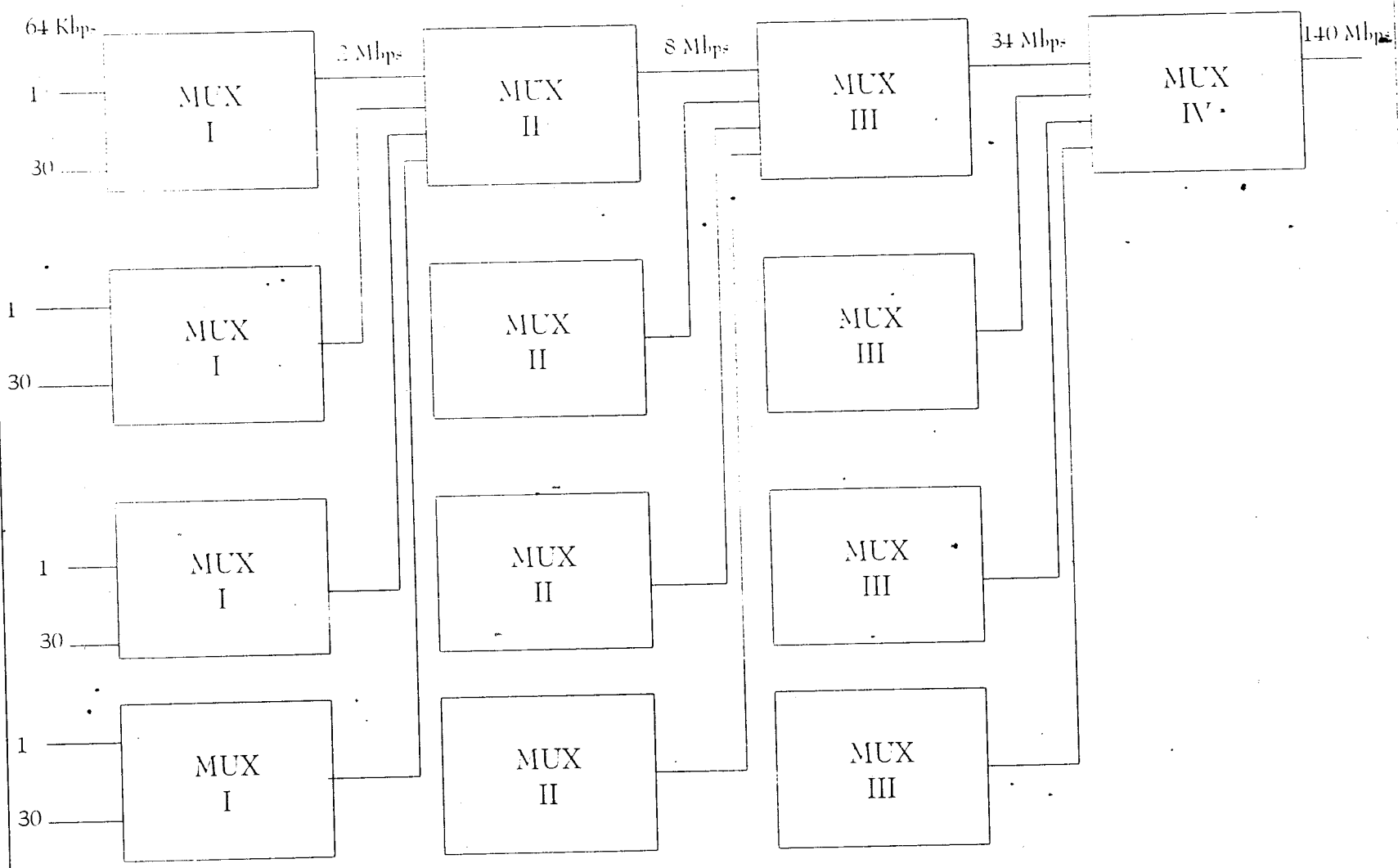
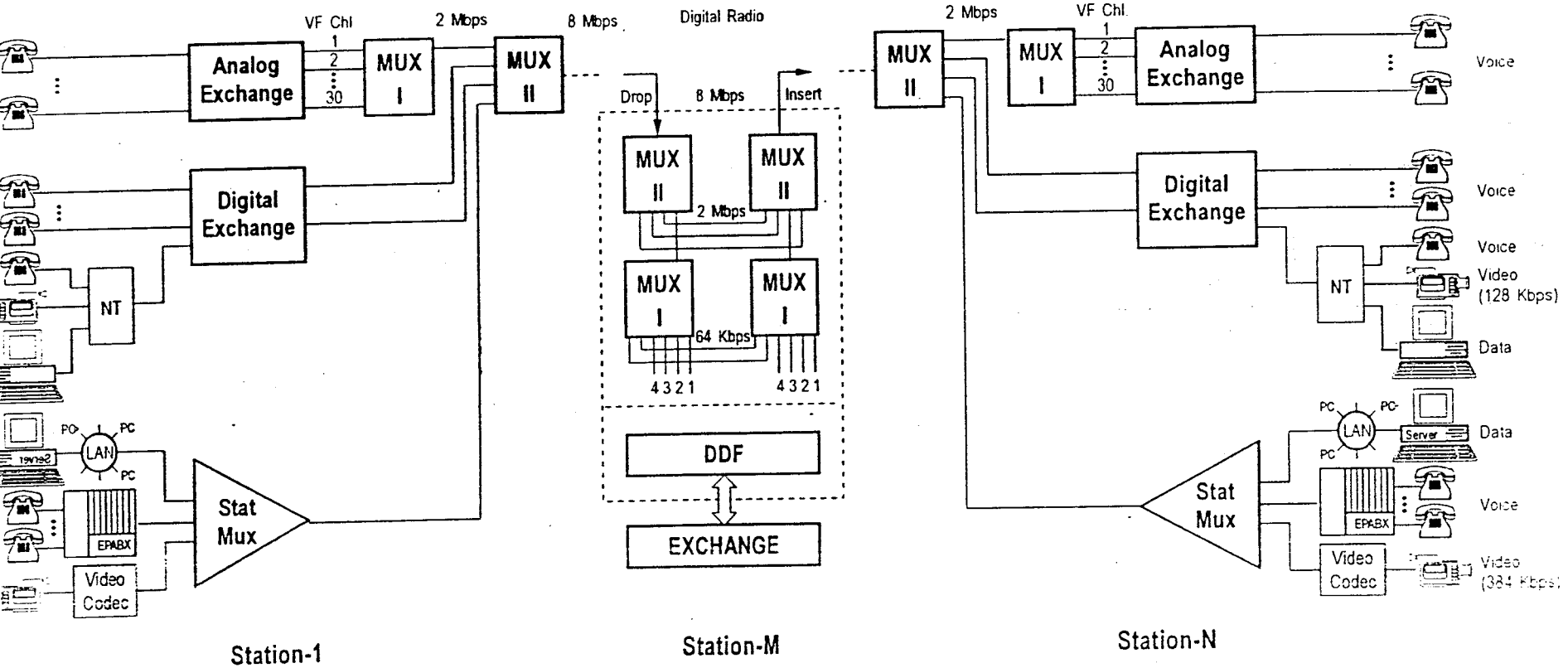


FIG. 1.4 EUROPEAN PDH

Fig.4.5 Typical Long Distance Transmission Network
(with Conventional Mux)



MULTIPLEXES	PDH STANDARDS (European)
0. Order MUX	64 Kbps
I. Order MUX	2.045 Mbps
II. Order MUX	8.448 Mbps
III. Order MUX	34.368 Mbps
IV. Order MUX	139.264 Mbps
V. Order MUX	565.148 Mbps

Tabel T.1.1 European PDH Hierarchy

CHAPTER-II

DIGITAL CROSS-CONNECT SWITCH

The Digital Cross-Connect Switch(DCS) is a versatile multiplex equipment used in long distance transmission network to drop/insert traffic channels with instant flexibility obviating the need for hierarchial multiplexing equipments.

Digital Cross-connect Switch provides 64Kbps cross- connection of voice/data channels between any incoming and outgoing digital PCM streams.

This chapter deals with the explanation about the digital cross-connect system and its architecture.It also gives an overview of 16-port DCS and its salient features.

2.1 Digital Cross-Connect Systems

All electronic(software controlled) cross-connect equipment is designated as Digital Cross-Connect System.Some of the capabilities of a DCS are the integration of the basic E1 or E2 signals within or between higher level signals, network-hubbing and text access.These units use time-slot interchanges to transfer channels among terminations. They thus allow interconnection of, for example, channel-3 of stream-7 to channel-18 of

stream-16. They eliminate channel banks at points where channels are transferred between carrier systems.

With a DCS system, the control of individual channels on E1 systems passing through the DCS may be given to the customer. In this case, switching commands enter the DCS-controller from the customer's site, allowing substantial ongoing reconfiguration of the customer's network.Security features limit the customer re-arrangement capability to only his own circuit.

2.2 Communication System Using Digital Cross-Connect Switch

Due to the drawbacks of using conventional MUX in long distance transmission network as explained in chapter-I we go in for Digital Cross-Connect Switch for smaller exchange.

When we use conventional MUX for higher channel capabilities, the number of back-to-back multiplexers used will be more. When the transmission network carries 34 or 140Mbps data, the situation becomes worse. But in the case of Digital Cross-Connect Switch, drop/insert of traffic channels is completely performed by software.

The deployment of DCS is also cost effective compared to traditional MUX/DEMUX for the captive network users and service

The long distance digital radio network connecting numbers of places and the typical channel multiplexing/demultiplexing equipment hierarchy for E2 level is explained in Fig.2.1.Here four 64Kbps service channels are utilised for add/dropp of channels.

2.3 DCS Architecture Model

A generic DCS system is shown in Fig.2.2.It is divided into three major modules.They are:

(i) Input/Output Interface Module(I/O)

(ii) Administration Module(AM)

(iii) Cross-Connect Module(CCM)

The explanation of the individual modules are given below.

2.3.1 Input/Output Interface Module(I/O)

The I/O module includes interface ports which terminates signals and passes them to the Cross-Connect Module and a microprocessor based controller monitors the I/O connections.

2.3.2 Administration Module (AM)

The AM module controls the entire Cross-Connect System and interfaces with the external operation systems or local operators. It includes main memory and non-volatile memory (eg,hard disk), a CPU-based

system controller within the AM stores all application programs(in ROM) including the restoration program, and controls and co-ordinates I/O and CCM modules. The main memory within the AM stores all configuration maps and other key information.

2.3.3 Cross-Connect Module (CCM)

The CCM module includes a Switching Matrix Controller(SMC) and a Cross-Connect Switching Matrix(CCSM). Switching Matrix Controller stores working map and controls re-configuration during the restoration mode based on new map AM i.e, it monitors the accuracy of the cross-connections.

2.4 Operating Principle

The basic operations for the DCS system includes two modes.One is normal mode and the other is the restoration mode.

2.4.1 Normal Mode

In this mode, the channel enters the input module (i.e,I/O),then it is forwarded to the CCSM of the CCM module for transport through, based on the residing cross-connections map.

2.4.2 Restoration Mode

This mode is implemented during power failure. When a restoration process is in progress, the restoration messages are terminated at the I/O

module and then forwarded to the system controller of the AM module for message processing. The purpose of the restoration message processing is to execute the restoration algorithm and eventually to obtain a new DCS configuration either from the pre-planned database stored in the hard disk or the main memory of the AM module, or by dynamically computing the new configuration for each received message.

Once the system controller has the new configuration map, it transfers the new map to the SMC which then updates the current configuration map.

The primary SMC verifies and tests whether the new ports specified in the new configuration map are correct and working. Once the verification and the testing are complete, the SMC initiates the change of the CCSM matrix configuration. Now the physical path arrangement within the CCSM happens.

2.5 Over View Of 16 – Port DCS

A 16-port Digital Cross-connect Switch provides cross connections at 64Kbps for all channels of 16-2Mbps (exactly 2.048Mbps) PCM streams.

As a highly efficient networking tool the Digital Cross-connect Switch simplifies consolidation and grooming of 2Mbps data. The major

areas of application are Public Telecom Networks(PTN) and also Private Networks like Railways,Defence etc.

2.6 Salient Features Of 16-Port DCS

1. Capacity to inter-connect 16 numbers of 2.048Mbps PCM streams.
2. System is fully modular,expandable in steps of two I/O ports upto sixteen I/O ports at 2.048Mbps.
3. 512 x 512 non-blocking cross-connections of 64Kbps channels.
4. Overwrite possible for signal and voice mappings.
5. Bit-wise manipulation(Set,Reset,Invert)of signalling bit mapping is possible.
6. Can work on Internal, External or Extracted Clock in any order of priority.
7. Voice channels can be put in conference mode.
8. Mappings can be made temporary or permanent. Permanent mappings are retained in case of power failure.
9. Under system/power failure conditions default mappings between all 2Mbps streams are provided.
10. Errors are indicated using alarms.
11. Network of Digital Cross-connect terminals can be established

12. User interface is through VT-100 terminal or remotely through another DCS.

13. Power supply for DCS is - 48V DC(Nominal).

Herewith, we have seen what is a Digital Cross - Connect System, its operating principle and a 16-port Digital Cross-Connect Switch.

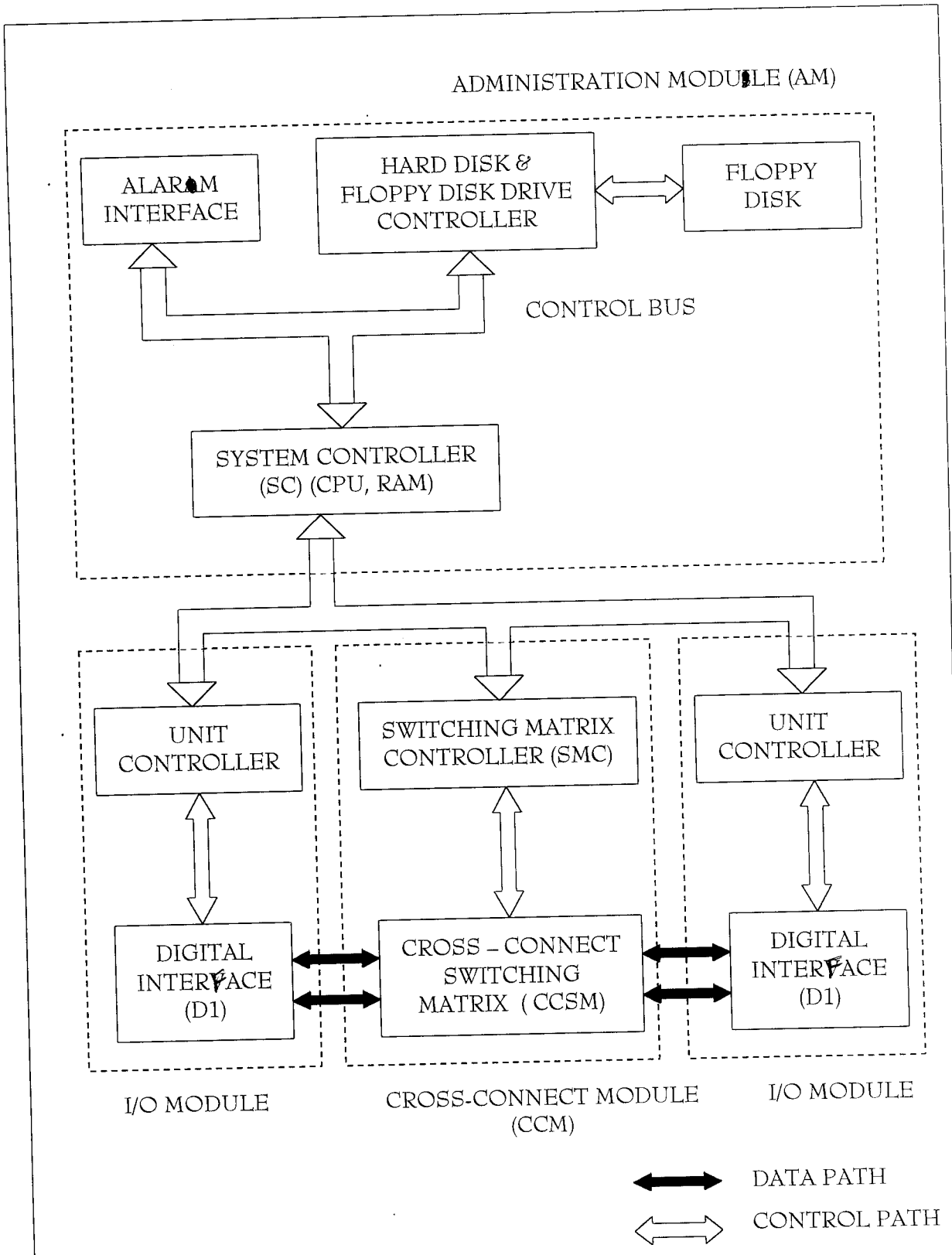
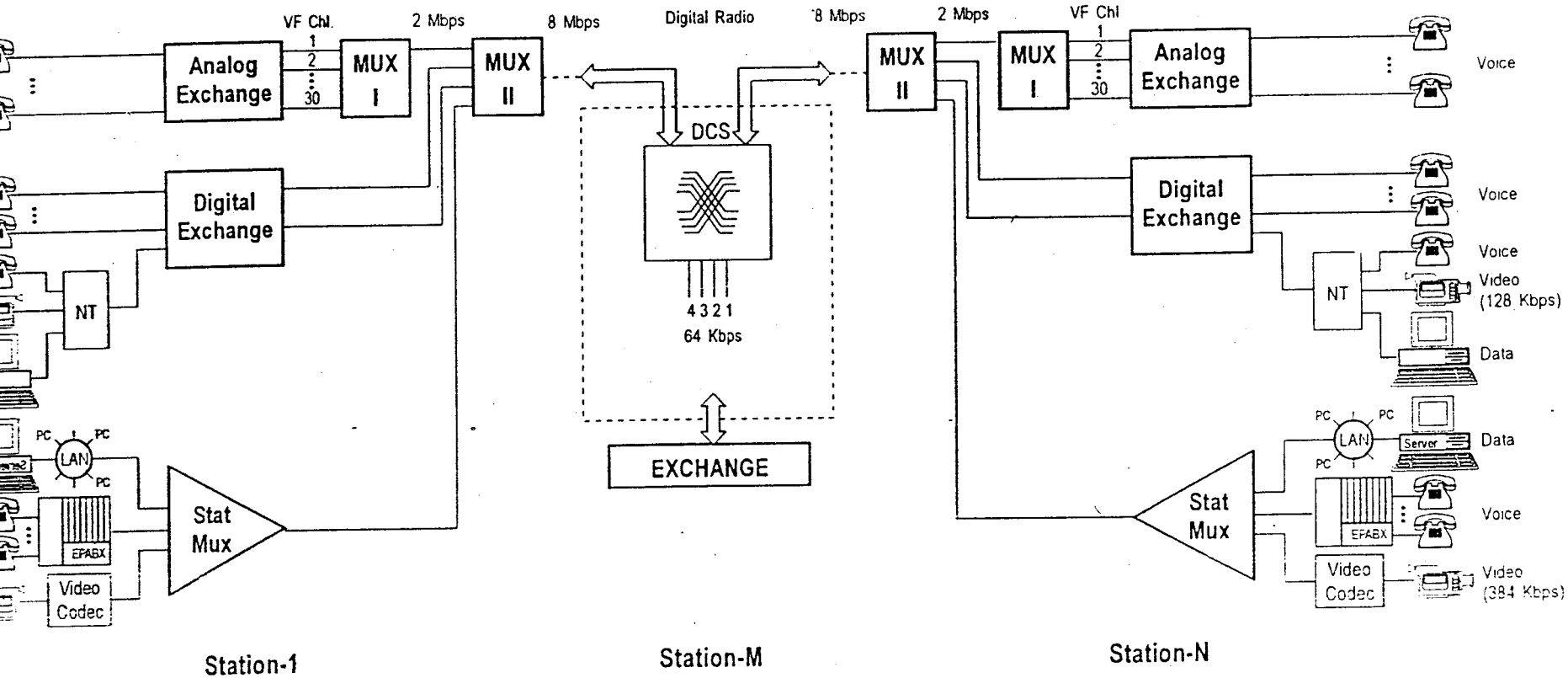


Fig. 2.2. DCS ARCHITECTURE MODEL

Fig. 2.1 Typical Long Distance Transmission Network
(with Digital Cross-connect Switch)



CHAPTER-III

DCS EQUIPMENT DESCRIPTION

This chapter deals with the various cards used in Digital Cross-Connect Switch and the way in which they are arranged. The explanation about various cards is given along with function of various integrated circuits used in the cards.

3.1 Cards In DCS

The following types of cards are equipped in DCC sub-rack.

1.Power Supply Card.

2.Control Card.

3.Timing and Switching Card.

4.Interface Card.

5.Back Panel.

Fig.3.1 shows how all the above cards are equipped in a 16-port DCS.

3.1.1 Power Supply Card

The Power Supply Card accepts -48V DC input and provides +/- 5.6V DC output. The circuit mainly comprises of switching transistors, transformers, input and output filters and pulse width modulators.

The unregulated DC input is switched around 30KHz and the ON time of the switch is varied to maintain the output voltage within the specified limits. The energy is stored in the chokes during the conduction time of the transistors and supplied to the load during half periods by the switching transistors. The voltages are rectified and power is smoothened by the capacitors. Further filtering is done by a set of inductors and capacitors.

The output voltage +5V is sampled and fed to a 741 op-amp and is compared with a reference level. The amplified error is fed to the input of the opto-coupler (IC SL-5500).This modulates the width of the pulse.The width modulated pulse is buffered through transistors and fed to the switching transistors through pulse transformers.

In case of overvoltage on either the +5.6V or -5.6V, the voltage regulator(IC LM-339) conducts and triggers the opto-coupler IC,thus shutting down the output voltages by turning off the driving pulses.The output voltages +5.6V and -5.6V is set by a set of potentiometers and resistors.The correct voltages present is indicated by an LED.

The failure of the power supply due to overvoltage trip, under voltage trip or input fuse fail is indicated by glowing of the LED.

The entire system load can be borne by either a single power supply card or shared by two cards.When both power supply cards are used,failure of

a single card will not affect the working of the equipment.The second power supply card can be jacked in or out even when the equipment is ON without affecting the working of the system.

3.1.2 Control Card

The control card regulates the working of the entire system and also includes the user interface circuitry. The versatile and widely used 80186 processor and its associated peripherals constitute the core of the control circuitry.The control circuitry can address 1MB of memory and 64K I/O ports. The program stored in EPROMS also includes the information necessary to initialize FPGA's used on the Timing- Switching and Interface cards.EEPROMS are used to provide the required non-volatility for mapping information. However, if the mapping information is specified to be temporary, the EEPROMS are not updated. A High Speed Data Link Controller(HDLC) is used to facilitate remote mapping/monitoring of other Digital Cross Connects connected in master-slave format.No separate data link is required for HDLC, instead two spare bits in any PCM stream may be used for this purpose.

Two RS232C ports are provided. One port is connected to a VT-100 terminal for user interaction. The second serial port is connected to a Network Management System(NMS) terminal. Two USARTs are used to

interface the microprocessor with the serial ports. RS232C Transreceiver chip converts TTL level signals to RS232C levels and vice-versa.

The system can process both hardware and software interrupts. Hardware interrupts are used to facilitate user interaction, either locally or remotely through another cross-connect. Software interrupts are used to provide an onboard real time clock and to provide certain built in safe guards for the microprocessor working.

On system hang, under voltage conditions etc., micromonitor chip provides a general system reset. System can also be reset by pressing the switch marked RST on the front plate of the card or through software upon user request. Card fail indication is denoted by an LED.

In addition to active control card, there will be cold standby backup for the active control card. All user entered mappings also get updated on the standby control card. If the active card fails, the system must be switched off and the standby card inserted in the active card position. System may then be powered on again.

3.1.3 Timing And Switching Card

The Timing and Switching Card generates all the timing signals required for the operation of the system and execute various types of mappings depending upon the information inputs from the control card.

The description of the TS card is grouped under the following headings.

3.1.3.1 Clock Selection

The 2.048MHz system clock can be chosen from an internal clock, an external clock or any of the extracted clocks of the four 2Mbit streams.The internal clock is derived from the onboard 16.384MHz oscillator. An op-amp converts the sinusoidal external clock input to TTL levels. The extracted clock from a particular stream is derived from the corresponding interface card. A hierarchy of priorities can be allotted to the various clock sources and switch over from/ to a higher/lower priority clock can be accomplished.

3.1.3.2 Generation Of 8.192MHz Signal

The Phase Locked Loop(PLL) chip is used to generate a 8.192MHz clock signal from the system clock.

3.1.3.3 Generation Of Timing Signals

Various timing markers are generated with respect to the chosen system clock. These includes Frames,Time slot and other timing signals required for the operation of the system. All these timing signals are generated from an FPGA IC.

3.1.3.4 Channel Mapping

A single channel mapping involves routing of the voice and signalling information from an input time slot to the output time slot. Entirely different methods are used to execute voice and signalling mapping. Voice mapping is done by a powerful custom built VLSI chip, whereas signalling mapping is accomplished using a set of dual port RAMs.

3.1.3.5 Conference Mapping

Conferencing of three(or more) voice channels is made possible by the use of PCM conference ICs. Each conference IC can put 32 channels in conference. The number of channels that can be put in a single conference path varies from 3 to 32. Thus 20 separate three way conference paths can be established. The possible number of conference paths gets reduced if more than three channels are used per path. Each bit of the common output signalling information of 'N' channels in conference will be the logical bit wise AND of the corresponding input signalling bit of all 'N' channels.

3.1.3.6 Mapping Overwrite

Overwrite are provided for voice and signalling mappings. Mapped voice information can be overwritten by a selected byte.For signalling mapping bit wise manipulation of data is possible.

3.1.3.7 Card Fail Indication

Failure of card is indicated by an LED and an appropriate error message is displayed on the monitor.

3.1.4 Interface Card

Each Interface Card caters for two 2.048MHz streams,both for transmit and receive. Consecutive numbers will be allocated to the two streams on the IF card, one of the streams(stream A) being even numbered and other(stream B) odd numbered. The stream numbers will be:

Even stream number=(IF Card No.)x2

Odd stream number=Even stream No.+1

On the receive side,both streams are plesiochronous and contain unmapped information. On the transmit side, streams are synchronous and contain mapped information.

On user request it is possible to provide a bypass between the two streams connected on the IF card.Under this condition all mappings pertaining to these two streams become invalid.

3.1.4.1 Receive Side Working

The PCM line interface chip converts the input bipolar signal to two unipolar signals RPOS and RNEG. This chip also extracts the clock

from the input signal. The primary PCM transreceiver chip decodes the input at RPOS,RNEG to give the received NRZ output RNRZO.

FPGA extracts the receive signal and spare bit information from both streams and also converts them from serial to parallel form.

The PCM transreceiver chip catagorises all receive alarms.

3.1.4.2 Transmit Side Working

FPGA does the parallel to serial conversion of signaling/spare bit data and multiplexes the mapped voice,signalling and spare bit information to give the separate transmit input of each stream. PCM transreceiver chip accepts the input and injects the frame and multiframe synchronization words. The resultant signal is encoded ,and converted to two unipolar outputs TPOS and TNEG. The PCM line interface chip converts the two unipolar signals to bipolar form. A transformer steps up the output signal to the required levels.

Herewith, we have seen about various cards used in digital cross-connect switch. The function of each card and the integrated circuits used is also discussed.

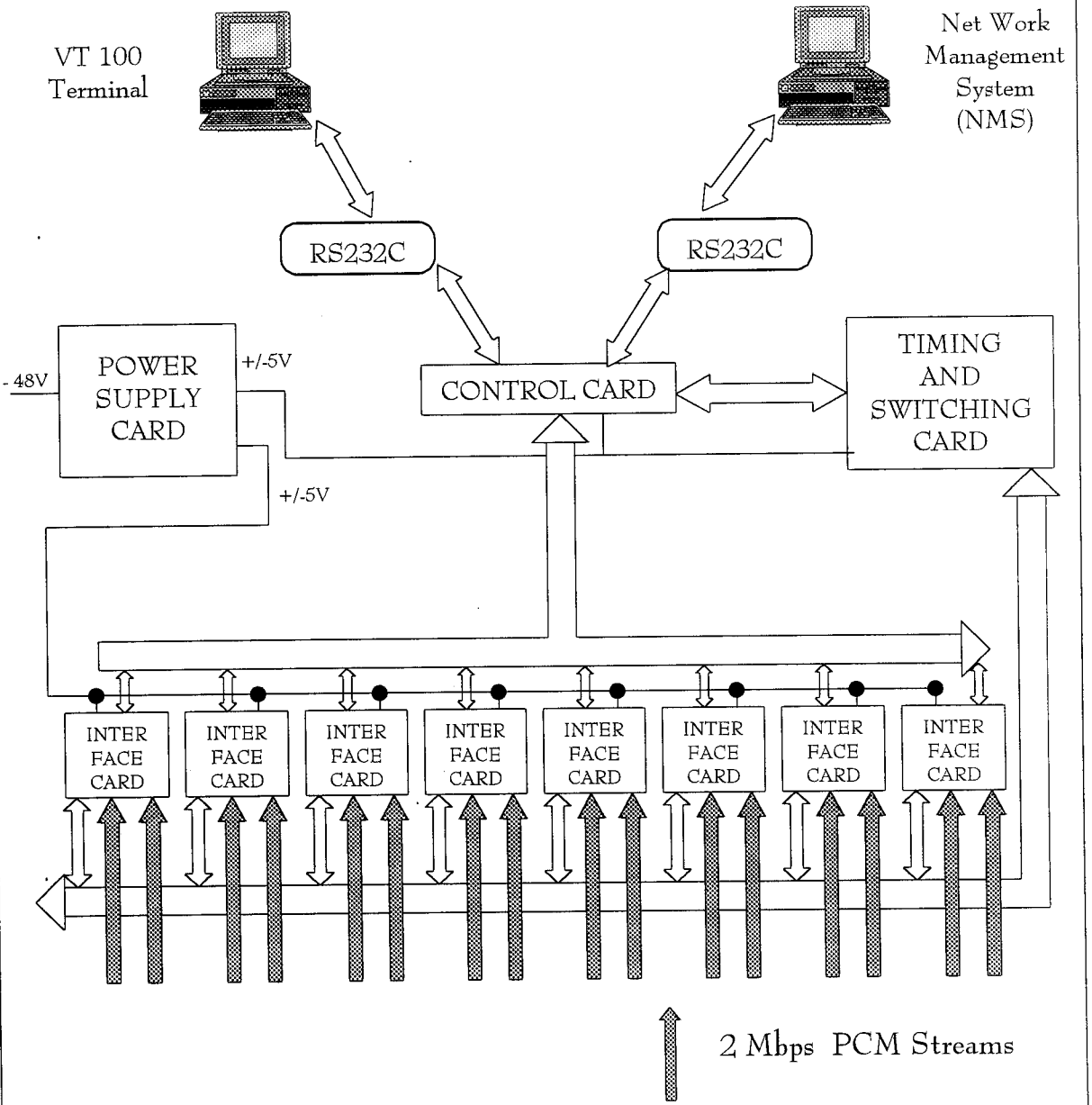


Fig. 3.1 16 Port DCS Block Diagram

CHAPTER IV

CONTROL MODULE FOR DCS

This chapter deals with the various integrated circuits used in the control card including the 80186 microprocessor. The entire hardware of the control card is described in the following sections.

4.1 Hardware Description

The hardware part of control module mainly constitutes the 80C186XL microprocessor and a High Level Data Link (HDLC) controller. Control card also includes various High Speed CMOS TTL compatiable (HCT)ICs along with various logic gates.

4.1.1 Architecture of 80186 Microprocessor

The 16-bit processor used in the control card circuit is 80C186XL. The architecture of 80C186XL microprocessor is shown in fig 4.1. The 80C186XL is a 16-bit microprocessor developed using VLSI technology. It combines 15 to 20 of the most common microprocessor system components onto one chip. The 80C186XL is object code compatible with the 8086/8088 microprocessors and adds ten new instruction types to the 8086/8088 instruction set.

4.1.1.1. 80C186XL Clock Generator

The 80C186XL provides an on-chip clock generator for both internal and external clock generation. The clock generation features a crystal oscillator, a divide-by-two counter, synchronous and asynchronous ready inputs and reset circuitry.

The crystal or clock frequency chosen must be twice the required processor operating frequency due to the internal divide by two counter. This counter is used to drive all internal phase clocks and the external CLKOUT signal. CLKOUT is a 50% duty cycle processor clock and can be used to drive other system components. All ac timings are referenced to CLKOUT.

4.1.1.2 Bus Interface Unit

The 80C186XL provides a local bus controller to generate the local bus control signals. In addition, it employs a HOLD/HLDA protocol for relinquishing the local bus to other bus masters. It also provides outputs that can be used to enable external buffers and to direct the flow of data on and off the local bus.

The bus controller is responsible for generating 20 bits of address, read and write strobes, bus cycle status information and data (for write operations) information. It is also responsible for reading data from the

local bus during a read operation. Synchronous and asynchronous ready input pins are provided to extend a bus cycle beyond the minimum four states (clocks).

The 80C186XL bus controller also generates two control signals ($\overline{DEN}$ and DT /$\overline{R}$) when interfacing to external transreceiver chips. This capability allows the addition of transceivers for simple buffering of the multiplexed address/data bus.

4.1.1.3 80C186XL Peripheral Architecture

All the 80C186XL integrated peripherals are controlled by 16-bit registers contained within an internal 256-byte control block. The contorl block may be mapped into either memory or I/O space. Internal logic will recognize control block addresses and respond to bus cycles.

The 80C186XL contains logic which provides programmable chip-select generation for both memories and peripherals. In addition, it can be programmed to provide READY (or WAIT state) generation. It can also provide latched address bits A1 and A2. The chip-select lines are active for all memory and I/O cycles in their programmed areas, whether they be generated by the CPU or by the integrated DMA unit.

The 80C186XL provides six memory chip select outputs for three address areas. They are upper memory, lower memory and midrange

memory. One each is provided for upper memory and lower memory, while four are provided for midrange memory.

The 80C186XL provides a chip select, called $\overline{\text{UCS}}$, for the upper memory. The upper memory is usually used as the system memory because after reset the 80C186XL begins executing at memory location FFFOH.

The 80C186XL provides a chip select for lower memory called $\overline{\text{LCS}}$. The bottom of memory contains the interrupt vector table, starting at location 00000H.

The 80C186XL provides four $\overline{\text{MCS}}$ lines which are active within a user locatable memory block. This block can be located within the 80C186XL 1Mbyte memory address space exclusive of the areas defined by $\overline{\text{UCS}}$ and $\overline{\text{LCS}}$. Both the base address and size of this memory block are programmable.

The 80C186XL can generate chip selects for up to seven peripheral devices. These chip selects are active for seven contiguous blocks of 128 bytes above a progammable base address. The base address may be located in either memory or I/O space.

The 80C186XL can generate a READY signal internally for each of the memory or peripheral $\overline{\text{CS}}$ lines. The number of WAIT states to be

states for all accesses to the area for which the chip select is active. In addition, the 80C186XL may be programmed to either ignore external READY for each chip-select range individually or to factor external READY with the integrated ready generator.

4.1.1.4 DMA Unit

The 80C186XL DMA controller provides two independent high-speed DMA channels. Data transfers can occur between memory and I/O spaces (e.g., Memory to I/O) or within the same space (e.g., Memory to Memory or I/O to I/O) . Data can be transferred either in bytes (8 bits) or in words (16 bits) to or from even or odd addresses. Each DMA channel maintains both a 20-bit source and destination pointer which can be optionally incremented or decremented after each data transfer (by one or two depending on byte or word transfers). Each data transfer consumes two bus cycles (a minimum of 8 clocks) one cycle to fetch data and the other to store data.

4.1.1.5 Timer/ Counter Unit

The 80C186XL provides three internal 16-bit programmable timers. Two of these are highly flexible and are connected to four external pins (two per timer). They can be used to count external events, time external events, generate nonrepetitive waveforms, etc. The third timer is

not connected to any external pins, and is useful for real-time coding and time delay applications. In addition, the third timer can be used as a prescaler to the other two, or as a DMA request source.

4.1.1.6 Interrupt Control Unit

The 80C186XL can receive interrupts from a number of sources, both internal and external. The 80C186XL has five external and two internal interrupt sources (Timer /Counters and DMA). The internal interrupt controller serves to merge these requests on priority basis, for individual service by the CPU.

4.1.1.7 DRAM Refresh Control Unit

The Refresh Control Unit (RCU) automatically generates DRAM refresh bus cycles. The RCU operates only in Enhanced Mode. After a programmable period of time, the RCU generates a memory read request to the BIU. If the address generated during a refresh bus cycle is within the range of a properly programmed chip select, that chip select will be activated when the BIU executes the refresh bus cycle.

4.1.1.8 Power Save Control

The 80C186XL when in Enchanced Mode, can enter a power saving state by internally dividing the processor clock frequency by a

programmable factor. This divided frequency is also available at the CLKOUT pin.

All internal logic, including the refresh control unit and the timers, have their clocks slowed down by the division factor. To maintain a real time count or a fixed DRAM refresh rate, these periphrals must by re-programmed when entering and leaving the power-save mode.

4.1.2 HDLC IC

A high speed data link controller (HDLC) SAB-82525 is used to facilitate remote mapping/monitoring of other Digital Cross–Connect Switch connected in master–slave format

4.1.3 Micromonitor Chip

In order to safeguard the microprocessor from voltage fluctuations the micromonitor chip is used (DS1232)

4.1.4 Dual Rs-232C Transmiter/Receiver

In order to convert TTL level to RS-232C leverl and vice-versa, a +5V powered dual RS-232C Transmitter/Receiver (DS 1228) is used.

4.1.5 HCT ICs

Various High Speed CMOS TTL compatiable ICs are used in the control card.

4.1.5.1 Buffer

A fully buffered signal will introduce a time delay to the system. This causes no difficulty unless memory or I/O devices are used which function at near the maximum speed of bus. The buffer's output currents have been increased so that more TTL unit loads may be driven. A quad buffer/line driver (74HCT 125) and six buffer/line driver (74 HCT244) are used.

4.1.5.2 Latch

The latch is a type of bistable device. Two D-type positive edge-triggered 3-state flip flops (74 HCT 173) are used.

4.1.6 Logic ICs

Various logic ICs like NAND, AND and NOT gates are used. The inverter performs a basic function called inversion to change one logic level to the opposite level. A HEX-INVERTER (74 HCT 04) is used. The AND gate performs logical multiplication. A quad 2-Input AND gate (74 HCT 08) is used. The OR gate performs logical addition. Quad 2-input OR Gate (74 HCT 32) is used. The NAND gate implies an AND function with a complemented output. A dual, four input NAND gate (74 HCT 20) is used.

4.1.7 Other HCT ICs

Various other HCT ICs used in control card are DECODER and OCTAL BUS TRANSRECEIVER. A 3- to – 8 DECODER (74 HCT 138) is used. It selects one of the eight output lines depending on the input. Three OCTAL BUS TRANSRECEIVER (74 HCT 245) are used.

4.1.8 Memory Chips

Two EEPROMS, two EPROMS and two RAMS constitute the memory of the control card circuitry . EEPROM used is 64K (8K x 8) CMOS AT28C64. EPROM used is 512K (64K x 8) CMOS AT27C512, RAM used is 424K(32K x 8), 6264.

4.1.9 USART IC

A device which can be programmed to do either asynchronous or synchronous communication, is often called a Universal Synchronous – Asynchronous Receiver Transmitter (USART). A 8251A is used to interface the microprocessor with the serial port.

4.2. Circuit Description

The circuit implements an 80186 16-bit processor. 8.192 MHz crystal is connected to the processor to generate an internal clock frequency of 4.96 MHz.

The lower order address bits(8 bits) is demultiplexed from the multiplexed address/data bus using 74HCT373, which is a three state octal latch. The latch is enabled by Address Latch Enable(ALE) signal from the processor, similarly the higher order bus is demultiplexed using 74HCT373.

The data bus is demultiplexed from the multiplexed address/data bus using two 74HCT245 which is a octal bus transreceiver. The lower order data bus is separated by enabling 74HCT245 using data enable($\overline{DEN}$) and A0. The higher order data bus is chosen by enabling 74HCT245 using data enable ($\overline{DEN}$) and Bus High Enable($\overline{BHE}$).

The data output of the processor (or) data input of the processor from external peripherals is decided by the DIR pin present in 74HCT245. The DIR pin is enabled by the DT/$\overline{R}$ (Data Transmit/Receive) from the processor. The Bus High Enable($\overline{BHE}$), Data Enable($\overline{DEN}$) and the Data Transmit/Receive (DT/$\overline{R}$) signals are provided through the latch 74HCT244.

All the data and address lines are available to the other cards and peripherals through Euro plugs.

Micro monitor chip(DS1232) is provided in the Control Card for monitoring voltage level and resetting the processor whenever necessary.For protecting the processor from voltage fluctuations , tolerance level choosen is 4.75V by grounding TOL pin. When the voltage level drops below 4.75V the RST signal is activated and during power up the RST signal is generated for atleast 250ms.The processor can also be reset by the use of push button reset which is activated by an external switch provided to the user.

The Micro monitor chip also resets the processor when it is idle for 1.2s by using the Strobe signal. The time delay is chosen by connecting the TD pin to 5V.

The processor receives interrupt from VT terminal through INT1. The High Speed Data Link Controller(HDLC) gives its interrupt to the processor through INT 2 . The Network Management System(NMS) interrupts through INT 3 of the processor.

The Read, Write, Programmable Chip Select($\overline{PCS5}$) and the RST signal from the microprocessor is made available to other cards through the latch 74HCT244. Card failure indication is provided by LED DS 1.

The system consists of two EPROMS each of 8 bit length and with memory capacity of 64K. There are used in parallel by the processor for an wordlength.

The two EPROMS 27C512 are selected by the address bit A17 which is high and Upper Chip Select($\overline{UCS}$) which is active low. For choosing the memory (27C512) for lower order data bits , address bit A0 must be low and it is logically ORed with A17 OR $\overline{UCS}$.

Similarly , the chip 27C512 is selected for higher order data bits by the signals Bus High Enable($\overline{BHE}$) which must be low and it is logically ORed with A17 OR $\overline{UCS}$. Address bits used for accessing these EPROMS are A1-A16.

The system also consists of two RAMS 6264, each of 8 bit length and capacity 32K.

The even bank memory is selected by Lower Chip Select ($\overline{LCS}$) and A0, where both should be low.

The odd memory bank is chosen by Lower Chip Select($\overline{\text{LCS}}$) and Bus High Enable($\overline{\text{BHE}}$), where both are active low signals. 28C64 is the EEPROM used for storing permanent mapping details.

The lower order memory bank is enabled by Memory Chip Select($\overline{\text{MCS0}}$) and A0, when both are low.

The higher order bank is selected using Memory Chip Select($\overline{\text{MCS0}}$) and Bus High Enable($\overline{\text{BHE}}$) , where again their levels are low.

The capacity of these EEPROMS are 8K individually with address lines accessing them are from A1 to A13. Their data lengths are 8 bits. The memory contents are read using the signal $\overline{\text{RD}}$ and written into the chip by enabling $\overline{\text{WR}}$.

For signal mapping dual port RAMS are used, which are present in the Timing and Switching Card. The dual port RAMS(DPRAMS) are enabled by using a decoder (74HCT138). The address bits used are A8 to A10.

The DPRAM chip is enabled by Memory Chip Select 2 ($\overline{\text{MCS2}}$). A High Speed Data Link Controller (HDLC) (82525) is used to facilitate Remote Mapping / Monitoring of other Digital Cross-connects

connected in master – slave format. No separate data link is required for HDLC. Instead two spare bits in any PCM stream may be used for this purpose.

The HDLC chip (82525) is enabled by memory chip select($\overline{MCS1}$). The address and data lines used are A1 to A7 and D0 to D7. The interrupt pin of HDLC is connected to INT 2 of the microprocessor. The HDLC chip is reset using RST input from the processor. There two channels (A and B) through which data are received (or) transmitted serially by RxDA,RxDB and TxDB.

Two USARTs (8251A) are used as an interface between the microprocessor and serial ports (RS-232C) which are connected to VT100 terminal and NMS terminal. A dual RS-232C Receiver/Transmitter that converts TTL levels to RS-232C levels for serial port connections. DS1228 is the USART interfacing with NMS terminal. This is enabled using programmable chip select 6 ($\overline{PCS}$ 6). The data from the NMS terminal is connected to R2IN of the dual RS-232C Receiver/Transmitter (DS1228),which is converted to TTL level and is outputted through pin R2 OUT and in turm to Receive Data (RxD) of USART 8251A. Now, the Receive Ready (RxRDY) signal goes high due to

the receiver buffer being full. The RxRDY is given as interrupt(NMS) to the microprocessor.

The microprocessor acknowledging the interrupt, gives out the read Signal($\overline{RD}$). Data is read in parallel form from the data pins D0 to D7 The data to be transmitted from the processor, is converted from TTL level to RS-232C level by connecting Transmit Data (TxD) pin to T2 in of the dual Transmitter/Receiver(DS1228).

Before this operation, the processor sends the WRITE($\overline{WR}$) signal to the USART. The data in RS-232C levels is sent from T2 out to the serial port.

The Receive Clock (RxC) and the Transmit Clock (TxC) is tied together and driven by the same clock frequency whether it is control or data ($C/\overline{D}$)is decided by A1.

Similarly, the USART 8251A used for VT100 terminal is enabled by Programmable Chip Select ($\overline{PCS1}$).

In this case the conversion of TTL to RS-232C levels and vice-versa are carried out by the pins T1 in,T1 out and R1 in, R2 out respectively.

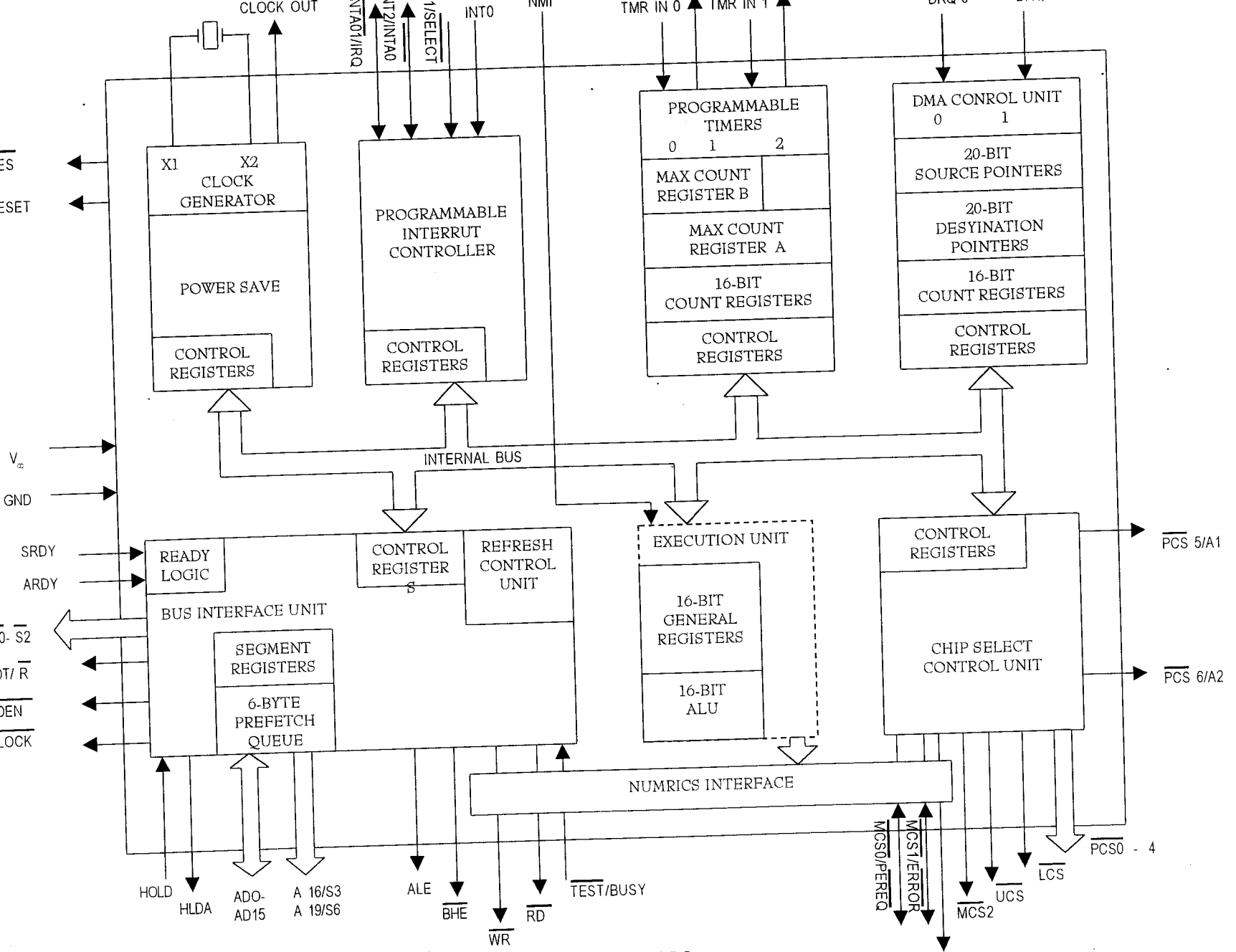
The RESET pin of USART is connected to the RST pin of the

4.3 Working Of The Control Card

The mapping details i.e., the input stream number and timeslot number which is to be mapped to a particular output stream number and timeslot number is given as the input to the VT100 terminal. Now an interrupt is given to the microprocessor by the VT100 terminal. The processor in turn enables USART through which data is received in the parallel form. If the mapping is to be permanent, the mapping details are stored in EEPROM. This also provides non-volatility for mapping information.If the mapping is to be temporary the data is stored in RAM. These are done by selecting the corresponding memory chips according to their utilities.

These mapping details are sent to control RAM (CRAM) of VLSI chip DSE001 which is going to take care of switching. The incoming PCM streams are stored in speech RAM(SRAM) which is modified by the details given in CRAM. The above mentioned process is for voice mapping.

Herewith, a detailed explanation about the operation of the control card circuitry and various ICs used in this module is given. Next chapter focusses on the software development and tools for assembly level programming.



BLOCK DIAGRAM 80C186

CHAPTER – V

SOFTWARE

Various integrated circuits and devices in control card is controlled by the 80186 microprocessor. Other cards are also intialized and controlled by the 80186 microprocessor. So, programming of 80186 microprocessor is of great importance. In this chapter, the source code necessary for intialization of various integrated circuits used in control card is explained along with intialisation of various other cards. Source code for voice mapping is also given. Assembler details are also given in this chapter.

5.1 OBJECTIVE

The main objectives of programming the 80186 microprocessor are:

1. Intialization of various integrated circuits in control card.
2. Intialization of other cards.
3. Voice, signal and spare-bit mapping(single or multiple).
4. Mapping over write.
5. Indication of fault in the system

In our project we have developed the software for the intialization of various integrated circuits in control card, intialization of other cards and program for voice mapping.

5.2 Assembly Language Program Development Tools

For all but the very simplest assembly language programs you will probably want to use some type of micro computer development system and program development tools to make your work easier. These systems usually contain several hundred Kbytes of RAM, a keyboard and video display, floppy and/or hard disk drives, a printer and an emulator.

5.2.1 Editor

An editor is a program which when run on a system, lets you type in the assembly language statements for your program. Examples of editors are ALTER which runs on Intel systems, EDLIN which runs on IBM PCs, and WORDSTAR which runs on most systems. The main function of an editor is to help you construct your assembly language program in just the right format so that the assembler will translate it correctly to machine language. This form of your program is called the source program.

5.2.2 Assembler

An assembler program is used to translate assembly language mnemonics to the correct binary code for each instruction. The assembler will read the source file of your program from the disk where you saved it after editing. An assembler usually reads your source file more than once. On the first pass through the source program the assembler finds

offset of labels and puts this information in a symbol table. On a second pass through the source program, the assembler produces the binary code for each instruction and assigns addresses to each .

The assembler generates two files on the floppy or hard disk. The first file is called the object file. The object file contains the binary codes for the instructions and information about the addresses of the instruction. This file contains the information that will eventually be loaded into memory and executed. The second file generated by the assembler is called the assembler list file. This file contains the assembly language statements, the binary codes for each instruction, and the offset for each instruction. You usually send this file to a printer so that you will have a printout of the entire program to work with when you are testing and troubleshooting the program. The assembler listing will also indicate any typing or syntax errors.

5.2.3 Linker

A linker is a program used to join together several object files into one large object file. When writing large programs it is usually much more efficient to divide the large program into smaller modules. Each module can be individually written, tested and debugged. When all of the modules work they can be linked together to form a large functioning program.

The linker produces a link file which contains the binary codes for all the combined modules. The linker also produces a link map file which contains the address information about the linked file. The linker however does not assign absolute addresses to the program, it only assigns relative addresses starting form zero. This form of program is said to be relocatable because it can be put anywhere in memory to be run.

5.2.4 Locator

A locator is a program used to assign the specific address of where the object code is to be loaded into memory.

5.3. Voice Mapping

Voice mapping involves routing of the voice information from an input time slot to the output time slot.

5.3.1. DSE 001 CHIP ORGANISATION

The digital switch element illustrated in fig5.1 has six major functional blocks viz.

1. IBUF
2. OBUF
3. SRAM
4. CRAM
5. Micro Intf.
6. Control Logic

5.3.1.1 IBUF

The IBUF has 16 serial PCM input lines. The data on these 16 PCM inputs is received at a fixed rate of 2.048 Mbits/sec. The IBUF unit performs the serial to parallel conversion of the 16 PCM inputs data stream. The resultant sixteen ,8-bit data words are sequentially stored in the speech RAM(SRAM). The 8-bit corresponds to the time slot information. All PCM inputs must be phase synchronous,i.e., the bit 0 of time slot 0 of all PCM inputs must occur at the same time. When FPIN is active the IBUF unit marks all the PCM inputs as bit 0 of time slot 0.

5.3.1.2 OBUF

The OBUF has sixteen serial PCM output lines. The data on these sixteen PCM lines is transmited at a fixed rate of 2.048 Mbits/sec. The OBUF receives sixteen sequential 8 bit words from the SRAM. This parallel data is converted into serial data stream. The FPOUT signal marks the beginning of the sixteen PCM outputs,i.e., the bit 0 of time slot 0 on all PCM output lines.

5.3.1.3 SRAM

This is a 512 x 8 random access memory which stores the speech samples of the 512 input time slots for one frame. The SRAM map is illustrated in fig 5.2. The samples of the input time slots are stored in

of the 16 PCM input links, while the next 16 locations store time slot 1 of the 16 PCM links and so on. For example, the data of time slot 31 of PCM link 15 is stored in location 511 of the SRAM.

5.3.1.4 CRAM

This is 512 x 10 RAM whose contents determines the input time slot to output time slot mapping (switching). The address of the individual CRAM location specifies the output time slot, while the content of the location specifies the input time slot. The CRAM map is illustrated in fig 5.3 . Of the ten bits of the CRAM, nine bits are used for addressing SRAM for effecting the switching and the tenth bit indicates the IDLE/$\overline{\text{BUSY}}$ state of the corresponding output time slot. When idle, the (Lower) CRAM contents are placed in the corresponding output time slot.

5.3.1.5 MICRO INTF

This block interfaces to microprocessor through the 8-bit bus and the control. Through this interface the microprocessor can write and read any location of CRAM and SRAM. Through this interface one can set-up or remove a switching path by correspondingly changing the CRAM contents. The write and read facility on SRAM is provided for test purposes though it could be used for other applications also.

5.3.1.6 CONTROL LOGIC

The control logic generates the timing signals required to control the logic of the system. The input to this unit is FPIN signal and SYSCLK clock. It generates the various control signals which are output for use in other parts of a switching system (both inside and outside the device).

5.3.2 Microprocessor Interface and Programming DSE 001 Chip

Fig 5.4 shows the microprocessor interface architecture. The interface has been designed to work with popular 8-bit and 16-bit microprocessors. The data bus is 8 bits wide and the control unit uses 3 address lines and 1 $\overline{R}/W$ line. The chip select to the control unit enables the command execution, while the command to be executed is selected by the three address and one $\overline{R}/W$ line. The Address and Data latches shown are for buffering the system data bus. The various command sequences that can be used for programming the device are illustrated in Tabel T.5.1.

5.3.3 Voice Mapping Techniques

Time switch must be capable of transferring the contents of any particular inlet time-slot into any specified outlet time-slot and be able to perform this function for every other inlet/outlet time-slot pair in any arbitary pairing. The incoming bit stream is stored time-slot by time-slot as

is stored indicating what sample is to be sent in which outgoing time-slot. The outgoing samples are therfore drawn from the speech store in the order defined by the control memory.

Time slot can be inter-changed by two techniques,

i. Sequentially writing into the Speech RAM(SRAM) and then randomly reading as directed by the Control RAM(CRAM)

ii. Randomly writing into the Speech RAM and then sequentially reading as directed by the Control RAM.

5.4 ALGORITHM

5.4.1 Initialisation of USART

a) Make sure USART is reset properly by sending 0's to control register address.

b) 8251A requires a worst case recovery time of 16 clock cycles for write recovery time so a delay is given.

c) Issue the reset command.

d) Select the mode word for : Baud rate factor : 2400 Kbps, even parity
Charter length = 8 , One stop bit.

e) Enable the transmission, receving .

5.4.2 Initialisation of PCB

a) Select upper chip select Block of 256KB.

b) Select zero wait state and no ready input required .

c) Output to U.C.S. control register.

d) Select L.C.S block of 16KB.

e) Select M.C.S block of 64Kb.

f) Select P.C.S. from 4000H.

g) Intialize all control registers.

5.4.3 Initialisation of Timer

a) Select Timer 0 control register, intilalize clocking and disable INT.

b) Select Timer 0, Maximum count register B and Intialize Baud rate = 2400

c) Select Timer 0, Maximum count register A and Intialize Baud rate = 2400

d) Select Timer 1 control register and enable external clocking and INT.

e) Select Timer 1, Maximum count register B and Generate a 10Hz wave form.

f) Select Timer 2, control register and disable it .

g) Select Timer 1, Maximum count register A and Generate a 10Hz wave form.

5.4.4 Initialization of Interupt and DMA

a) Mask VT 100, HDLS and NMS INT

b) Set the priorty level of Timer Control register as 2.

c) DMA 0, DMA1, KB INT are masked.

d) Set INT1 control register for VT 100 Terminal, Priority level = 0, Unmasked, Not Cascaded, No SFNM

e) Select INT 2 control register for HDLC INT, Level Triggered, Priority level = 2

f) Select INT 3 control register for NMS INT, Unmask it, Priority level = 7

5.4.5 Initialisation of TS Card :

a) Read TS card buffer.

b) CHECK whether TS card is loaded.

c) If not loaded ON Bay alarm.

d) If loaded Intialize it.

5.4.6 Initialisation of IF Card

a) Intialize current IF Card as zero

b) Find present Card Number.

c) Determine the offset address of the present card number

d) Read the main buffer content from that address

e) From this content check whether the card is loaded or not

f) If loaded, output that, the card is loaded and then go for another card until less than 8 cards.

g) If not loaded, output that, the card is not loaded.

5.4.7 Voice Mapping

a) Enter input time slot and stream number.

b) Check for a valid input.

c) From input time slot and stream number corresponding address of CRAM in DSE 001 chip is found.

d) Enter output time slot and stream number.

e) Check for a valid input.

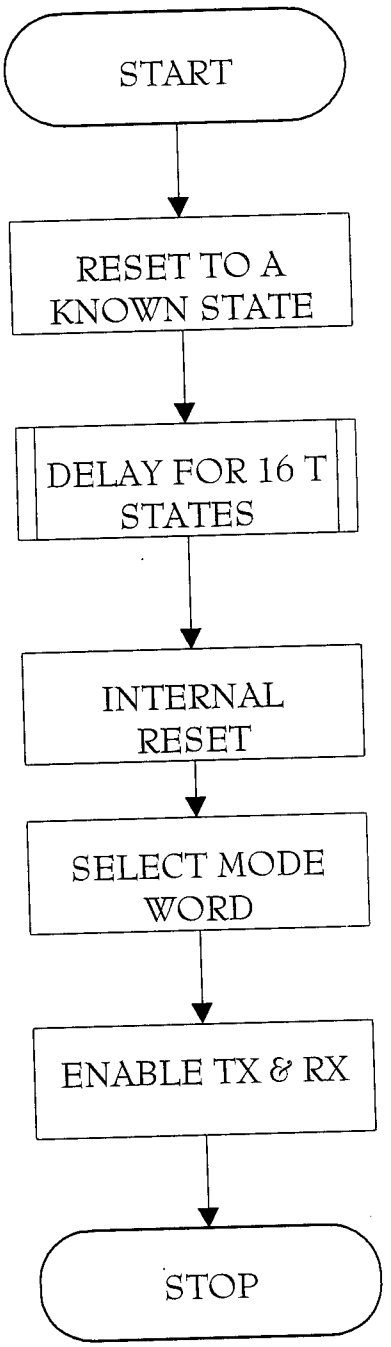
f) Find the corresponding address of CRAM .

g) Swap the contents of the two address.

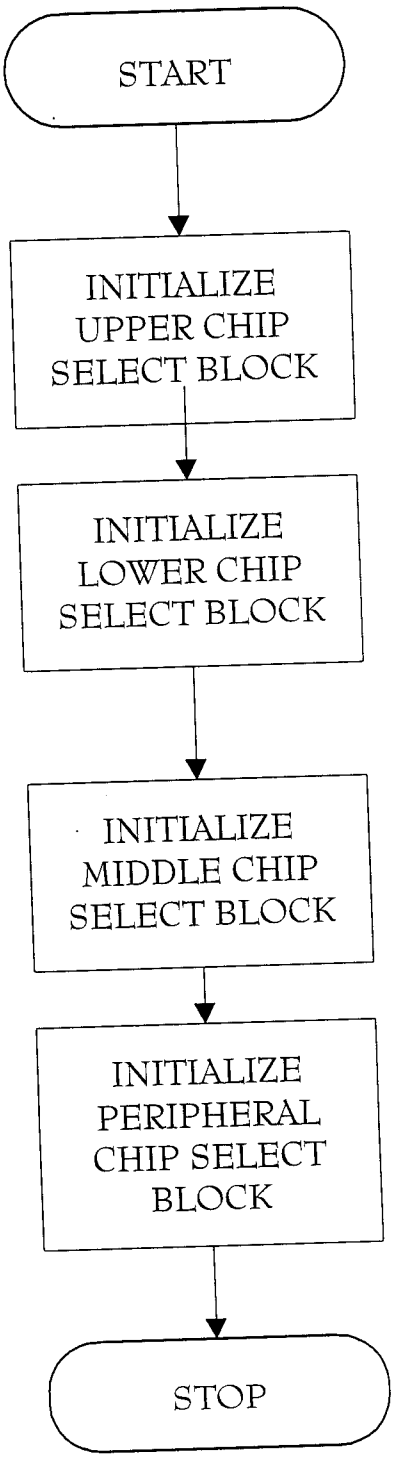
h) Write the swapped contents in the corresponding address.

5.5 Flow Chart

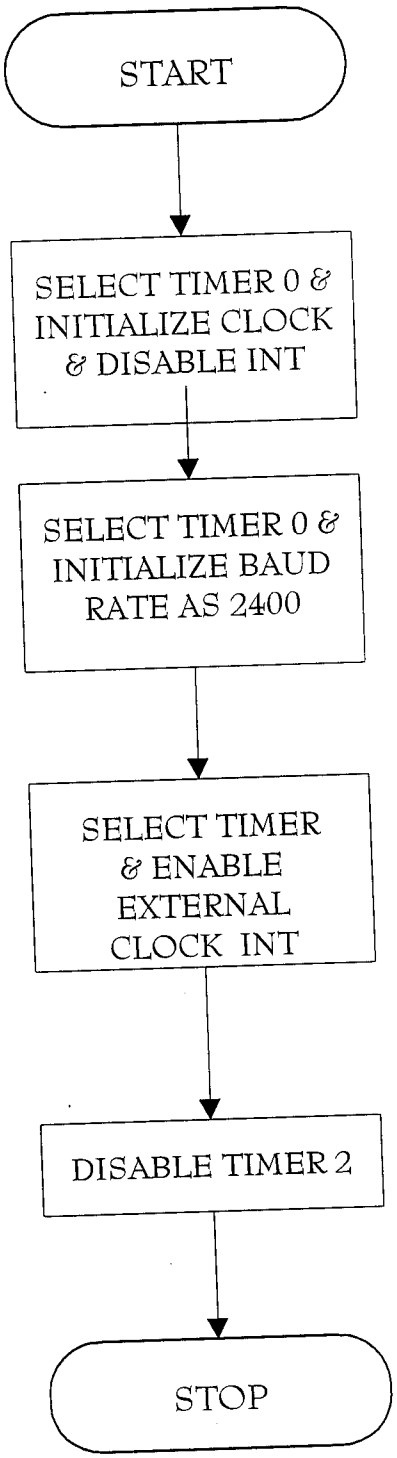
1. Initialisation of USART



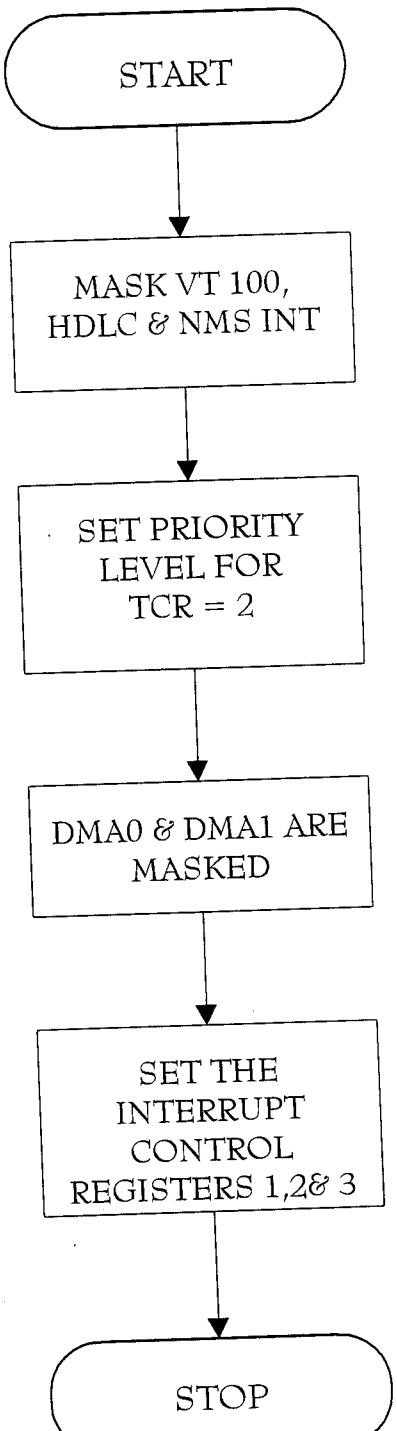
2. Initialisation of PCB



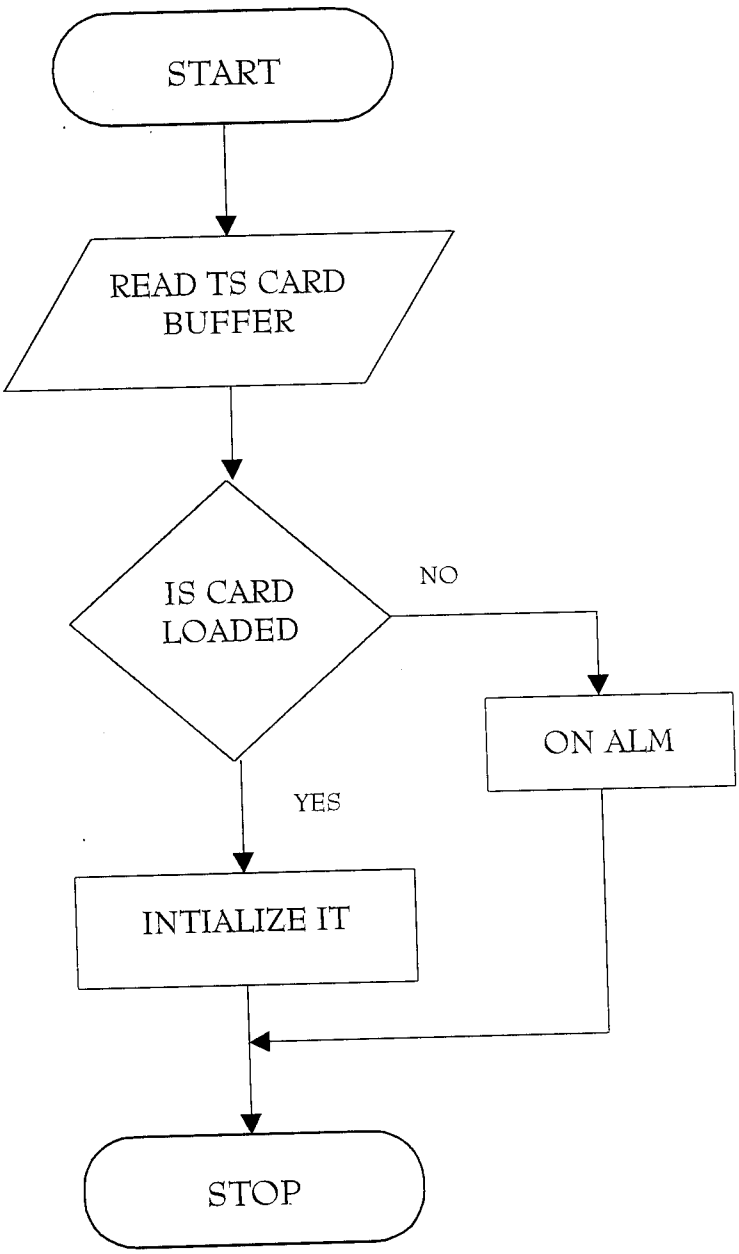
3. INITIALIZATION OF TIMER



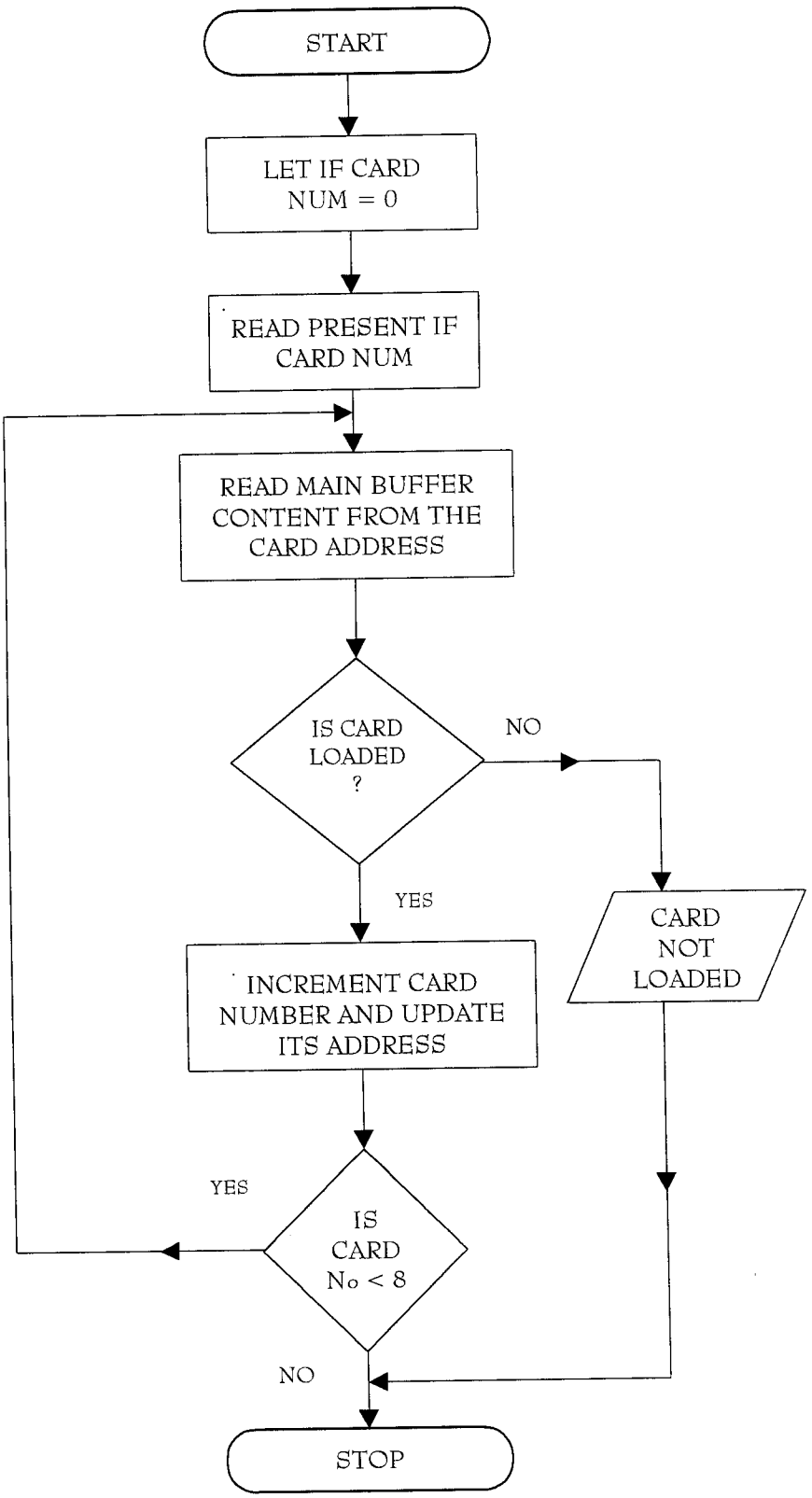
4. INITIALISATION OF INTERRUPT & DMA



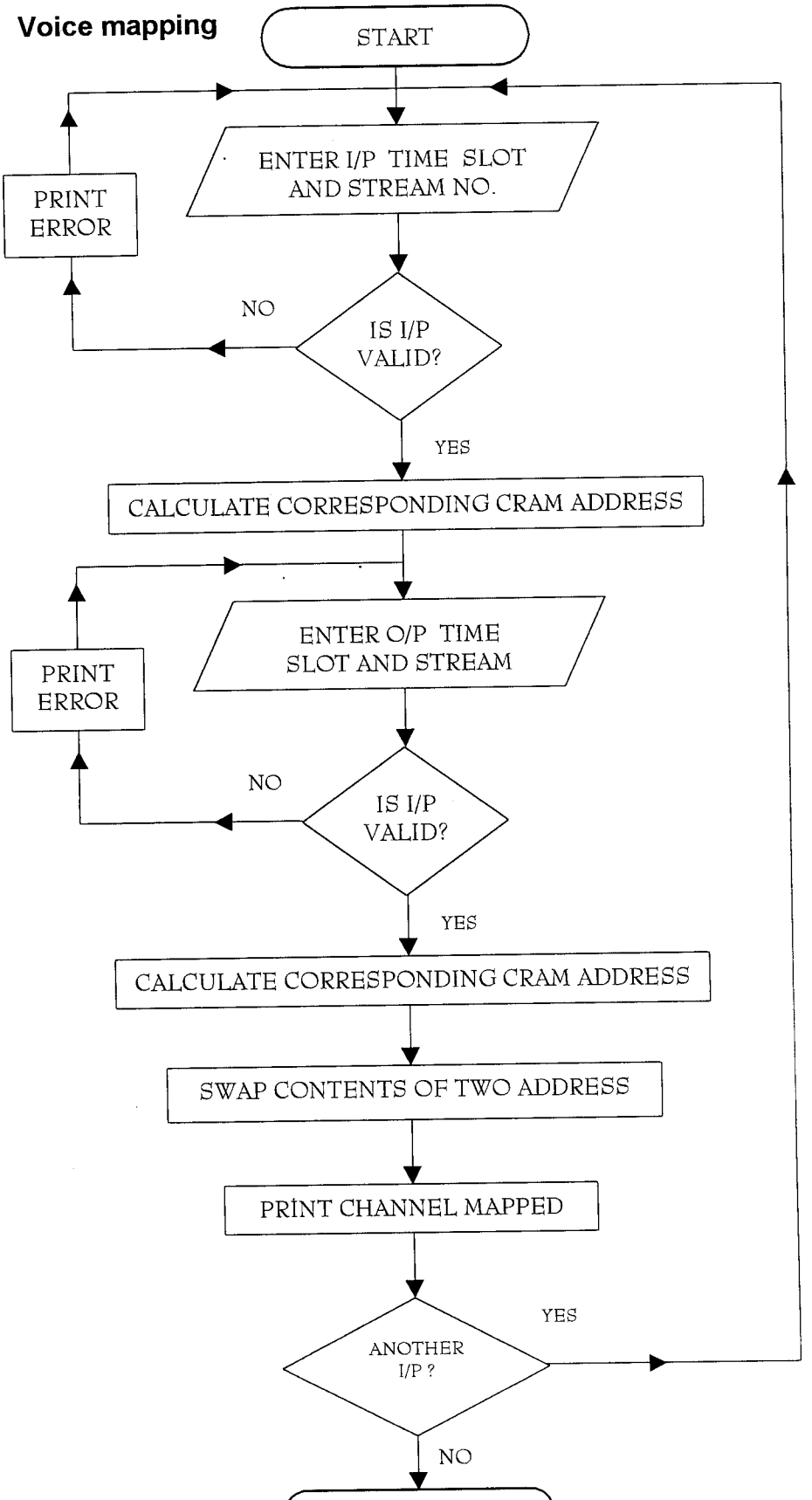
5. INITIALISATION OF TS CARD



6. Initialisation of if card



7. Voice mapping



5.6 Source Code

```
$MOD186

;SOFTWARE FOR INITIALISATION OF VARIOUS IC'S IN CONTROL
;CARD & INITIALISATION OF OTHER CARDS

;GLOBAL LABELS
;--------------

PUBLIC      DEF_SEG
PUBLIC      AON_BAY_ALM
PUBLIC      AON-CON-ALM
PUBLIC      RD_IFM_BUF
PUBLIC      PRT_CHAR
PUBLIC      PRT_MES_COM
PUBLIC      PRT_STG2
PUBLIC      PRT_INI_IFM
PUBLIC      PRT_TS_FAIL
PUBLIC      PRT_INIT_TS
Public      tog_con_lat

;EXTERNAL LABELS
;---------------
EXTRN PRT-MES-INTS
EXTRN PRT-MES-INPCM
EXTRN PRT-MES-OUTTS
EXTRN PRT-MES-OUTPCM
EXTRN PRT-MES-ERR
EXTRN PRT-MES-MAPPED
EXTRN PRT-MES-ANY

CODE1  SEGMENT  PUBLIC
ASSUME CS:CODE1
     JMP  FAR  PTR INIT1
CODE1 ENDS

; INITIALISATION OF 80186 PERIPHERAL CONTROL BLOCK
;-------------------------------------------------

CODE2  SEGMENT  PUBLIC
ASSUME CS:CODE2

INIT1:     MOV        DX,FFA0H
     MOV   AX,3FC4H  ;A0 SELECTS UCS BLK OF 256K BYTES
     OUT   DX,AX
     ADD   DX,0002H
     MOV   AX,03C4H  ;SELECTS LCS BLK OF 16K BYTES
```

```
        ADD   DX,0006H   ;MPCS REG
        MOV   AX,0F44H   ;64K MCS BLK,PCS 0_6 USED AS MEMORY
        OUT   DX,AX
        SUB   DX,0002H   ;MMCS REG
        MOV   AX,2004H   ;MCS BLK FROM 20000H
        OUT   DX,AX
        SUB   DX,0002H   ;PHERIPHERAL CHIP SELECT BASE ADDR.
                         ;REG
        MOV   AX,043CH   ;PCS FROM 4000H IN MEM
        OUT   DX,AX
        SUB   AX,AX
        MOV   DS,AX      ;DS SEG 0
        MOV   DS:BYTE PTR [SEL_CON_LAT1],FFH
                         ;STROBE 1 TO STB I/P OF MICRO-
                         ;MONITROR CHIP
        MOV   DS:BYTE PTR [SEL_CON_LAT1],F7H
                         ;STROBE 0 TO STB I/P OF MICRO-
                    ;MONITROR CHIP
      MOV   DS:BYTE PTR [SEL_CON_LAT1],FFH
                         ;STROBE 1 TO STB I/P OF MICRO-
                    ;MONITROR CHIP

;INTIALISATION OF TIMER IN  80186
;--------------------------------

        MOV   DX,FF56H   ;TMR 0 CONTROL REG
        MOV   AX,C003H   ;INT CLOCKING,INT DISABLED
        OUT   DX,AX
        SUB   DX,0002H   ;TMR 0 MAX COUNT REGB
        MOV   AX,000DH   ;BAUD RATE OF 2400
        OUT   DX,AX
        SUB   DX,0002H   ;TMR 0 MAX COUNT REGA
        MOV   AX,000DH
        OUT   DX,AX
        MOV   DX,FF5EH   ;TMR 1 CONTROL REG
        MOV   AX,F007H   ;EXT CLOCKING,INT ENABLED
        OUT   DX,AX
        SUB   DX,0002H   ;TMR 1 MAX COUNT REGB
        MOV   AX,0F62H   ;10 HZ WAVWFORM
        OUT   DX,AX
        SUB   DX,0002H   ;TMR 1 MAX COUNT REGA
        MOV   AX,0F62H   ;10 HZ WAVEFORM
        OUT   DX,AX
        MOV   DX,FF66H   ;TMR 2 CONTROL REG
        MOV   AX,4000H   ;TMR 2 NOT USED
        OUT   DX,AX
```

```
INTIALISATION  OF INTERRUPTS & DMA
;---------------------------------

     MOV  DX,FF28H  ;INT CONT GEN MASK REG
     MOV  AX,009CH  ;NMS(INT 3),KB(INT 0),DMA INTS
                    ;MASKED
     OUT  DX,AX
     MOV  DX,0FF32H ;TIMER INT CONT  REG
     MOV  AX,0002H ;PRIO LEVEL =2
     OUT  DX,AX
     ADD  DX,0002H  ;DMA 0 INT CONT REG
     MOV  AX,000FH  ;DMA 0 INT MASKED
     OUT  DX,AX
     ADD  DX,0002H  ;DMA 1 INT CONT REG
     MOV  AX,000FH  ;DMA 1 INT MASKED
     OUT  DX,AX
     MOV  DX,0FF38H ;INT0 CONT  REG
     MOV  AX,000FH  ;KB INT MASKED
     OUT  DX,AX
     ADD  DX,0002H  ;INT1 CONT  REG
     MOV   AX,0000H    ;VT 100 TERMINAL,  EDGE
     ;TRIG,PRIO     LEVEL=0,UNMASKED,NOT CASCADEDF,NO
     ;SFNM
     OUT  DX,AX
     ADD  DX,0002H  ;INT2 CONT  REG
     MOV  AX,0011H  ;HDLC INT, LEV TRIG,PRIO LEVEL=1
     OUT  DX,AX
     ADD  DX,0002H  ;INT3 CONT  REG
     MOV  AX,000FH  ;NMS INT MASKED,PRIO LEVEL=7
     OUT  DX,AX
     JMP  FAR  PTR INIT2
CODE2 ENDS

;MAIN PROGRAM
;-------------

CODE3 SEGMENT PUBLIC
ASSUME CS:CODE3

INIT2:    SUB  AX,AX
          MOV  DS,AX      ;DS  SEG=0000H
          MOV  SS,AX      ;SS SEG =0000H
          MOV  AX,2000H
          MOV  ES,AX      ;ES SEG=2000H
          MOV  SP,1FFEH
          CLD             ;CLEAR DIRECTION FLAG FOR AUTO
                          ; INCREMENT
          CLI             ;CLEAR INTERRUPT
```

```
; INITIALISATION OF CONTROL CARD LATCHES
;---------------------------------------

SEL_CON_LAT0    EQU  4000H
SEL_CON_LAT1    EQU  4180H
STO_CON_LAT0    EQU  2493H
STO_CON_LAT1    EQU  2490H
CON_CARD_BUF    EQU  4200H
SUB_RACK_POS    EQU  2494H

INIT_LAT: MOV  AL,DS:BYTE PTR [CON_CARD_BUF]
          AND   AL,3FH
          MOV  DS:BYTE PTR [SUB_RACK_POS],AL
               ; SUB-RACK NUMBER
          MOV  AL,FFH
               ;NO ALM TO PS CARD,TR DISABLED
          MOV  DS:BYTE PTR [SEL_CON_LAT0],AL
          MOV  DS:BYTE PTR [STO_CON_LAT0],AL
          MOV   DS:BYTE PTR [SEL_CON_LAT1],FEH
               ;NO BAY ALM/BP
          MOV  DS:BYTE PTR [STO_CON_LAT1],FEH

;INITIALISATION OF USART
;-----------------------

URT_COM_REG     EQU  4302H      ;COMMAND WORD
                                ;REGISTER
URT_DATA_REG    EQU  4300H      ;STATUS   REGISTER
INIT_URT:       MOV  CX,0003H ;COUNT
INIT_URT1:      MOV  DS:BYTE PTR [URT_COM_REG],00H
                          ;RESET USART TO KNOWN STATE
                NOP  ;DELAY
                NOP
                LOOP  INIT_URT1
                MOV  DS:BYTE PTR [URT_COM_REG],40H
                          ;INTERNAL RST
                MOV  DS:BYTE PTR [URT_COM_REG],7EH ;MODE
;WORD FOR BAUD RATE=2400Kbps,CHAR LEN=8,EVEN PARITY,1
;STOP BIT
                MOV  DS:BYTE PTR [URT_COM_REG],15H
                          ;TR,REC ENABLE
```

```
;INITIALISATION OF TS CARD
;-------------------------

TS_BUF_SEL      EQU  42AAH
INIT_TS:  CALL FAR PTR PRT_DEFAULT
          MOV  CX,0008H  ;NO OF TRIES
INIT_TS2: MOV  AL,DS:BYTE PTR [TS_BUF_SEL]
          AND  AL,18H
          CMP  AL,00H    ;IS TS CARD LOADED?
          JZ   INIT_TS1  ;JMP INIT-TS1 IF LOADED
          LOOP INIT_TS2  ;CONTINUE CHECK
          CALL FAR PTR PRT_TS_NOT
          CALL FAR PTR AON_BAY_ALM
          JMP  INIT_IF
INIT_TS1: CALL FAR PTR PRT_INIT_TS
          CALL  FAR PTR DEF_SEG

;INITIALISATION OF IF CARDS
;--------------------------

IND_CARD_BLK   EQU  2928H
INIT_IF:  MOV  DS:BYTE PTR [IND_CARD_BLK],00H
                    ;CURR IF CARD NO
          MOV  BX,0EB0H  ;CARD LOADED BLK
INIT_IF4: MOV  CX,0008H  ;NO OF TRIES
INIT_IF2: CALL FAR PTR RD_IFM_BUF
          AND  DL,0C0H
          JZ   INIT_IF1
          LOOP INIT_IF2
          MOV  BYTE PTR [BX],11H   ;CARD NOT LOADED
          JMP  INIT_IF3
INIT_IF1: MOV  BYTE PTR [BX],00H ;CARD  LOADED
          CALL  FAR PTR PRT_INI_IFM
          CALL FAR PTR DEF_SEG
INIT_IF3: INC  BX              ;NEXT CARD
          INC  DS:BYTE PTR [IND_CARD_BLK]
          CMP  DS:BYTE PTR [IND_CARD_BLK],08H
               ; ANOTHER CARD? INTIALIZE IT
          JB   INIT_IF4

;NEXT  SUB_ROUTINE SETS DS,SS TO 0000H AND ES TO 2000H
;-----------------------------------------------------

DEF_SEG PROC FAR
          PUSH    AX
          SUB     AX,AX
          MOV     DS,AX
          MOV     SS,AX
```

```
            MOV   ES,AX
            POP   AX
            RET
DEF_SEG ENDP

;SUB ROUTINE TO TOGGLE STROBE INPUT TO MICROMONITOR
;CHIP
;-------------------------------------------------------

tog_con_lat proc far
     PUSH  AX
     CALL  FAR PTR DEF_SEG
     MOV   AL,DS:BYTE PTR [STO_CON_LAT1]
     OR    AL,08H
     MOV   DS:BYTE PTR [SEL_CON_LAT1],AL ; STROBE 1 TO
;STB I/P OF MICRO-MONITROR CHIP
     AND   AL,0F7H
     MOV   DS:BYTE PTR [SEL_CON_LAT1],AL ; STROBE 0 TO
;STB I/P OF MICRO-MONITROR CHIP
     OR    AL,08H
     MOV   DS:BYTE PTR [SEL_CON_LAT1],AL ;  STROBE 1 TO
;STB I/P OF MICRO-MONITROR CHIP
     POP   AX
     RET
tog_con_lat endp

;SUB ROUTINE TO ON CONTROL CARD ALARM
;-------------------------------------

AON_CON_ALM PROC FAR
     PUSH  AX
     MOV   AL,DS:BYTE PTR [STO_CON_LAT0]
     AND   AL,0FDH
     MOV   DS:BYTE PTR [SEL_CON_LAT0],AL
     MOV   DS:BYTE PTR [STO_CON_LAT0],AL
     POP   AX
     RET
AON_CON_ALM ENDP

;SUB ROUTINE TO ON BAY ALARM
;----------------------------

AON_BAY_ALM PROC FAR
     PUSH AX
     MOV  AL,DS:BYTE PTR [STO_CON_LAT1]
      OR  AL,01H
     MOV  DS:BYTE PTR [SEL_CON_LAT1],AL
     MOV  DS:BYTE PTR [STO_CON_LAT1],AL
```

```
     RET
AON_BAY_ALM ENDP

;SUB ROUTINES FOR MESSAGES
;-------------------------

MES_INIT_TS     DB      'INITIALISING TS CARD...$'
MES_TS_NOT      DB      'TS CARD NOT LOADED!$'
MES_TS_FAIL     DB      'TS CARD FAIL OR NOT LOADED!$'
MES_INI_IFM     DB      'INITIALISING IF CARD :$'
MES_DEFAULT     DB      '  $' ,0AH
                DB      'DIGITAL CROSS CONNECT$ ' ,0AH
                DB      '$  ',0AH
MES-INTS        DB      'ENTER INPUT TIMESLOT NUMBER $'
MES-INPCM       DB      'ENTER INPUT STREAM NUMBER $'
MES-OUTTS       DB      'ENTER OUTPUT TIMESLOT NUMBER $'
MES-OUTPCM      DB      'ENTER OUTPUT STREAM NUMBER $'
MES-ERR         DB      'INVALID INPUT $'
MES-MAPPED      DB      'VOICE MAPPING DONE $'
MES-ANY         DB      'ANY MORE MAPPING PRESS1 ELSE 0$'


;SUB ROUTINES FOR PRINTING ON VT 100 TERMINAL
;--------------------------------------------

;PRINT ONE CHAR IN AL ON VT 100 SCREEN
;-------------------------------------

PRT_CHAR PROC FAR
          CALL FAR PTR DEF_SEG
          call far ptr tog_con_lat
          PUSH AX
          PUSH CX
          MOV  CX,FFFFH  ;NO OF TRIES
          MOV  AH,AL
PRT_CHAR2: MOV AL,DS:BYTE PTR [URT_COM_REG]
           AND AL,05H
          CMP  AL,05H    ;TR BUF FREE?
          JZ   PRT_CHAR1
          LOOP PRT_CHAR2
          CALL FAR PTR AON_CON_ALM
          CALL FAR PTR AON_BAY_ALM
          JMP  PRT_CHAR3
PRT_CHAR1: MOV DS:BYTE PTR [URT_DATA_REG],AH
PRT_CHAR3: POP CX
          POP  AX
          RET
PRT_CHAR ENDP
```

```
;SUB ROUTINES TO PRINT STRING FROM [BX] ON VT_100
;TERMINAL
;-----------------------------------------------------

PRT_STG    PROC FAR
           PUSH AX
           PUSH BX
           PUSH CX
           MOV  CX,FFFFH  ;NO OF TRIES
PRT_STG1   MOV  AL,DS:BYTE PTR [URT_COM_REG]
           AND  AL,05H
           CMP  AL,05H    ;TR BUF FREE?
           JZ   PRT_STG1A
           LOOP PRT_STG1
           CALL FAR PTR AON_CON_ALM
           CALL FAR PTR AON_BAY_ALM
           JMP  PRT_STG3
PRT_STG1A:MOV  AL,0AH     ;0AH IS FOR NEW LINE
           CALL FAR PTR PRT_CHAR
PRT_STG2:  MOV  CX,0FFFFH  ;NO OF TRIES
PRT_STG2B:MOV  AL,DS:BYTE PTR [URT_COM_REG]
           AND  AL,05H
           CMP  AL,05H     ;TR BUF FREE?
           JZ   PRT_STG2A
           LOOP PRT_STG2B
           CALL FAR PTR AON_CON_ALM
           CALL FAR PTR AON_BAY_ALM
           JMP  PRT_STG3
PRT_STG2A:MOV  AL,CS:BYTE PTR [BX] ;OFFSET OF MESSAGE
           CMP  AL,24H          ;END OF MESSAGE?
           JZ   PRT_STG3
           CALL FAR PTR PRT_CHAR
           INC  BX               ;NEXT CHR
           JMP  PRT_STG2
PRT_STG3:  POP  CX
           POP  BX
           POP  AX
           RET
PRT_STG ENDP

PRT_INIT_TS PROC    FAR
           PUSH  BX
           MOV   BX,OFFSET MES_INIT_TS
PRT_MES_COM:CALL  FAR PTR PRT_STG
             POP   BX
             RET
PRT_INIT_TS ENDP
```

```
            PUSH  BX
            MOV   BX,OFFSET MES_TS_NOT
            JMP   PRT_MES_COM
PRT_TS_NOT ENDP

PRT_INI_IFM PROC FAR
            PUSH  AX
            PUSH  BX
            MOV   BX,OFFSET MES_INI_IFM
            CALL  FAR PTR PRT_STG
            MOV   AL,DS:BYTE PTR [IND_CARD_BLK]
            OR    AL,30H
            CALL  FAR PTR PRT_CHAR
            POP   BX
            POP   AX
            RET
PRT_INI_IFM ENDP

PRT_DEFAULT PROC FAR
            PUSH  BX
            MOV   BX,OFFSET MES_DEFAULT
            JMP   PRT_MES_COM
PRT_DEFAULT ENDP


PRT_TS_FAIL PROC    FAR
            PUSH  BX
            MOV   BX,OFFSET MES_TS_FAIL
            JMP   PRT_MES_COM
PRT_TS_FAIL ENDP

PRT_MES_INTS PROC   FAR
            PUSH  BX
            MOV   BX,OFFSET MES_INTS
            JMP   PRT_MES_COM
PRT_MES_INTS ENDP

PRT_MES_INPCM PROC  FAR
            PUSH  BX
            MOV   BX,OFFSET MES_INPCM
            JMP   PRT_MES_COM
PRT_MES_INPCM ENDP
PRT_MES_OUTTS PROC  FAR
            PUSH  BX
            MOV   BX,OFFSET MES_OUTTS
            JMP   PRT_MES_COM
PRT_MES_OUTTS ENDP
PRT_MES_ANY PROC    FAR
```

```
            MOV    BX,OFFSET MES_ANY
            JMP    PRT_MES_COM
PRT_MES_ANY ENDP
PRT_MES_OUTPCM PROC FAR
            PUSH   BX
            MOV    BX,OFFSET MES_OUTPCM
            JMP    PRT_MES_COM
PRT_MES_OUTPCM ENDP
PRT_MES_ERR PROC    FAR
            PUSH   BX
            MOV    BX,OFFSET MES_ERR
            JMP    PRT_MES_COM
PRT_MES_ERR ENDP
PRT_MES_MAPPED PROC FAR
            PUSH   BX
            MOV    BX,OFFSET MES_MAPPED
            JMP    PRT_MES_COM
PRT_MES_MAPPED ENDP


;NEXT SUB_ROUTINE RETURNS IN DL IF CARD M MAIN BUFFER
;CONTENT
;-----------------------------------------------------
 RD_IFM_BUF PROC FAR
            PUSH AX
            PUSH BX
            PUSH SI
            MOV  SI,80C0H ;IF CARD 0 BUF 0 ADD IN
            MOV  AX,0100H ;OFFFSET BY 256 BYTES PER CARD
            SUB  BX,BX
            MOV  BL,DS:BYTE PTR [2928H]  ;CARD NUMBER
            MUL  BX
            ADD  SI,AX
            MOV  DL,ES:BYTE PTR [SI] ;MAIN BUFFER CONTENT
            POP  SI
            POP  BX
            POP  AX
            RET
RD_IFM_BUF ENDP


CODE3 ENDS
END
```

```
; PROGRAM FOR VOICE MAPPING (SINGLE)
;-----------------------------------

CODE 4 SEGMENT      EXTRN
ASSUME CS: CODE4
VOICE_MAP       :    CALL FAR PTR PRT-MES_INTS
     IN   AL,3EH ; ENTER INPUT TIME SLOT NUMBER
     MOV  DH,AL
     CMP  AL,31; CHECK FOR VALID I/P
     JBE  GO_ON
     CALL FAR PTR PRT_MES_ERR
     JMP  VOICE-MAP
GO_ON      :    CALL FAR PTR PRT-MES-INPCM
     IN   AL,3EH ;  ENTER INPUT STREAM NUMBER
     MOV  DL,AL
     CMP  AL,15; CHECK FOR VALID I/P
     JBE  CONT-PRO
     CALL      FAR PTR PRT-MES-ERR
     JMP  VOICE-MAP
CONT-PRO  :
     MOV  AL,DH
     CBW  ; CONVERT BYTE TO WORD
     ROL  AX,04
     MOV  BX,AX
     MOV  AL,DL
     CBW
     ADD  AX,BX; ADDRESS OF CRAM IN DSE 001 CHIP
     PUSH AX
VOICE_MAP1      :    CALL FAR PTR PRT-MES_OUTTS
     IN   AL,3EH ; ENTER OUTPUT TIME SLOT NUMBER
     MOV  DH,AL
     CMP  AL,31; CHECK FOR VALID I/P
     JBE  GO_ON1
     CALL FAR PTR PRT_MES_ERR
     JMP  VOICE-MAP1
GO_ON1     :    CALL FAR PTR PRT-MES-OUTPCM
     IN   AL,3EH ;  ENTER OUTPUT STREAM NUMBER
     MOV  DL,AL
     CMP  AL,15; CHECK FOR VALID I/P
     JBE  CONT-PRO1
     CALL FAR PTR PRT-MES-ERR
     JMP  VOICE-MAP1
CONT-PRO1 :
     MOV  AL,DH
     CBW  ; CONVERT BYTE TO WORD
     ROL  AX,04
     MOV  BX,AX
     MOV  AL,DL
```

```
        ADD  AX,BX; ADDRESS OF CRAM IN DSE 001 CHIP
        PUSH AX
        POP  AX
        POP  BX

  ; WRITING INTO CONTROL RAM OF DSE001 CHIP
  ;----------------------------------------
        MOV  BP,0000H; LOAD ADDRESS LOWER
        MOV  [BP], AL
        MOV  BP,0002H; LOAD ADDRESS HIGHER
        MOV  [BP],AH
        MOV  BP,0004H; LOAD DATA LOWER
        MOV  [BP], BL
        MOV  BP,0007H ; LOAD DATA HIGHER
        MOV  [BP], BH
        MOV  BP,0008H; WRITE INTO CRAM
        MOV  BP,0000H; LOAD ADDRESS LOWER
        MOV  [BP],BL
        MOV  BP,0002H; LOAD ADDRESS HIGHER
        MOV  [BP],BH
        MOV  BP,0004H; LOAD DATA LOWER
        MOV  [BP],AL
        MOV  BP,0007H; LOAD DATA HIGHER
        MOV  [BP],AH
        MOV  BP,0008H;WRITE INTO CRAM
        CALL FAR PTR PRT-MES-MAPPED
        CALL FAR PTR PRT-MES - ANY
        IN AL,3EH; ANY MORE MAPPINGS?
        JNZ VOICE MAP
  CODE4 ENDS
  END
```

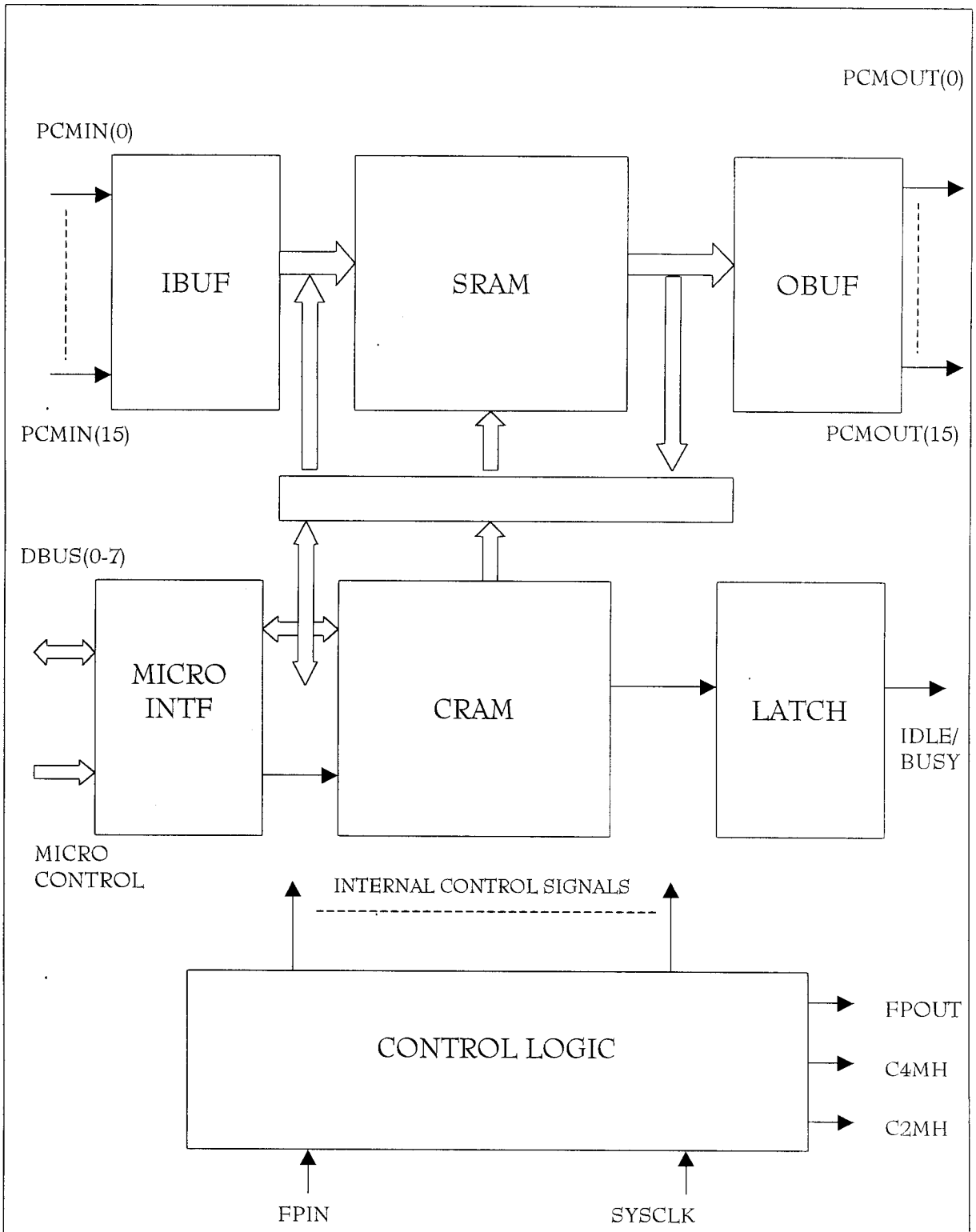


Fig 5.1 DSE 001 CHIP ORGANISATION

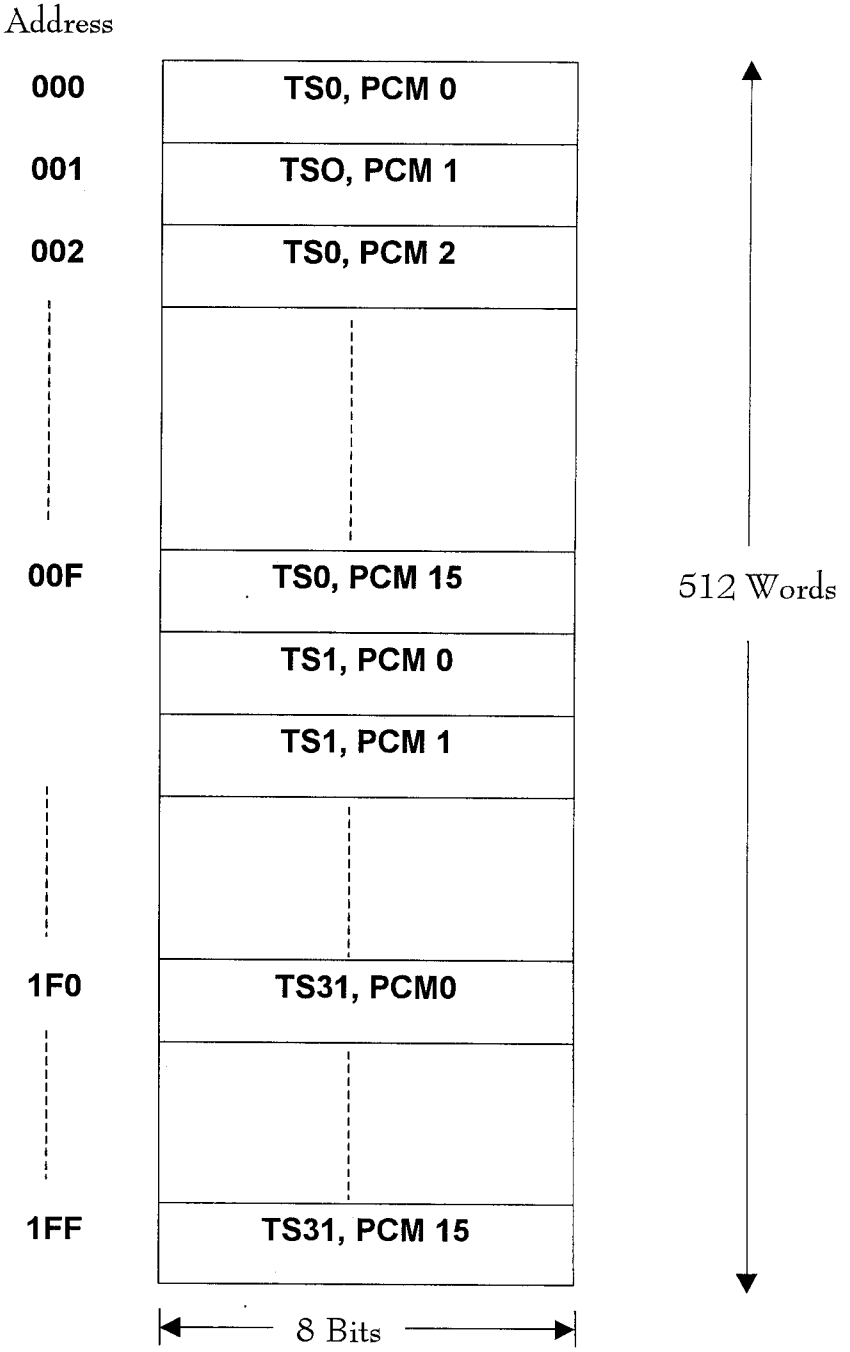
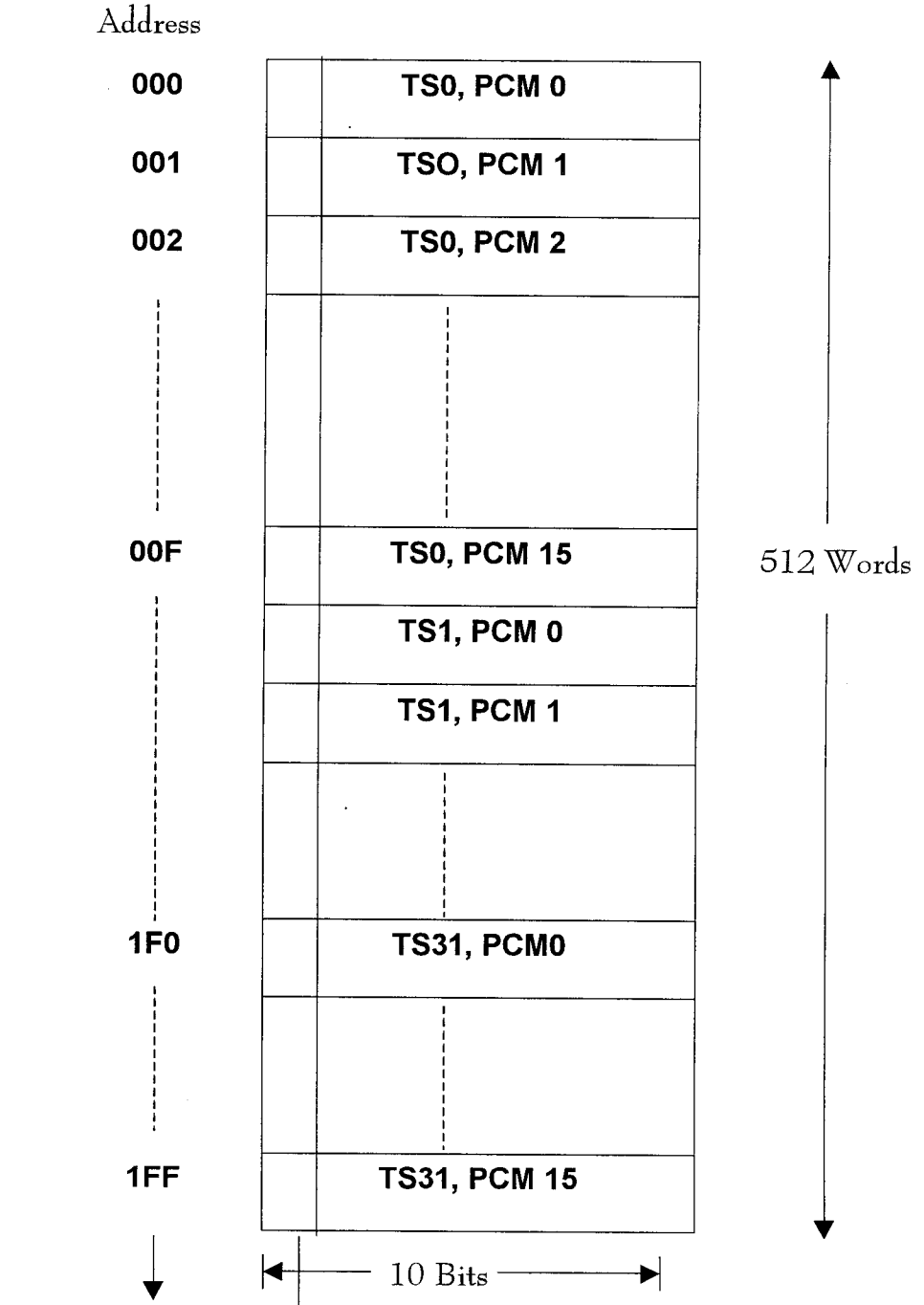


Fig. 5.2 SRAM MAP


Address
000
001
002
00F
1F0
1FF
TS0, PCM 0
TSO, PCM 1
TS0, PCM 2
TS0, PCM 15
TS1, PCM 0
TS1, PCM 1
TS31, PCM0
TS31, PCM 15
512 Words
10 Bits
Address to CRAM refers to outgoing PCm Link + Time slot
Indicate Idle/Busy Status

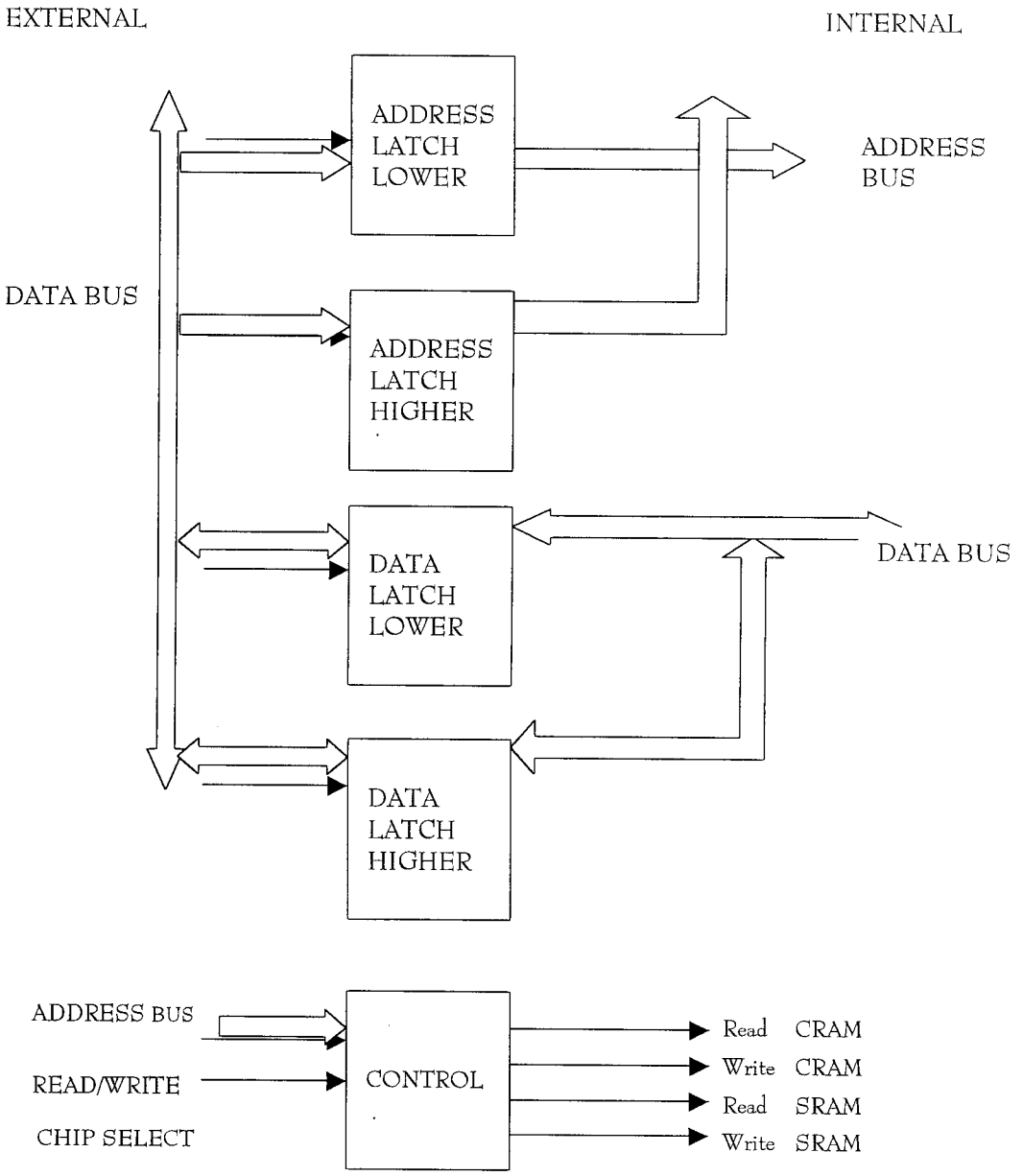


Fig 5.4 MICROPROCESSOR INTERFACE

No.	$\overline{R/W}$	A3	A2	A1	DESCRIPTION
1	1	0	0	0	Load ADDRESS LOWER
2	1	0	0	1	Load ADDRESS HIGHER
3	1	0	1	0	Load DATA LOWER
4	1	0	1	1	Load DATA HIGHER
5	1	1	0	0	Write CRAM
6	1	1	0	1	Read from CRAM to Data register
7	1	1	1	0	Write SRAM
8	1	1	1	1	Read from SRAM into Data register
9	0	0	1	0	Read DATA LOWER
10	0	0	1	1	Read DATA HIGHER

TABEL 5.1 MICROPROCESSOR COMMANDS

CONCLUSION

The control card was interfaced with various other cards in Digital Cross - Connect Switch and has been tested successfully.

The product is under production and it will be installed in public telecom networks for places with small number of subscribers shortly. It has been planned to installed in Railways and Defence , later.

It is of low cost, portable and moreover fully controlled by software.

At present, we have adapted single channel mapping method. In future we will go for multiple channel mapping methods in which N X 64Kbps channels can be dropped at a time.

In the present DCS systems, the standby cards are in cold standby mode, i.e., whenever a fault occurs we have to manually replace the cards. In future, we can modify the design apt for the hot standby mode, i.e., whenever a fault occurs in the card, the stand-by-card is chosen automatically.

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INTERNET ADDRESS

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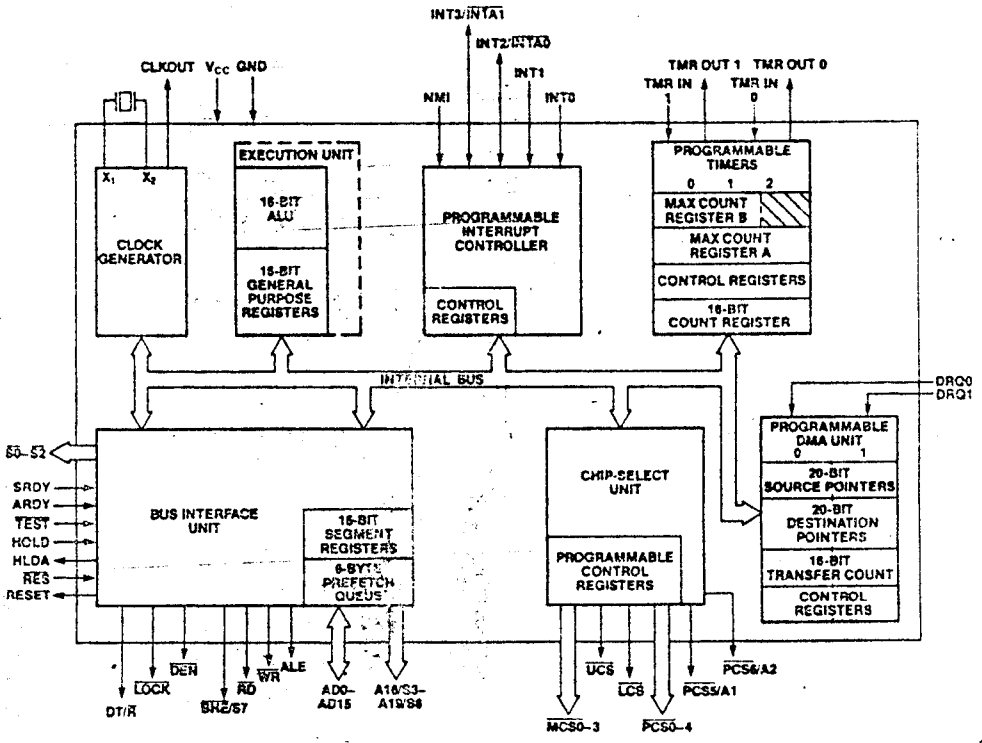
80186
HIGH INTEGRATION 16-BIT MICROPROCESSOR

- Integrated Feature Set
  - Enhanced 8086-2 CPU
  - Clock Generator
  - 2 Independent, High-Speed DMA Channels
  - Programmable Interrupt Controller
  - 3 Programmable 16-bit Timers
  - Programmable Memory and Peripheral Chip-Select Logic
  - Programmable Wait State Generator
  - Local Bus Controller
- Available in 12.5 MHz (80186-12), 10 MHz (80186-10) and 8 MHz (80186) Versions
- High-Performance Processor
  - At 8 MHz provides 2 times the Performance of the Standard 8086
  - 4 MByte/Sec Bus Bandwidth Interface @ 8 MHz
  - 6.25 MByte/Sec Bus Bandwidth Interface @ 12.5 MHz
- Direct Addressing Capability to 1 MByte of Memory and 64 KByte I/O
- Completely Object Code Compatible with All Existing 8086, 8088 Software
  - 10 New Instruction Types
- Complete System Development Support
  - Development Software; Assembler, PL/M, Pascal, Fortan, and System Utilities
  - In-Circuit-Emulator (I^2ICE^{TM}-186)
- High Performance Numerical Coprocessing Capability Through 8087 Interface
- Available in 68 Pin:
  - Plastic Leaded Chip Carrier (PLCC)
  - Ceramic Pin Grid Array (PGA)
  - Ceramic Leadless Chip Carrier (LCC)

(See Packaging Spec, Order #231369)



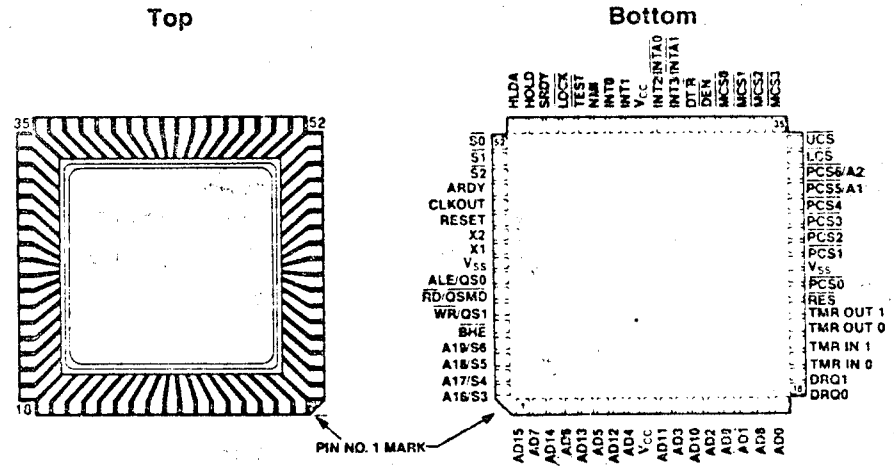
210451-1

Figure 1. 80186 Block Diagram

A. GOPINATH

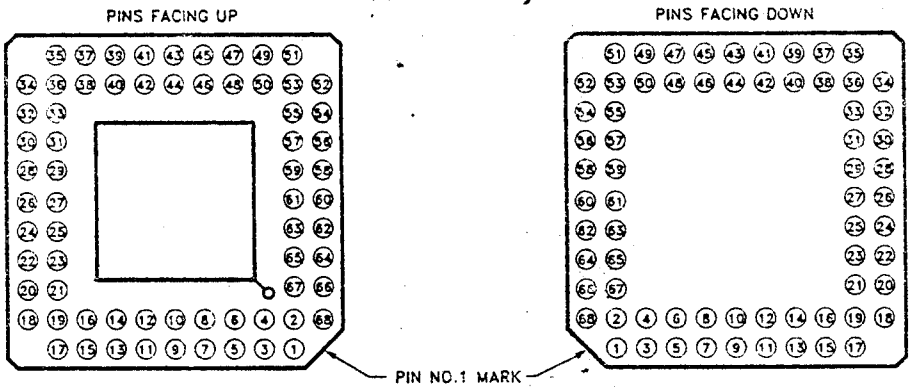
he Intel 80186 is a highly integrated 16-bit microprocessor. The 80186 effectively combines 15–20 of the ıost common 8086 system components onto one. The 80186 provides two times greater throughput than the tandard 5 MHz 8086. The 80186 is upward compatible with 8086 and 8088 software and adds 10 new ıstruction types to the existing set.

Leadless Chip Carrier



210451-2

Pin Grid Array



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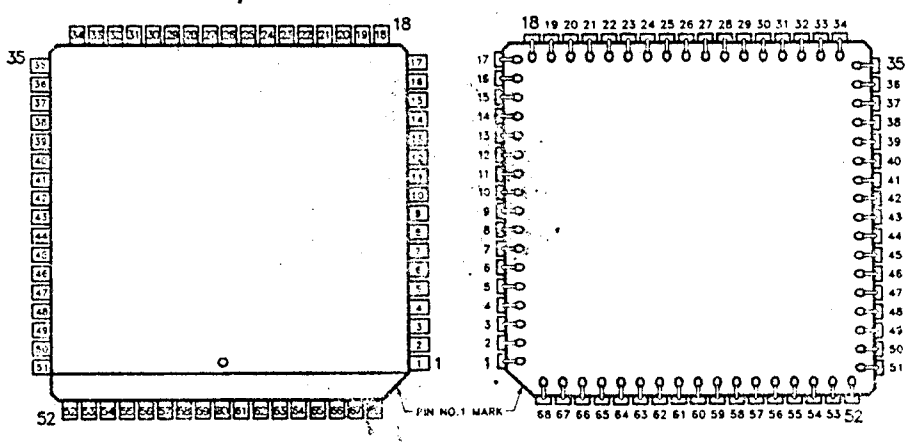
Plastic Leaded Chip Carrier



210451-19

Table 1. 80186 Pin Description

Symbol	Pin No.	Type	Name and Function
V_{CC}, V_{CC}	9, 43	I	**System Power:** +5 volt power supply.
V_{SS}, V_{SS}	26, 60	I	System Ground.
RESET	57	O	Reset Output indicates that the 80186 CPU is being reset, and can be used as a system reset. It is active HIGH, synchronized with the processor clock, and lasts an integer number of clock periods corresponding to the length of the $\overline{RES}$ signal.
X1, X2	59, 58	I	Crystal Inputs, X1 and X2, provide an external connection for a fundamental mode parallel resonant crystal for the internal crystal oscillator. X1 can interface to an external clock instead of a crystal. In this case, minimize the capacitance on X2 or drive X2 with complemented X1. The input or oscillator frequency is internally divided by two to generate the clock signal (CLKOUT).
CLKOUT	56	O	Clock Output provides the system with a 50% duty cycle waveform. All device pin timings are specified relative to CLKOUT. CLKOUT has sufficient MOS drive capabilities for the 8087 Numeric Processor Extension.
$\overline{RES}$	24	I	System Reset causes the 80186 to immediately terminate its present activity, clear the internal logic, and enter a dormant state. This signal may be asynchronous to the 80186 clock. The 80186 begins fetching instructions approximately 7 clock cycles after $\overline{RES}$ is returned HIGH. $\overline{RES}$ is required to be LOW for greater than 4 clock cycles and is internally synchronized. For proper initialization, the LOW-to-HIGH transition of $\overline{RES}$ must occur no sooner than 50 microseconds after power up. This input is provided with a Schmitt-trigger to facilitate power-on $\overline{RES}$ generation via an RC network. When $\overline{RES}$ occurs, the 80186 will drive the status lines to an inactive level for one clock, and then tri-state them.
$\overline{TEST}$	47	I	$\overline{TEST}$ is examined by the WAIT instruction. If the $\overline{TEST}$ input is HIGH when "WAIT" execution begins, instruction execution will suspend. $\overline{TEST}$ will be resampled until it goes LOW, at which time execution will resume. If interrupts are enabled while the 80186 is waiting for $\overline{TEST}$, interrupts will be serviced. This input is synchronized internally.
TMR IN 0, TMR IN 1	20 21	I I	Timer Inputs are used either as clock or control signals, depending upon the programmed timer mode. These inputs are active HIGH (or LOW-to-HIGH transitions are counted) and internally synchronized.
TMR OUT 0, TMR OUT 1	22 23	O O	Timer outputs are used to provide single pulse or continous waveform generation, depending upon the timer mode selected.
DRQ0 DRQ1	18 19	I I	DMA Request is driven HIGH by an external device when it desires that a DMA channel (Channel 0 or 1) perform a transfer. These signals are active HIGH, level-triggered, and internally synchronized.
NMI	46	I	Non-Maskable Interrupt is an edge-triggered input which causes a type 2 interrupt. NMI is not maskable internally. A transition from a LOW to HIGH initiates the interrupt at the next instruction boundary. NMI is latched internally. An NMI duration of one clock or more will guarantee service. This input is internally synchronized.
INT0, INT1 INT2/$\overline{INTA0}$ INT3/$\overline{INTA1}$	45, 44 42 41	I I/O I/O	Maskable Interrupt Requests can be requested by strobing one of these pins. When configured as inputs, these pins are active HIGH. Interrupt Requests are synchronized internally. INT2 and INT3 may be configured via software to provide active-LOW interrupt-acknowledge output signals. All interrupt inputs may be configured via software to be either edge- or level-triggered. To ensure recognition, all interrupt requests must remain active until the interrupt is acknowledged. When iRMX mode is selected, the function of these pins changes (see Interrupt Controller section of this data sheet).

Table 1. 80186 Pin Description (Continued)

Symbol	Pin No.	Type	Name and Function
9/S6, 8/S5, 7/S4, 6/S3	65 66 67 68	O O O O	Address Bus Outputs (16–19) and Bus Cycle Status (3–6) reflect the four most significant address bits during T_1. These signals are active HIGH. During T_2, T_3, T_W, and T_4, status information is available on these lines as encoded below:
			Low / **High** S6: Processor Cycle / DMA Cycle S3, S4, and S5 are defined as LOW during T_2–T_4.
)15–AD0	10–17, 1–8	I/O	Address/Data Bus (0–15) signals constitute the time multiplexed memory or I/O address (T_1) and data (T_2, T_3, T_W, and T_4) bus. The bus is active HIGH. A_0 is analogous to $\overline{BHE}$ for the lower byte of the data bus, pins D_7 through D_0. It is LOW during T_1 when a byte is to be transferred onto the lower portion of the bus in memory or I/O operations.
$\overline{E}$/S7	64	O	During T_1 the Bus High Enable signal should be used to determine if data is to be enabled onto the most significant half of the data bus; pins D_{15}–D_8. $\overline{BHE}$ is LOW during T_1 for read, write, and interrupt acknowledge cycles when a byte is to be transferred on the higher half of the bus. The S_7 status information is available during T_2, T_3, and T_4. S_7 is logically equivalent to $\overline{BHE}$. The signal is active LOW, and is tristated OFF during bus HOLD.
			$\overline{BHE}$ and A0 Encodings **$\overline{BHE}$ Value** / **A0 Value** / **Function** 0 / 0 / Word Transfer 0 / 1 / Byte Transfer on upper half of data bus (D15–D8) 1 / 0 / Byte Transfer on lower half of data bus (D_7–D_0) 1 / 1 / Reserved
E/QS0	61	O	Address Latch Enable/Queue Status 0 is provided by the 80186 to latch the address into the 8282/8283 address latches. ALE is active HIGH. Addresses are guaranteed to be valid on the trailing edge of ALE. The ALE rising edge is generated off the rising edge of the CLKOUT immediately preceding T_1 of the associated bus cycle, effectively one-half clock cycle earlier than in the standard 8086. The trailing edge is generated off the CLKOUT rising edge in T_1 as in the 8086. Note that ALE is never floated.
/QS1	63	O	Write Strobe/Queue Status 1 indicates that the data on the bus is to be written into a memory or an I/O device. $\overline{WR}$ is active for T_2, T_3, and T_W of any write cycle. It is active LOW, and floats during "HOLD." It is driven HIGH for one clock during Reset, and then floated. When the 80186 is in queue status mode, the ALE/QS0 and $\overline{WR}$/QS1 pins provide information about processor/instruction queue interaction.
			QS1 / **QS0** / **Queue Operation** 0 / 0 / No queue operation 0 / 1 / First opcode byte fetched from the queue 1 / 1 / Subsequent byte fetched from the queue 1 / 0 / Empty the queue

Table 1. 80186 Pin Description (Continued)

Symbol	Pin No.	Type	Name and Function
OLD (input) LDA (output)	50 51	I O	HOLD indicates that another bus master is requesting the local bus. The HOLD input is active HIGH. HOLD may be asynchronous with respect to the 80186 clock. The 80186 will issue a HLDA (HIGH) in response to a HOLD request at the end of T_4 or T_1. Simultaneous with the issuance of HLDA, the 80186 will float the local bus and control lines. After HOLD is detected as being LOW, the 80186 will lower HLDA. When the 80186 needs to run another bus cycle, it will again drive the local bus and control lines.
$\overline{UCS}$	34	O	Upper Memory Chip Select is an active LOW output whenever a memory reference is made to the defined upper portion (1K–256K block) of memory. This line is not floated during bus HOLD. The address range activating $\overline{UCS}$ is software programmable.
$\overline{LCS}$	33	O	Lower Memory Chip Select is active LOW whenever a memory reference is made to the defined lower portion (1K–256K) of memory. This line is not floated during bus HOLD. The address range activating $\overline{LCS}$ is software programmable.
$\overline{MCS0}$–3	38, 37, 36, 35	O	Mid-Range Memory Chip Select signals are active LOW when a memory reference is made to the defined mid-range portion of memory (8K–512K). These lines are not floated during bus HOLD. The address ranges activating $\overline{MCS0}$–3 are software programmable.
$\overline{PCS0}$ $\overline{PCS1}$–4	25 27, 28, 29, 30	O O	Peripheral Chip Select signals 0–4 are active LOW when a reference is made to the defined peripheral area (64K byte I/O space). These lines are not floated during bus HOLD. The address ranges activating $\overline{PCS0}$–4 are software programmable.
$\overline{PCS5}$/A1	31	O	Peripheral Chip Select 5 or Latched A1 may be programmed to provide a sixth peripheral chip select, or to provide an internally latched A1 signal. The address range activating $\overline{PCS5}$ is software programmable. When programmed to provide latched A1, rather than $\overline{PCS5}$, this pin will retain the previously latched value of A1 during a bus HOLD. A1 is active HIGH.
$\overline{PCS6}$/A2	32	O	Peripheral Chip Select 6 or Latched A2 may be programmed to provide a seventh peripheral chip select, or to provide an internally latched A2 signal. The address range activating $\overline{PCS6}$ is software programmable. When programmed to provide latched A2, rather than $\overline{PCS6}$, this pin will retain the previously latched value of A2 during a bus HOLD. A2 is active HIGH.
$T/\overline{R}$	40	O	Data Transmit/Receive controls the direction of data flow through the external 8286/8287 data bus transceiver. When LOW, data is transferred to the 80186. When HIGH the 80186 places write data on the data bus.
$\overline{EN}$	39	O	Data Enable is provided as an 8286/8287 data bus transceiver output enable. $\overline{DEN}$ is active LOW during each memory and I/O access. $\overline{DEN}$ is HIGH whenever $DT/\overline{R}$ changes state.

Table 1. 80186 Pin Description (Continued)

Symbol	Pin No.	Type	Name and Function
$\overline{RD}$/QSMD	62	O	Read Strobe indicates that the 80186 is performing a memory or I/O read cycle. $\overline{RD}$ is active LOW for T_2, T_3, and T_W of any read cycle. It is guaranteed not to go LOW in T_2 until after the Address Bus is floated. $\overline{RD}$ is active LOW, and floats during "HOLD". $\overline{RD}$ is driven HIGH for one clock during Reset, and then the output driver is floated. A weak internal pull-up mechanism of the $\overline{RD}$ line holds it HIGH when the line is not driven. During RESET the pin is sampled to determine whether the 80186 should provide ALE, $\overline{WR}$ and $\overline{RD}$, or if the Queue-Status should be provided. $\overline{RD}$ should be connected to GND to provide Queue-Status data.
ARDY	55	I	Asynchronous Ready informs the 80186 that the addressed memory space or I/O device will complete a data transfer. The ARDY input pin will accept an asynchronous input, and is active HIGH. Only the rising edge is internally synchronized by the 80186. This means that the falling edge of ARDY must be synchronized to the 80186 clock. If connected to V_{CC}, no WAIT states are inserted. Asynchronous ready (ARDY) or synchronous ready (SRDY) must be active to terminate a bus cycle. If unused, this line should be tied LOW.
SRDY	49	I	Synchronous Ready must be synchronized externally to the 80186. The use of SRDY provides a relaxed system-timing specification on the Ready input. This is accomplished by eliminating the one-half clock cycle which is required for internally resolving the signal level when using the ARDY input. This line is active HIGH. If this line is connected to V_{CC}, no WAIT states are inserted. Asynchronous ready (ARDY) or synchronous ready (SRDY) must be active before a bus cycle is terminated. If unused, this line should be tied LOW.
$\overline{LOCK}$	48	O	$\overline{LOCK}$ output indicates that other system bus masters are not to gain control of the system bus while $\overline{LOCK}$ is active LOW. The $\overline{LOCK}$ signal is requested by the LOCK prefix instruction and is activated at the beginning of the first data cycle associated with the instruction following the LOCK prefix. It remains active until the completion of the instruction following the LOCK prefix. No prefetches will occur while $\overline{LOCK}$ is asserted. When executing more than one LOCK instruction, always make sure there are 6 bytes of code between the end of the first LOCK instruction and the start of the second LOCK instruction. $\overline{LOCK}$ is active LOW, is driven HIGH for one clock during RESET, and then floated.
$\overline{S0}$, $\overline{S1}$, $\overline{S2}$	52–54	O	Bus cycle status $\overline{S0}$–$\overline{S2}$ are encoded to provide bus-transaction information:

80186 Bus Cycle Status Information

$\overline{S2}$	$\overline{S1}$	$\overline{S0}$	Bus Cycle Initiated
0	0	0	Interrupt Acknowledge
0	0	1	Read I/O
0	1	0	Write I/O
0	1	1	Halt
1	0	0	Instruction Fetch
1	0	1	Read Data from Memory
1	1	0	Write Data to Memory
1	1	1	Passive (no bus cycle)

The status pins float during "HOLD."
$\overline{S2}$ may be used as a logical M/$\overline{IO}$ indicator, and $\overline{S1}$ as a DT/$\overline{R}$ indicator.
The status lines are driven HIGH for one clock during Reset, and then floated until a bus cycle begins.

Table 1. 80186 Pin Description (Continued)

Symbol	Pin No.	Type	Name and Function
$\overline{RD}$/QSMD	62	O	Read Strobe indicates that the 80186 is performing a memory or I/O read cycle. $\overline{RD}$ is active LOW for T_2, T_3, and T_W of any read cycle. It is guaranteed not to go LOW in T_2 until after the Address Bus is floated. $\overline{RD}$ is active LOW, and floats during "HOLD". $\overline{RD}$ is driven HIGH for one clock during Reset, and then the output driver is floated. A weak internal pull-up mechanism of the $\overline{RD}$ line holds it HIGH when the line is not driven. During RESET the pin is sampled to determine whether the 80186 should provide ALE, $\overline{WR}$ and $\overline{RD}$, or if the Queue-Status should be provided. $\overline{RD}$ should be connected to GND to provide Queue-Status data.
ARDY	55	I	Asynchronous Ready informs the 80186 that the addressed memory space or I/O device will complete a data transfer. The ARDY input pin will accept an asynchronous input, and is active HIGH. Only the rising edge is internally synchronized by the 80186. This means that the falling edge of ARDY must be synchronized to the 80186 clock. If connected to V_{CC}, no WAIT states are inserted. Asynchronous ready (ARDY) or synchronous ready (SRDY) must be active to terminate a bus cycle. If unused, this line should be tied LOW.
SRDY	49	I	Synchronous Ready must be synchronized externally to the 80186. The use of SRDY provides a relaxed system-timing specification on the Ready input. This is accomplished by eliminating the one-half clock cycle which is required for internally resolving the signal level when using the ARDY input. This line is active HIGH. If this line is connected to V_{CC}, no WAIT states are inserted. Asynchronous ready (ARDY) or synchronous ready (SRDY) must be active before a bus cycle is terminated. If unused, this line should be tied LOW.
$\overline{LOCK}$	48	O	$\overline{LOCK}$ output indicates that other system bus masters are not to gain control of the system bus while $\overline{LOCK}$ is active LOW. The $\overline{LOCK}$ signal is requested by the LOCK prefix instruction and is activated at the beginning of the first data cycle associated with the instruction following the LOCK prefix. It remains active until the completion of the instruction following the LOCK prefix. No prefetches will occur while $\overline{LOCK}$ is asserted. When executing more than one LOCK instruction, always make sure there are 6 bytes of code between the end of the first LOCK instruction and the start of the second LOCK instruction. $\overline{LOCK}$ is active LOW, is driven HIGH for one clock during RESET, and then floated.
$\overline{S0}$, $\overline{S1}$, $\overline{S2}$	52–54	O	Bus cycle status $\overline{S0}$–$\overline{S2}$ are encoded to provide bus-transaction information: **80186 Bus Cycle Status Information** $\overline{S2}$ / $\overline{S1}$ / $\overline{S0}$ / Bus Cycle Initiated 0 / 0 / 0 / Interrupt Acknowledge 0 / 0 / 1 / Read I/O 0 / 1 / 0 / Write I/O 0 / 1 / 1 / Halt 1 / 0 / 0 / Instruction Fetch 1 / 0 / 1 / Read Data from Memory 1 / 1 / 0 / Write Data to Memory 1 / 1 / 1 / Passive (no bus cycle) The status pins float during "HOLD." $\overline{S2}$ may be used as a logical M/$\overline{IO}$ indicator, and $\overline{S1}$ as a DT/$\overline{R}$ indicator. The status lines are driven HIGH for one clock during Reset, and then floated until a bus cycle begins.

GENERAL PURPOSE	
MOV	Move byte or word
PUSH	Push word onto stack
POP	Pop word off stack
PUSHA	Push all registers on stack
POPA	Pop all registers from stack
XCHG	Exchange byte or word
XLAT	Translate byte
INPUT/OUTPUT	
IN	Input byte or word
OUT	Output byte or word
ADDRESS OBJECT	
LEA	Load effective address
LDS	Load pointer using DS
LES	Load pointer using ES
FLAG TRANSFER	
LAHF	Load AH register from flags
SAHF	Store AH register in flags
PUSHF	Push flags onto stack
POPF	Pop flags off stack
ADDITION	
ADD	Add byte or word
ADC	Add byte or word with carry
INC	Increment byte or word by 1
AAA	ASCII adjust for addition
DAA	Decimal adjust for addition
SUBTRACTION	
SUB	Subtract byte or word
SBB	Subtract byte or word with borrow
DEC	Decrement byte or word by 1
NEG	Negate byte or word
CMP	Compare byte or word
AAS	ASCII adjust for subtraction
DAS	Decimal adjust for subtraction
MULTIPLICATION	
MUL	Multiply byte or word unsigned
IMUL	Integer multiply byte or word
AAM	ASCII adjust for multiply
DIVISION	
DIV	Divide byte or word unsigned
IDIV	Integer divide byte or word
AAD	ASCII adjust for division
CBW	Convert byte to word
CWD	Convert word to doubleword

MOVS	Move byte or word string
INS	Input bytes or word string
OUTS	Output bytes or word string
CMPS	Compare byte or word string
SCAS	Scan byte or word string
LODS	Load byte or word string
STOS	Store byte or word string
REP	Repeat
REPE/REPZ	Repeat while equal/zero
REPNE/REPNZ	Repeat while not equal/not zero
LOGICALS	
NOT	"Not" byte or word
AND	"And" byte or word
OR	"Inclusive or" byte or word
XOR	"Exclusive or" byte or word
TEST	"Test" byte or word
SHIFTS	
SHL/SAL	Shift logical/arithmetic left byte or word
SHR	Shift logical right byte or word
SAR	Shift arithmetic right byte or word
ROTATES	
ROL	Rotate left byte or word
ROR	Rotate right byte or word
RCL	Rotate through carry left byte or word
RCR	Rotate through carry right byte or word
FLAG OPERATIONS	
STC	Set carry flag
CLC	Clear carry flag
CMC	Complement carry flag
STD	Set direction flag
CLD	Clear direction flag
STI	Set interrupt enable flag
CLI	Clear interrupt enable flag
EXTERNAL SYNCHRONIZATION	
HLT	Halt until interrupt or reset
WAIT	Wait for $\overline{\text{TEST}}$ pin active
ESC	Escape to extension processor
LOCK	Lock bus during next instruction
NO OPERATION	
NOP	No operation
HIGH LEVEL INSTRUCTIONS	
ENTER	Format stack for procedure entry
LEAVE	Restore stack for procedure exit
BOUND	Detects values outside prescribed range

Figure 4. 80186 Instruction Set

CONDITIONAL TRANSFERS	
JA/JNBE	Jump if above/not below nor equal
JAE/JNB	Jump if above or equal/not below
JB/JNAE	Jump if below/not above nor equal
JBE/JNA	Jump if below or equal/not above
JC	Jump if carry
JE/JZ	Jump if equal/zero
JG/JNLE	Jump if greater/not less nor equal
JGE/JNL	Jump if greater or equal/not less
JL/JNGE	Jump if less/not greater nor equal
JLE/JNG	Jump if less or equal/not greater
JNC	Jump if not carry
JNE/JNZ	Jump if not equal/not zero
JNO	Jump if not overflow
JNP/JPO	Jump if not parity/parity odd
JNS	Jump if not sign
JO	Jump if overflow
JP/JPE	Jump if parity/parity even
JS	Jump if sign
UNCONDITIONAL TRANSFERS	
CALL	Call procedure
RET	Return from procedure
JMP	Jump
ITERATION CONTROLS	
LOOP	Loop
LOOPE/LOOPZ	Loop if equal/zero
LOOPNE/LOOPNZ	Loop if not equal/not zero
JCXZ	Jump if register CX = 0
INTERRUPTS	
INT	Interrupt
INTO	Interrupt if overflow
IRET	Interrupt return

Figure 4. 80186 Instruction Set (Continued)

access operands that do not reside in one of the r immediately available segments, a full 32-bit nter can be used to reload both the base (seg- nt) and offset values.

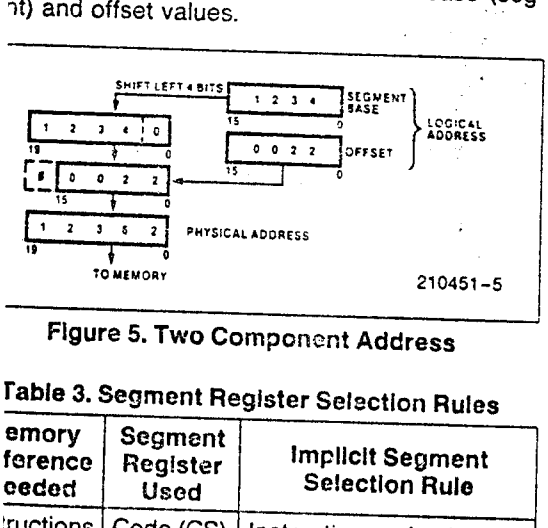


Figure 5. Two Component Address

Table 3. Segment Register Selection Rules

emory ference eeded	Segment Register Used	Implicit Segment Selection Rule
tructions	Code (CS)	Instruction prefetch and immediate data.
ck	Stack (SS)	All stack pushes and pops; any memory references which use BP Register as a base register.
ernal a bal)	Extra (ES)	All string instruction references which use the DI register as an index.
al Data	Data (DS)	All other data references.

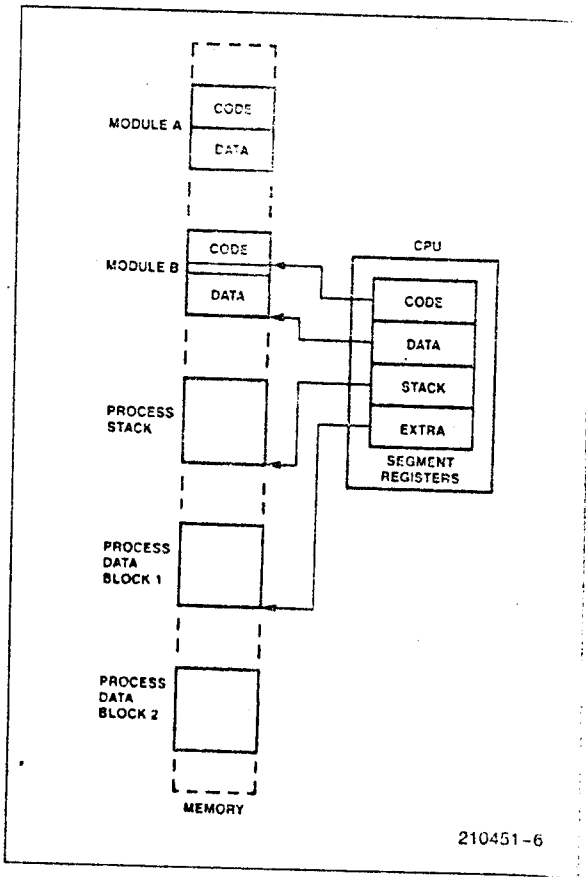


Figure 6. Segmented Memory Helps Structure Software

Addressing Modes

The 80186 provides eight categories of addressing modes to specify operands. Two addressing modes are provided for instructions that operate on register or immediate operands:

- *Register Operand Mode:* The operand is located in one of the 8- or 16-bit general registers.
- *Immediate Operand Mode:* The operand is included in the instruction.

Six modes are provided to specify the location of an operand in a memory segment. A memory operand address consists of two 16-bit components: a segment base and an offset. The segment base is supplied by a 16-bit segment register either implicitly chosen by the addressing mode or explicitly chosen by a segment override prefix. The offset, also called the effective address, is calculated by summing any combination of the following three address elements:

- the *displacement* (an 8- or 16-bit immediate value contained in the instruction);
- the *base* (contents of either the BX or BP base registers); and
- the *index* (contents of either the SI or DI index registers).

Any carry out from the 16-bit addition is ignored. Eight-bit displacements are sign extended to 16-bit values.

Combinations of these three address elements define the six memory addressing modes, described below.

- *Direct Mode:* The operand's offset is contained in the instruction as an 8- or 16-bit displacement element.
- *Register Indirect Mode:* The operand's offset is in one of the registers SI, DI, BX, or BP.
- *Based Mode:* The operand's offset is the sum of an 8- or 16-bit displacement and the contents of a base register (BX or BP).
- *Indexed Mode:* The operand's offset is the sum of an 8- or 16-bit displacement and the contents of an index register (SI or DI).
- *Based Indexed Mode:* The operand's offset is the sum of the contents of a base register and an Index register.
- *Based Indexed Mode with Displacement:* The operand's offset is the sum of a base register's contents, an index register's contents, and an 8- or 16-bit displacement.

Data Types

The 80186 directly supports the following data types:

- *Integer:* A signed binary numeric value contained in an 8-bit byte or a 16-bit word. All operations assume a 2's complement representation. Signed 32- and 64-bit integers are supported using the 80186/20 Numeric Data Processor.
- *Ordinal:* An unsigned binary numeric value contained in an 8-bit byte or a 16-bit word.
- *Pointer:* A 16- or 32-bit quantity, composed of a 16-bit offset component or a 16-bit segment base component in addition to a 16-bit offset component.
- *String:* A contiguous sequence of bytes or words. A string may contain from 1 to 64K bytes.
- *ASCII:* A byte representation of alphanumeric and control characters using the ASCII standard of character representation.
- *BCD:* A byte (unpacked) representation of the decimal digits 0–9.
- *Packed BCD:* A byte (packed) representation of two decimal digits (0–9). One digit is stored in each nibble (4-bits) of the byte.
- *Floating Point:* A signed 32-, 64-, or 80-bit real number representation. (Floating point operands are supported using the 80186/20 Numeric Data Processor configuration.)

In general, individual data elements must fit within defined segment limits. Figure 7 graphically represents the data types supported by the 80186.

I/O Space

The I/O space consists of 64K 8-bit or 32K 16-bit ports. Separate instructions address the I/O space with either an 8-bit port address, specified in the instruction, or a 16-bit port address in the DX register. 8-bit port addressos are zero extended such that A_{15}–A_8 are LOW. I/O port addresses 00F8(H) through 00FF(H) are reserved.

Interrupts

An interrupt transfers execution to a new program location. The old program address (CS:IP) and machine state (Status Word) are saved on the stack to allow resumption of the interrupted program. Interrupts fall into three classes: hardware initiated, INT instructions, and instruction exceptions. Hardware initiated interrupts occur in response to an external input and are classified as non-maskable or maskable.

GENERAL PURPOSE	
MOV	Move byte or word
PUSH	Push word onto stack
POP	Pop word off stack
PUSHA	Push all registers on stack
POPA	Pop all registers from stack
XCHG	Exchange byte or word
XLAT	Translate byte
INPUT/OUTPUT	
IN	Input byte or word
OUT	Output byte or word
ADDRESS OBJECT	
LEA	Load effective address
LDS	Load pointer using DS
LES	Load pointer using ES
FLAG TRANSFER	
LAHF	Load AH register from flags
SAHF	Store AH register in flags
PUSHF	Push flags onto stack
POPF	Pop flags off stack
ADDITION	
ADD	Add byte or word
ADC	Add byte or word with carry
INC	Increment byte or word by 1
AAA	ASCII adjust for addition
DAA	Decimal adjust for addition
SUBTRACTION	
SUB	Subtract byte or word
SBB	Subtract byte or word with borrow
DEC	Decrement byte or word by 1
NEG	Negate byte or word
CMP	Compare byte or word
AAS	ASCII adjust for subtraction
DAS	Decimal adjust for subtraction
MULTIPLICATION	
MUL	Multiply byte or word unsigned
IMUL	Integer multiply byte or word
AAM	ASCII adjust for multiply
DIVISION	
DIV	Divide byte or word unsigned
IDIV	Integer divide byte or word
AAD	ASCII adjust for division
CBW	Convert byte to word
CWD	Convert word to doubleword

MOVS	Move byte or word string
INS	Input bytes or word string
OUTS	Output bytes or word string
CMPS	Compare byte or word string
SCAS	Scan byte or word string
LODS	Load byte or word string
STOS	Store byte or word string
REP	Repeat
REPE/REPZ	Repeat while equal/zero
REPNE/REPNZ	Repeat while not equal/not zero
LOGICALS	
NOT	"Not" byte or word
AND	"And" byte or word
OR	"Inclusive or" byte or word
XOR	"Exclusive or" byte or word
TEST	"Test" byte or word
SHIFTS	
SHL/SAL	Shift logical/arithmetic left byte or word
SHR	Shift logical right byte or word
SAR	Shift arithmetic right byte or word
ROTATES	
ROL	Rotate left byte or word
ROR	Rotate right byte or word
RCL	Rotate through carry left byte or word
RCR	Rotate through carry right byte or word
FLAG OPERATIONS	
STC	Set carry flag
CLC	Clear carry flag
CMC	Complement carry flag
STD	Set direction flag
CLD	Clear direction flag
STI	Set interrupt enable flag
CLI	Clear interrupt enable flag
EXTERNAL SYNCHRONIZATION	
HLT	Halt until interrupt or reset
WAIT	Wait for $\overline{\text{TEST}}$ pin active
ESC	Escape to extension processor
LOCK	Lock bus during next instruction
NO OPERATION	
NOP	No operation
HIGH LEVEL INSTRUCTIONS	
ENTER	Format stack for procedure entry
LEAVE	Restore stack for procedure exit
BOUND	Detects values outside prescribed range

Figure 4. 80186 Instruction Set

Addressing Modes

The 80186 provides eight categories of addressing modes to specify operands. Two addressing modes are provided for instructions that operate on register or immediate operands:

- *Register Operand Mode:* The operand is located in one of the 8- or 16-bit general registers.
- *Immediate Operand Mode:* The operand is included in the instruction.

Six modes are provided to specify the location of an operand in a memory segment. A memory operand address consists of two 16-bit components: a segment base and an offset. The segment base is supplied by a 16-bit segment register either implicitly chosen by the addressing mode or explicitly chosen by a segment override prefix. The offset, also called the effective address, is calculated by summing any combination of the following three address elements:

- the *displacement* (an 8- or 16-bit immediate value contained in the instruction);
- the *base* (contents of either the BX or BP base registers); and
- the *index* (contents of either the SI or DI index registers).

Any carry out from the 16-bit addition is ignored. Eight-bit displacements are sign extended to 16-bit values.

Combinations of these three address elements define the six memory addressing modes, described below.

- *Direct Mode:* The operand's offset is contained in the instruction as an 8- or 16-bit displacement element.
- *Register Indirect Mode:* The operand's offset is in one of the registers SI, DI, BX, or BP.
- *Based Mode:* The operand's offset is the sum of an 8- or 16-bit displacement and the contents of a base register (BX or BP).
- *Indexed Mode:* The operand's offset is the sum of an 8- or 16-bit displacement and the contents of an index register (SI or DI).
- *Based Indexed Mode:* The operand's offset is the sum of the contents of a base register and an Index register.
- *Based indexed Mode with Displacement:* The operand's offset is the sum of a base register's contents, an index register's contents, and an 8- or 16-bit displacement.

Data Types

The 80186 directly supports the following data types:

- *Integer:* A signed binary numeric value contained in an 8-bit byte or a 16-bit word. All operations assume a 2's complement representation. Signed 32- and 64-bit integers are supported using the 80186/20 Numeric Data Processor.
- *Ordinal:* An unsigned binary numeric value contained in an 8-bit byte or a 16-bit word.
- *Pointer:* A 16- or 32-bit quantity, composed of a 16-bit offset component or a 16-bit segment base component in addition to a 16-bit offset component.
- *String:* A contiguous sequence of bytes or words. A string may contain from 1 to 64K bytes.
- *ASCII:* A byte representation of alphanumeric and control characters using the ASCII standard of character representation.
- *BCD:* A byte (unpacked) representation of the decimal digits 0–9.
- *Packed BCD:* A byte (packed) representation of two decimal digits (0–9). One digit is stored in each nibble (4-bits) of the byte.
- *Floating Point:* A signed 32-, 64-, or 80-bit real number representation. (Floating point operands are supported using the 80186/20 Numeric Data Processor configuration.)

In general, individual data elements must fit within defined segment limits. Figure 7 graphically represents the data types supported by the 80186.

I/O Space

The I/O space consists of 64K 8-bit or 32K 16-bit ports. Separate instructions address the I/O space with either an 8-bit port address, specified in the instruction, or a 16-bit port address in the DX register. 8-bit port addresses are zero extended such that A_{15}–A_8 are LOW. I/O port addresses 00F8(H) through 00FF(H) are reserved.

Interrupts

An interrupt transfers execution to a new program location. The old program address (CS:IP) and machine state (Status Word) are saved on the stack to allow resumption of the interrupted program. Interrupts fall into three classes: hardware initiated, INT instructions, and instruction exceptions. Hardware initiated interrupts occur in response to an external input and are classified as non-maskable or maskable.

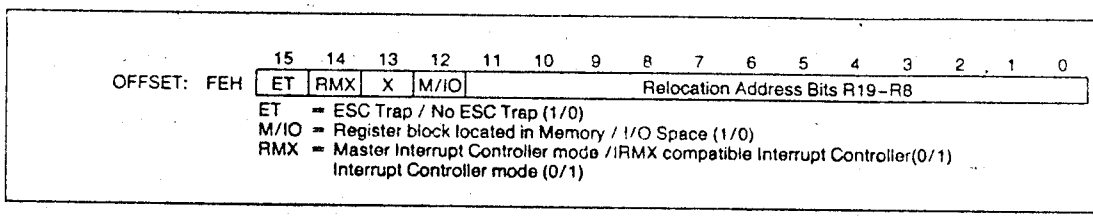


Figure 9. Relocation Register

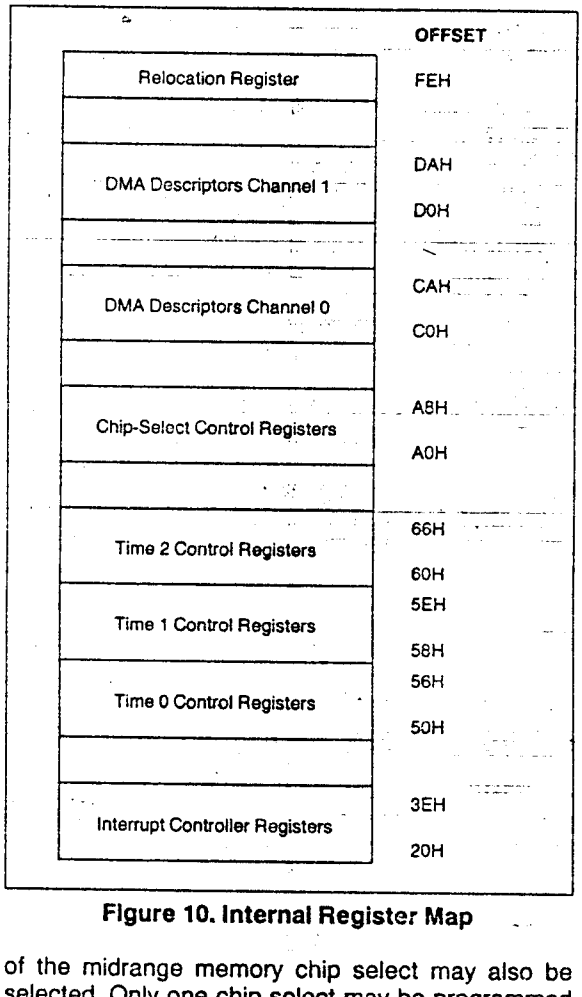


Figure 10. Internal Register Map

of the midrange memory chip select may also be selected. Only one chip select may be programmed to be active for any memory location at a time. All chip select sizes are in bytes, whereas 80186 memory is arranged in words. This means that if, for example, 16 64K x 1 memories are used, the memory block size will be 128K, not 64K.

Upper Memory $\overline{CS}$

The 80186 provides a chip select, called $\overline{UCS}$, for the top of memory. The top of memory is usually used as the system memory because after reset the 80186 begins executing at memory location FFFF0H.

The upper limit of memory defined by this chip select is always FFFFFH, while the lower limit is programmable. By programming the lower limit, the size of the select block is also defined. Table 7 shows the relationship between the base address selected and the size of the memory block obtained.

Table 7. UMCS Programming Values

Starting Address (Base Address)	Memory Block Size	UMCS Value (Assuming R0=R1=R2=0)
FFC00	1K	FFF8H
FF800	2K	FFB8H
FF000	4K	FF38H
FE000	8K	FE38H
FC000	16K	FC38H
F8000	32K	F838H
F0000	64K	F038H
E0000	128K	E038H
C0000	256K	C038H

The lower limit of this memory block is defined in the UMCS register (see Figure 11). This register is at offset A0H in the internal control block. The legal values for bits 6–13 and the resulting starting address and memory block sizes are given in Table 7. Any combination of bits 6–13 not shown in Table 7 will result in undefined operation. After reset, the UMCS register is programmed for a 1K area. It must be reprogrammed if a larger upper memory area is desired.

Any internally generated 20-bit address whose upper 16 bits are greater than or equal to UMCS (with bits 0–5 "0") will cause UCS to be activated. UMCS bits R2–R0 are used to specify READY mode for the area of memory defined by this chip-select register, as explained below.

Lower Memory $\overline{CS}$

The 80186 provides a chip select for low memory called $\overline{LCS}$. The bottom of memory contains the interrupt vector table, starting at location 00000H.

The lower limit of memory defined by this chip select is always 0H, while the upper limit is programmable. By programming the upper limit, the size of the memory block is also defined. Table 8 shows the relationship between the upper address selected and the size of the memory block obtained.

Table 8. LMCS Programming Values

Upper Address	Memory Block Size	LMCS Value (Assuming R0 = R1 = R2 = 0)
003FFH	1K	0038H
007FFH	2K	0078H
00FFFH	4K	00F8H
01FFFH	8K	01F8H
03FFFH	16K	03F8H
07FFFH	32K	07F8H
0FFFFH	64K	0FF8H
1FFFFH	128K	1FF8H
3FFFFH	256K	3FF8H

The upper limit of this memory block is defined in the LMCS register (see Figure 12). This register is at offset A2H in the internal control block. The legal values for bits 6–15 and the resulting upper address and memory block sizes are given in Table 8. Any combination of bits 6–15 not shown in Table 8 will result in undefined operation. After reset, the LMCS register value is undefined. However, the $\overline{LCS}$ chip-select line will not become active until the LMCS register is accessed.

Any internally generated 20-bit address whose upper 16 bits are less than or equal to LMCS (with bits 0–5 "1") will cause $\overline{LCS}$ to be active. LMCS register bits R2–R0 are used to specify the READY mode for the area of memory defined by this chip-select register.

Mid-Range Memory $\overline{CS}$

The 80186 provides four $\overline{MCS}$ lines which are active within a user-locatable memory block. This block can be located anywhere within the 80186 1M byte memory address space exclusive of the areas defined by $\overline{UCS}$ and $\overline{LCS}$. Both the base address and size of this memory block are programmable.

The size of the memory block defined by the mid-range select lines, as shown in Table 9, is determined by bits 8–14 of the MPCS register (see Figure 13). This register is at location A8H in the internal control block. One and only one of bits 8–14 must be set at a time. Unpredictable operation of the $\overline{MCS}$ lines will otherwise occur. Each of the four chip-select lines is active for one of the four equal contiguous divisions of the mid-range block. Thus, if the total block size is 32K, each chip select is active for 8K of memory with $\overline{MCS0}$ being active for the first range and $\overline{MCS3}$ being active for the last range.

The EX and MS in MPCS relate to peripheral functionally as described in a later section.

Table 9. MPCS Programming Values

Total Block Size	Individual Select Size	MPCS Bits 14–8
8K	2K	0000001B
16K	4K	0000010B
32K	8K	0000100B
64K	16K	0001000B
128K	32K	0010000B
256K	64K	0100000B
512K	128K	1000000B

The base address of the mid-range memory block is defined by bits 15–9 of the MMCS register (see Figure 14). This register is at offset A6H in the internal control block. These bits correspond to bits A19–A13 of the 20-bit memory address. Bits A12–A0 of the base address are always 0. The base address may be set at any integer multiple of the size of the total memory block selected. For example, if the mid-range block size is 32K (or the size of the block for which each $\overline{MCS}$ line is active is 8K), the block could be located at 10000H or 18000H, but not at 14000H, since the first few integer multiples of a 32K memory block are 0H, 8000H, 10000H, 18000H, etc. After reset, the contents of both of these registers is undefined. However, none of the $\overline{MCS}$ lines will be active until both the MMCS and MPCS registers are accessed.

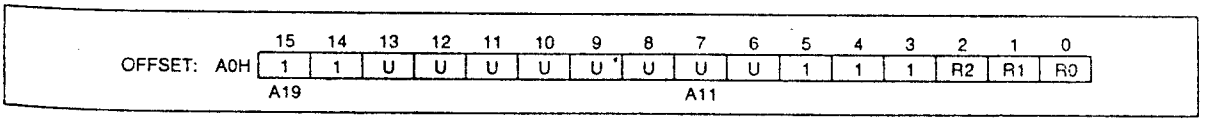
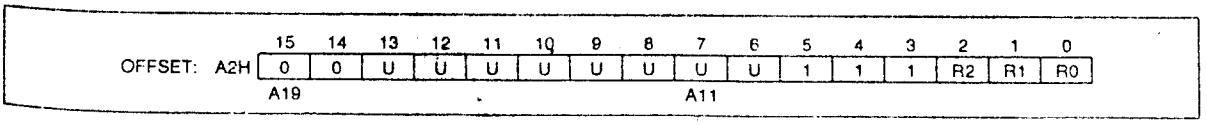


Figure 11. UMCS Register



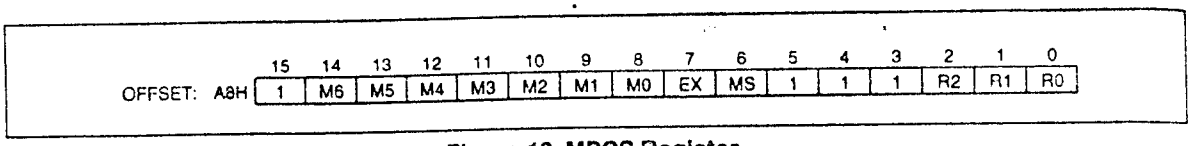


Figure 13. MPCS Register

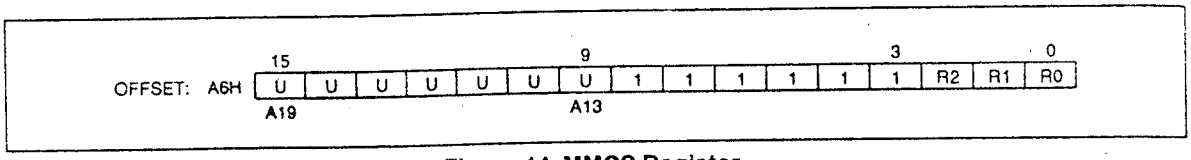


Figure 14. MMCS Register

MMCS bits R2–R0 specify READY mode of operation for all mid-range chip selects. All devices in mid-range memory must use the same number of WAIT states.

The 512K block size for the mid-range memory chip selects is a special case. When using 512K, the base address would have to be at either locations 00000H or 80000H. If it were to be programmed at 00000H when the $\overline{LCS}$ line was programmed, there would be an internal conflict between the $\overline{LCS}$ ready generation logic and the $\overline{MCS}$ ready generation logic. Likewise, if the base address were programmed at 80000H, there would be a conflict with the $\overline{UCS}$ ready generation logic. Since the $\overline{LCS}$ chip-select line does not become active until programmed, while the $\overline{UCS}$ line is active at reset, the memory base can be set only at 00000H. If this base address is selected, however, the $\overline{LCS}$ range must not be programmed.

Peripheral Chip Selects

The 80186 can generate chip selects for up to seven peripheral devices. These chip selects are active for seven contiguous blocks of 128 bytes above a programmable base address. This base address may be located in either memory or I/O space.

Seven $\overline{CS}$ lines called $\overline{PCS0}$–6 are generated by the 80186. The base address is user-programmable; however it can only be a multiple of 1K bytes, i.e., the least significant 10 bits of the starting address are always 0.

$\overline{PCS5}$ and $\overline{PCS6}$ can also be programmed to provide latched address bits A1, A2. If so programmed, they cannot be used as peripheral selects. These outputs can be connected directly to the A0, A1 pins used for selecting internal registers of 8-bit peripheral chips. This scheme simplifies the hardware interface because the 8-bit registers of peripherals are simply treated as 16-bit registers located on even boundaries in I/O space or memory space where only the lower 8-bits of the register are significant: the upper 8-bits are "don't cares."

The starting address of the peripheral chip-select block is defined by the PACS register (see figure 15). This register is located at offset A4H in the internal control block. Bits 15–6 of this register correspond to bits 19–10 of the 20-bit Programmable Base Address (PBA) of the peripheral chip-select block. Bits 9–0 of the PBA of the peripheral chip-select block are all zeros. If the chip-select block is located in I/O space, bits 12–15 must be programmed zero, since the I/O address is only 16 bits wide. Table 10 shows the address range of each peripheral chip select with respect to the PBA contained in PACS register.

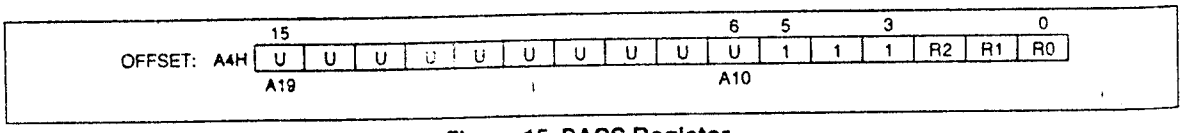


Figure 15. PACS Register

user should program bits 15–6 to correspond to desired peripheral base location. PACS bits 0–2 used to specify READY mode for $\overline{PSC0}$–$\overline{PCS3}$.

Table 10. PCS Address Ranges

PCS Line	Active between Locations
PCS0	PBA —PBA+127
PCS1	PBA+128—PBA+255
PCS2	PBA+256—PBA+383
PCS3	PBA+384—PBA+511
PCS4	PBA+512—PBA+639
PCS5	PBA+640—PBA+767
PCS6	PBA+768—PBA+895

mode of operation of the peripheral chip selects fined by the MPCS register (which is also used t the size of the mid-range memory chip-select , see Figure 16). This register is located at off-8H in the internal control block. Bit 7 is used to t the function of $\overline{PCS5}$ and $\overline{PCS6}$, while bit 6 is to select whether the peripheral chip selects apped into memory or I/O space. Table 11 ibes the programming of these bits. After reset, ontents of both the MPCS and the PACS regis-re undefined, however none of the PCS lines active until both of the MPCS and PACS reg-are accessed.

Table 11. MS, EX Programming Values

Description
1 = Peripherals mapped into memory space.
0 = Peripherals mapped into I/O space.
0 = 5 $\overline{PCS}$ lines. A1, A2 provided.
1 = 7 $\overline{PCS}$ lines. A1, A2 are not provided.

bits 0–2 are used to specify READY mode for -$\overline{PCS6}$ as outlined below.

DY Generation Logic

)186 can generate a "READY" signal internal-ach of the memory or peripheral $\overline{CS}$ lines. The r of WAIT states to be inserted for each pe-l or memory is programmable to provide 0–3 ates for all accesses to the area for which the lect is active. In addition, the 80186 may be nmed to either ignore external READY for ip-select range individually or to factor exter-ADY with the integrated ready generator.

control consists of 3 bits for each $\overline{CS}$ line or f lines generated by the 80186. The interpre-f the ready bits is shown in Table 12.

Table 12. READY Bits Programming

R2	R1	R0	Number of WAIT States Generated
0	0	0	0 wait states, external RDY also used.
0	0	1	1 wait state inserted, external RDY also used.
0	1	0	2 wait states inserted, external RDY also used.
0	1	1	3 wait states inserted, external RDY also used.
1	0	0	0 wait states, external RDY ignored.
1	0	1	1 wait state inserted, external RDY ignored.
1	1	0	2 wait states inserted, external RDY ignored.
1	1	1	3 wait states inserted, external RDY ignored.

The internal ready generator operates in parallel with external READY, not in series if the external READY is used (R2 = 0). This means, for example, if the internal generator is set to insert two wait states, but activity on the external READY lines will insert four wait states, the processor will only insert four wait states, not six. This is because the two wait states generated by the internal generator overlapped the first two wait states generated by the external ready signal. Note that the external ARDY and SRDY lines are always ignored during cycles accessing internal peripherals.

R2–R0 of each control word specifies the READY mode for the corresponding block, with the exception of the peripheral chip selects: R2–R0 of PACS set the $\overline{PCS0}$–3 READY mode, R2–R0 of MPCS set the $\overline{PCS4}$–6 READY mode.

Chip Select/Ready Logic and Reset

Upon reset, the Chip-Select/Ready Logic will perform the following actions:

- All chip-select outputs will be driven HIGH.
- Upon leaving RESET, the $\overline{UCS}$ line will be programmed to provide chip selects to a 1K block with the accompanying READY control bits set at 011 to allow the maximum number of internal wait states in conjunction with external Ready consideration (i.e., UMCS resets to FFFBH).
- No other chip select or READY control registers have any predefined values after RESET. They will not become active until the CPU accesses their control registers. Both the PACS and MPCS registers must be accessed before the $\overline{PCS}$ lines will become active.

OFFSET: A8H	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	1	M6	M5	M4	M3	M2	M1	M0	EX	MS	1	1	1	R2	R1	R0

Figure 16. MPCS Register

DMA CHANNELS

The 80186 DMA controller provides two independent high-speed DMA channels. Data transfers can occur between memory and I/O spaces (e.g., Memory to I/O) or within the same space (e.g., Memory to Memory or I/O to I/O). Data can be transferred either in bytes (8 bits) or in words (16 bits) to or from even or odd addresses. Each DMA channel maintains both a 20-bit source and destination pointer which can be optionally incremented or decremented after each data transfer (by one or two depending on byte or word transfers). Each data transfer consumes 2 bus cycles (a minimum of 8 clocks), one cycle to fetch data and the other to store data. This provides a maximum data transfer rate of one Mword/sec or 2 MBytes/sec.

DMA Operation

Each channel has six registers in the control block which define each channel's specific operation. The control registers consist of a 20-bit Source pointer (2 words), a 20-bit destination pointer (2 words), a 16-bit Transfer Counter, and a 16-bit Control Word. The format of the DMA Control Blocks is shown in Table 13. The Transfer Count Register (TC) specifies the number of DMA transfers to be performed. Up to 64K byte or word transfers can be performed with automatic termination. The Control Word defines the channel's operation (see Figure 18). All registers may be modified or altered during any DMA activity. Any changes made to these registers will be reflected immediately in DMA operation.

Table 13. DMA Control Block Format

Register Name	Register Address	
	Ch. 0	Ch. 1
Control Word	CAH	DAH
Transfer Count	C8H	D8H
Destination Pointer (upper 4 bits)	C6H	D6H
Destination Pointer	C4H	D4H
Source Pointer (upper 4 bits)	C2H	D2H
Source Pointer	C0H	D0H

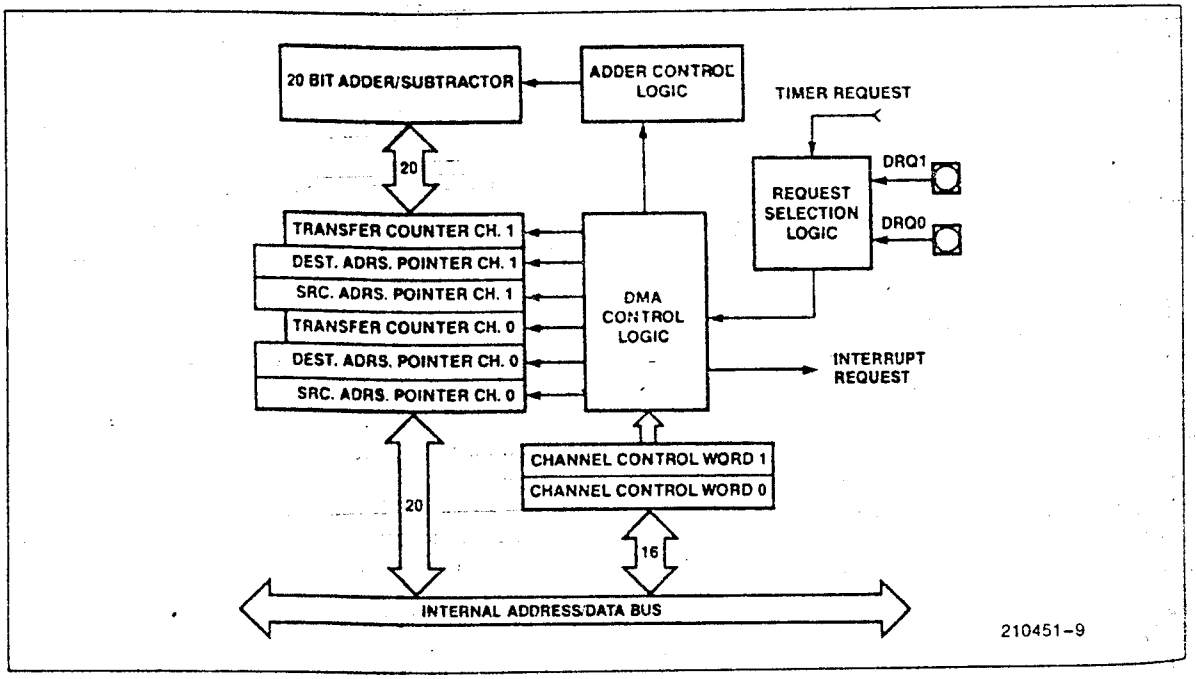


Figure 17. DMA Unit Block Diagram

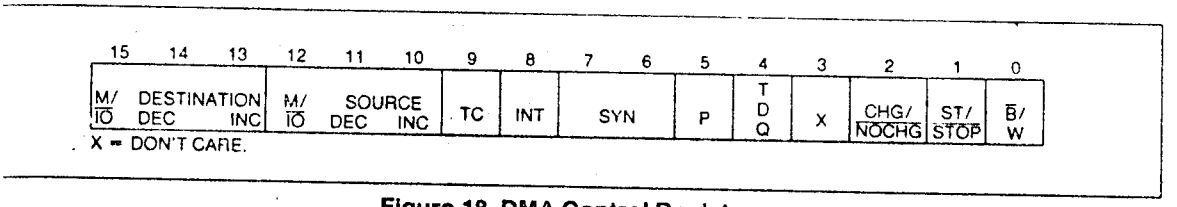


Figure 18. DMA Control Register

MA Channel Control Word Register

ch DMA Channel Control Word determines the de of operation for the particular 81086 DMA nnel. This register specifies:

the mode of synchronization;

whether bytes or words will be transferred;

whether interrupts will be generated after the last ransfer;

whether DMA activity will cease after a programmed number of DMA cycles;

he relative priority of the DMA channel with respect to the other DMA channel;

whether the source pointer will be incremented, decremented, or maintained constant after each ransfer;

whether the source pointer addresses memory or /O space;

whether the destination pointer will be incremented, decremented, or maintained constant after ach transfer; and

whether the destination pointer will address nemory or I/O space.

DMA channel control registers may be changed e the channel is operating. However, any changade during operation will affect the current DMA sfer.

A Control Word Bit Descriptions

:	Byte/Word (0/1) Transfers.
STOP:	Start/stop (1/0) Channel.
/NOCHG:	Change/Do not change (1/0) ST/STOP bit. If this bit is set when writing to the control word, the ST/STOP bit will be programmed by the write to the control word. If this bit is cleared when writing the control word, the ST/STOP bit will not be altered. This bit is not stored; it will always be a 0 on read.
	Enable Interrupts to CPU on Transfer Count termination.
TC:	If set, DMA will terminate when the contents of the Transfer Count register reach zero. The ST/STOP bit will also be reset at this point if TC is set. If this bit is cleared, the DMA unit will decrement the transfer count register for each DMA cycle, but the DMA transfer will not stop when the contents of the TC register reach zero.
SYN (2 bits)	00 No synchronization. NOTE: The ST bit will be cleared automatically when the contents of the TC register reach zero regardless of the state of the TC bit.
	01 Source synchronization.
	10 Destination synchronization.
	11 Unused.
SOURCE:INC	Increment source pointer by 1 or 2 (depends on B/W) after each transfer.
M/IO	Source pointer is in M/IO space (1/0).
DEC	Decrement source pointer by 1 or 2 (depends on B/W) after each transfer.
DEST: INC	Increment destination pointer by 1 or 2 (B/W) after each transfer.
M/IO	Destination pointer is in M/IO space (1/0).
DEC	Decrement destination pointer by 1 or 2 (depending on B/W) after each transfer.
P	Channel priority—relative to other channel.
	0 low priority.
	1 high priority.
	Channels will alternate cycles if both set at same priority level.
TDRQ	0: Disable DMA requests from timer 2.
	1: Enable DMA requests from timer 2.
Bit 3	Bit 3 is not used.

If both INC and DEC are specified for the same pointer, the pointer will remain constant after each cycle.

DMA Destination and Source Pointer Registers

Each DMA channel maintains a 20-bit source and a 20-bit destination pointer. Each of these pointers takes up two full 16-bit registers in the peripheral control block. The lower four bits of the upper register contain the upper four bits of the 20-bit physical address (see Figure 18a). These pointers may be individually incremented or decremented after each transfer. If word transfers are performed the pointer is incremented or decremented by two. Each pointer may point into either memory or I/O space. Since the DMA channels can perform transfers to or from odd addresses, there is no restriction on values for the pointer registers. Higher transfer rates can be obtained if all word transfers are performed to even addresses, since this will allow data to be accessed in a single memory access.

DMA Transfer Count Register

Each DMA channel maintains a 16-bit transfer count register (TC). This register is decremented after every DMA cycle, regardless of the state of the TC bit in the DMA Control Register. If the TC bit in the DMA control word is set or unsynchronized transfers are programmed, however, DMA activity will terminate when the transfer count register reaches zero.

DMA Requests

Data transfers may be either source or destination synchronized, that is either the source of the data or the destination of the data may request the data transfer. In addition, DMA transfers may be unsynchronized; that is, the transfer will take place continually until the correct number of transfers has occurred. When source or unsynchronized transfers are performed, the DMA channel may begin another transfer immediately after the end of a previous DMA transfer. This allows a complete transfer to take place every 2 bus cycles or eight clock cycles (assuming no wait states). No prefetching occurs when destination synchronization is performed, however. Data will not be fetched from the source address until the destination device signals that it is ready to receive it. When destination synchronized transfers are requested, the DMA controller will relinquish control of the bus after every transfer. If no other bus activity is initiated, another DMA cycle will begin after two processor clocks. This is done to allow the destination device time to remove its request if another transfer is not desired. Since the DMA controller will relinquish the bus the CPU can initiate a bus cycle. As a result, a complete bus cycle will often be inserted between destination synchronized transfers. These lead to the maximum DMA transfer rates shown in Table 14.

Table 14. Maximum DMA Transfer Rates

Type of Synchronization Selected	CPU Running	CPU Halted
Unsynchronized	2MBytes/sec	2MBytes/sec
Source Synch	2MBytes/sec	2MBytes/sec
Destination Synch	1.3MBytes/sec	1.3MByte/sec

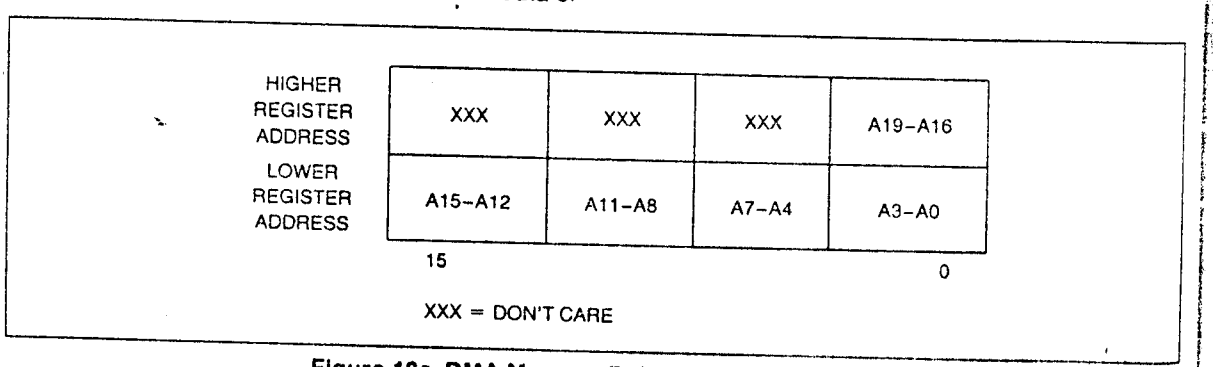


Figure 18a. DMA Memory Pointer Register Format

Timer Operation

The timers are controlled by 11 16-bit registers in the internal peripheral control block. The configuration of these registers is shown in Table 15. The count register contains the current value of the timer. It can be read or written at any time independent of whether the timer is running or not. The value of this register will be incremented for each timer event. Each of the timers is equipped with a MAX COUNT register, which defines the maximum count the timer will reach. After reaching the MAX COUNT register value, the timer count value will reset to zero during that same clock, i.e., the maximum count value is never stored in the count register itself. Timers 0 and 1 are, in addition, equipped with a second MAX COUNT register, which enables the timers to alternate their count between two different MAX COUNT values programmed by the user. If a single MAX COUNT register is used, the timer output pin will switch LOW for a single clock, 1 clock after the maximum count value has been reached. In the dual MAX COUNT register mode, the output pin will indicate which MAX COUNT register is currently in use, thus allowing nearly complete freedom in selecting waveform duty cycles. For the timers with two MAX COUNT registers, the RIU bit in the control register determines which is used for the comparison.

Each timer gets serviced every fourth CPU-clock cycle, and thus can operate at speeds up to one-quarter the internal clock frequency (one-eighth the crystal rate). External clocking of the timers may be done at up to a rate of one-quarter of the internal CPU-clock rate (2 MHz for an 8 MHz CPU clock). Due to internal synchronization and pipelining of the timer circuitry, a timer output may take up to 6 clocks to respond to any individual clock or gate input.

Since the count registers and the maximum c registers are all 16 bits wide, 16 bits of resolutio provided. Any Read or Write access to the timer add one wait state to the minimum four-clock cycle, however. This is needed to synchronize coordinate the internal data flows between the i nal timers and the internal bus.

The timers have several programmable options

- All three timers can be set to halt or continu a terminal count.
- Timers 0 and 1 can select between internal external clocks, alternate between MAX CO registers and be set to retrigger on exte events.
- The timers may be programmed to cause ar terrupt on terminal count.

These options are selectable via the timer mo control word.

Timer Mode/Control Register

The mode/control register (see Figure) allo the user to program the specific mode of operat or check the current programmed status for any the three integrated timers.

Table 15. Timer Control Block Format

Register Name	Register Offset		
	Tmr. 0	Tmr. 1	Tmr. 2
Mode/Control Word	56H	5EH	66H
Max Count B	54H	5CH	not prese
Max Count A	52H	5AH	62H
Count Register	50H	58H	60H

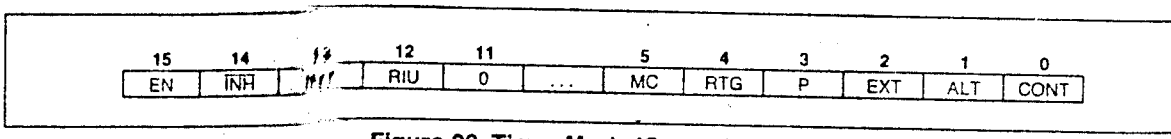


Figure 20. Timer Mode/Control Register

In-Service Register

This register can be read from or written into. It contains the in-service bit for each of the internal interrupt sources. The format for this register is shown in Figure 35. Bit positions 2 and 3 correspond to the DMA channels; positions 0, 4, and 5 correspond to the integral timers. The source's IS bit is set when the processor acknowledges its interrupt request.

Interrupt Request Register

This register indicates which internal peripherals have interrupt requests pending. The format of this register is shown in Figure 35. The interrupt request bits are set when a request arrives from an internal source, and are reset when the processor acknowledges the request.

Mask Register

The register contains a mask bit for each interrupt source. The format for this register is shown in Figure 35. If the bit in this register corresponding to a particular interrupt source is set, any interrupts from that source will be masked. These mask bits are exactly the same bits which are used in the individual control registers, i.e., changing the state of a mask bit in this register will also change the state of the mask bit in the individual interrupt control register corresponding to the bit.

Control Registers

These registers are the control words for all the internal interrupt sources. The format of these registers is shown in Figure 36. Each of the timers and both of the DMA channels have their own Control Register.

The bits of the Control Registers are encoded as follows:

pr_x: 3-bit encoded field indicating a priority level for the source; note that each source must be programmed at specified levels.

msk: mask bit for the priority level indicated by pr_x bits.

	OFFSET
LEVEL 5 CONTROL REGISTER (TIMER 2)	3AH
LEVEL 4 CONTROL REGISTER (TIMER 1)	38H
LEVEL 3 CONTROL REGISTER (DMA 1)	36H
LEVEL 2 CONTROL REGISTER (DMA 0)	34H
LEVEL 0 CONTROL REGISTER (TIMER 0)	32H
INTERRUPT STATUS REGISTER	30H
INTERRUPT-REQUEST REGISTER	2EH
IN-SERVICE REGISTER	2CH
PRIORITY-LEVEL MASK REGISTER	2AH
MASK REGISTER	28H
SPECIFIC EOI REGISTER	22H
INTERRUPT VECTOR REGISTER	20H

Figure 33. Interrupt Controller Registers (iRMX™ 86 Mode)

15	14	13	•	•	•	•	8	7	6	5	4	3	2	1	0
0	0	0					0	0	0	0	0	0	L2	L1	L0

Figure 34. Specific EOI Register Format

15	14	13	•	•	•	•	8	7	6	5	4	3	2	1	0
0	0	0					0	0	0	TMR2	TMR1	D1	D0	0	TMR0

Figure 35. In-Service, Interrupt Request, and Mask Register Format

rrupt Vector Register

register provides the upper five bits of the inter-vector address. The format of this register is n in Figure 37. The interrupt controller itself dos the lower three bits of the interrupt vector etermined by the priority level of the interrupt st.

ormat of the bits in this register is:

-bit field indicating the upper five bits of the ector address.

ty-Level Mask Register

egister indicates the lowest priority-level inter-hich will be serviced.

coding of the bits in this register is:

-bit encoded field indication priority-level val-ue. All levels of lower priority will be masked.

pt Status Register

gister is defined exactly as in Non-iRMX See Fig. 26.)

Interrupt Controller and Reset

Upon RESET, the interrupt controller will perform the following actions:

- All SFNM bits reset to 0, implying Fully Nested Mode.
- All PR bits in the various control registers set to 1. This places all sources at lowest priority (level 111).
- All LTM bits reset to 0, resulting in edge-sense mode.
- All Interrupt Service bits reset to 0.
- All Interrupt Request bits reset to 0.
- All MSK (Interrupt Mask) bits set to 1 (mask).
- All C (Cascade) bits reset to 0 (non-cascade).
- All PRM (Priority Mask) bits set to 1, implying no levels masked.
- Initialized to non-iRMX 86 mode.

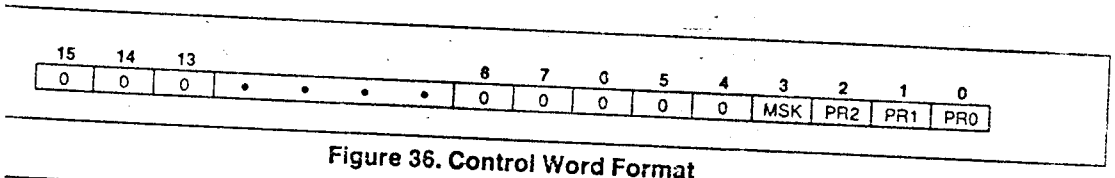


Figure 36. Control Word Format

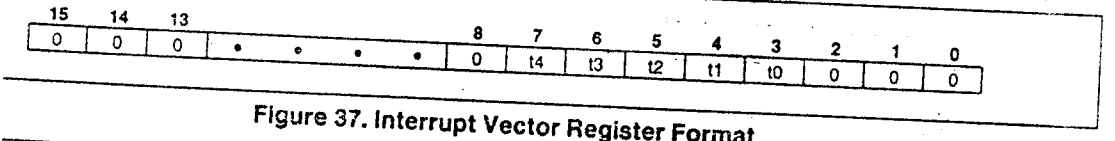


Figure 37. Interrupt Vector Register Format

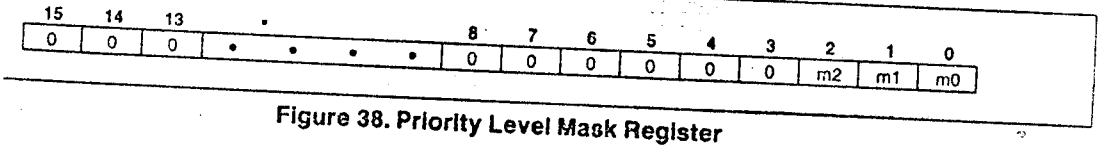


Figure 38. Priority Level Mask Register

INSTRUCTION SET SUMMARY

Function	Format	Clock Cycles	Comments
DATA TRANSFER			
MOV = Move:			
Register to Register/Memory	1000100w | mod reg r/m	2/12	
Register/memory to register	1000101w | mod reg r/m	2/9	
Immediate to register/memory	1100011w | mod 000 r/m | data | data if w = 1	12–13	8/16-bit
Immediate to register	1011w reg | data | data if w = 1	3–4	8/16-bit
Memory to accumulator	1010000w | addr-low | addr-high	9	
Accumulator to memory	1010001w | addr-low | addr-high	8	
Register/memory to segment register	10001110 | mod 0 reg r/m	2/9	
Segment register to register/memory	10001100 | mod 0 reg r/m	2/11	
PUSH = Push:			
Memory	11111111 | mod 1 1 0 r/m	16	
Register	01010 reg	10	
Segment register	000reg 110	9	
Immediate	011010s0 | data | data if s = 0	10	
PUSHA = Push All	01100000	36	
POP = Pop:			
Memory	10001111 | mod 0 0 0 r/m	20	
Register	01011 reg	10	
Segment register	000reg 111 (reg≠01)	8	
POPA = Pop All	01100001	51	
XCHG = Exchange:			
Register/memory with register	1000011w | mod reg r/m	4/17	
Register with accumulator	10010 reg	3	
IN = Input from:			
Fixed port	1110010w | port	10	
Variable port	1110110w	8	
OUT = Output to:			
Fixed port	1110011w | port	9	
Variable port	1110111w	7	
XLAT = Translate byte to AL	11010111	11	
LEA = Load EA to register	10001101 | mod reg r/m	6	
LDS = Load pointer to DS	11000101 | mod reg r/m (mod≠11)	18	
LES = Load pointer to ES	11000100 | mod reg r/m (mod≠11)	18	
LAHF = Load AH with flags	10011111	2	
SAHF = Store AH into flags	10011110	3	
PUSHF = Push flags	10011100	9	
POPF = Pop flags	10011101	8	

Shaded areas indicate instructions not available in 8086, 8088 microsystems.

INSTRUCTION SET SUMMARY (Continued)

Function	Format	Clock Cycles	Comments
DATA TRANSFER (Continued)			
SEGMENT = Segment Override:			
CS	00101110	2	
SS	00110110	2	
DS	00111110	2	
ES	00100110	2	
ARITHMETIC			
ADD = Add:			
Reg/memory with register to either	000000dw | mod reg r/m	3/10	
Immediate to register/memory	100000sw | mod 000 r/m | data | data if s w = 01	4/16	
Immediate to accumulator	0000010w | data | data if w = 1	3/4	8/16-bit
ADC = Add with carry:			
Reg/memory with register to either	000100dw | mod reg r/m	3/10	
Immediate to register/memory	100000sw | mod 010 r/m | data | data if s w = 01	4/16	
Immediate to accumulator	0001010w | data | data if w = 1	3/4	8/16-bit
INC = Increment:			
Register/memory	1111111w | mod 000 r/m	3/15	
Register	01000 reg	3	
SUB = Subtract:			
Reg/memory and register to either	001010dw | mod reg r/m	3/10	
Immediate from register/memory	100000sw | mod 101 r/m | data | data if s w = 01	4/16	
Immediate from accumulator	0010110w | data | data if w = 1	3/4	8/16-bit
SBB = Subtract with borrow:			
Reg/memory and register to either	000110dw | mod reg r/m	3/10	
Immediate from register/memory	100000sw | mod 011 r/m | data | data if s w = 01	4/16	
Immediate from accumulator	0001110w | data | data if w = 1	3/4	8/16-bit
DEC = Decrement			
Register/memory	1111111w | mod 001 r/m	3/15	
Register	01001 reg	3	
CMP = Compare:			
Register/memory with register	0011101w | mod reg r/m	3/10	
Register with register/memory	0011100w | mod reg r/m	3/10	
Immediate with register/memory	100000sw | mod 111 r/m | data | data if s w = 01	3/10	
Immediate with accumulator	0011110w | data | data if w = 1	3/4	8/16-bit
NEG = Change sign	1111011w | mod 011 r/m	3	
AAA = ASCII adjust for add	00110111	8	
DAA = Decimal adjust for add	00100111	4	
AAS = ASCII adjust for subtract	00111111	7	
DAS = Decimal adjust for subtract	00101111	4	
MUL = Multiply (unsigned):	1111011w | mod 100 r/m		
Register-Byte		26–28	
Register-Word		35–37	
Memory-Byte		32–34	
Memory-Word		41–43	

Shaded areas indicate instructions not available in 8086, 8088 microsystems.

INSTRUCTION SET SUMMARY (Continued)

Function	Format	Clock Cycles	Comments
ARITHMETIC (Continued)			
IMUL = Integer multiply (signed):	1111011w | mod101 r/m		
Register-Byte		25–28	
Register-Word		34–37	
Memory-Byte		31–34	
Memory-Word		40–43	
IMUL = Integer immediate multiply (signed)	011010s1 | mod reg r/m | data | data if s=0	22–25/ 29–32	
DIV = Divide (unsigned):	1111011w | mod110 r/m		
Register-Byte		29	
Register-Word		38	
Memory-Byte		35	
Memory-Word		44	
IDIV = Integer divide (signed):	1111011w | mod111 r/m		
Register-Byte		44–52	
Register-Word		53–61	
Memory-Byte		50–58	
Memory-Word		59–67	
AAM = ASCII adjust for multiply	11010100 | 00001010	19	
AAD = ASCII adjust for divide	11010101 | 00001010	15	
CBW = Convert byte to word	10011000	2	
CWD = Convert word to double word	10011001	4	
LOGIC			
Shift/Rotate Instructions:			
Register/Memory by 1	1101000w | mod TTT r/m	2/15	
Register/Memory by CL	1101001w | mod TTT r/m	5+n/17+n	
Register/Memory by Count	1100000w | mod TTT r/m | count	5+n/17+n	
	TTT Instruction 000 ROL 001 ROR 010 RCL 011 RCR 100 SHL/SAL 101 SHR 111 SAR		
AND = And:			
Reg/memory and register to either	001000dw | mod reg r/m	3/10	
Immediate to register/memory	1000000w | mod100 r/m | data | data if w=1	4/16	
Immediate to accumulator	0010010w | data | data if w=1	3/4	8/16-bit
TEST = And function to flags, no result:			
Register/memory and register	1000010w | mod reg r/m	3/10	
Immediate data and register/memory	1111011w | mod000 r/m | data | data if w=1	4/10	
Immediate data and accumulator	1010100w | data | data if w=1	3/4	8/16-bit
OR = Or:			
Reg/memory and register to either	000010dw | mod reg r/m	3/10	
Immediate to register/memory	1000000w | mod001 r/m | data | data if w=1	4/16	
Immediate to accumulator	0000110w | data | data if w=1	3/4	8/16-bit

Shaded areas indicate instructions not available in 8086, 8088 microsystems.

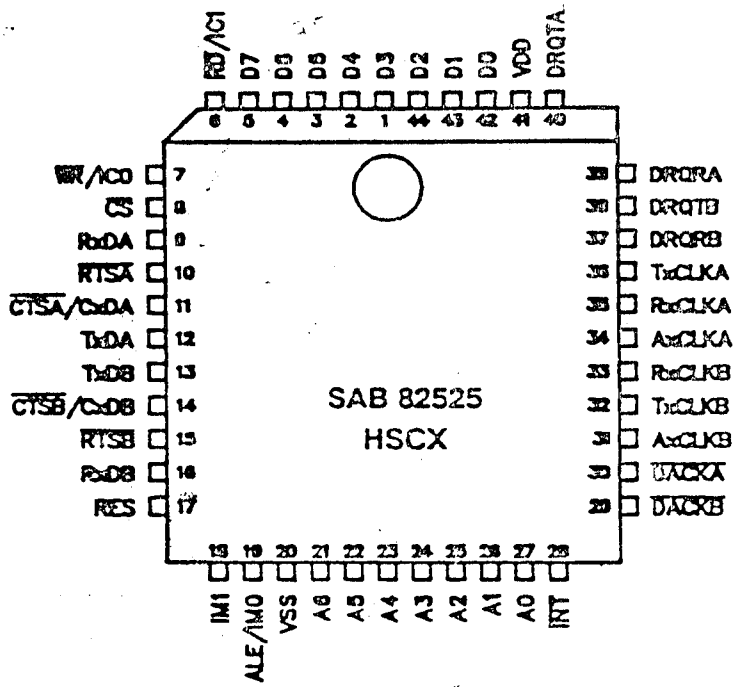
INSTRUCTION SET SUMMARY (Continued)

Function	Format	Clock Cycles	Comments
PROCESSOR CONTROL			
CLC = Clear carry	11111000	2	
CMC = Complement carry	11110101	2	
STC = Set carry	11111001	2	
CLD = Clear direction	11111100	2	
STD = Set direction	11111101	2	
CLI = Clear interrupt	11111010	2	
STI = Set interrupt	11111011	2	
HLT = Halt	11110100	2	
WAIT = Wait	10011011	6	if $\overline{test}$ = 0
LOCK = Bus lock prefix	11110000	2	
ESC = Processor Extension Escape	11011TTT mod LLL r/m (TTT LLL are opcode to processor extension)	6	

Shaded areas indicate instructions not available in 8086, 8088 microsystems.

1.3. PIN CONFIGURATION AND FUNCTIONS

1.3.1 PLCC package 44 pins



Symbol	Pin	Typ	Function
DO D1 D2 D3 D4 D5 D6 D7	42 43 44 1 2 3 4 5	I / O	DATA BUS The Data Bus lines are bi-directional three-state lines which interface with the system's Data Bus. These lines carry data and command/status to and from the HSCX.

Figure 1.2: SAB 82525 Pin Configuration

Symbol	Pin	Typ	Function
$\overline{RD}$ / IC1	6	I	READ, Intel Bus Mode, IM1 connected to low This signal indicates a read operation. When the HSCX is selected via CS the READ signal enables the bus drivers to put data from an internal register adressed via A0-A6 on the Data Bus. When the HSCX is selected for DMA transfers via DACK, the RD signal enables the bus driver to put data from the respective Receive FIFO on the Data Bus. Inputs to A0-A6 are ignored. INPUT CONTROL 1, Motorola Bus Mode, IM1 connected to high If Motorola Bus Mode has been selected this pin serves either as E = Enable, active high (IM0 tied to low) or DS = Data Strobe, active low (IM0 tied to high) input (depending on the selection via IM0) to control Read/Write operations.
$\overline{WR}$ / IC0	7	I	WRITE, Intel Bus Mode This signal indicates a write operation. When CS is active the HSCX loads an internal register with data provided via the Data Bus. When DACK is active for DMA transfers the HSCX loads data from the Data Bus on the top of the respective transmit FIFO. INPUT CONTROL 0, Motorola Bus Mode In Motorola Bus Mode, this pin serves as the R/W input to distinguish between Read or Write operations.
$\overline{CS}$	8	I	CHIP SELECT A low signal selects the HSCX for a Read/Write operation.
RXDA RXDB	9 16	I	RECEIVE DATA (Channel A/Channel B) Serial data is received on these pins at standard TTL or CMOS levels.

Symbol	Pin	Typ	Function
$\overline{\text{RTSA}}$ $\overline{\text{RTSB}}$	10 15	O	REQUEST TO SEND (Channel A/Channel B) When the RTS bit in the MODE register is set, the RTS signal goes low. When the RTS is reset, the signal goes high if the transmitter has finished and there is no further request for a transmission. In a bus configuration, this pin can be programmed via CCR2 to: - go low during the actual transmission of a frame shifted by one clock period, excluding collision bits. - go low during the reception of a data frame. - stay always high (RTS disabled).
$\overline{\text{CTSA}}$ / CXDA $\overline{\text{CTSB}}$ / CXDB	11 14	I	CLEAR TO SEND (Channel A/Channel B) A low on the CTS inputs enables the respective transmitter. Additionally, an interrupt may be issued if a state transition occurs at the CTS pin (programmable feature). If no "Clear To Send" function is required, the CTS inputs can be connected directly to GND. COLLISION DATA (Channel A/Channel B) In a bus configuration, the external serial bus must be connected to the respective CxD pin for collision detection.
TXDA TXDB	12 13	O	TRANSMIT DATA (channel A/Channel B) Transmit Data is shifted out via these pins at standard TTL or CMOS levels. These pins can be programmed to work either as push-pull, or open drain outputs supporting bus configurations.
RES	17	I	RESET A high signal on this input forces the HSCX into the reset state. The HSCX is in power-up mode during reset and in power- down mode after reset. The minimum pulse which is 1.8 micro seconds.

Symbol	Pin	Typ	Function
IM 1	18	I	INPUT MODE 1 Connecting this pin to either VSS or VDD the bus interface can be adepted to either SIEMENS/INTEL or Motorola environment. IM1 = LOW: Intel Bus Mode IM1 = HIGH: Motorola Bus Mode
ALE / IM0	19	I	ADDRESS LATCH ENABLE (Intel Bus Mode) A high on this line indicates an address on the external address/data bus, which will select one of the HSCX's internal registers. The address is latched by the HSCX with the falling edge of ALE. This allows the HSCX to be directly connected to a CPU with multiplexed Address/Data Bus compatible to SAB 82520 HSCC. The Address Input Pins A0-A6 must be externally connected to the Data Bus Pins (D0-D6 for 8-bit CPU's, D1-D7 for 16-bit CPU's, i.e. multiply all internal register addresses by 2). INPUT MODE 0, Motorola Bus Mode In Motorola Bus Mode, the level at this pin determines the function of the IC1 pin (see description of pin 6).
V SS	20	I	GROUND (0V)
A0 A1 A2 A3 A4 A5 A6	27 26 25 24 23 22 21	I	ADDRESS BUS These inputs interface with seven bits of the System's Address Bus to select one of the internal registers for read or write. They are usually connected at A0-A6 in 8-Bit systems or at A1- A7 in 16-Bit systems.

Symbol	Pin	Typ	Function
$\overline{INT}$	28	O	INTERRUPT REQUEST The signal is activated, when the HSCX requests an interrupt. The CPU may determine the particular source and cause of the interrupt by reading the HSCX's interrupt status registers. (ISTA, EXIR). INT is an open drain output, thus the interrupt requests outputs of several HSCX's can be connected to one interrupt input in a "wired-or" combination. This pin must be connected to a pull up register.
$\overline{DACKA}$ $\overline{DACKB}$	30 29	I	DMA ACKNOWLEDGE (Channel A/Channel B) When low, this input signal from the DMA controller notifies the HSCX, that the requested DMA cycle controlled via DRQxx (pins 37-40) is in progress, i.e. the DMA controller has achieved bus mastership from the CPU and will start data transfer cycles (either read or write). Together with RD, if DMA has been requested from the receiver, or with WR, if DMA has been requested from the transmitter, this input works like CS to enable a data byte to be read from or written to the top of the Receive or Transmit FIFO of the specified channel. If DACKn is active, the input to pins A0-A6 is ignored and the FIFOs are implicitly selected. If the DACKn signals are not used, these pins must be connected to VDD!
AxCLKA AxCLKB	34 31	I	ALTERNATIVE CLOCK (Channel A/Channel B) These pins realize several input functions. Depending on the selected clock mode, they may supply either a - CD (=Carrier Detect) Modem Control or General Purpose Input. This pin can be programmed to functions as receiver enable if the "auto start" feature is selected (CAS bit in XBCH set). The state at this pin can be read from VSTR register. - or a receive strobe signal (clock mode 1) - or a frame synchronisation signal in timeslot oriented operation mode (clock mode 5) - or, together with RxCLK, a crystal connection for the internal oscillator (clock mode 4,6,7)

Symbol	Pin	Typ	Function
TxCLKA TxCLKB	36 32	I / O	TRANSMIT CLOCK (Channel A/Channel B) The functions of these pins depend on the programmed clock mode, provided that the TSS bit in the CCR2 register is reset. Programmed as inputs (if the TIO bit in CCR2 is reset), they may supply either - the transmit clock for the respective channel (clock mode 0,2,6), - or a transmit strobe signal (clock mode 1). Programmed as outputs (if the TIO bit in CCR2 is set), the TxCLK pins supply either the - transmit clock of the respective channel which is generated either * from the baud rate generator (clock mode 2,6; TSS bit in CCR2 set), * or from the DPLL circuit (clock mode 3,7), * or from the cristal oscillator (clock mode 4) - or a tristate control signal indicating the programmed transmit time slot (clock mode 5).
RxCLKA RxCLKB	35 33	I	RECEIVE CLOCK (Channel A/Channel B) The functions of these pins also depend on the programmed clock mode. In each channel, RxCLK may supply either - the receive clock (clock mode 0) - or the receive and transmit clock (clock mode 1,5) - or the clock for the baud rate generator (clock mode 2,3), - or a crystal connection for the internal oscillator (clock mode 4,6,7, RxCLKA/B together with AxCLKA)
DRQRA DRQRB	39 37	O	DMA REQUEST RECEIVER (Channel A/Channel B) The receiver of the HSCX requests a DMA data transfer by activating this line. The DRQRn remains high as long as the Receive FIFO requires data transfers, thus always blocks of data (32,16,8, or 4 bytes) are transfered. DRQRn is deactivated immediately following the falling edge of the last read cycle.

Symbol	Pin	Typ	Function
DRQTA DRQTB	40 38	O	DMA REQUEST TRANSMITTER (Channel A/Channel B) The transmitter of the HSCX requests a DMA data transfer by activating this line. The DRQTn remains high as long as the Transmit FIFO requires data transfers. The amount of data bytes to be transfered from system memory to the HSCX (= byte count) must be written first to the XBCH, XBCL registers. Always blocks of data (n * 32 bytes + REST, n = 0,1,....) are transfered till the Byte Count is reached. DRQTn is deactivated immediately following the falling edge of the last WR cycle.
V_{DD}	41	I	POWER +5V power supply.

1.4. SYSTEM INTEGRATION

1.4.1 General Aspects

Figure 1.3 gives a general overview of the system integration of HSCX.

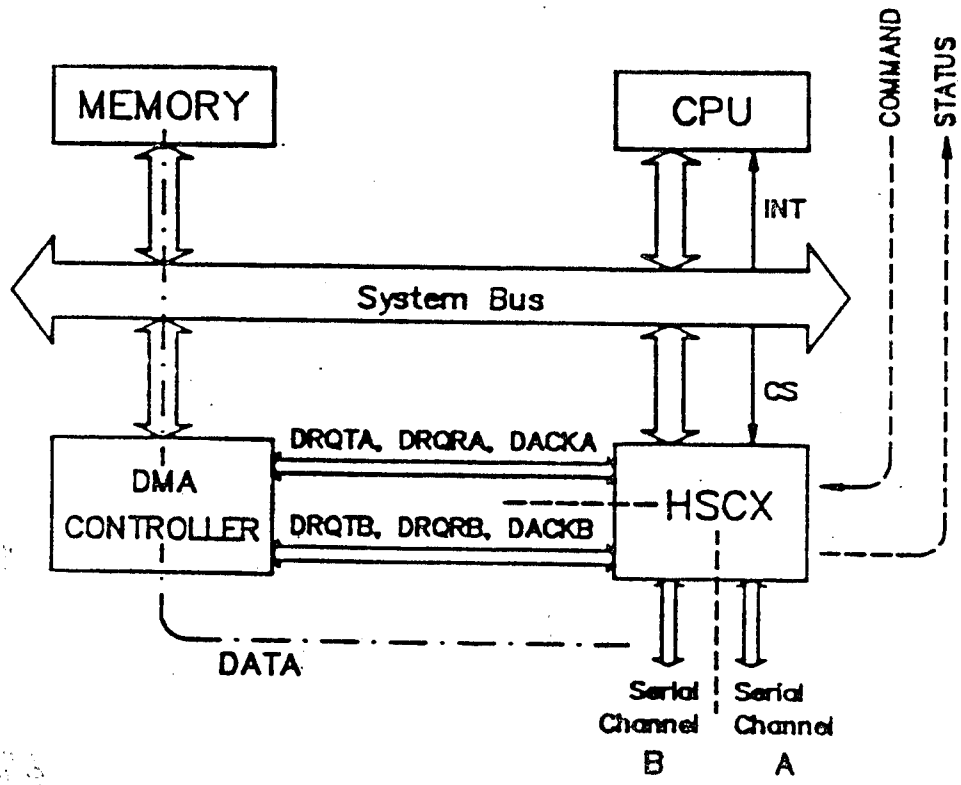


Figure 1.3: General System Integration of HSCX

The HSCX's bus interface consists of an 8-bit bidirectional Data bus (D0 - D7), seven Address Line inputs (A0 - A6), three control inputs (RD / DS, WR / R/W,CS), one interrupt request output (INT) and a 4-channel DMA interface (DRQTA, DRQRA, DACKA, DRQTB, DRQRB, DACKB). Mode input pins (strapping options) allow the bus interface to be configured for either SIEMENS/INTEL or Motorola environment.

Generally, there are two types of transfers occuring via the system bus:
- Command/Status transfers, which are always controlled by the CPU. The CPU sets the operation mode (Initialization), controls function sequences and gets status information by writing or reading the HSCX's registers (via CS, WR or RD, and register address via A0-A6).
- Data Transfers, which are effectively performed by DMA without CPU interaction using the HSCX's DMA interface (DMA Mode). Optionally, interrupt controlled data transfer can be done by the CPU (Interrupt Mode).

1.4.2.3 HSCX with SAB 80186 Microprocessor and SAB 82258 Advanced DMA Controller (ADMA)

In applications, where two high-speed channels are required, a 16-bit system with 80186 CPU and 82258 ADMA is suitable. This is shown in figure 1.6.

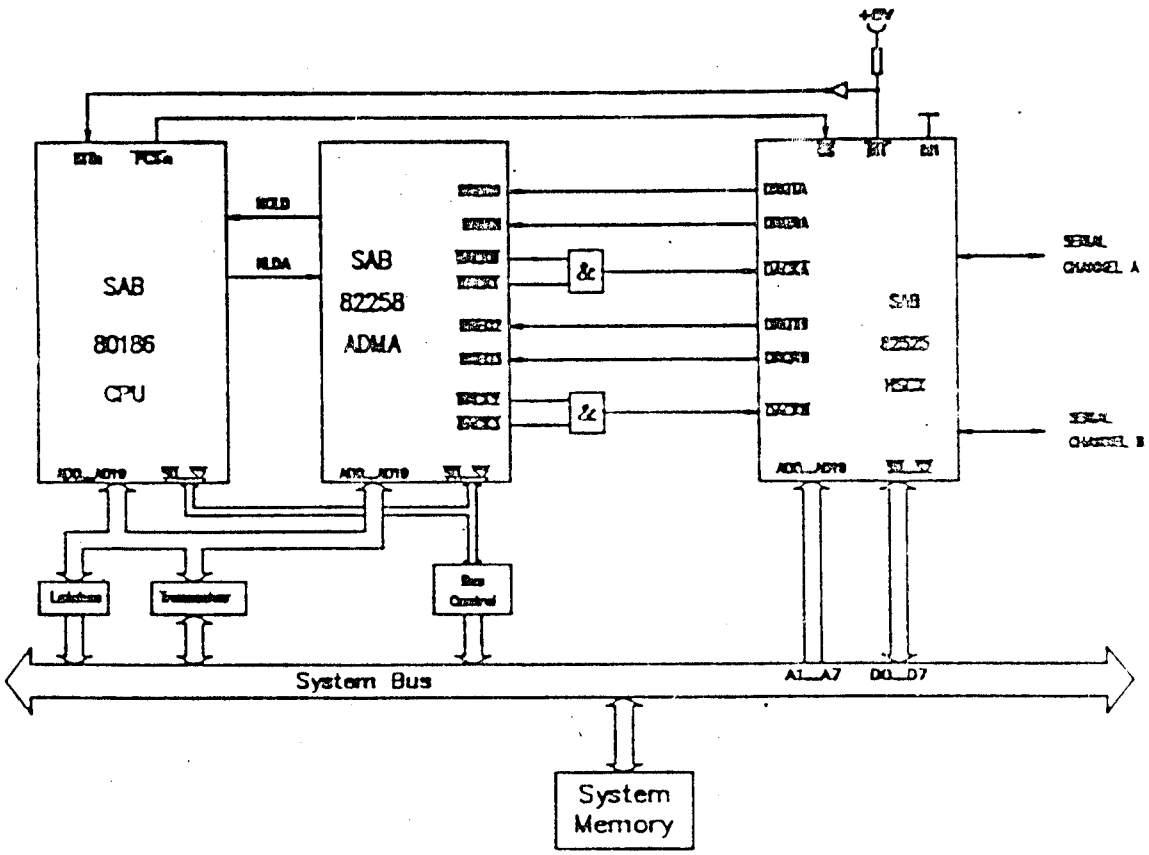


Figure 1.6: HSCX with 80186 CPU / 82258 ADMA

The four Selector Channels of ADMA are used for serving the four DMA Request sources of HSCX, allowing very high data rates at both the system bus and the serial channels.
Another big advantage of the ADMA is it's Data Chaining feature, providing an optimized memory management for receive and transmit data. Recording the HSCX, a linked chain of 32 byte deep buffers can be set up, which are subsequently filled with the contents of the HSCX's FIFOS during reception. Not used buffers can be saved and linked to another buffer chain reserved for the reception of the next frame.
As a result, it's not necessary to reserve a very large space in system memory, determined by the

maximum frame length of every received frame.
In this example, the ADMA works directly at the CPU's local bus and shares the same bus interface logic (Address Latches, Transceivers, Bus Controller) with the 80186. Since one DMA Acknowledge line is provided for each DMA Request, two $\overline{\text{DACK}}$ outputs must be anded together for input to the HSCX.
The HSCX's Data lines are connected to the lower half of the system data bus (D0...D7) and the Address lines to A1...A7, thus (from the CPU's point of view) all internal register addresses must be multiplied by two (even register addresses only).
e.g. CMDR register: HSCX Address 61H < = > System Address C2H

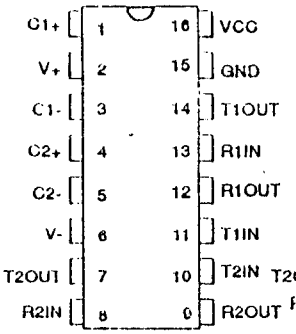
DALLAS SEMICONDUCTOR

DS1228
+5V Powered Dual RS-232 Transmitter/Receiver

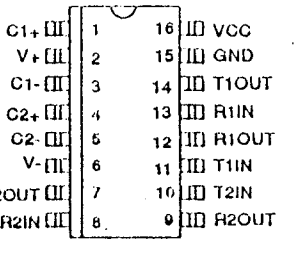
FEATURES

- Operates from a single 5V power supply
- Two drivers and two receivers
- Meets all EIA RS-232-C specifications
- On-board voltage doubler
- On-board voltage inverter
- ± 30V input levels
- ± 9V output levels with + 5V supply
- Low-power CMOS
- Pin-compatible with the MAX 232
- Optional 16-pin SOIC surface mount package

PIN ASSIGNMENT



16-Pin DIP (300 MIL)
See Mech. Drawing
Sect. 16, Pg. 1



16-Pin SOIC (300 MIL)
See Mech. Drawing
Sect. 16, Pg. 6

PIN DESCRIPTION

C1+, C1	Capacitor 1 Connections
C2+, C2	Capacitor 2 Connections
V+, V-	± 10 Volts
T1IN, T2IN	Transmitter In
T1OUT, T2OUT	Transmitter Out
R1IN, R2IN	Receiver In
R1OUT, R2OUT	Receiver Out
V_{CC}	+5 Volts
GND	Ground

DESCRIPTION

The DS1228 is a dual RS-232-C Receiver/Transmitter that meets all EIA specifications while operating from a single, +5 volt supply. The DS1228 has two internal charge pumps. One of the charge pumps is used to generate +10 volts. The other is used to generate -10 volts. The DS1228 also contains four level translators. Two of the level translators are RS-232 transmitters which convert TTL/CMOS inputs into ± 9V RS-232 outputs. The other two level translators are capable of operating with up to ±30 V inputs. The DS1228 is suitable for all RS-232 communications and is particularly valuable where higher voltage power supplies for RS-232 drivers are not available. The power supply section of the DS1228 supplies ± 10 volts from the V_{CC} input.

See the DS1229 data sheet for electrical specifications and operation.

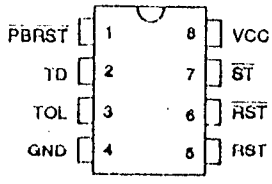
DALLAS SEMICONDUCTOR

DS123
MicroMonitor Chi

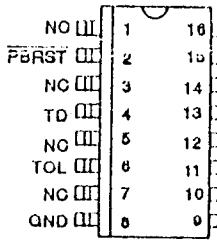
FEATURES

- Halts and restarts an out-of-control microprocessor
- Holds microprocessor in check during power transients
- Automatically restarts microprocessor after power failure
- Monitors pushbutton for external override
- Accurate 5% or 10% microprocessor power supply monitoring
- Eliminates the need for discrete components
- Space-saving, 8-pin mini-DIP
- Optional 16-pin SOIC surface mount package
- Industrial temperature -40°C to +85°C available, designated N

PIN ASSIGNMENT



DS1232 8-Pin DIP
(300 Mil)
See Mech. Drawing
Sect. 16, Pg. 1



DS1232S 16-Pin SOIC
(300 Mil)
See Mech. Drawing
Sect. 16, Pg. 6

PIN DESCRIPTION

$\overline{PBRST}$	- Pushbutton Reset Input
TD	- Time Delay Set
TOL	- Selects 5% or 10% V_{CC} Detect
GND	- Ground
RST	- Reset Output (Active High)
$\overline{RST}$	- Reset Output (Active Low, Open Drain
$\overline{ST}$	- Strobe Input
V_{CC}	- +5 Volt Power
NC	- No Connections

DESCRIPTION

The DS1232 MicroMonitor Chip monitors three vital conditions for a microprocessor: power supply, software execution, and external override. First, a precision temperature-compensated reference and comparator circuit monitors the status of V_{CC}. When an out-of-tolerance condition occurs, an internal power fail signal is generated which forces reset to the active state. When V_{CC} returns to an in-tolerance condition, the reset signals are kept in the active state for a minimum of 250 ms to allow the power supply and processor to stabilize.

The second function the DS1232 performs is pushbutton reset control. The DS1232 debounces the pushbutton input and guarantees an active reset pulse width 250 ms minimum. The third function is a watchdog time The DS1232 has an internal timer that forces the reset signals to the active state if the strobe input is not driven low prior to time-out. The watchdog timer function can be set to operate on time-out settings of approximately 150 ms, 600 ms, and 1.2 seconds.

OPERATION – POWER MONITOR

The DS1232 detects out-of-tolerance power supply conditions and warns a processor based system of impending power failure. When V_{CC} falls below a preset level as defined by TOL (Pin 3), the V_{CC} comparator outputs the signals RST (Pin 5) and $\overline{RST}$ (Pin 6). When TOL is connected to ground, the RST and $\overline{RST}$ signals become active as V_{CC} falls below 4.75 volts. When TOL is connected to V_{CC}, the RST and $\overline{RST}$ signals become active as V_{CC} falls below 4.5 volts. The RST and $\overline{RST}$ are excellent control signals for a microprocessor, as processing is stopped at the last possible moments of valid V_{CC}. On power-up, RST and $\overline{RST}$ are kept active for a minimum of 250 ms to allow the power supply and processor to stabilize.

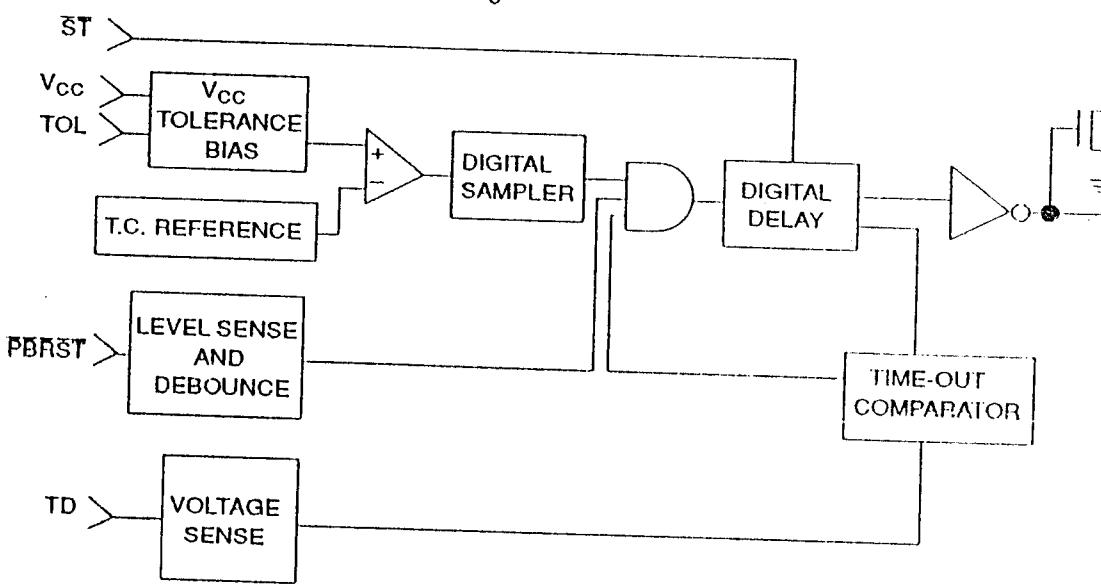
OPERATION – PUSHBUTTON RESET

The DS1232 provides an input pin for direct connection to a pushbutton (Figure 2). The pushbutton reset input requires an active low signal. Internally, this input is debounced and timed such that RST and $\overline{RST}$ signals of at least 250 ms minimum are generated. The 250 ms delay starts as the pushbutton reset input is released from low level.

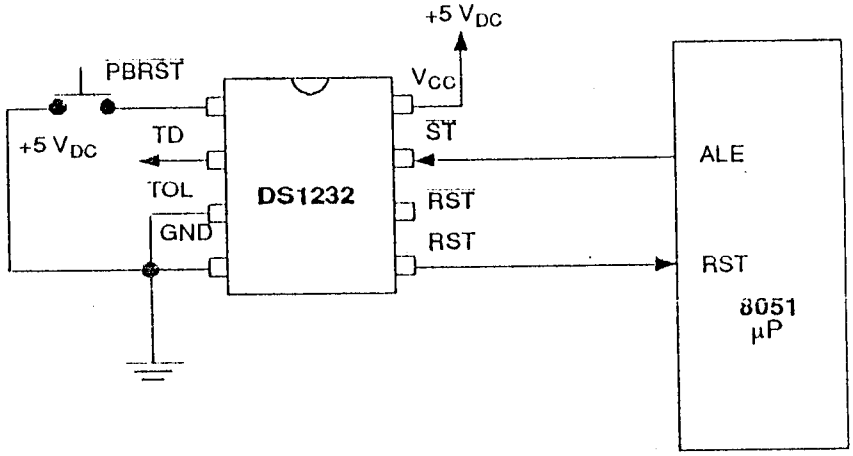
OPERATION – WATCHDOG TIMER

A watchdog timer function forces RST and $\overline{R}$ to the active state when the $\overline{ST}$ input is not stim a predetermined time period. The time perio the TD input to be typically 150 ms with TD co ground, 600 ms with TD left unconnected, an onds with TD connected to V_{CC}. The watch starts timing out from the set time period as soo and $\overline{RST}$ are inactive. If a high-to-low transiti on the $\overline{ST}$ input pin prior to time-out, the watch is reset and begins to time-out again. If the timer is allowed to time-out, then the RST and nals are driven to the active state for 250 ms The $\overline{ST}$ input can be derived from microproc dress signals, data signals, and/or contro When the microprocessor is functioning norma signals would, as a matter of routine, cause th dog to be reset prior to time-out. To guarantee watchdog timer does not time-out, a high-to-lo tion must occur at or less than the minimum Table 1. A typical circuit example is shown in

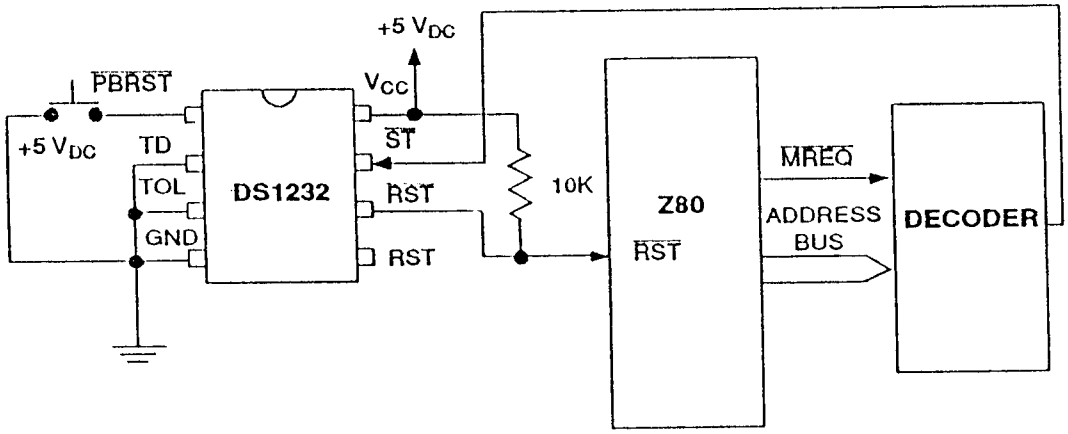
MICROMONITOR BLOCK DIAGRAM Figure 1



PUSHBUTTON RESET Figure 2



WATCHDOG TIMER Figure 3



OPERATION – POWER MONITOR

The DS1232 detects out-of-tolerance power supply conditions and warns a processor-based system of impending power failure. When V_{CC} falls below a preset level as defined by TOL (Pin 3), the V_{CC} comparator outputs the signals RST (Pin 5) and $\overline{RST}$ (Pin 6). When TOL is connected to ground, the RST and $\overline{RST}$ signals become active as V_{CC} falls below 4.75 volts. When TOL is connected to V_{CC}, the RST and $\overline{RST}$ signals become active as V_{CC} falls below 4.5 volts. The RST and $\overline{RST}$ are excellent control signals for a microprocessor, as processing is stopped at the last possible moments of valid V_{CC}. On power-up, RST and $\overline{RST}$ are kept active for a minimum of 250 ms to allow the power supply and processor to stabilize.

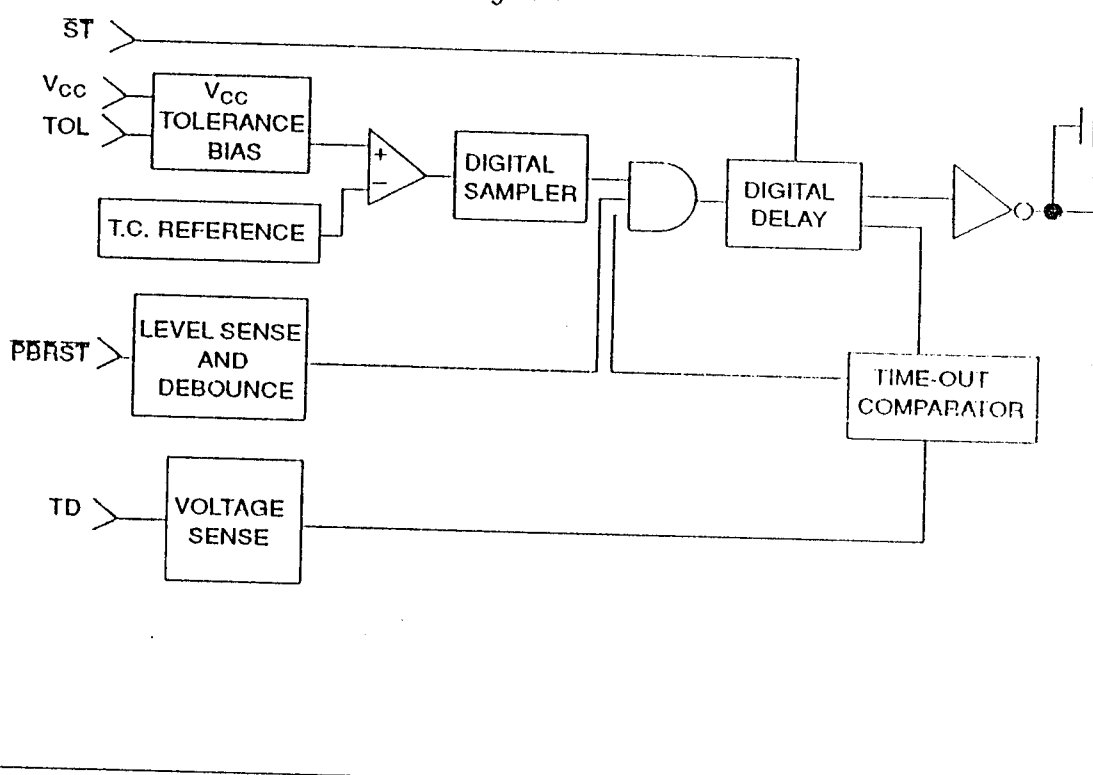
OPERATION – PUSHBUTTON RESET

The DS1232 provides an input pin for direct connection to a pushbutton (Figure 2). The pushbutton reset input requires an active low signal. Internally, this input is debounced and timed such that RST and $\overline{RST}$ signals of at least 250 ms minimum are generated. The 250 ms delay starts as the pushbutton reset input is released from low level.

OPERATION – WATCHDOG TIMER

A watchdog timer function forces RST and $\overline{RST}$ to the active state when the $\overline{ST}$ input is not stimulated within a predetermined time period. The time period is set by the TD input to be typically 150 ms with TD connected to ground, 600 ms with TD left unconnected, and 2.4 seconds with TD connected to V_{CC}. The watchdog timer starts timing out from the set time period as soon as RST and $\overline{RST}$ are inactive. If a high-to-low transition occurs on the $\overline{ST}$ input pin prior to time-out, the watchdog timer is reset and begins to time-out again. If the watchdog timer is allowed to time-out, then the RST and $\overline{RST}$ signals are driven to the active state for 250 ms. The $\overline{ST}$ input can be derived from microprocessor address signals, data signals, and/or control signals. When the microprocessor is functioning normally these signals would, as a matter of routine, cause the watchdog to be reset prior to time-out. To guarantee that the watchdog timer does not time-out, a high-to-low transition must occur at or less than the minimum specified in Table 1. A typical circuit example is shown in

MICROMONITOR BLOCK DIAGRAM Figure 1



TAL BUFFER/LINE DRIVER; 3-STATE

TURES

utput capability: bus driver
C category: MSI

IERAL DESCRIPTION

74HC/HCT244 are high-speed
te CMOS devices and are pin
patible with low power Schottky
(LSTTL). They are specified in
pliance with JEDEC standard no. 7A.

74HC/HCT244 are octal
nverting buffer/line drivers with
e outputs. The 3 state outputs are
olled by the output enable inputs
and $2\overline{OE}$. A HIGH on $n\overline{OE}$ causes
utputs to assume a high impedance
state.
"244" is identical to the "240" but
on-inverting outputs.

CTION TABLE

INPUTS		OUTPUT
)E	nA_n	nY_n
	L	L
	H	H
	X	Z

IGH voltage level
)W voltage level
n't care
gh impedance OFF-state

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay $1A_n$ to $1Y_n$; $2A_n$ to $2Y_n$	C_L = 15 pF; V_{CC} = 5 V	9	11	ns
C_I	input capacitance	[1]	3.5	3.5	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	35	35	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$1\overline{OE}$	output enable input (active LOW)
2, 4, 6, 8	$1A_0$ to $1A_3$	data inputs
3, 5, 7, 9	$2Y_0$ to $2Y_3$	bus outputs
10	GND	ground (0 V)
17, 15, 13, 11	$2A_0$ to $2A_3$	data inputs
18, 16, 14, 12	$1Y_0$ to $1Y_3$	bus outputs
19	$2\overline{OE}$	output enable input (active LOW)
20	V_{CC}	positive supply voltage

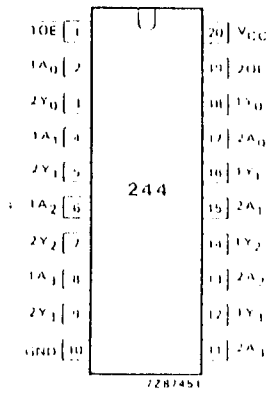


Fig. 1 Pin configuration.

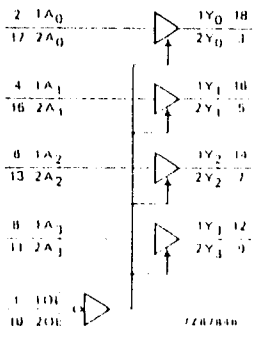


Fig. 2 Logic symbol.

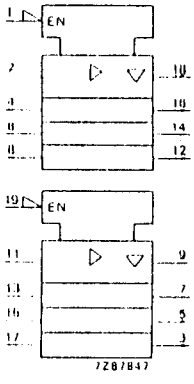


Fig. 3 IEC logic symbol.

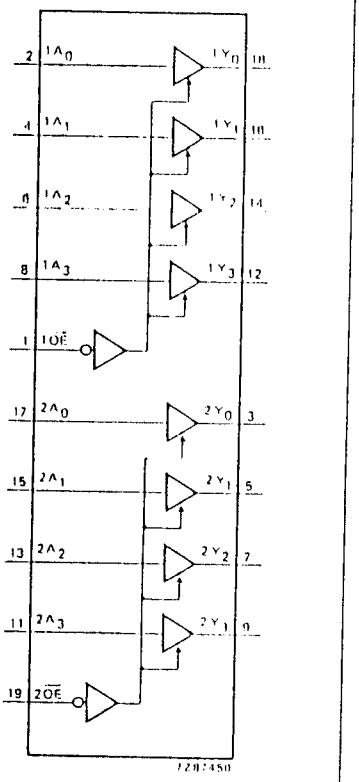


Fig. 4 Functional diagram.

QUAD D-TYPE FLIP-FLOP; POSITIVE-EDGE TRIGGER; 3-STATE

FEATURES

- Gated input enable for hold (do nothing) mode
- Gated output enable control
- Edge-triggered D-type register
- Asynchronous master reset
- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT173 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT173 are 4-bit parallel load registers with clock enable control, 3-state buffered outputs (Q_0 to Q_3) and master reset (MR).

When the two data enable inputs ($\overline{E}_1$ and $\overline{E}_2$) are LOW, the data on the D_n inputs is loaded into the register synchronously with the LOW-to-HIGH clock (CP) transition. When one or both $\overline{E}_n$ inputs are HIGH one set-up time prior to the LOW-to-HIGH clock transition, the register will retain the previous data. Data inputs and clock enable inputs are fully edge-triggered and must be stable only one set-up time prior to the LOW-to-HIGH clock transition.

The master reset input (MR) is an active HIGH asynchronous input. When MR is HIGH, all four flip-flops are reset (cleared) independently of any other input condition.

The 3-state output buffers are controlled by a 2-input NOR gate. When both output enable inputs ($\overline{OE}_1$ and $\overline{OE}_2$) are LOW, the data in the register is presented to the Q_n outputs. When one or both $\overline{OE}_n$ inputs are HIGH, the outputs are forced to a high impedance OFF-state. The 3-state output buffers are completely independent of the register operation; the $\overline{OE}_n$ transition does not affect the clock and reset operations.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay CP to Q_n MR to Q_n	C_L = 15 pF V_{CC} = 5 V	17 13	17 17	ns ns
f_{max}	maximum clock frequency		88	88	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	20	20	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2	$\overline{OE}_1$, $\overline{OE}_2$	output enable input (active LOW)
3, 4, 5, 6	Q_0 to Q_3	3-state flip-flop outputs
7	CP	clock input (LOW-to-HIGH, edge-triggered)
8	GND	ground (0 V)
9, 10	$\overline{E}_1$, $\overline{E}_2$	data enable inputs (active LOW)
14, 13, 12, 11	D_0 to D_3	data inputs
15	MR	asynchronous master reset (active HIGH)
16	V_{CC}	positive supply voltage

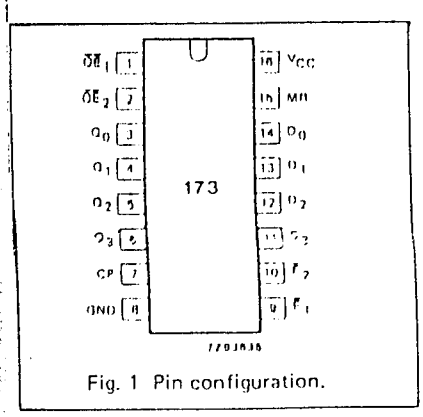


Fig. 1 Pin configuration.

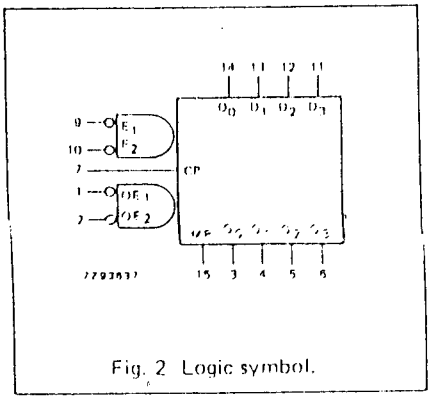


Fig. 2 Logic symbol.

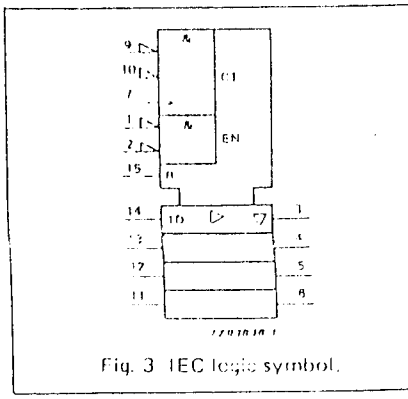


Fig. 3 IEC logic symbol.

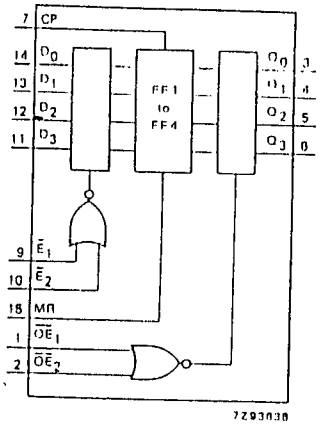


Fig. 4 Functional diagram.

FUNCTION TABLE

REGISTER OPERATING MODES	INPUTS					OUTPUTS
	MR	CP	$\bar{E}_1$	$\bar{E}_2$	D_n	Q_n (register)
reset (clear)	H	X	X	X	X	L
parallel load	L	↑	l	l	l	L
	L	↑	l	l	h	H
hold (no change)	L	X	h	X	X	q_n
	L	X	X	h	X	q_n

3-STATE BUFFER OPERATING MODES	INPUTS			OUTPUTS			
	Q_n (register)	$\bar{OE}_1$	$\bar{OE}_2$	Q_0	Q_1	Q_2	Q_3
read	L	L	L	L	L	L	L
	H	L	L	H	H	H	H
disabled	X	H	X	Z	Z	Z	Z
	X	X	H	Z	Z	Z	Z

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
q = lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW-to-HIGH CP transition
X = don't care
Z = high impedance OFF-state
↑ = LOW-to-HIGH CP transition

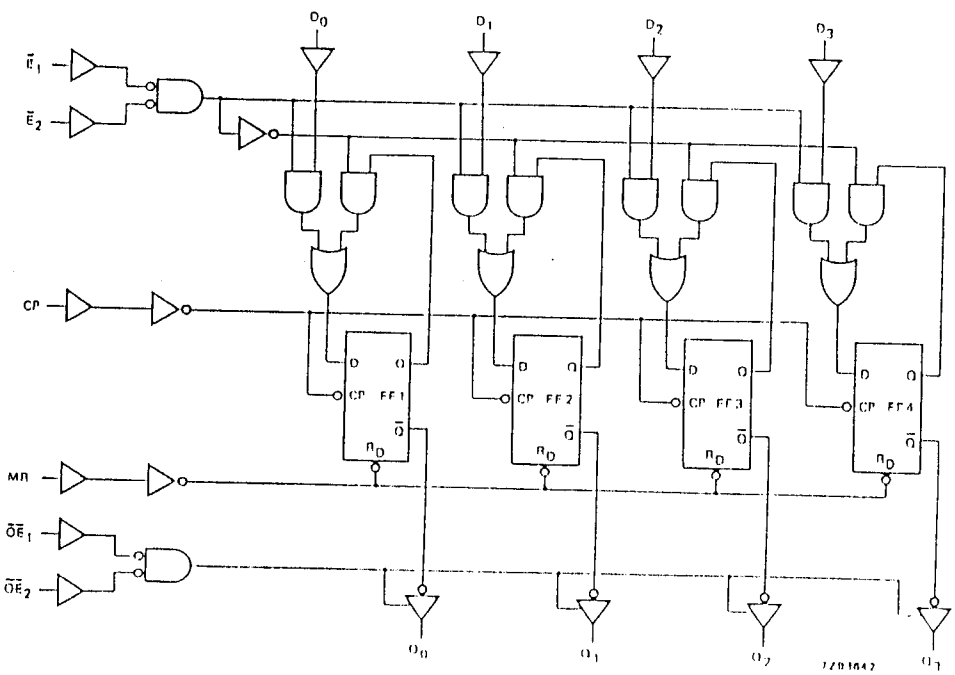


Fig. 5 Logic diagram.

2-INPUT OR GATE

RES

ıut capability: standard
category: SSI

IAL DESCRIPTION

HC/HCT32 are high-speed
CMOS devices and are pin
ble with low power Schottky
STTL). They are specified in
nce with JEDEC standard no. 7A.
HC/HCT32 provide the
OR function.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/ t_{PLH}	propagation delay nA, nB to nY	C_L = 15 pF V_{CC} = 5 V	6	9	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	16	28	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	data inputs
2, 5, 10, 13	1B to 4B	data inputs
3, 6, 8, 11	1Y to 4Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

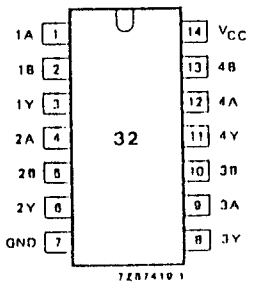


Fig. 1 Pin configuration.

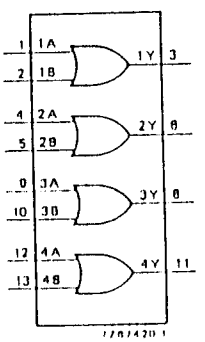


Fig. 2 Logic symbol.

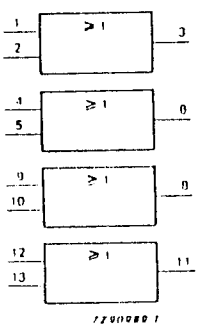


Fig. 3 IEC logic symbol.

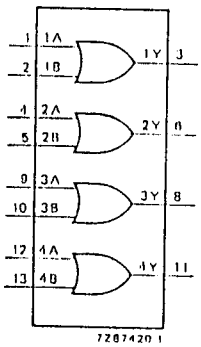


Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS		OUTPUT
nA	nB	nY
L	L	L
L	H	H
H	L	H
H	H	H

H = HIGH voltage level
L = LOW voltage level

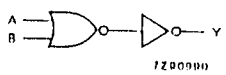


Fig. 5 Logic diagram 74HC (one gate).

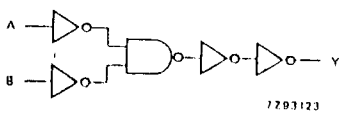


Fig. 6 Logic diagram 74HCT (one gate).

CHARACTERISTICS FOR 74HC

the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

ɔut capability: standard
category: SSI

CHARACTERISTICS FOR 74HC

) = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

MBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC									
		+25			−40 to +85		−40 to +125			V_{CC} V	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.			
L/ H	propagation delay nA, nB to nY		22 8 6	90 18 15		115 23 20		135 27 23	ns	2.0 4.5 6.0	Fig. 7
L/ H	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 7

INVERTER

'URES

itput capability: standard
C category: SSI

ERAL DESCRIPTION

4HC/HCT04 are high-speed
e CMOS devices and are pin
atible with low power Schottky
(LSTTL). They are specified in
liance with JEDEC standard no. 7A.
'4HC/HCT04 provide six inverting
rs.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/ t_{PLH}	propagation delay nA to nY	C_L = 15 pF; V_{CC} = 5 V	7	8	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	21	24	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 3, 5, 9, 11, 13	1A to 6A	data inputs
2, 4, 6, 8, 10, 12	1Y to 6Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

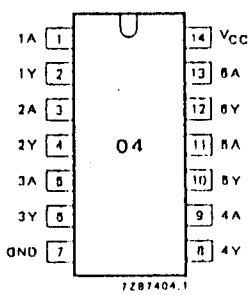


Fig. 1 Pin configuration.

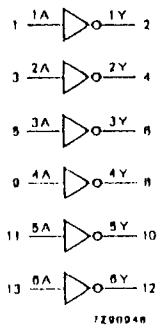


Fig. 2 Logic symbol.

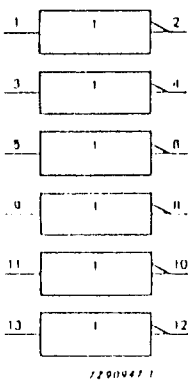


Fig. 3 IEC logic symbol.

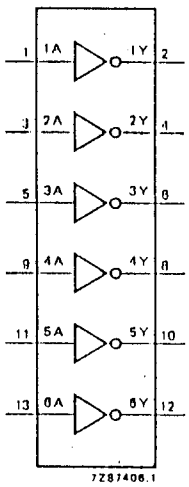


Fig. 4 Functional diagram.

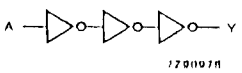


Fig. 5 Logic diagram (one inverter).

FUNCTION TABLE

INPUT	OUTPUT
nA	nY
L H	H L

H = HIGH voltage level
L = LOW voltage level

CHARACTERISTICS FOR 74HC

...he DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

...ut capability: standard
...category: SSI

CHARACTERISTICS FOR 74HC

... = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

...MBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC									
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.	max.		V_{CC} V	WAVEFORMS
...IL/ ...H	propagation delay nA to nY		25 9 7	85 17 14		105 21 18		130 26 22	ns	2.0 4.5 6.0	Fig. 6
...HL/ ...H	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6

DUAL 4-INPUT NAND GATE

FEATURES

- Output capability: standard
- I_{CC} category: SSI

GENERAL DESCRIPTION

The 74HC/HCT20 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT20 provide the 4 input NAND function.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL} / t_{PLH}	propagation delay nA, nB, nC, nD to nY	C_L = 15 pF; V_{CC} = 5 V	8	13	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	22	17	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 9	1A, 2A	data inputs
2, 10	1B, 2B	data inputs
3, 11	n.c.	not connected
4, 12	1C, 2C	data inputs
5, 13	1D, 2D	data inputs
6, 8	1Y, 2Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

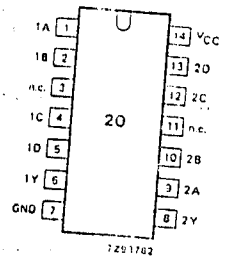


Fig. 1 Pin configuration.

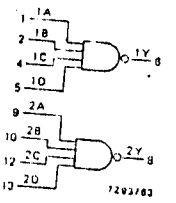


Fig. 2 Logic symbol.

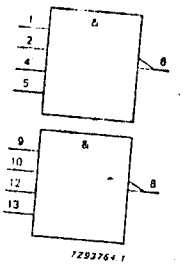


Fig. 3 IEC logic symbol.

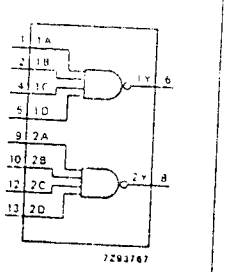


Fig. 4 Functional diagram.

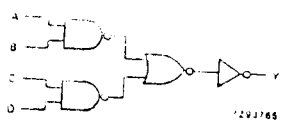


Fig. 5 HC logic diagram (one gate).

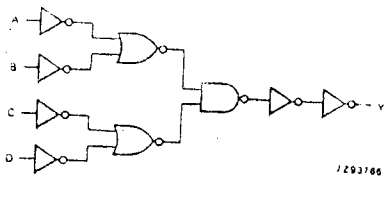


Fig. 6 HCT logic diagram (one gate).

FUNCTION TABLE

INPUTS				OUTPUT
nA	nB	nC	nD	nY
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

H = HIGH voltage level
L = LOW voltage level
X = don't care

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: SSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC									
		+25			−40 to +85		−40 to +125			V_{CC} V	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay nA, nB, nC, nD to nY		28 10 8	90 18 15		115 23 20		135 27 23	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 7

3-TO-8 LINE DECODER/DEMULTIPLEXER; INVERTING

FEATURES

- Demultiplexing capability
- Multiple input enable for easy expansion
- Ideal for memory chip select decoding
- Active LOW mutually exclusive outputs
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT138 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT138 decoders accept three binary weighted address inputs (A_0, A_1, A_2) and when enabled, provide 8 mutually exclusive active LOW outputs ($\overline{Y}_0$ to $\overline{Y}_7$).

The "138" features three enable inputs: two active LOW ($\overline{E}_1$ and $\overline{E}_2$) and one active HIGH (E_3). Every output will be HIGH unless $\overline{E}_1$ and $\overline{E}_2$ are LOW and E_3 is HIGH.

This multiple enable function allows easy parallel expansion of the "138" to a 1-of-32 (5 lines to 32 lines) decoder with just four "138" ICs and one inverter.

The "138" can be used as an eight output demultiplexer by using one of the active LOW enable inputs as the data input and the remaining enable inputs as strobes. Unused enable inputs must be permanently tied to their appropriate active HIGH or LOW state.

The "138" is identical to the "238" but has inverting outputs.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay A_n to $\overline{Y}_n$	C_L = 15 pF; V_{CC} = 5 V	12	17	ns
t_{PHL}/t_{PLH}	E_3 to $\overline{Y}_n$ / $\overline{E}_n$ to $\overline{Y}_n$		14	19	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	67	67	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2, 3	A_0 to A_2	address inputs
4, 5	$\overline{E}_1$, $\overline{E}_2$	enable inputs (active LOW)
6	E_3	enable input (active HIGH)
8	GND	ground (0 V)
15, 14, 13, 12, 11, 10, 9, 7	$\overline{Y}_0$ to $\overline{Y}_7$	outputs (active LOW)
16	V_{CC}	positive supply voltage

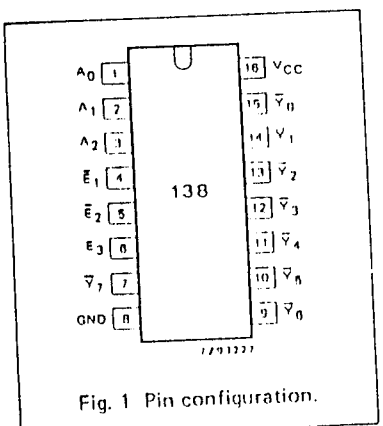


Fig. 1 Pin configuration.

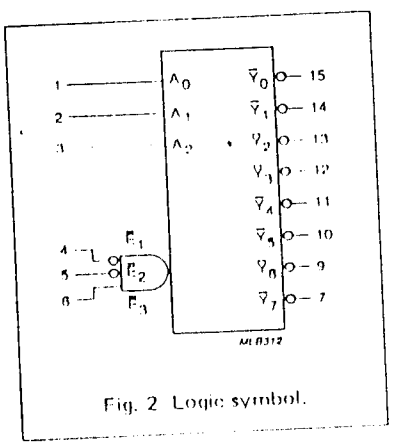


Fig. 2 Logic symbol.

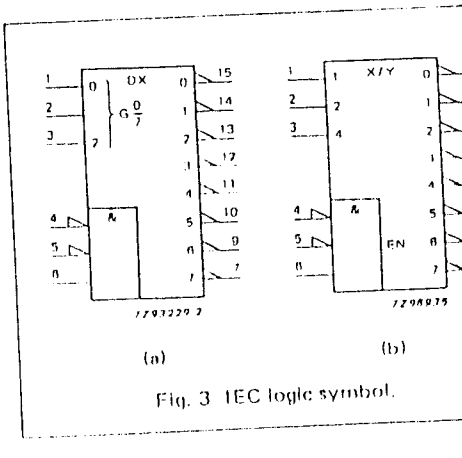


Fig. 3 IEC logic symbol.

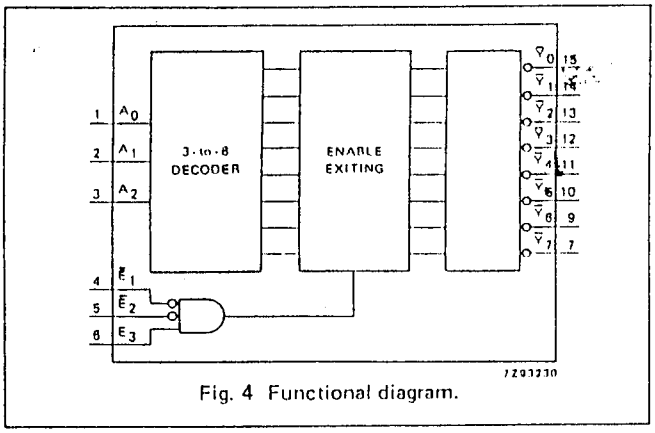


Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS						OUTPUTS							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{Y}_0$	$\overline{Y}_1$	$\overline{Y}_2$	$\overline{Y}_3$	$\overline{Y}_4$	$\overline{Y}_5$	$\overline{Y}_6$	$\overline{Y}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH voltage level
L = LOW voltage level
X = don't care

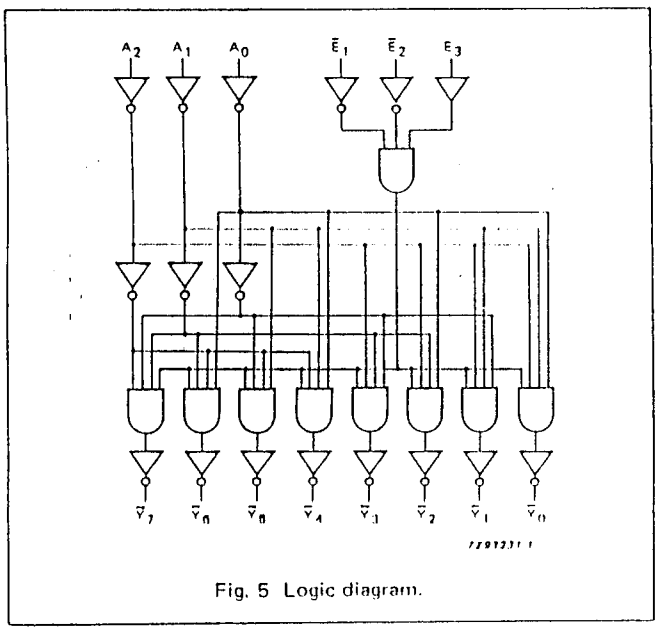


Fig. 5 Logic diagram.

AL BUS TRANSCEIVER; 3-STATE

TURES

:tal bidirectional bus interface
)n-inverting 3-state outputs
itput capability: bus driver
C category: MSI

ERAL DESCRIPTION

4HC/HCT245 are high-speed
CMOS devices and are pin
otible with low power Schottky
LSTTL). They are specified in
lance with JEDEC standard no. 7A.

4HC/HCT245 are octal
eivers featuring non-inverting
bus compatible outputs in both
nd receive directions.
245" features an output enable
nput for easy cascading and a
eceive (DIR) for direction control.
ntrols the outputs so that the
are effectively isolated.
245" is similar to the "640" but
ie (non-inverting) outputs.

CTION TABLE

INPUTS		INPUTS/OUTPUTS	
	DIR	A_n	B_n
	L	A = B	inputs
	H	inputs	B = A
	X	Z	Z

GH voltage level
W voltage level
n't care
h Impedance OFF-state

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay A_n to B_n; B_n to A_n	C_L = 15 pF; V_{CC} = 5 V	7	10	ns
C_I	input capacitance		3.5	3.5	pF
$C_{I/O}$	input/output capacitance		10	10	pF
C_{PD}	power dissipation capacitance per transceiver	notes 1 and 2	30	30	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	DIR	direction control
2, 3, 4, 5, 6, 7, 8, 9	A_0 to A_7	data inputs/outputs
10	GND	ground (0 V)
18, 17, 16, 15, 14, 13, 12, 11	B_0 to B_7	data inputs/outputs
19	$\overline{OE}$	output enable input (active LOW)
20	V_{CC}	positive supply voltage

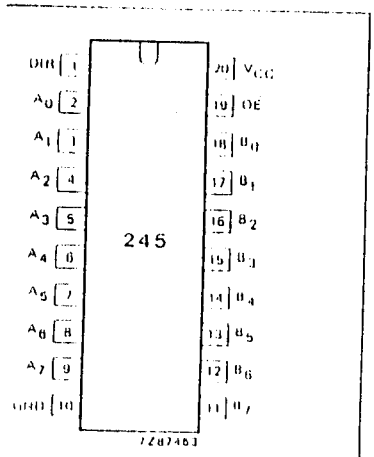


Fig. 1 Pin configuration.

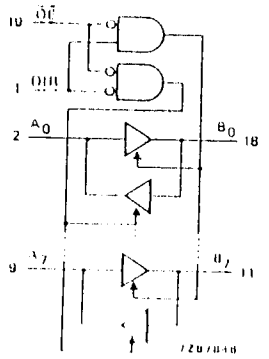


Fig. 2 Logic symbol

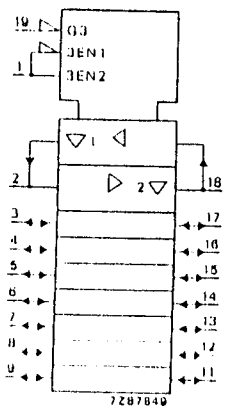


Fig. 3 IEC

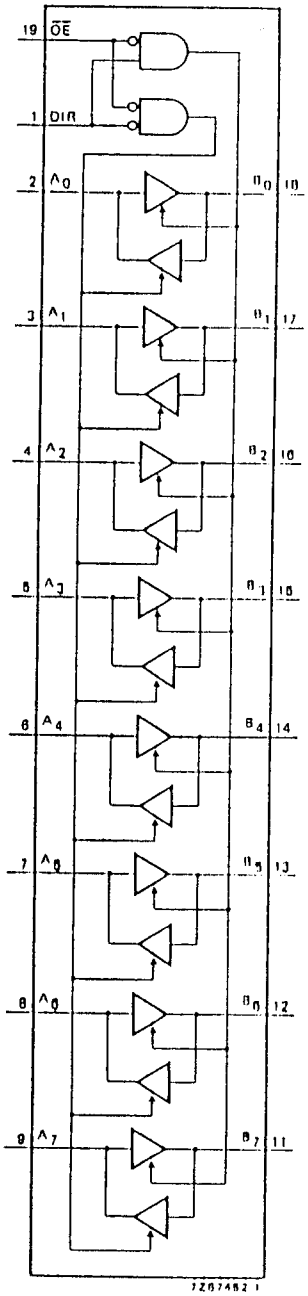


Fig. 4 Functional diagram.

2-INPUT AND GATE

ES

t capability: standard
ategory: SSI

AL DESCRIPTION

C/HCT08 are high-speed
MOS devices and are pin
le with low power Schottky
TTL). They are specified in
ce with JEDEC standard no. 7A.
C/HCT08 provide the 2-input
ction.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	C_L = 15 pF V_{CC} = 5 V	7	11	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	10	20	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

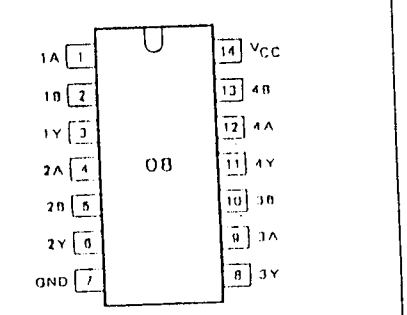
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

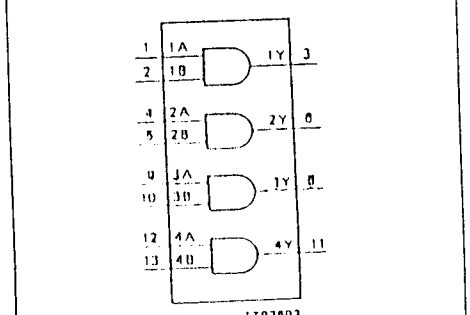
PACKAGE OUTLINES

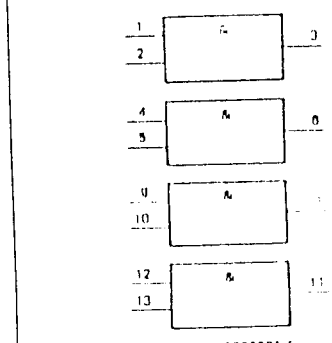
SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	data inputs
2, 5, 10, 13	1B to 4B	data inputs
3, 6, 8, 11	1Y to 4Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage







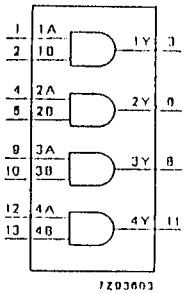


Fig. 4 Functional diagram.

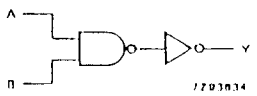


Fig. 5 HC logic diagram (one gate).

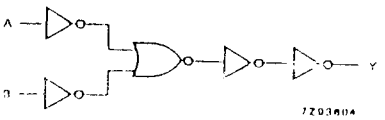


Fig. 6 HCT logic diagram (one gate).

CTION TABLE

INPUTS		OUTPUT
A	nB	nY
	L	L
	H	L
	L	L
	H	H

IGH voltage level
OW voltage level

IARACTERISTICS FOR 74HC

e DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

t capability: standard
tegory: SSI

HARACTERISTICS FOR 74HC

= 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

BOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC									
		+25			−40 to +85		−40 to +125			V_{CC} V	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.			
/	propagation delay nA, nB to nY		25 9 7	90 18 15		115 23 20		135 27 23	ns	2.0 4.5 6.0	Fig. 7
/	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 7

512K (64K x 8) OTP CMOS EPROM

Features

- Fast Read Access Time - 45 ns
- Low Power CMOS Operation
  - µA max. Standby
  - mA max. Active at 5 MHz
- JEDEC Standard Packages
  - 28-Lead 600-mil PDIP
  - 32-Lead PLCC
  - 28-Lead TSOP and SOIC
- 5V ± 10% Supply
- High Reliability CMOS Technology
  - 2,000V ESD Protection
  - 200 mA Latchup Immunity
- Rapid™ Programming Algorithm - 100 µs/byte (typical)
- CMOS and TTL Compatible Inputs and Outputs
- Integrated Product Identification Code
- Commercial and Industrial Temperature Ranges

Description

The AT27C512R is a low-power, high performance 524,288 bit one-time programmable read only memory (OTP EPROM) organized 64K by 8 bits. It requires only one 5V power supply in normal read mode operation. Any byte can be accessed in less than 45 ns, eliminating the need for speed reducing WAIT states on high performance microprocessor systems.

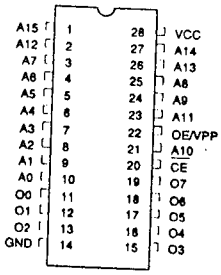
Atmel's scaled CMOS technology provides high speed, lower active power consumption, and significantly faster programming. Power consumption is typically only in the Active Mode and less than 10 µA in Standby.

(continued)

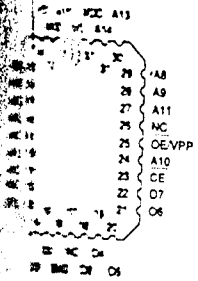
Pin Configurations

Name	Function
A0 - A15	Addresses
O0 - O7	Outputs
CE	Chip Enable
OE/VPP	Output Enable/VPP
NC	No Connect

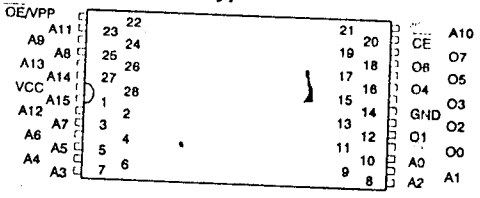
PDIP, SOIC Top View



PLCC Top View



TSOP Top View
Type 1



Note: PLCC Package Pins 1 and 17 are DON'T CONNECT.

0015H

Description (Continued)

The AT27C512R is available in a choice of industry standard JEDEC-approved one-time programmable (OTP) plastic PDIP, PLCC, SOIC, and TSOP packages. All devices feature two-line control ($\overline{CE}$, $\overline{OE}$) to give designers the flexibility to prevent bus contention.

With 64K byte storage capability, the AT27C512R allows firmware to be stored reliably and to be accessed by the system without the delays of mass storage media.

Atmel's 27C512R has additional features to ensure high quality and efficient production use. The Rapid™ Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 100 µs/byte. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages.

System Considerations

Switching between active and standby co
Chip Enable pin may produce transien
sions. Unless accommodated by the syste
transients may exceed data sheet limits,
vice non-conformance. At a minimum, a 0
quency, low inherent inductance, cera
should be utilized for each device. This ca
be connected between the Vcc and Grou
the device, as close to the device as possib
to stabilize the supply voltage level on
boards with large EPROM arrays, a 4.7 µF b
capacitor should be utilized, again connecte
Vcc and Ground terminals. This capacitor s
tioned as close as possible to the point wh
supply is connected to the array.

D 2-INPUT AN GATE

TURES

tput capability: standard
C category: SSI

ERAL DESCRIPTION

4HC/HCT08 are high-speed
CMOS devices and are pin
atible with low power Schottky
LSTTL). They are specified in
liance with JEDEC standard no. 7A.
4HC/HCT08 provide the 2-input
function.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	C_L = 15 pF; V_{CC} = 5 V	7	11	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	10	20	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

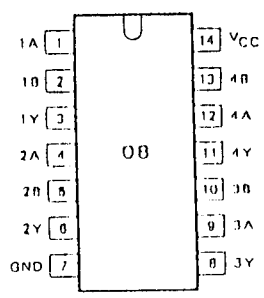
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacitance in pF
   f_o = output frequency in MHz; V_{CC} = supply voltage in V
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

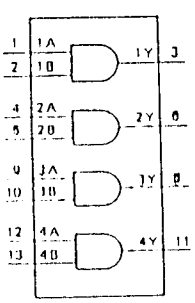
PACKAGE OUTLINES

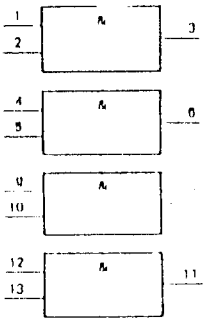
SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	data inputs
2, 5, 10, 13	1B to 4B	data inputs
3, 6, 8, 11	1Y to 4Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage







2

64K (8K x 8) CMOS E^2PROM

ccess Time - 120 ns
rite - 200 µs or 1 ms
Byte Write Cycle
Address and Data Latches
Control Timer
atic Clear Before Write
oprocessor Control
/BUSY Open Drain Output
Polling

Active Current
CMOS Standby Current
ability
rance: 10^4 or 10^5 Cycles
Retention: 10 Years
Supply
d TTL Compatible Inputs and Outputs
proved Byte-Wide Pinout
rcial and Industrial Temperature Ranges

ction

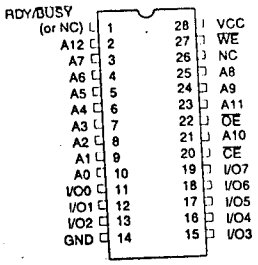
64 is a low-power, high-performance 8,192 words by 8 bit nonvolatile Erasable and Programmable Read Only Memory with popular, easy to es. The device is manufactured with Atmel's reliable nonvolatile technol-

(continued)

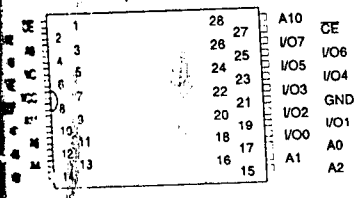
nfigurations

Function
Addresses
Chip Enable
Output Enable
Write Enable
Data Inputs/Outputs
Ready/Busy Output
No Connect
Don't Connect

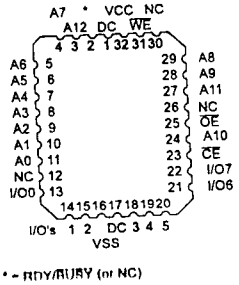
PDIP, SOIC
Top View



TSOP
Top View



LCC, PLCC
Top View



* = RDY/BUSY (or NC)

Note: PLCC package pins 1 and 17 are DON'T CONNECT.

0001F

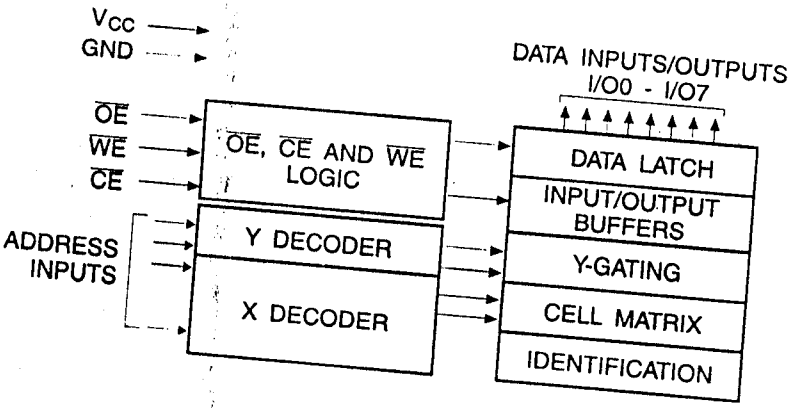
Description (Continued)

The AT28C64 is accessed like a Static RAM for the read or write cycles without the need for external components. During a byte write, the address and data are latched internally, freeing the microprocessor address and data bus for other operations. Following the initiation of a write cycle, the device will go to a busy state and automatically clear and write the latched data using an internal control timer. The device includes two methods for detecting the end of a write cycle, level detection of RDY/$\overline{BUSY}$ (unless pin 1 is N.C.) and DATA POLLING of I/O7. Once the end of a write cycle has been detected, a new access for a read or write can begin.

The CMOS technology offers fast access times of 120 ns at low power dissipation. When the chip is deselected, standby current is less than 100 µA.

Atmel's 28C64 has additional features to ensure high quality and manufacturability. The device utilizes error correction internally for extended endurance and for improved data retention characteristics. An extra 32-bytes E^2PROM are available for device identification or tracking.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to VCC + 0.6V
Voltage on $\overline{OE}$ and A9 with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Device Operation

READ: The AT28C64 is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in a high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual line control gives designers increased flexibility in preventing bus contention.

BYTE WRITE: Writing data into the AT28C64 is similar to writing into a Static RAM. A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{OE}$ high and $\overline{CE}$ or $\overline{WE}$ low (respectively) initiates a byte write. The address location is latched on the falling edge of $\overline{WE}$ (or $\overline{CE}$); the new data is latched on the rising edge. Internally, the device performs a self-clear before write. Once a byte write has been started, it will automatically time itself to completion. Once a programming operation has been initiated and for the duration of twc, a read operation will effectively be a polling operation.

FAST BYTE WRITE: The AT28C64E offers a byte write time of 200 µs maximum. This feature allows the entire device to be rewritten in 1.6 seconds.

RDY/$\overline{BUSY}$: Pin 1 is an open drain READY/$\overline{BUSY}$ output that can be used to detect the end of a write cycle. RDY/$\overline{BUSY}$ is actively pulled low during the write cycle and is released at the completion of the write. The open drain connection allows for OR-tying of several devices to the same RDY/$\overline{BUSY}$ line. Pin 1 is not connected for the AT28C64X.

$\overline{DATA}$ POLLING: The AT28C64 provides $\overline{DATA}$ POLLING to signal the completion of a write cycle. During a write cycle, an attempted read of the data being written results in the complement of that data for I/O_7 (the other outputs are indeterminate). When the write cycle is finished, true data appears on all outputs.

WRITE PROTECTION: Inadvertent writes to the device are protected against in the following ways. (a) V_{CC} sense— if V_{CC} is below 3.8V (typical) the write function is inhibited. (b) V_{CC} power on delay— once V_{CC} has reached 3.8V the device will automatically time out 5 ms (typical) before allowing a byte write. (c) Write Inhibit— holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits byte write cycles.

CHIP CLEAR: The contents of the entire memory of the AT28C64 may be set to the high state by the CHIP CLEAR operation. By setting $\overline{CE}$ low and $\overline{OE}$ to 12 volts, the chip is cleared when a 10 msec low pulse is applied to $\overline{WE}$.

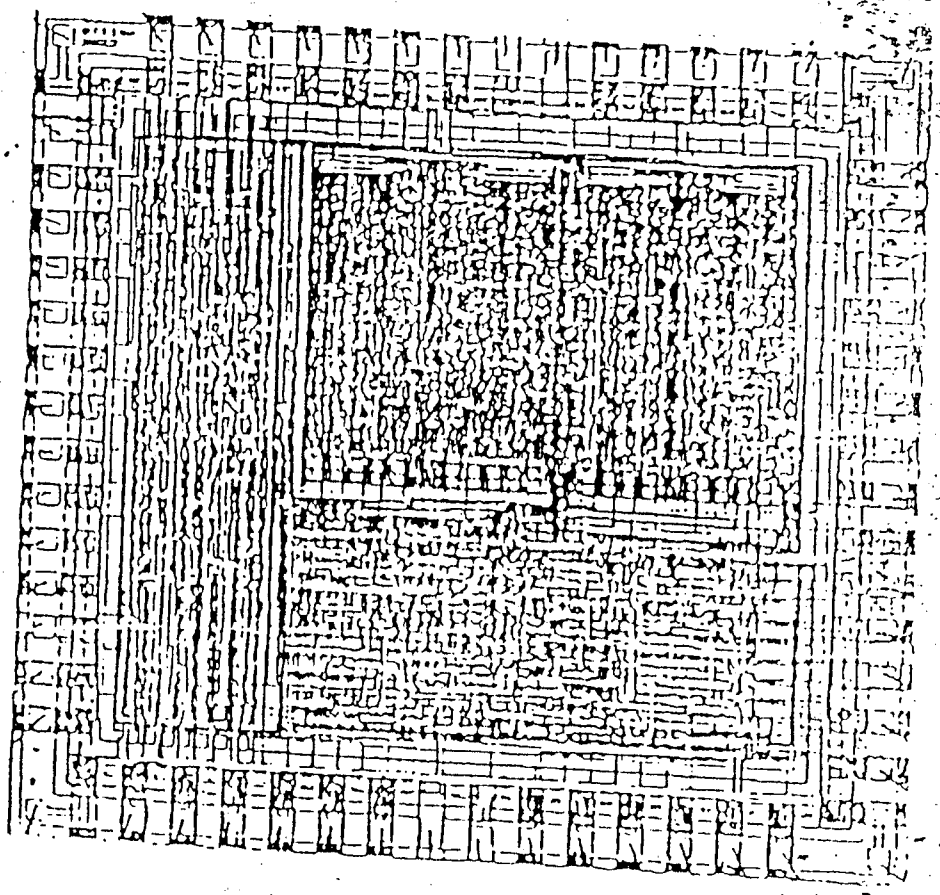
DEVICE IDENTIFICATION: An extra 32-bytes of E^2PROM memory are available to the user for device identification. By raising A9 to 12 ± 0.5V and using address locations 1FE0H to 1FFFH the additional bytes may be written to or read from in the same manner as the regular memory array.

ESD Training

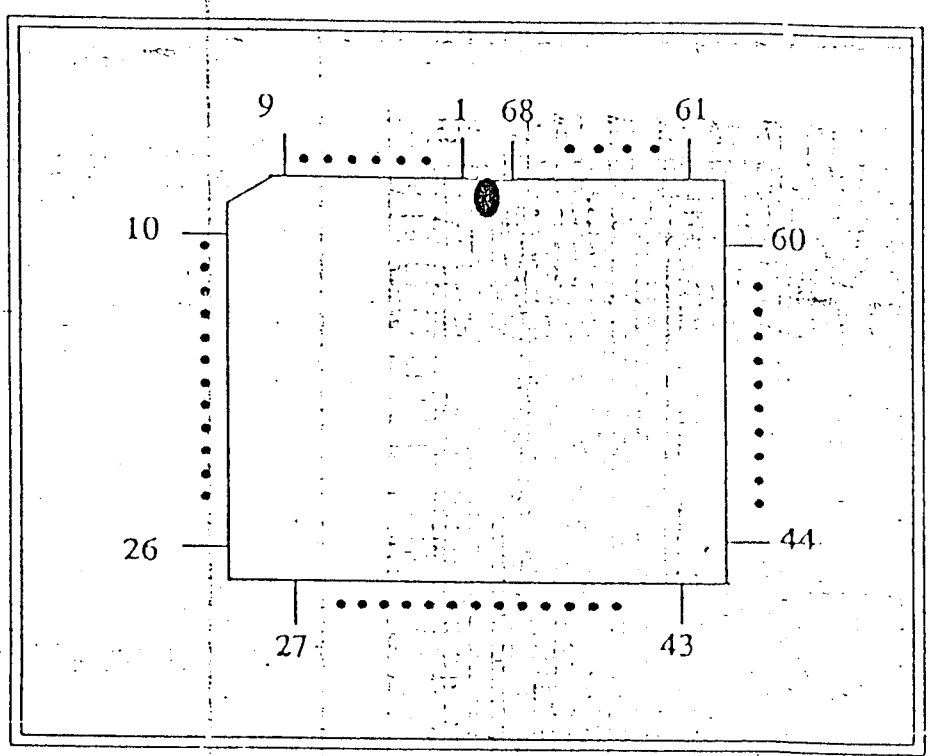
DCC

DATA SHEET

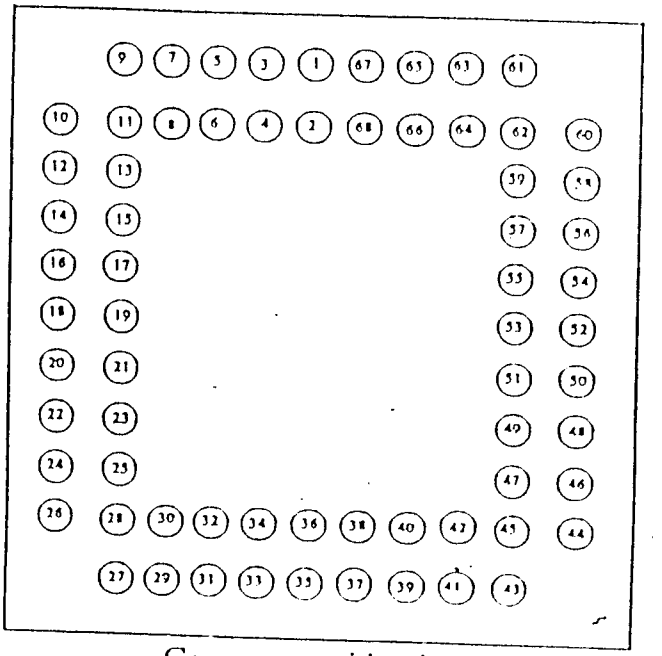
DIGITAL SWITCH ELEMENT



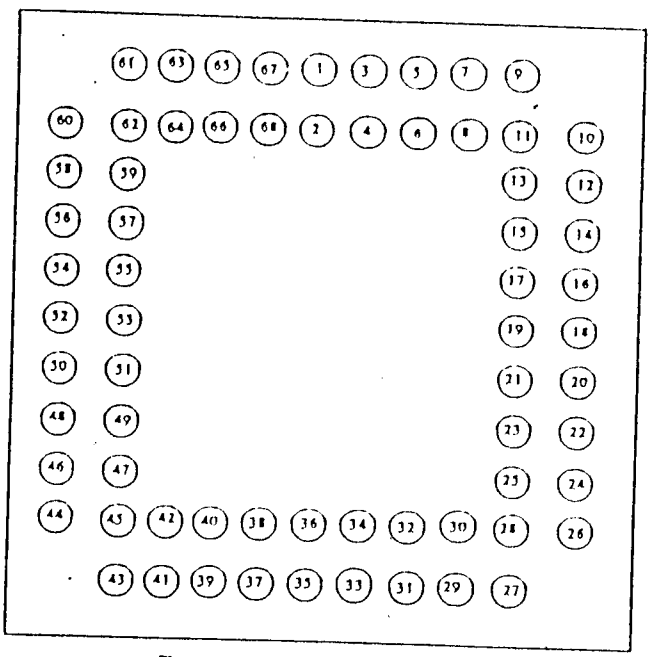
Pin-out diagram of the device(Component side)



PLCC Socket View



Component side view



Pattern side view

PIN DESCRIPTION

N.C. = Not connected.

Pin No.	Pin Name	Type	Other
1.	VSS	POWER	
2.	DB(3)	BIDIRECTIONAL	TTLin/4ma out
3.	DB(2)	BIDIRECTIONAL	TTLin/4ma out
4.	DB(1)	BIDIRECTIONAL	TTLin/4ma out
5.	DB(0)	DIDIRECTIONAL	TTLin/4ma out
6.	R/W	INPUT	TTL
7.	A1	INPUT	TTL
8.	A2	INPUT	TTL
9.	N.C.		
10.	N.C.		
11.	A3	INPUT	TTL
12.	VSS	POWER	
13.	PCMIN 8	INPUT	TTL
14.	PCMIN 9	INPUT	TTL
15.	PCMIN 10	INPUT	TTL
16.	PCMIN 11	INPUT	TTL
17.	PCMIN 12	INPUT	TTL
18.	PCMIN 13	INPUT	TTL
19.	PCMIN 14	INPUT	TTL
20.	PCMIN 15	INPUT	TTL

contd...

Pin No.	Pin Name	Type	Other
21.	CSB	INPUT	TTL
22.	IDLE/$\overline{\text{BUSY}}$	OUTPUT	4 mA drive
23.	VSS	POWER	
24.	PCMOUT0	OUTPUT	4 mA drive
25.	PCMOUT1	OUTPUT	4 mA drive
26.	N.C.		
27.	N.C.		
28.	PCMOUT2	OUTPUT	4 mA drive
29.	PCMOUT3	OUTPUT	4 mA drive
30.	PCMOUT4	OUTPUT	4 mA drive
31.	PCMOUT5	OUTPUT	4 mA drive
32.	PCMOUT6	OUTPUT	4 mA drive
33.	PCMOUT7	OUTPUT	4 mA drive
34.	C4mh	OUTPUT	4 mA drive
35.	VDD	POWER	
36.	VSS	POWER	
37.	C2mh	OUTPUT	4 mA drive
38.	PCMOUT8	OUTPUT	4 mA drive
39.	PCMOUT9	OUTPUT	4 mA drive
40.	PCMOUT10	OUTPUT	4 mA drive
41.	PCMOUT11	OUTPUT	4 mA drive
42.	PCMOUT12	OUTPUT	4 mA drive
43.	N.C.		
44.	N.C.		

contd..

Pin No.	Pin Name	Type	Other
45.	PCMOUT13	OUTPUT	4 mA drive
46.	PCMOUT14	OUTPUT	4 mA drive
47.	PCMOUT15	OUTPUT	4 mA drive
48.	VDD	POWER	
49.	PCMIN0	INPUT	TTL
50.	PCMIN1	INPUT	TTL
51.	PCMIN2	INPUT	TTL
52.	PCMIN3	INPUT	TTL
53.	PCMIN4	INPUT	TTL
54.	PCMIN5	INPUT	TTL
55.	PCMIN6	INPUT	TTL
56.	PCMIN7	INPUT	TTL
57.	VDD	POWER	
58.	fpout	OUTPUT	4 mA drive
59.	fpin	INPUT	TTL
60.	N.C.		
61.	N.C.		
62.	SPDTEST	INPUT	TTL pullup
63.	SYSCLK	CLOCK INPUT	TTL
64.	DE(7)	BIDIRECTIONAL	TTLin/5mA out
65.	DB(6)	BIDIRECTIONAL	TTLin/4mA out
66.	DB(5)	BIDIRECTIONAL	TTLin/4mA out
67.	DB(4)	BIDIRECTIONAL	TTLin/4mA out
68.	VDD	POWER	

Non pull-up

fpout	Active low output framing pulse. This signal from the device indicates that the bit-0 of time slot-0 is available on the PCMOUT lines.
PCMOUT (0..15)	PCM output links, each carrying a serial stream at 2.048 mbits/s comprising of 32, 8 bit time slots (256 bits/frame).
Idle/$\overline{\text{Busy}}$	This signal indicates whether the corresponding output time slot is busy or not. A logic 1 indicates that the Time slot is idle. When idle, the output Time slot carries the corresponding (Lower) CRAM content. This signal comes ahead of time (see timing details).
C2mh	Sysclk divide by 4 output signal.
C4mh	Sysclk divide by 2 output signal.
Sysclk	System clock for the device. For 2.048 mbits/s PCM stream, the clock frequency is 8.192.
SPD TEST	Active low (pulled high internally). This signal disables the SRAM being written by the IBUF. This feature is used for performing diagnostic check on SRAM.

SIGNAL DESCRIPTION

DB (0.7)	Bidirectional data bus for the micro interface. The external microprocessor Reads and Writes data through this interface.
A1..A3	Function select address lines : These lines are used to select various commands that are used to program the device.
$\overline{R/W}$	Active low indicates Read function while high corresponds to write function.
$\overline{CSB}$	Active low chip select signal enables the command execution.
fpin	Active low framing pulse. This signal indicates to the device that bit 0 of time slot-0 on the PCMIN line. This signal provides the framing information of the incoming PCM streams (PCMIN0 ..PCMIN15). The fpin pulse is level sensitive and must be half the SYSCLK (8.192 MHz) as given in timing diagram. Failure to meet this spec.will make the switch to malfunction.
PCMIN(0..15)	PCM input links, each link carrying a serial stream at 2.048 mbits/s comprising of 32, 8 bit time slots (256 bits/frame). These inputs are not internally pulled and hence unused PCM inputs must be externally pulled up.