AUTOCROSS – AUTOMATED CAR SPEED TESTING USING 8031 MICROCONTROLLER AND FM TRANSMISSION

P-1353

A
Project Report
Submitted In partial fulfilment of the requirements
for the award of the Degree of

BACHELOR OF ENGINEERING IN ELECTRONICS AND COMMUNICATION ENGINEERING
of the Bharathiar University Coimbatore.

Submitted by

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Coimbatore – 641 006

1999 - 2000

KUMARAGURU COLLEGE OF TECHNOLOGY

Coimbatore - 641 006

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Certificate

This is to Certify that the Project report entitled

"AUTOCROSS – AUTOMATED CAR SPEED TESTING USING 8031 MICROCONTROLLER AND FM TRANSMISSION"

has been submitted by

Mr. C. GIRISH, V. VIJAYARAM, AJAY KRISHNAN, N.KARTHIK, K.AKILAN

in partial fulfillment for the award of the Degree of Bachelor of Engineering in the Electrical and Electronics Engineering Branch of the Bharathiar University, Coimbatore - 641 046 during the academic year 1999 - 2000.

(Guide)

(Head of the Department)

Certified that the candidate was examined by us in the project work viva-voce Examination held on .....

and the University Register numbers are ***9627D0205, 9627D0249, 9627D0191, 9627D0210, 9627D0192.***

(Internal Examiner)

(External Examiner)

Unity ElectroSystems

REF: UES/99-00/CERT/001
DATE: March 13, 2000

CERTIFICATE

This is to certify that the following students of final year B.E (ECE), Kumaraguru College of Technology, Coimbatore – 641 006, have done the project entitled "Autocross-Automated Car Speed Testing using 8031 Microcontroller and FM Transmission" in our organization during the period from July 1999 to March 2000 under the supervision of the undersigned.

1. C.GIRISH - 9627D0205
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4. N.KARTHIK - 9627D0210
5. K.AKILAN - 9627D0192

They were sincere, hardworking and took much initiatives during the period of the project. Their conduct and character have been very good.

Thanking you,

Yours sincerely,

For Unity Electro Systems [P] Ltd.,

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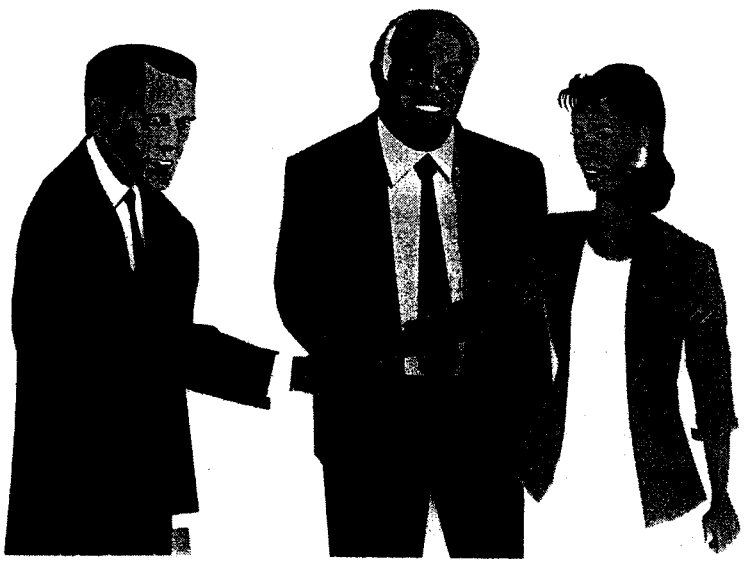
DEDICATED TO OUR BELOVED PARENTS



ACKNOWLEDGEMENT

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We are extremely thankful to our beloved Principal **Dr K . K . PADMANABHAN , B.Sc (Engg) , M. Tech ., Ph.D.,** for his unflinching support during the course of the project .

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We are highly indebted to our guide **Asst. Prof . S.GOVINDARAJU , M.E , MISTE** , for his guidance , constant motivation and invaluable support during the course of the project .

Our sincere gratitude are due to **Mr R . MAHALINGAM , M.D ,UNITY ELECTRO SYSTEMS , COIMBATORE** , for his encouragement and timely advises during the execution of the project . We also thank **Mr SRIDHAR and Ms VIMAL BHARATHI** for their immense help in hardware and software respectively .

Last but not the least , we thank all the faculty members , non-teaching staffs and our friends for their help and support .

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CONTENTS

SYNOPSIS

SYNOPSIS

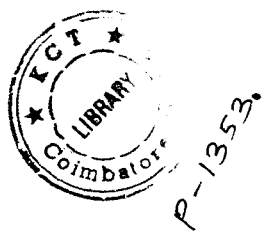
"AUTO CROSS" is an attempt to automate the process of vehicle speed testing. This finds application in vehicle manufacturing plants where the vehicles have to under go a test drive of rigorous standards .The purpose of automation is to improve the accuracy of speed performance of the vehicle , after being manufactured during test drive. The main purpose of automation is to improve the accuracy with which the vehicle speed is tested over the conventional methods.

The vehicle is allowed to travel an average distance of 400-500 metres and the time taken to traverse this distance is calculated automatically by locating sensors at suitable points.This sensor information is sent through wireless means, which activates the microcontroller based circuitry. The results of the time taken is displayed for each test run.

INTRODUCTION

1. INTRODUCTION

" All history – as well as current experience - points to the fact that it is man , not nature , who provide the primary resource : that the key development comes out of the mind of man . Suddenly , there is an outburst of daring , initiative, invention . . . "



- E . F SCHUMACHER

in Small Is Beautiful

The automobile is one such invention of a daring man, HENRY FORD . This project attempts to completely automate the speed test of an automobile .

HARDWARE USED :

- Microcontroller (8031)
- FM Transmitter (400 - 500) meters
- FM Receiver
- Infrared Sensors
- DTMF Coding
- 8279 controlled LED display

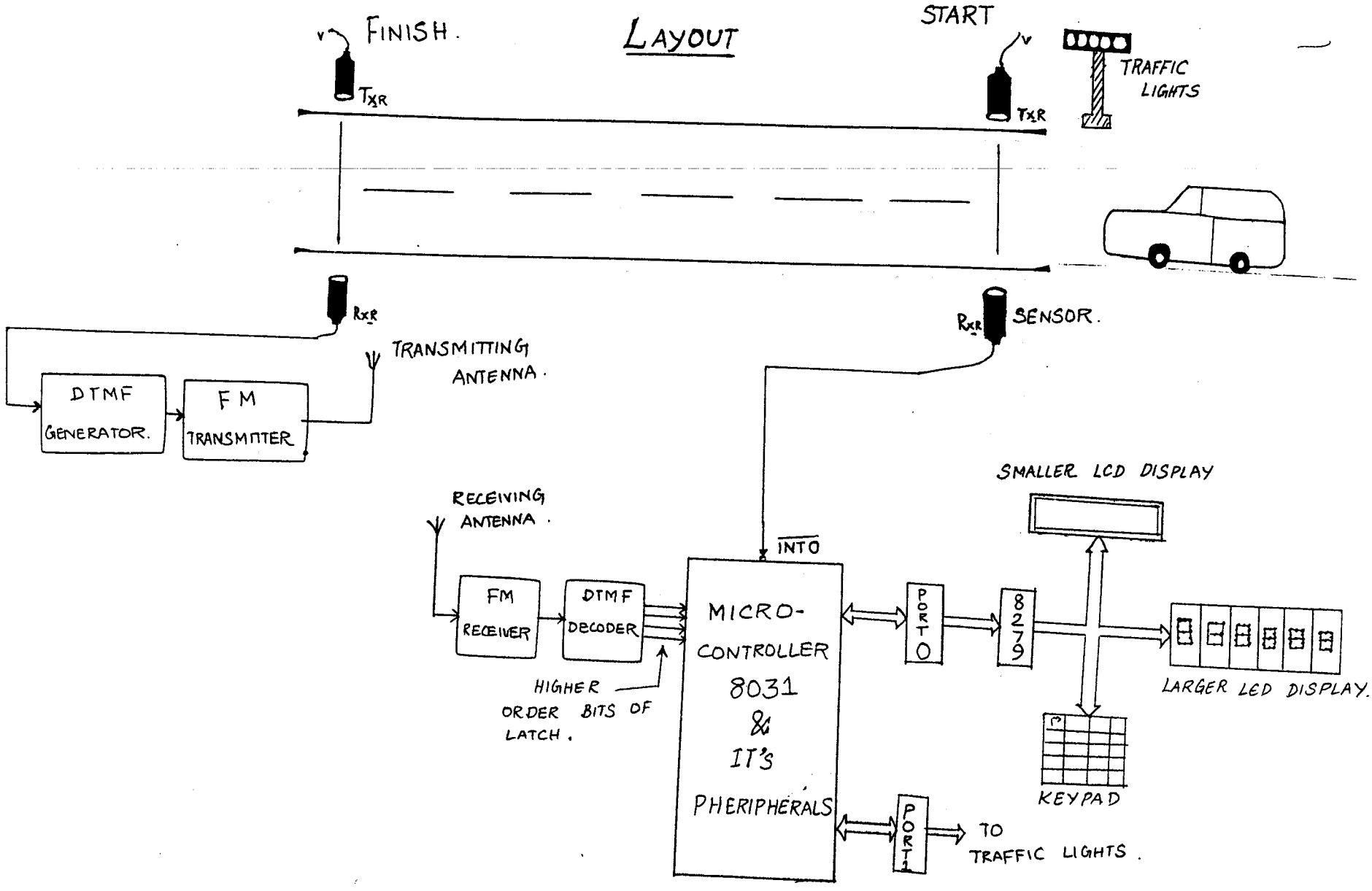
SOFTWARE USED :

- Microcontroller programming using C – compiler.

ADVANTAGES :

Our main aim has been to automate the whole process of car speed testing. This cuts down labour cost and improves the accuracy with which the car speed is tested. Such tests are carried out on parts of various shapes on which the car is allowed to run, thus testing the efficiency of the car on these paths. In a world where time management is so important, automation helps in saving valuable time .

PROJECT LAYOUT


FINISH.
LAYOUT
START
TXR
TXR
TRAFFIC LIGHTS
RXR
RXR
SENSOR.
TRANSMITTING ANTENNA.
DTMF GENERATOR.
FM TRANSMITTER
SMALLER LCD DISPLAY
RECEIVING ANTENNA.
INTO
FM RECEIVER
DTMF DECODER
MICRO-CONTROLLER 8031 & IT'S PHERIPHERALS
PORT 0
8279
LARGER LCD DISPLAY.
HIGHER ORDER BITS OF LATCH.
KEYPAD
PORT 1
TO TRAFFIC LIGHTS.

2. DESCRIPTION

The process starts by pressing the 'START' button on the keypad .This 'START' button activates the 5 traffic lights that go 'ON' one after the other .This action is controlled by software through the 5 bits of PORT 1 of the microcontroller 8031 . After the last digit goes 'ON' TIMER 0 gets activated and at the same time the count is displayed simultaneously in the LCD and LED display . This is the indication for the vehicle to start it's test run . The vehicle start is sensed by two infrared sensors that produce a pulse when cut. This pulse activates the TIMER 1 of the microcontroller and the count is again displayed both in the LCD and LED display .

After covering the required distance of (400-500) meters, the vehicle cuts the sensors kept at the finish line. The pulse thus produced is fed to the DTMF encoder that encodes the pulse in terms of '0's and '1's. This encoded message is then transmitted to the start using an FM transmitter. At the start, the encoded message is received by an FM receiver, that directly feeds to the DTMF decoder. Once the message is decoded , it is fed to the higher order bits of the

buffer that is constantly checked for any inputs . These decoded bits deactivate the TIMERS '1' and ' 0' and the final time elapsed is displayed in the LCD and LED displays .In order to start the process all over again, for a new vehicle , the 'RESET' key is used .

HARDWARE

MICRO CONTROLLER

3.1 8031 MICRO-CONTROLLER

FEATURES:-

The 8031 MICRO- CONTROLLER consists of the following:

- 8 bit CPU
- 128 Bytes of ON – CHIP RAM
- 21 Special fuction registers
- Extensive Boolean processing (single bit logic) capablities
- Full Duplex UART
- 6 Source/ 5-vector interrupt structure in two priority levels
- Two 16-bit / counters
- 64 K program memory address space
- 64 K data memory address space
- 32 bi-directional and individually addressable I/O lines
- 4 K ROM
- ON-CHIP clock oscillator

INTERRUPTS:

In order to use any of the interrupts in 8031 the following steps must be taken;

1. Set the EA (ENABLE ALL) bit in the IE register to 1
2. Set the corresponding individual interrupt enable bit in the IE register to 1
3. Begin the Interrupt Service Routine at the corresponding vector address of that interrupt

INTERRUPT SOURCE	VECTOR ADDRESS
IE 0	0003 H
TF 0	000B H
1E 1	0013 H
TF 1	001B H
R1 & T1	0023 H
TF2 & EXF2	002B H

For external interrupts $\overline{\text{INT 0}}$ ⟶ P3.2 and $\overline{\text{INT 1}}$ ⟶ P3.3 must be set to 1 .

For the interrupt is to be level or transition activated .

ITx = 0 → Level activated

ITx = 1 → Transition activated

PIN CONFIGURATION:

Vcc:

Supply Voltage.

Vss:

Circuit ground.

PORT 0:-

PORT 0 is an 8 bit open drain bi direction I/O port. As an output port each pin can sink 8 LS TTL inputs. PORT 0 is also the multiplexed low order address and data bus during access to external program and data memory.

PORT 1:-

PORT 1 is an 8 bit bi -directional I/O port with internal pullups .The port 1 output buffers can sink source 4 LS TTL inputs.

PORT 2:-

PORT 2 is an 8 bit bi - directional I/O port with internal pullups. It emits the higher order address byte during access to external memory. It also receives the higher order address byte and control signals during program verification . Port 2 can sink / source 4 LS TTL inputs.

PORT 3:-

PORT 3 is an 8 bit bi – directional I/O port with internal pullups. It also serves the function of various special features of the MCS 51 family as listed below

PORT PIN	ALTERNATIVE FUNCTION
P 3.0	RXD (Serial I/P port)
P 3.1	TXD (Serial O/P port)
P 3.2	$\overline{\text{INTO}}$ (External interrupt 0)
P 3.3	$\overline{\text{INT 1}}$ (External interrupt 1)
P 3.4	T 0 (Timer 0 external Input)
P 3.5	T 1 (Timer 1 external input)
P 3.6	$\overline{\text{WR}}$ (external data memory with strobe)
P 3.7	$\overline{\text{RD}}$ (external data memory with strobe)

RST :

Reset Input . A HIGH on this pin for two machine cycles while the oscillator is running resets the device .

ALE :

Address Latch Enable output pulse for latching the low byte as the address during accesses to external memory .

$\overline{\text{PSEN}}$:

Program Store Enable is the read strobe to external program memory . $\overline{\text{PSEN}}$ is activated twice each machine cycle during fetches from external program memory. $\overline{\text{PSEN}}$ is the not activated during fetches from natural internal program memory .

$\overline{\text{EA}}$:

When $\overline{\text{EA}}$ is held HIGH the CPU executes out as internal program memory . When $\overline{\text{EA}}$ is held LOW the CPU executes out as external program memory .

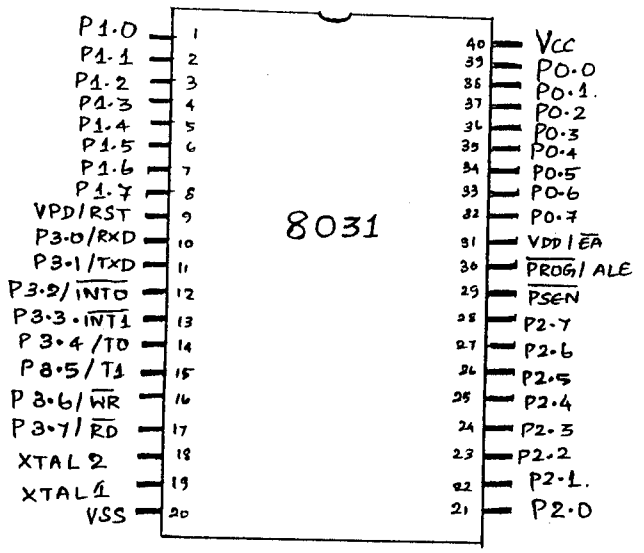
XTAL 1:

Input to the inverting oscillator amplifier .

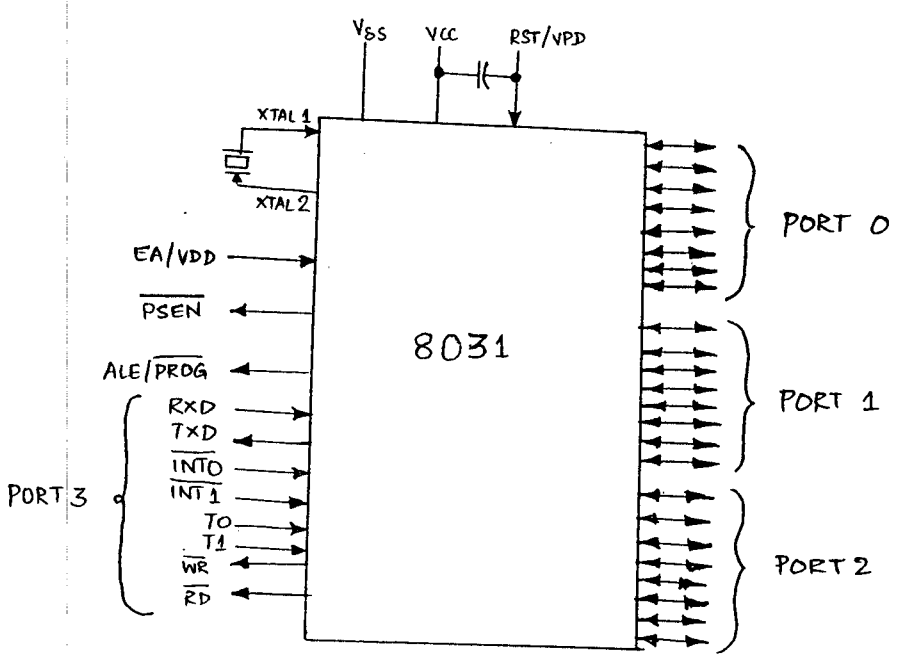
XTAL 2 :

Output to the inverting oscillator amplifier.

8031 MICROCONTROLLER PINOUT DIAGRAM.



8031 MICROCONTROLLER LOGIC DIAGRAM.



3.1.1 8031 MICROCONTROLLER INTERFACING WITH EXTERNAL PROGRAM AND DATA MEMORY.

Port Bit Assignment:

Port 0 : Multiplexed Address / Date bus AD0 – AD7

Port 1 : P1.0 – P1.4 is used to control the five traffic lights

Port 2 : Higher order Address Bus A8 – A15.

Port 3 : P3.2 bit (INT0) is used for output of sensor at start.

- Lower order 4 bits of INPUT LATCH (74LS573) is used for keys (RESET Key, START Key, INCREMENT key, DECREMENT Key)
- Higher order 4 bits of INPUT LATCH (74LS573) is used for out put DTMF receiver.

3.1.2 TIMER:

In 8031 micro controller, two timers are there namely Timer 0 and Timer 1.

TCON: TIMER/COUNTER CONTROL REGISTER, BIT ADDRESSABLE.

TF1	TR1	TFO	TR0	IE1	IT1	IE0	IT0

TF1 - Timer 1 overflow flag, set by hardware when Timer/Counter 1 overflows, cleared by hardware as processor vector to the interrupt service routine.

TF0 - Timer 0 overflow flag, set by hardware when the Timer / counter 0 overflows, cleared by hardware as processor vector to the service routine.

TR0 - Timer 0 run control bit , set/cleared by software to turn timer / counter 0 ON/OFF.

IE1 - External Interrupt 1 edge flag, set by hardware when external interrupt edge is detected, cleared by hardware when interrupt is processed.

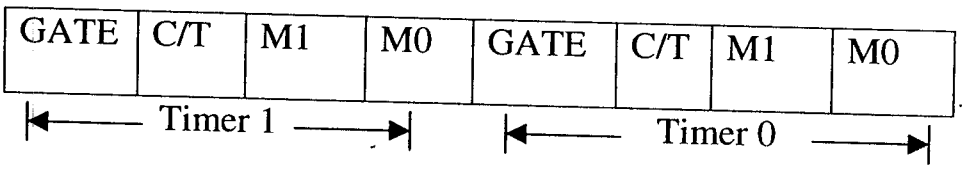
IT1 - Interrupt 1 type control bit, set/cleared by software to specify falling edge/low level triggered external interrupt.

IE0 - External interrupt 0 edge flag, set by hardware when external interrupt edge detected, cleared by hardware when interrupt is processed.

IT0 - Interrupt 0 type control bit, set / cleared by software to specify falling edge / low level triggered external interrupt.

TMOD: TIMER /COUNTER MODE CONTROL REGISTER

NOT BIT ADDRESSABLE



GATE - When TRX (in TCON) is set and GATE=1 Timer/Counter X will run only while INTXPin is high (hardware control)

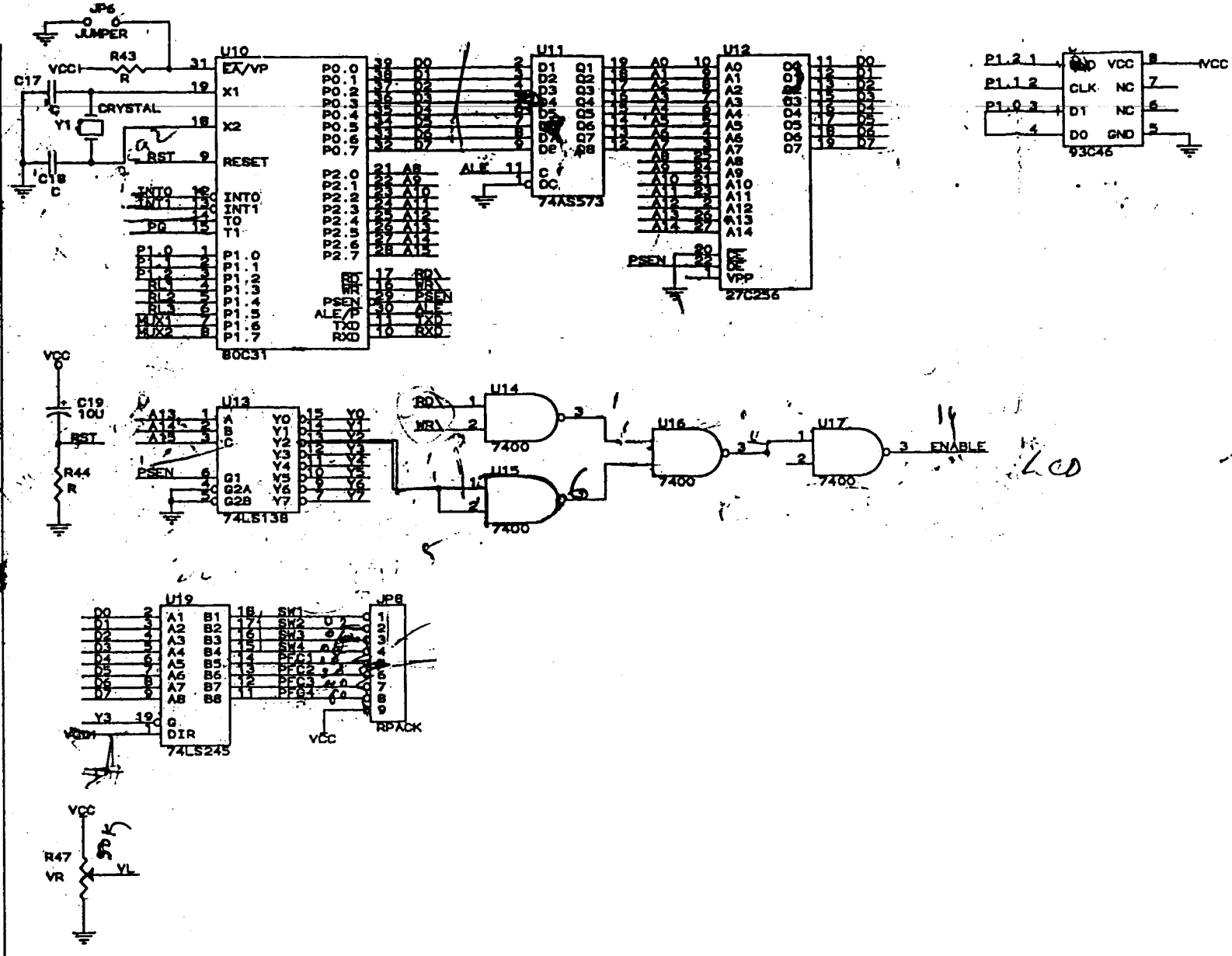
Whcn GATE=0 TIMER/COUNTER X will run only while TRX=1 (Software Control)

C/T - Timer or Counter Selector, cleared for Timer Operation, set for Counter Operation (Input from TXpin)

Modes -

M1	M2	Operating mode
0	0	0 13-bit timer (mcs-48 Comptaible)
0	1	1 16-bit timer/counter
1	0	2 8-bit Auto – reload Timer/counter
1	1	3 (Timer 0) TL0 is an 8-bit Timer/Counter controlled by the standard Timer 0 control bits, THO is an 8-bit Timer and is controlled by Timer 1 control bits.
1	1	3 (Timer1) Timer/counter 1 stopped.

Interfacing With External Program And Data Memory



3.1.3 DECODER:

THE HC138A decodes a three-bit address to one of eight active LOW outputs. This device features three chip select inputs, two active LOW and active –HIGH to facilitate the demultiplexing, cascading and chip – selecting functions.

3.1.4 LATCH:

The Latch (74LS573) appears transparent to data i.e., output changes asynchronously, when latch enable is HIGH. When the Latch enable goes LOW, data meeting the setup and hold times becomes latches.

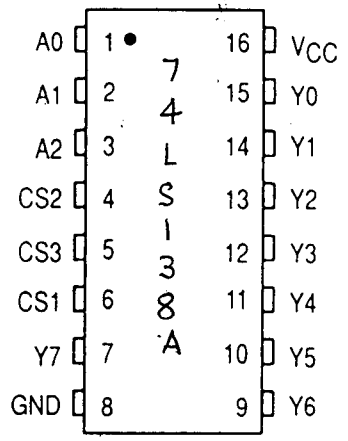
3.1.5 BUFFER:

The HC245A is a 3-state non inverting transceiver that is used for 2 way asynchronous communication between data buses. The device has an active – LOW output enable pin which is used to place the input ports into HIGH impedance states.

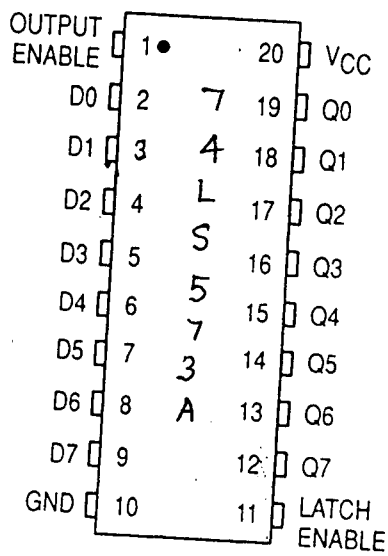
3.1.6 EPROM:

Eerasable programmable read only memory (EPROM) stores a bit by changing the floating gate of an FET. Information is stored by using an EPROM programmer which applies high voltages to charge the gate. All the

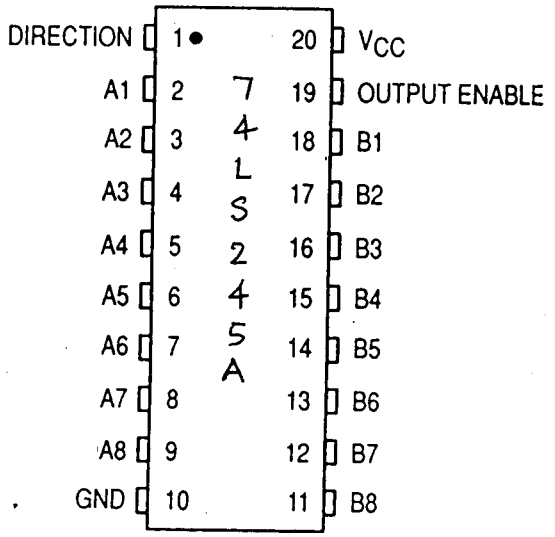
DECODER



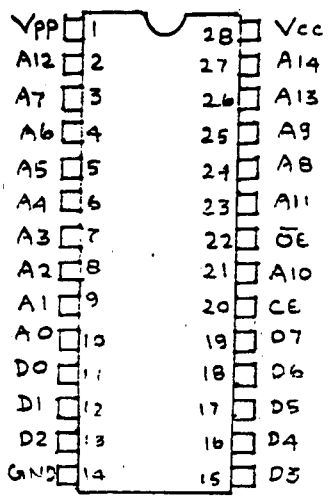
LATCH



BUFFER



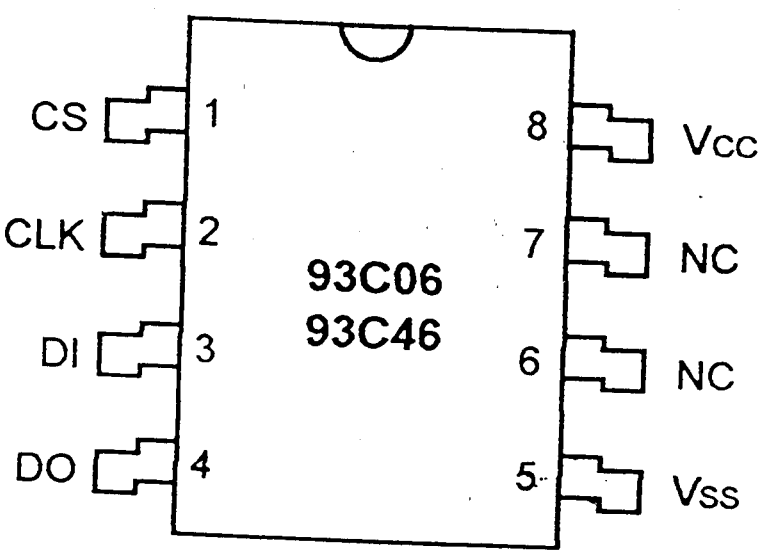
EPROM.



information can be erased by exposing the chip to ultraviolet light through its quartz window and the chip can be reprogrammed.

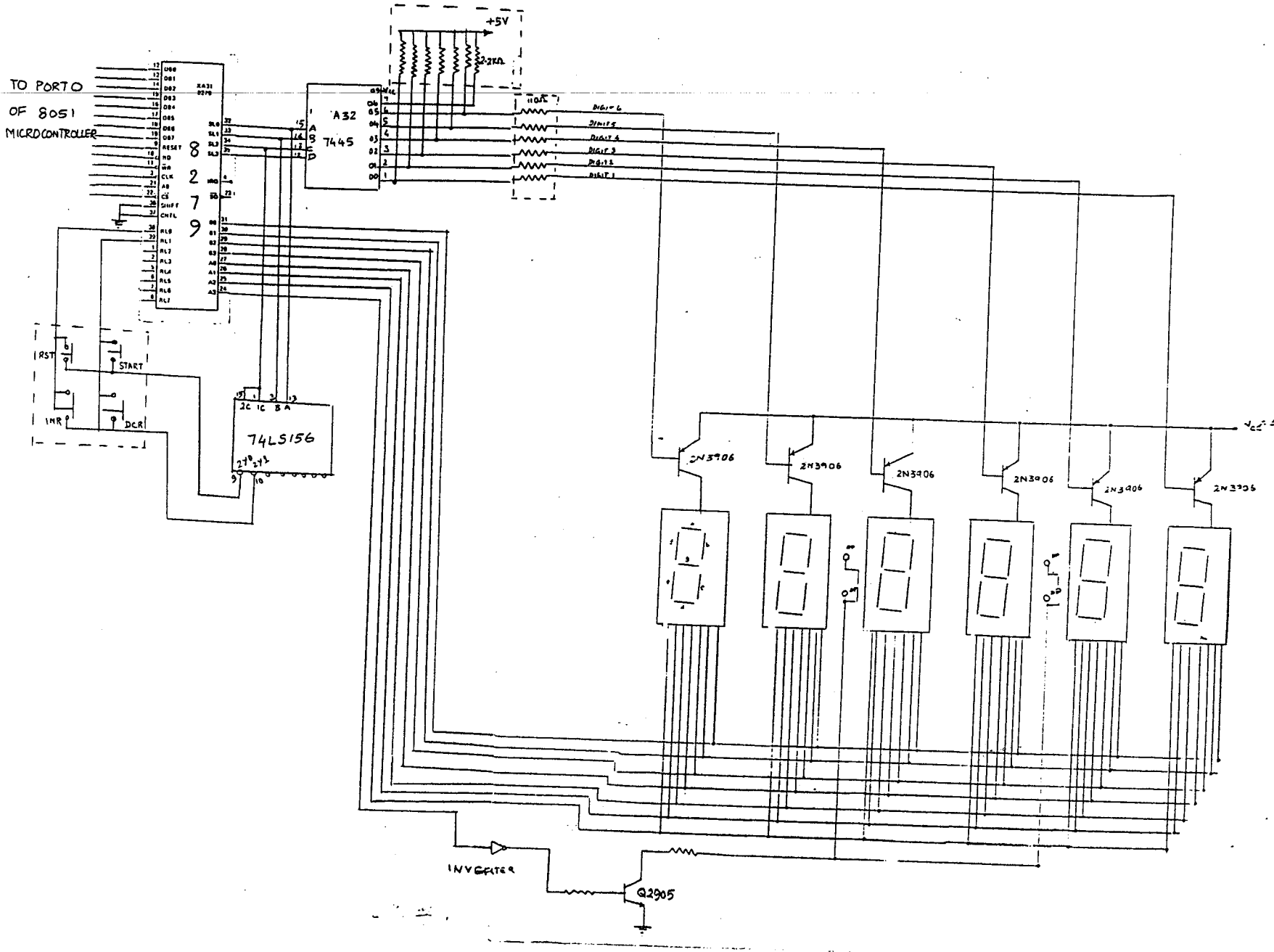
3.1.7 EEPROM:

Electrically erasable PROM (IC 93C06/46) is functionally similar to EPROM except that information can be altered by using electrical signals at the register level rather than erasing all the information. This is mainly used in remote control application.



KEYBOARD / DISPLAY

KEYBOARD AND DISPLAY INTERFACE USING 8279



3.2 KEYBOARD AND DISPLAY INTERFACE WITH 8279

3.2.1 8279:

8279 is a dedicated keyboard and display controller usually interfaced with the microcontroller. The chip automatically controls the display refreshing and multiplexing. It contains the debounce circuitry needed for any normal key switch. It also contains an 8x3 – bit RAM which can be configured as a first in first out (FIFO) buffer or it can represent the actual condition of all switches at any given time.

3.2.1.1 CONTROLLING DISPLAY USING MULTIPLEXING TECHNIQUE:

Multiplexing is the technique where only one digit is ON at a time in a sequence, which continues indefinitely. Since ON time is in micro seconds, the display appears as static for human eye.

The seven segment codes for the numbers to be displayed is stored in a 16 bit RAM. The 8279 first outputs the binary number for the first digit to 7445 decoder on scan lines to turn one of the digit driver transistor. The 8279 then outputs the seven segment code for the first digit on the A3-A0 & B3-B0 lines. This will light the first digit with the desired pattern. After

around 490 micro seconds, the 8279 produces a blanking code for 120 micro seconds to avoid ghosting of information from one digit to the next. Next the seven segment for digit 2 is put on A&B lines. This then lights the desired pattern on digit 2. After 490 micro seconds, the 8279 blanks the display again and goes as to digit 3 , this process continues repeatedly. With 6 digits it takes a total of 4 milli seconds to come to digit one, called scan time. This it automatically keeps the display refreshed.

3.2.1.2 SCANNING THE KEYBOARD MATRIX

The count sequence from scan lines through the 74LS156 decoder puts a low on one row of the key-board at time. The column lines of the keyboard are connected to the return lines, RL0 – RL7 of 8279. As a low is put on each row, the 8279 checks these return lines one at a time to see if any of them are low. If 8279 finds any of return lines low, indicating a keypress, it waits for a debounce time of about 10 milli seconds and checks again. If the key is still pressed, the 8279 produces an 8-bit code . Three bits of this code represent the row in which it found the pressed key and another 3 bits represent the column of the pressed key. The upper 2 bits of the SHIFT and CONTROL key. The 8 bit code is stored in 8 byte FIFO RAM.

3.2.2 KEYPAD :

The keypad consists of four keys namely the increment decrement , reset and start key. The reset key is used in case there happens to be a false start .

The increment and decrement keys are used to move to the next and previous competitor respectively. Start key is used to start the entire process . The scanning of keypad is done by 2 X 2 matrix in the 8279 controller .

3.2.3 DECODERS :

The digit selection of the display is done through a 7445 BCD to DECIMAL decoder called the 1 of 10 low decoder . When a four bit BCD code from scan lines of 8279 is applied to the input of decoder , the output corresponding to that BCD number will go low .

The 8279 generates a continous count sequence from 0000 to 1111 over and over again . This causes digits to be selected one by one using the multiplexing technique.

Another decoder used is 74LS156 1 to 8 low decoder , which selects the output according to the binary input. This also acts in continuos count sequence such that one row is kept low and the columns are checked . Then it moves to the next low and so on. Here as we use just four keys , only two binary inputs are given . The 3 to 8 decoder

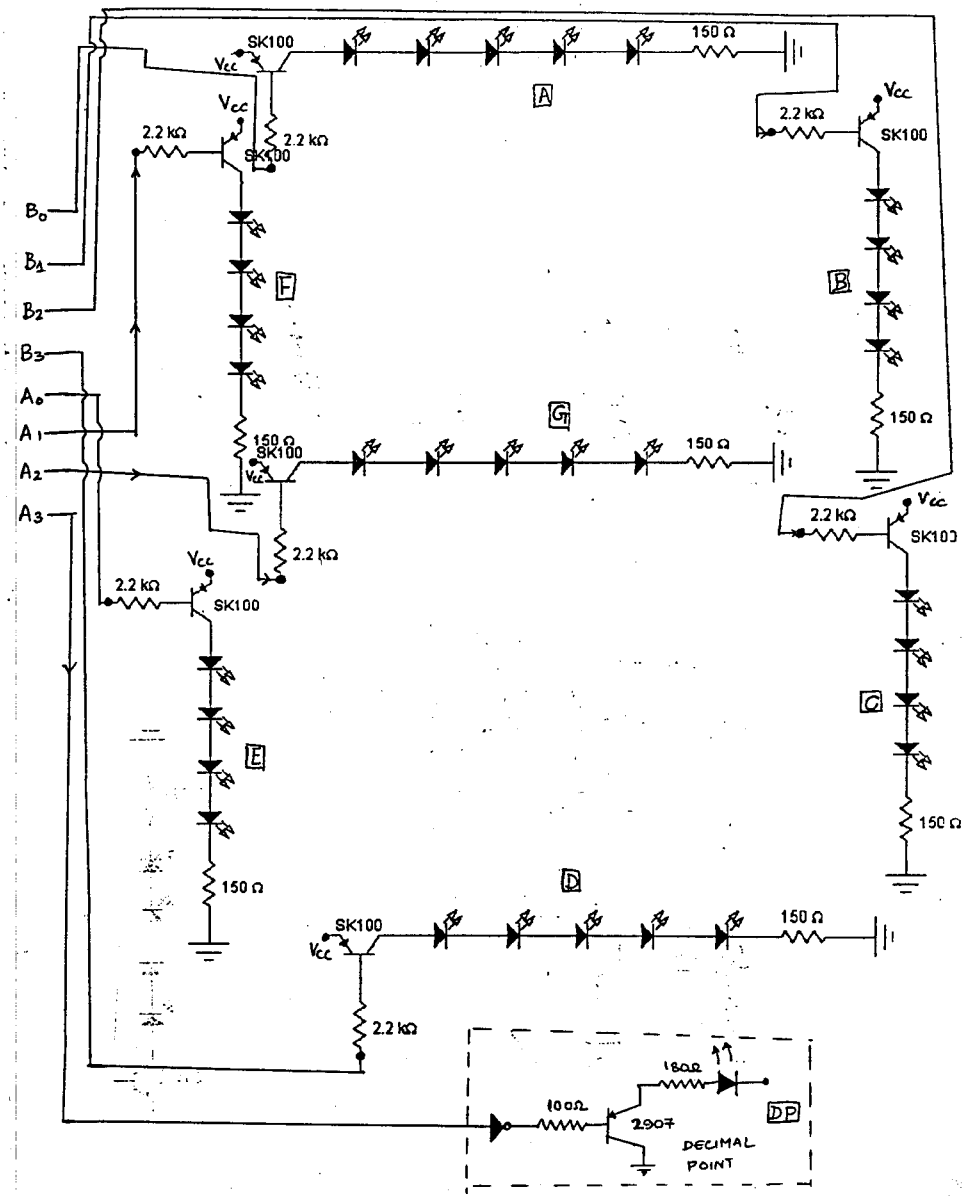
is used as a purpose of future expansion if the number of keys are to be increased .

3.2.4 LAYOUT :

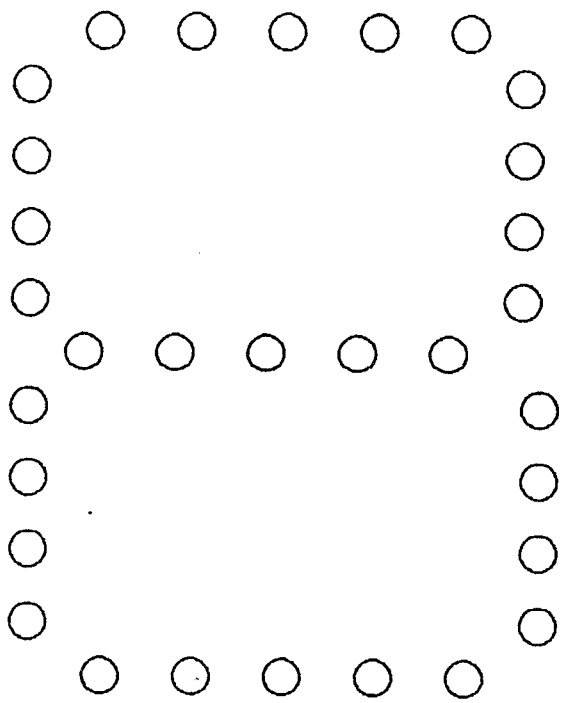
The layout of one digit uses 10mm LEDs . Here four LEDs are used in vertical segment and five LEDs are used in horizontal segment with a total height of six inches and length of 4.5 inches .

3.2.5 CIRCUITRY:

Each segment requires 20 to 30 m A to drive the LEDs. The 8279 can only source around 0.2 to 0.3 m A , so to drive the LEDs connected in series. We use driver transistor BC548 with beta value of around 100 with seven segment in one digit a total of 200 m A is drawn from supply when one digit is turned ON . Since we use multiplexing only 200 m A is consumed when display is ON and power consumption is reduced to great extent .


SK100
Vcc
150 Ω
A
2.2 kΩ
B
F
G
C
E
D
DP
B0
B1
B2
B3
A0
A1
A2
A3
100Ω
180Ω
2907
DECIMAL
POINT

LAYOUT FOR ONE DIGIT



COMMUNICATION

3.3 COMMUNICATION

As it is a wireless transmission from finish to start of the race (400metres) ,the efficient method of transmission would be using frequency modulation.

3.3.1 FREQUENCY MODULATION :

Frequency modulation is a system in which the amplitude of the modulated carrier is kept constant , while its frequency is varied by modulating signal. FM transmission is more resistant to noise . The amount by which the carrier frequency is varied from its unmodulated value , called the deviation, is made propotional to the instantaneous value of the modulating voltage . The rate at which this frequency variation or oscillation takes place is naturally equal to the modulating frequency . The amplitude of frequency modulated wave remains constant at all times; this is , infact the greatest single advantage of FM .

3.3.1.1 Mathematical representation of FM :

The instantaneous frequency 'f ' of the frequency modulated wave is given by

$$f = fc\ (1+k\ Vm\ Cos\ wmt)$$

where

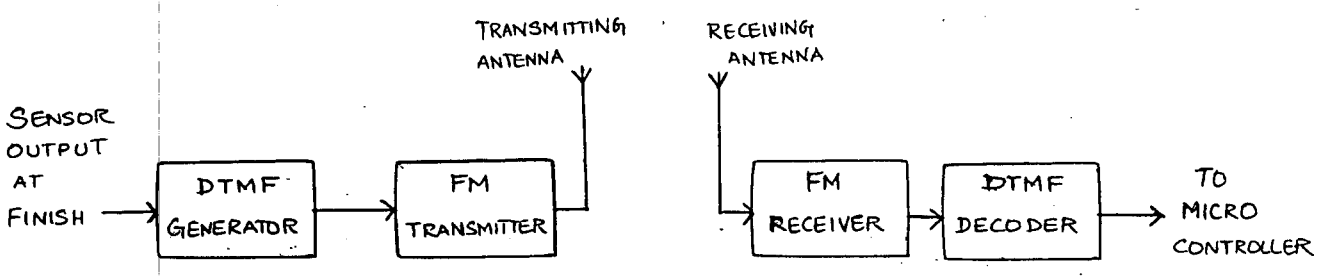
fc = unmodulated carrier frequency .

k = propotionality constant .

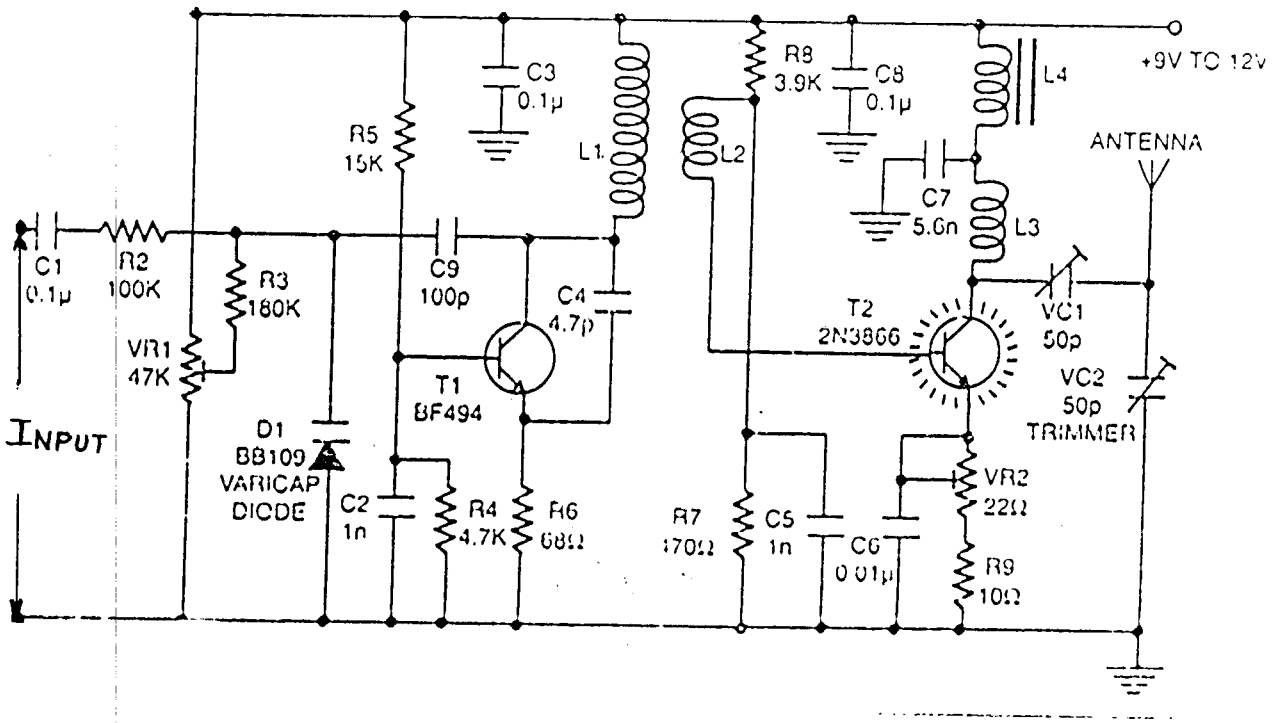
Vm CosWmt= instantaneous modulating voltage .

3.3.2 FM TRANSMITTER :

- **BLOCK DIAGRAM**



- **CIRCUIT DIAGRAM**



3.3.2.1 REACTANCE MODULATOR METHOD :

- **VARACTOR DIODE :**

Varactor diode is a semiconductor diode whose junction capacitance varies linearly with applied bias when the diode is back-biased .

Varactor diode may also be used to produce frequency modulation ; they are employed togather with a reactance modulator , to provide automatic frequency correction for an FM transmitter. It is seen that the diode has been back-biased to provide the junction capacitance effect , and since this is varied by the modulating voltage which is in series with it, the junction capacitance will also vary, causing the oscillator frequency to change accordingly .

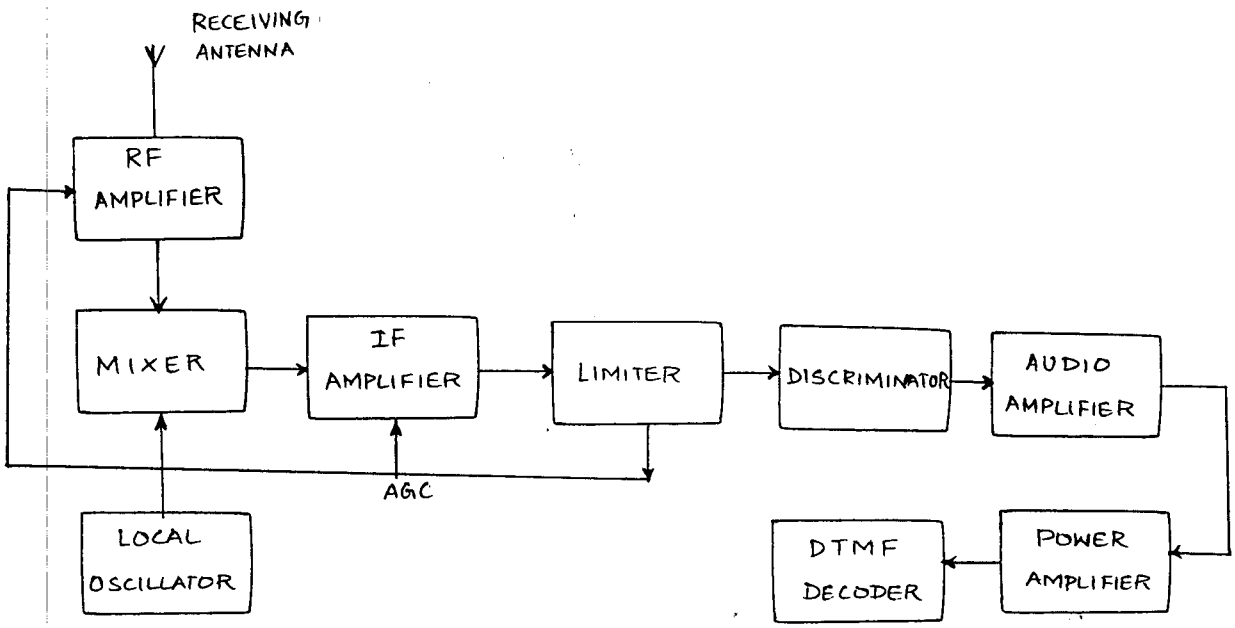
3.3.2.2 DESCRIPTION OF CIRCUIT :

The circuit built around transmitter T1(BF494) is a basic low-power variable frequency VHF oscillator . The output of the oscillator is about 50mW . Transistor T2(2N3866) forms a VHF class. A power amplifier . It boosts the oscillator signal's power four to five times. Thus , 200-250 mW of power is generated at the collector of transistor T2 .

Potentiometer VR1 is used to vary the fundamental frequency whereas potentiometer VR2 is used as power control . Transistor T2 must be mounted on a heat sink . Adjust both trimmers VC1 and VC2 for maximum transmission power .

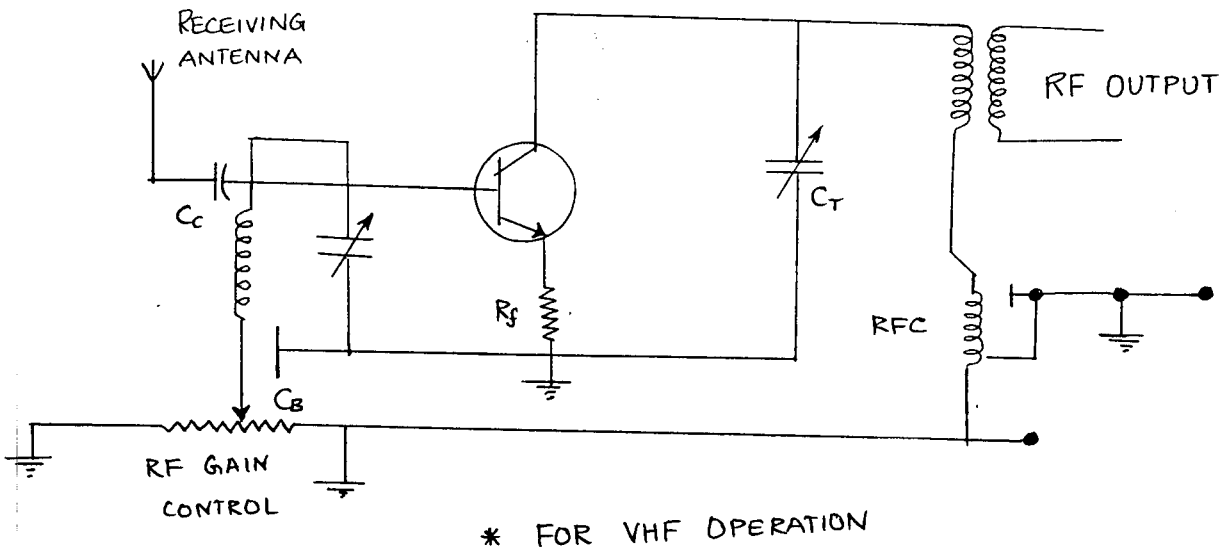
3.3.3 FM RECEIVER

The FM Receiver is a superheterodyne receiver, and the block diagram is given below



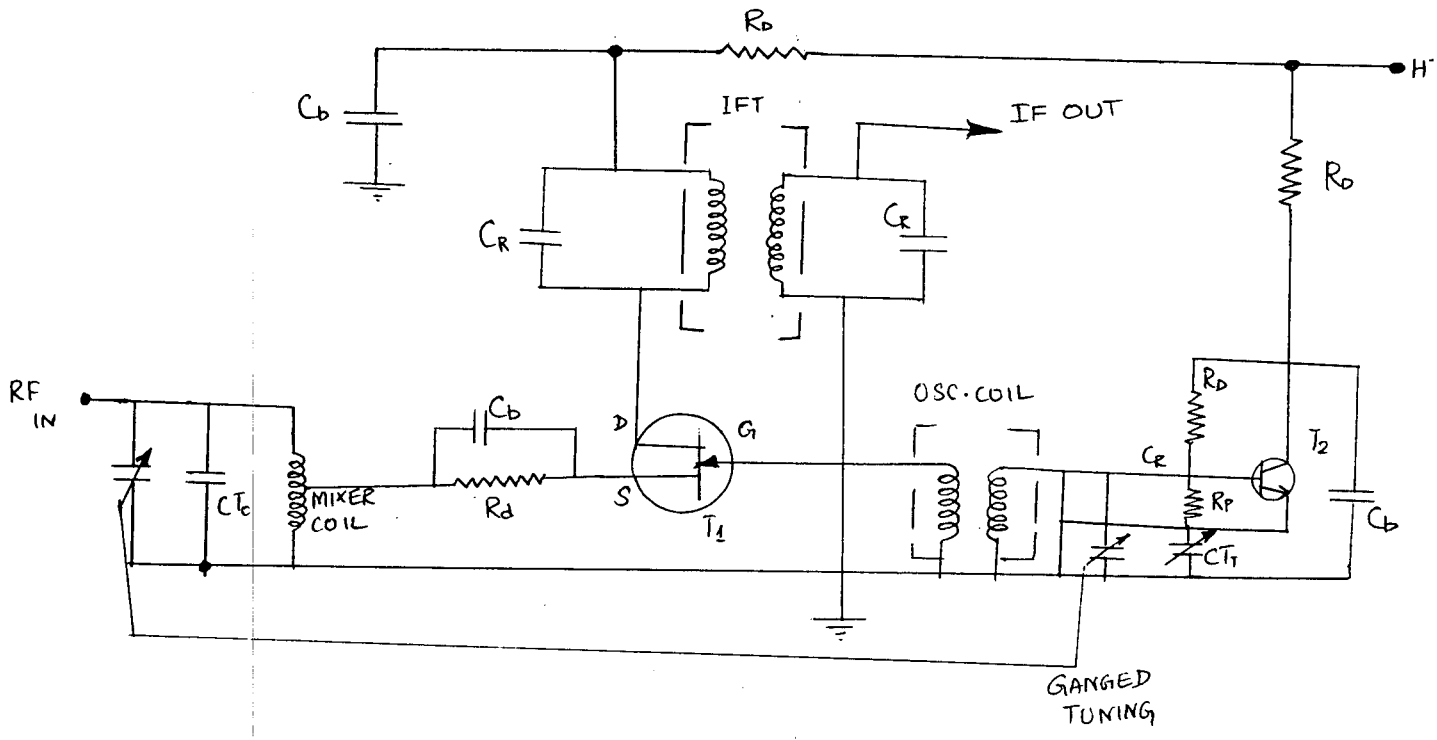
3.3.3.1 RF AMPLIFIER:

An RF amplifier is always used in an FM receiver .It's main purpose is to reduce the bandwidths needed for FM. It is also required to match the input impedance of the receiver to that of antenna.



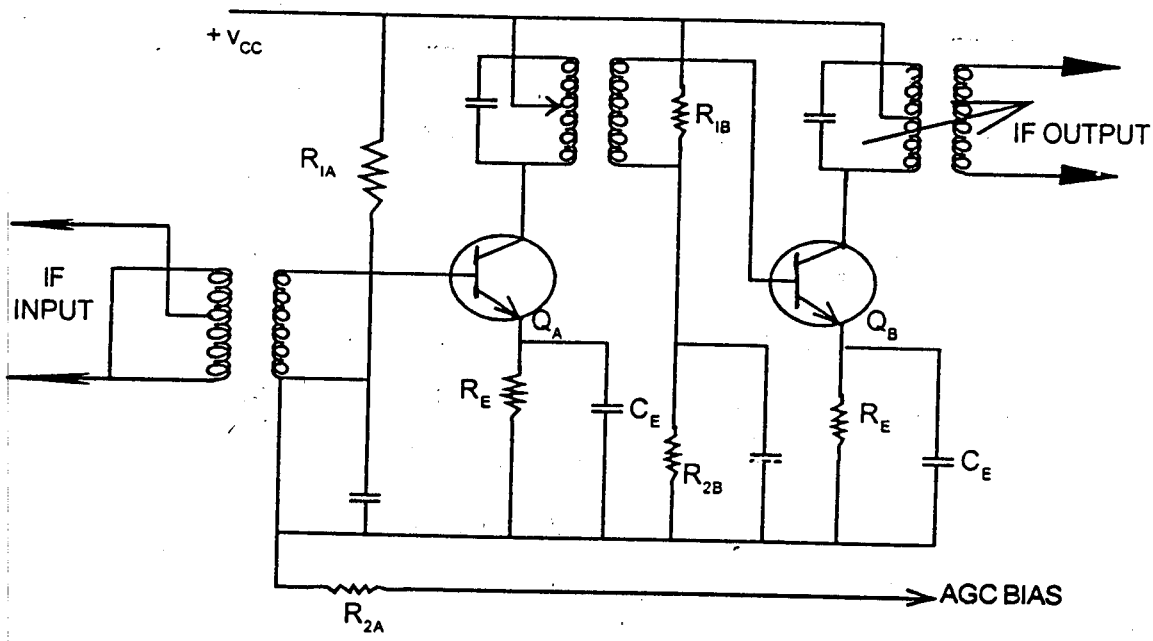
3.3.3.2 MIXERS:

The oscillator circuit takes any of the usual forms,with a colpitt's and clapp predominant, being suited to VHF operation. A very satisfactory arrangement for the front end of an FM receiver consists of FETs for the RF amplifier and mixer , and a bipolar transistor . Separately excited oscillators are normally used.



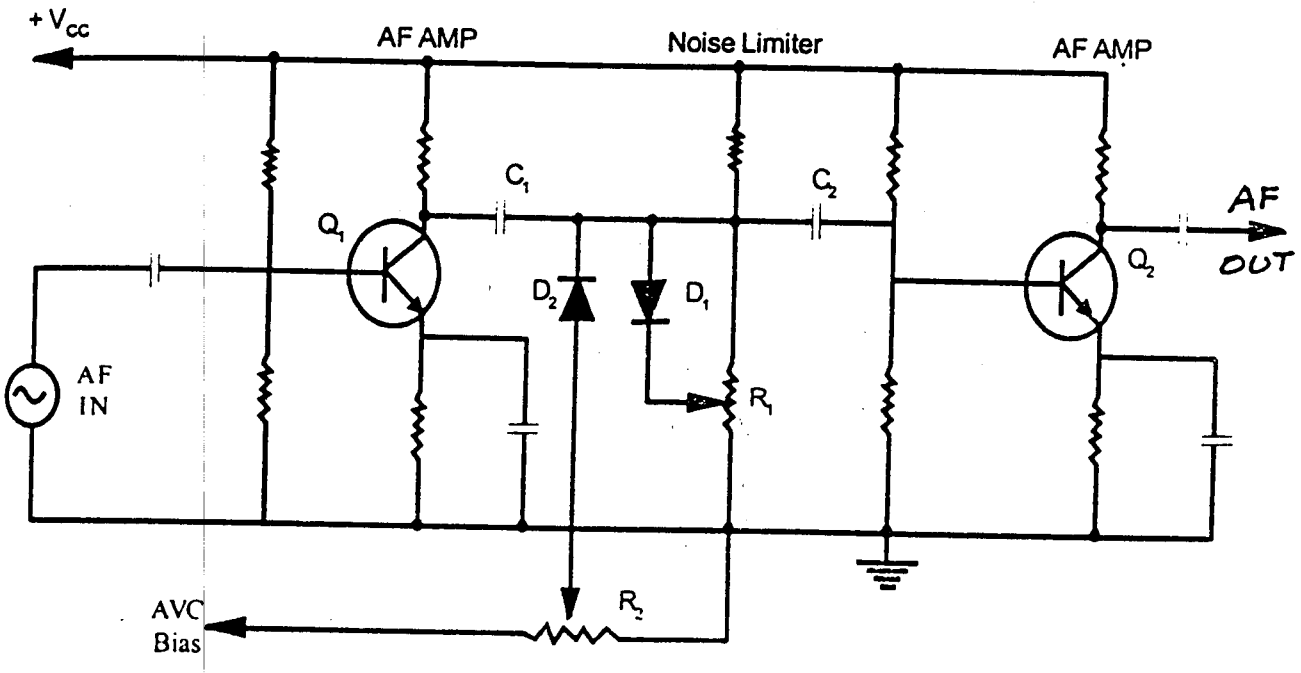
3.3.3.3 INTERMEDIATE FREQUENCY AMPLIFIERS:

Very high intermediate frequency and bandwidth is required for FM receiver.Typical receivers operating at 88 – 108 MHz band have an IF of 10.7 MHz and a bandwidth of 200 KHz . As bandwidth increases ,the gain per stage may be low.Hence two IF amplifier stages are often used.



3.3.3.4 AMPLITUDE LIMITING :

An amplitude limiter should be used in an FM receiver to make the full advantage provided by FM demodulator . On the grounds that any amplitude changes in the signal fed to the FM demodulator are spurious .They must therfore be removed if distortion is to be avoided. The limiter is a form of clipping device , a circuit whose output tends to remain constant despite changes in the input signal A potentiometer is used to limit the amplitude in the circuit.


+ V_{cc}
AF AMP
Noise Limiter
AF AMP
C_1
C_2
Q_1
Q_2
AF
OUT
D_2
D_1
AF
IN
R_1
AVC
Bias
R_2

3.3.4 DTMF CODING

Dual tone multiple frequency (DTMF) addresssignaling is used by the telephone industry to signal over the voice transmission path of the telephone system . A signaling method that employs fixed combinations of two specific voice frequencies , one of which is selected from a group of four low frequencies , and the other from the group of either three or four relatively high frequencies .

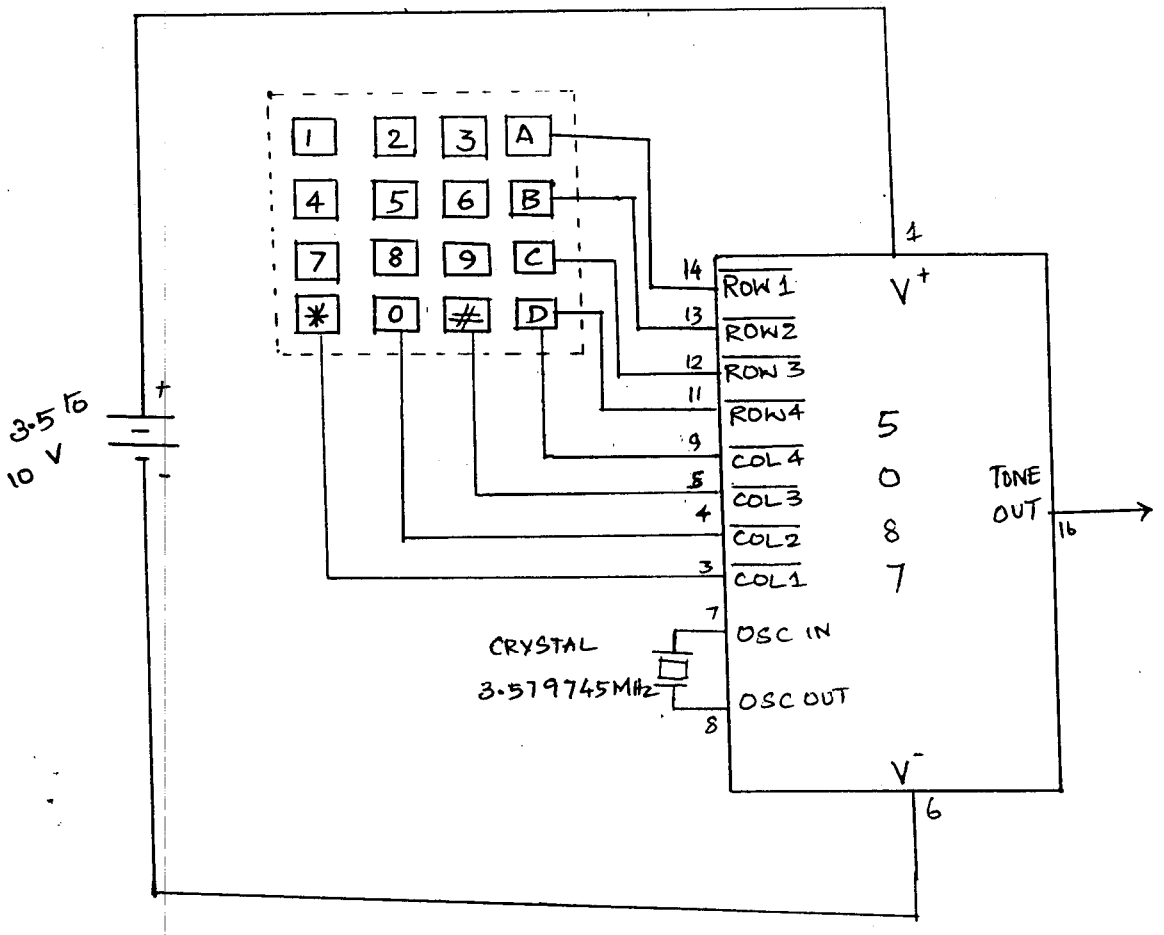
This method of signaling uses 16 distinct voice band frequency signals , each consisting of two sinusoidal signals ,one from a " low group " and one from a " high group " of frequencies . The characters that represent is DTMF signals are as shown in the table

Nominal low group frequencies (hertz)	Nominal high – group frequencies (hertz)			
	1209	1336	1447	1663
697	1	2	3	A
770	4	5	6	B
852	7	8	9	C
941	*	0	#	D

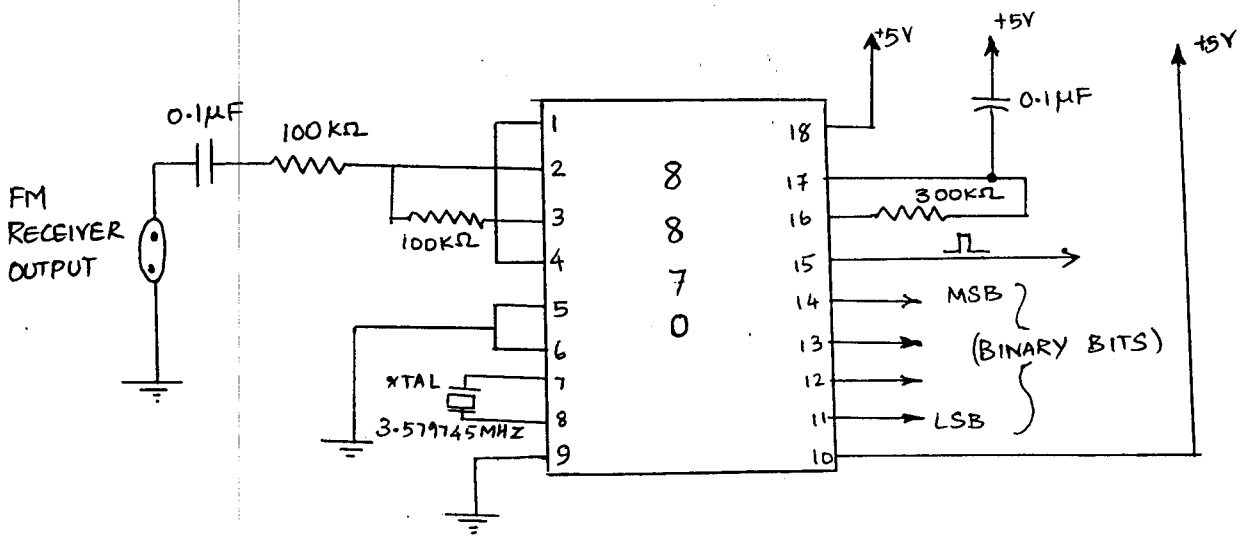
A , B , C, and D buttons are used in special applications and are not part of common telephone keyboard.

DTMF signals , unlike dial pulses , can pass through the entire connection to the called party , and therefore lend themselves to various schemes such as remote control or tone coded data transmission , after the connection is established .

BASIC DTMF ENCODER CIRCUIT



DTMF DECODER



FEATURES :

- Low power consumption .
- Adjustable acquisition and release times .
- Power - down and inhibit modes .
- Single 5 volt power supply .
- Dial tone suppression .

APPLICATION :

- Telephone switch equipment .

8870 DECODER :

8870 decoder uses a digital counting technique to determine the frequencies of the limited tones and to verify that they correspond to standard DTMF frequencies . A complex averaging algorithm is used to protect against tone simulation by extraneous signals while tolerating small frequency variations .

3.3.5 DTMF DECODER

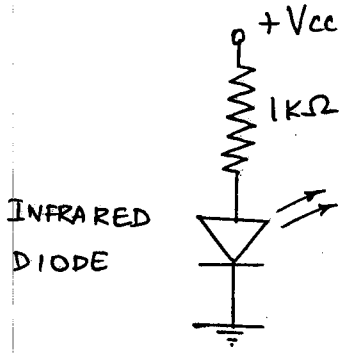
8870 is a full DTMF receiver that integrates with bandsplit filter and decoder functions into a single 18 – pin IP package. Manufactured using state - of – the - art CMOS process technology, the M 8870 offers low power consumption and precise data handling. It's filter section uses switched capacitor technology for both the low and high group filters and for dial tone rejection .

It uses digital counting techniques to detect and decode all 16 DTMF tone pairs into 4 - bit codes . External component count is minimised by provision of an on - chip differential amplifier, clock generator and latched tri – state interface bus . Minimal external components required to include a low – cost 3.579745 MHz color burst crystal , a timing resistor and a timing capacitor .

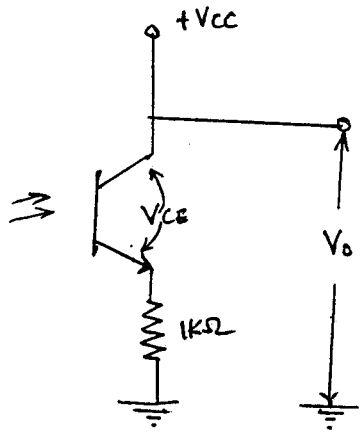
SENSORS

3.4 SENSORS

CIRCUIT :

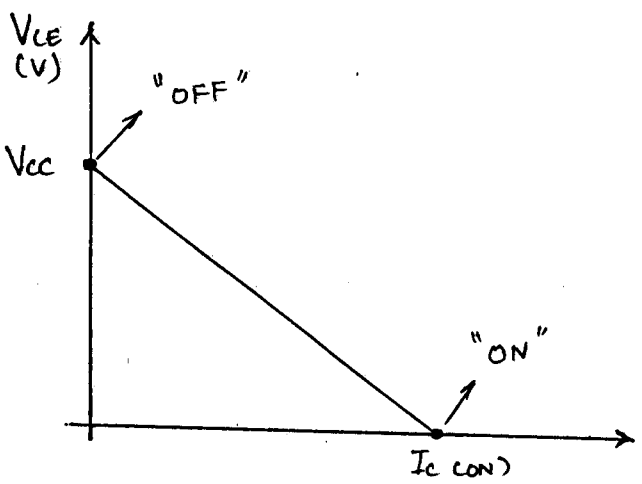


IR
TRANSMITTER



IR
RECEIVER

CHARACTERISTICS :



SOFTWARE

SOFTWARE OVERVIEW :

Software consists of an application software and the assembly language programming .The application software is written in **C** for **DOS** environment.The assembly language program is also written in **C** which is cross compiled using an **AVC51** cross compiler which converts **C** code into hexadecimal code for **8031 microcontroller** and is written to the **EPROM** using a **EPROM** programmer.

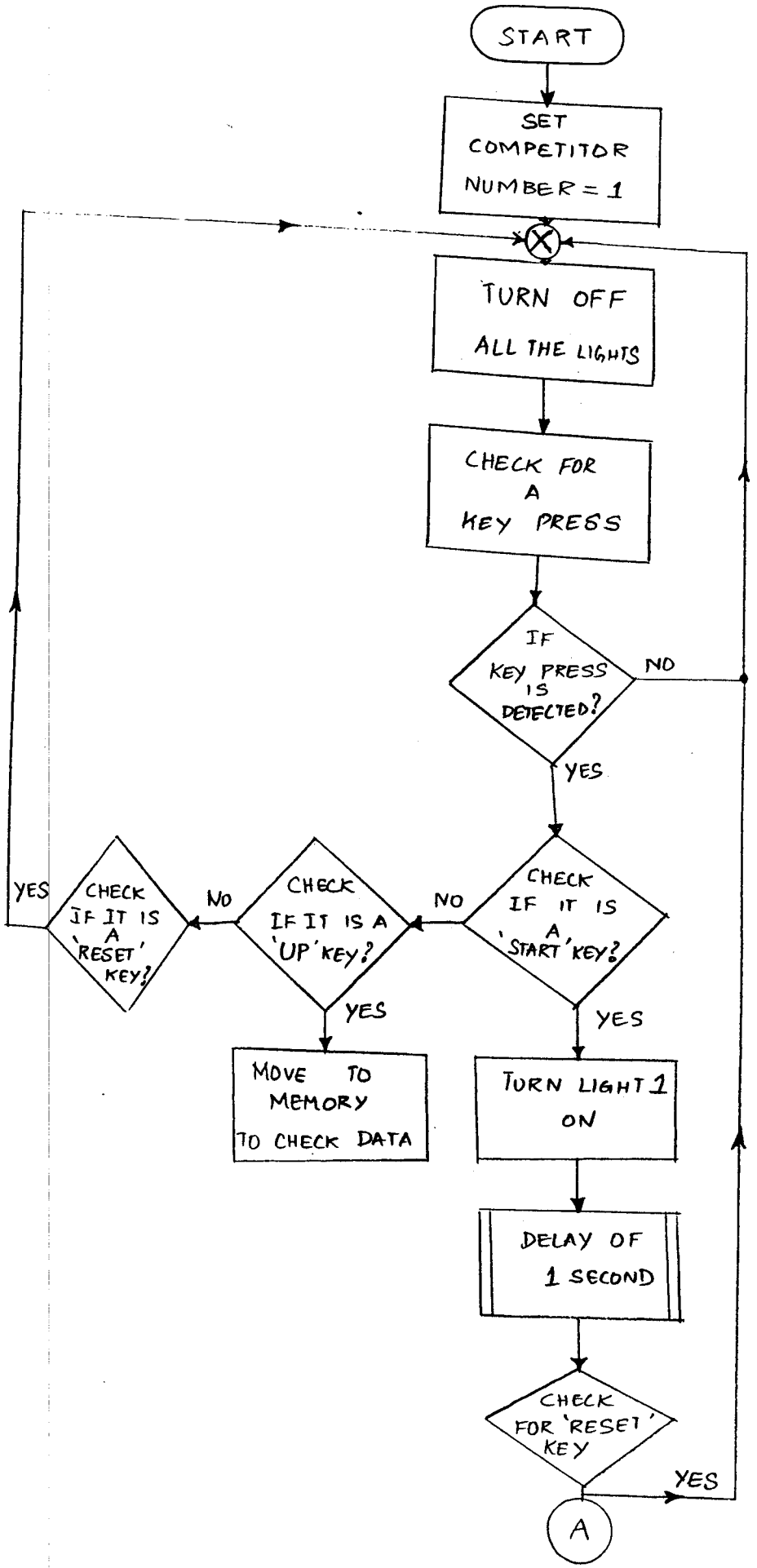
The application software consists of the following modules:

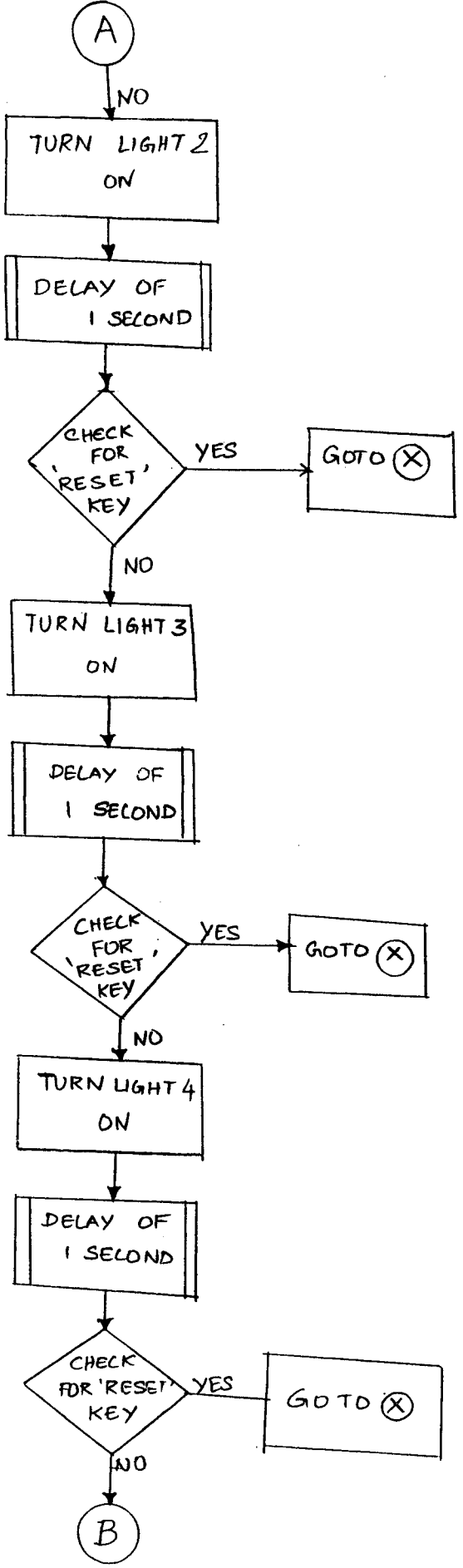
- To turn **ON** the traffic lights.
- To turn the **TIMER ON** when the vehicle cuts the sensor .
- To display the time using the **LCD** display.
- To deactivate the **TIMER** at the end of the test run.
- To store the results in the **EEPROM.**

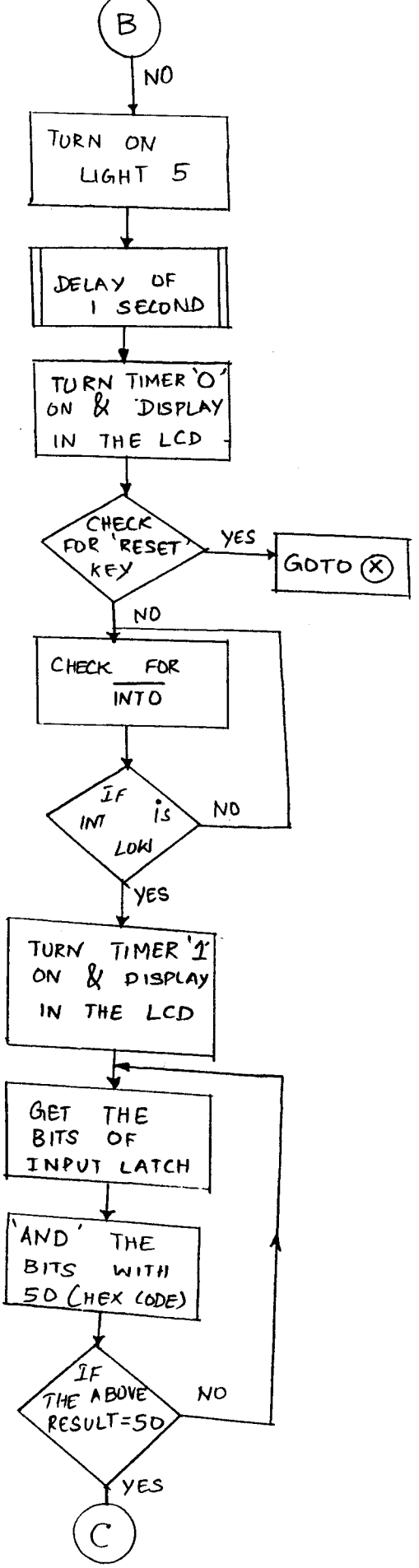
ASSEMBLY LANGUAGE PROGRAM(FIRMWARE):

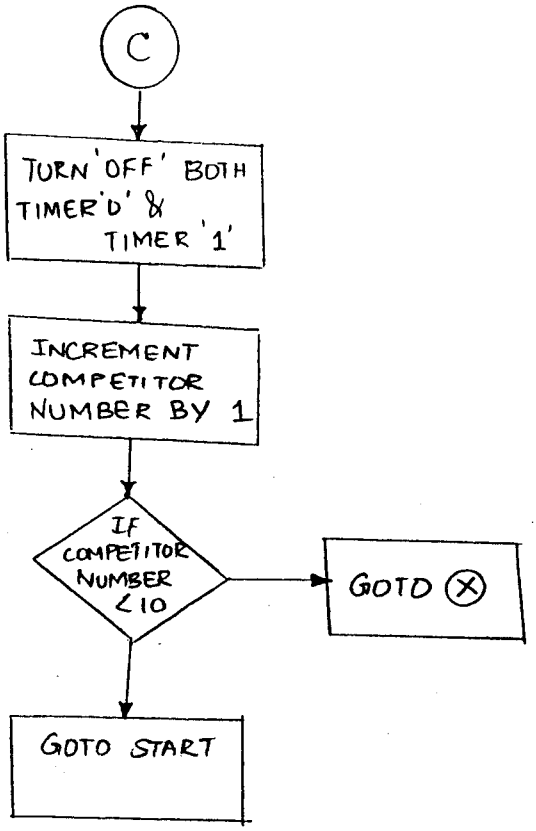
This performs the following :

1. Initialises **8031** registers .
2. Initialises the interrupt service subroutines so that the processor updates the memory locations.
3. Initialises the **LCD** display module.
4. The processor after initialising all the interrupt services subroutines checks for the interrupt in the **INT0** pin which gets activated when the vehicle cuts the sensor at the start. At the same time the **TIMER0** also gets activated.


START
SET COMPETITOR NUMBER = 1
TURN OFF ALL THE LIGHTS
CHECK FOR A KEY PRESS
IF KEY PRESS IS DETECTED?
NO
YES
CHECK IF IT IS A 'START' KEY?
NO
CHECK IF IT IS A 'UP' KEY?
NO
CHECK IF IT IS A 'RESET' KEY?
YES
YES
YES
TURN LIGHT 1 ON
MOVE TO MEMORY TO CHECK DATA
DELAY OF 1 SECOND
CHECK FOR 'RESET' KEY
YES
A


A
NO
TURN LIGHT 2 ON
DELAY OF 1 SECOND
CHECK FOR 'RESET' KEY
YES
GOTO ⊗
NO
TURN LIGHT 3 ON
DELAY OF 1 SECOND
CHECK FOR 'RESET' KEY
YES
GOTO ⊗
NO
TURN LIGHT 4 ON
DELAY OF 1 SECOND
CHECK FOR 'RESET' KEY
YES
GOTO ⊗
NO
B


B
NO
TURN ON LIGHT 5
DELAY OF 1 SECOND
TURN TIMER '0' ON & DISPLAY IN THE LCD
CHECK FOR 'RESET' KEY
YES
GOTO ⊗
NO
CHECK FOR $\overline{\text{INT0}}$
IF INT is LOW
NO
YES
TURN TIMER '1' ON & DISPLAY IN THE LCD
GET THE BITS OF INPUT LATCH
'AND' THE BITS WITH 50 (HEX CODE)
IF THE ABOVE RESULT=50
NO
YES
C


C
TURN 'OFF' BOTH TIMER 'O' & TIMER '1'
INCREMENT COMPETITOR NUMBER BY 1
IF COMPETITOR NUMBER < 10
GOTO ⊗
GOTO START

CONCLUSION

BIBLIOGRAPHY

APPENDIX

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage: '155, '156 . . . . . 5.5 V
'LS155A, 'LS156 . . . . . 7 V
Off-state output voltage: '156 . . . . . 5.5 V
'LS156 . . . . . 7 V
Operating free-air temperature range: SN54', SN54LS' Circuits . . . . . −55°C to 125°C
SN74', SN74LS' Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54155			SN74155			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−800			−800	μA
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54155 SN74155			UNIT
				MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −8 mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA			0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V				40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	SN54155	−20		−55	mA
			SN74155	−18		−57	
I_{CC}	Supply current	V_{CC} = MAX, See Note 2	SN54155		25	35	mA
			SN74155		25	40	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 2: I_{CC} is measured with outputs open, A, B, and 1C inputs at 4.5 V, and 2C, 1G, and 2G inputs grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

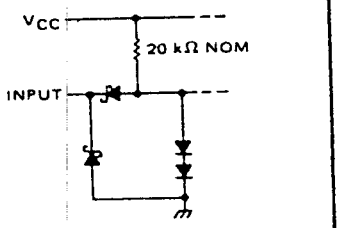
PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	LEVELS OF LOGIC	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A, B, $2\overline{C}$, $1\overline{G}$, or $2\overline{G}$	Y	2	C_L = 15 pF, R_L = 400 Ω, See Note 3		13	20	ns
t_{PHL}	A, B, $2\overline{C}$, $1\overline{G}$, or $2\overline{G}$	Y	2			18	27	ns
t_{PLH}	A or B	Y	3			21	32	ns
t_{PHL}	A or B	Y	3			21	32	ns
t_{PLH}	1C	Y	3			16	24	ns
t_{PHL}	1C	Y	3			20	30	ns

¶t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 3: See General Information Section for load circuits and voltage waveforms.

schematics of inputs and outputs (continued)

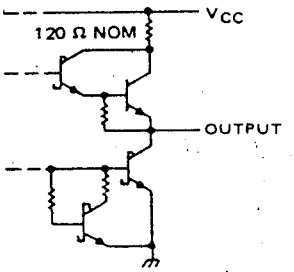
'LS155A, 'LS156

EQUIVALENT OF EACH INPUT



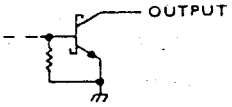
'LS155A

TYPICAL OF ALL OUTPUTS

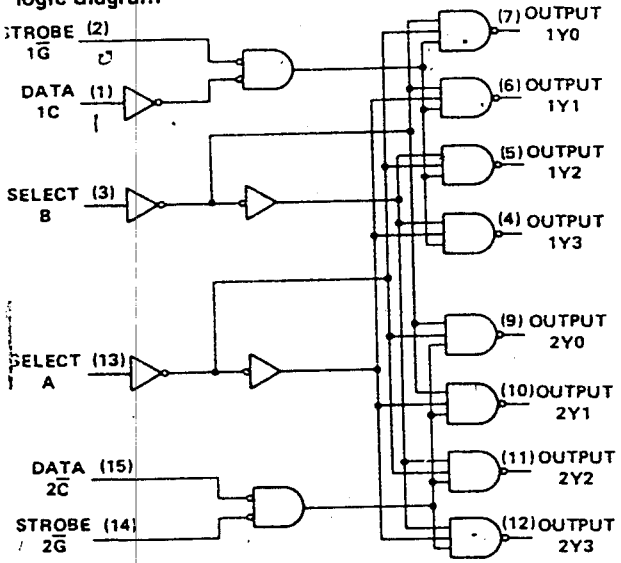


'LS156

TYPICAL OF ALL OUTPUTS

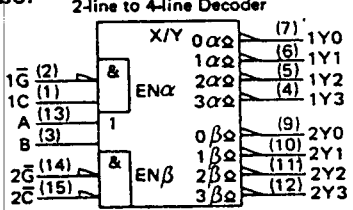


logic diagram

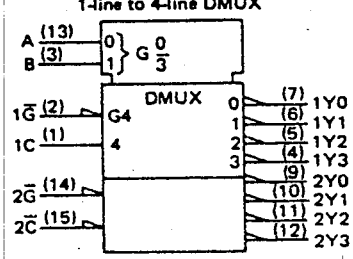


logic symbol

2-line to 4-line Decoder



1-line to 4-line DMUX



Pin numbers shown on logic notation are for D, J or N packages.

FUNCTION TABLES
2-LINE-TO-4-LINE DECODER
OR 1-LINE-TO-4-LINE DEMULTIPLEXER

INPUTS				OUTPUTS			
SELECT		STROBE	DATA				
B	A	1$\overline{G}$	1C	1Y0	1Y1	1Y2	1Y3
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

INPUTS				OUTPUTS			
SELECT		STROBE	DATA				
B	A	2$\overline{G}$	2$\overline{C}$	2Y0	2Y1	2Y2	2Y3
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

FUNCTION TABLE
3-LINE-TO-8-LINE DECODER
OR 1-LINE-TO-8-LINE DEMULTIPLEXER

INPUTS				OUTPUTS							
SELECT			STROBE OR DATA	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
C†	B	A	$\overline{G}$‡	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

†C = inputs 1C and 2$\overline{C}$ connected together
‡$\overline{G}$ = inputs 1$\overline{G}$ and 2$\overline{G}$ connected together
H = high level, L = low level, X = irrelevant

MC54/74HC138A

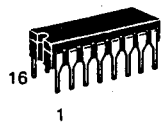
l-of-8 Decoder/Demultiplexer

ligh–Performance Silicon–Gate CMOS

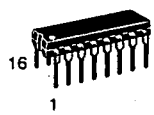
The MC54/74HC138A is identical in pinout to the LS138. The device ıputs are compatible with standard CMOS outputs; with pullup resistors, ıey are compatible with LSTTL outputs.

The HC138A decodes a three–bit Address to one–of–eight active–low utputs. This device features three Chip Select inputs, two active–low and ne active–high to facilitate the demultiplexing, cascading, and chip–select-ıg functions. The demultiplexing function is accomplished by using the ıddress inputs to select the desired device output; one of the Chip Selects is sed as a data input while the other Chip Selects are held in their active tates.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 100 FETs or 29 Equivalent Gates



J SUFFIX
CERAMIC PACKAGE
CASE 620–10



N SUFFIX
PLASTIC PACKAGE
CASE 648–08

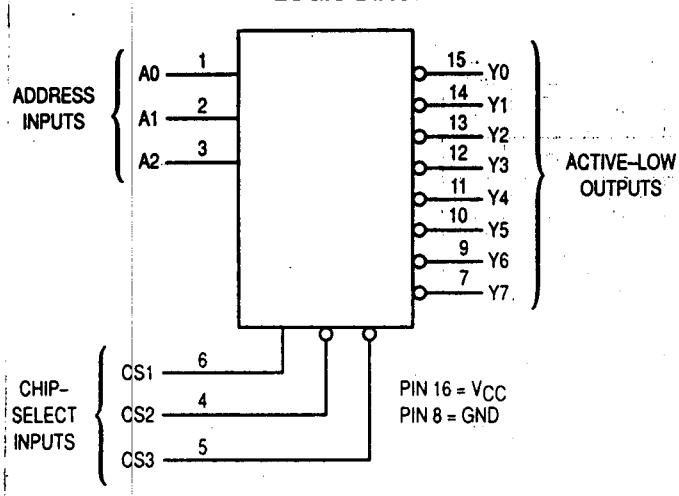
D SUFFIX
SOIC PACKAGE
CASE 751B–05

DT SUFFIX
TSSOP PACKAGE
CASE 948F–01

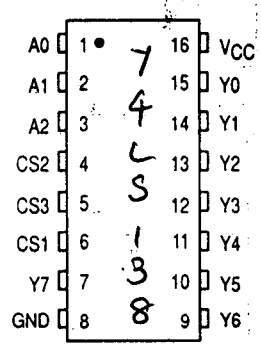
ORDERING INFORMATION

MC54HCXXXAJ	Ceramic
MC74HCXXXAN	Plastic
MC74HCXXXAD	SOIC
MC74HCXXXADT	TSSOP

LOGIC DIAGRAM



PIN ASSIGNMENT



FUNCTION TABLE

Inputs						Outputs							
CS1	CS2	CS3	A2	A1	A0	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

H = high level (steady state); L = low level (steady state);
X = don't care

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Maximum current into any output (off-state) . . . . . 1 mA
Operating free-air temperature range: SN5445 Circuits . . . . . −55°C to 125°C
SN7445 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN5445			SN7445			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Off-state output voltage			30			30	V
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA				−1.5	V
$V_{O(on)}$	On-state output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V	$I_{O(on)}$ = 80 mA		0.5	0.9	V
			$I_{O(on)}$ = 20 mA			0.4	
$I_{O(off)}$	Off-state output current	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, $V_{O(off)}$ = 30 V				250	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V				40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−1.6	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2	SN5445		43	62	mA
			SN7445		43	70	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

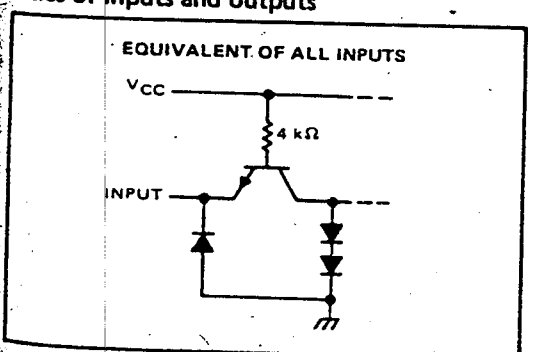
NOTE 2: I_{CC} is measured with all inputs grounded and outputs open.

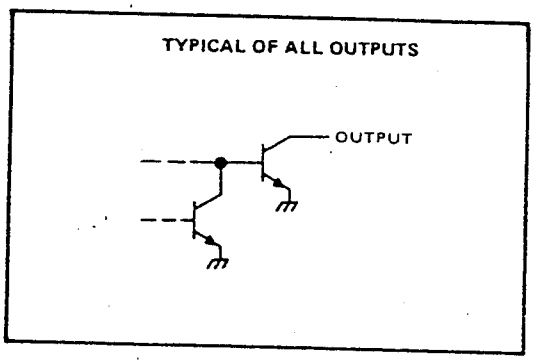
switching characteristics, V_{CC} = 5 V, T_A = 25°C

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF, R_L = 100 Ω, See Note 3			50	ns
t_{PHL}	Propagation delay time, high-to-low-level output				50	ns

NOTE 3: See General Information Section for load circuits and voltage waveforms.

schematics of inputs and outputs





ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature ..... 0°C to 70°C
Storage Temperature ..... −65°C to 125°C
Voltage on any Pin with
Respect to Ground ..... −0.5V to +7V
Power Dissipation ..... 1 Watt

**Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

D.C. CHARACTERISTICS T_A = 0°C to 70°C V_{SS} = 0V (Note 3)*

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IL1}	Input Low Voltage for Return Lines	−0.5	1.4	V	
V_{IL2}	Input Low Voltage for All Others	−0.5	0.8	V	
V_{IH1}	Input High Voltage for Return Lines	2.2		V	
V_{IH2}	Input High Voltage for All Others	2.0		V	
V_{OL}	Output Low Voltage		0.45	V	(Note 1)
V_{OH1}	Output High Voltage on Interrupt Line	3.5		V	(Note 2)
V_{OH2}	Other Outputs	2.4			I_{OH} = −400 μA 8279-5 −100 μA 8279
I_{IL1}	Input Current on Shift, Control and Return Lines		+10 −100	μA μA	$V_{IN} = V_{CC}$ V_{IN} = 0V
I_{IL2}	Input Leakage Current on All Others		±10	μA	$V_{IN} = V_{CC}$ to 0V
I_{OFL}	Output Float Leakage		±10	μA	$V_{OUT} = V_{CC}$ to 0.45V
I_{CC}	Power Supply Current		120	mA	
C_{IN}	Input Capacitance		10	pF	f_C = 1 MHz Unmeasured Pins Returned to V_{SS}(6)
C_{OUT}	Output Capacitance		20	pF	

A.C. CHARACTERISTICS T_A = 0°C to 70°C, V_{SS} = 0V (Note 3)*

Bus Parameters

READ CYCLE

Symbol	Parameter	8279		8279-5		Unit
		Min	Max	Min	Max	
t_{AR}	Address Stable Before $\overline{READ}$	50		0		ns
t_{RA}	Address Hold Time for $\overline{READ}$	5		0		ns
t_{RR}	$\overline{READ}$ Pulse Width	420		250		ns
t_{RD}(4)	Data Delay from $\overline{READ}$		300		150	ns
t_{AD}(4)	Address to Data Valid		450		250	ns
t_{DF}	$\overline{READ}$ to Data Floating	10	100	10	100	ns
t_{RCY}	Read Cycle Time	1		1		μs
t_{AW}	Address Stable Before $\overline{WRITE}$	50		0		ns
t_{WA}	Address Hold Time for $\overline{WRITE}$	20		0		ns

MC74HCT573A

Octal 3-State Noninverting Transparent Latch with LSTTL Compatible Inputs

High–Performance Silicon–Gate CMOS

The MC74HCT573A is identical in pinout to the LS573. This device may be used as a level converter for interfacing TTL or NMOS outputs to High–Speed CMOS inputs.

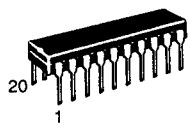
These latches appear transparent to data (i.e., the outputs change asynchronously) when Latch Enable is high. When Latch Enable goes low, data meeting the setup and hold times becomes latched.

The Output Enable input does not affect the state of the latches, but when Output Enable is high, all device outputs are forced to the high–impedance state. Thus, data may be latched even when the outputs are not enabled.

The HCT573A is identical in function to the HCT373A but has the Data Inputs on the opposite side of the package from the outputs to facilitate PC board layout.

The HCT573A is the noninverting version of the HC563.

- Output Drive Capability: 15 LSTTL Loads
- TTL/NMOS–Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 10 µA
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 234 FETs or 58.5 Equivalent Gates
  - — Improved Propagation Delays
  - — 50% Lower Quiescent Power



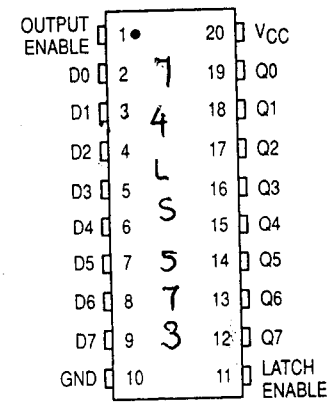
N SUFFIX
PLASTIC PACKAGE
CASE 738–03

DW SUFFIX
SOIC PACKAGE
CASE 751D–04

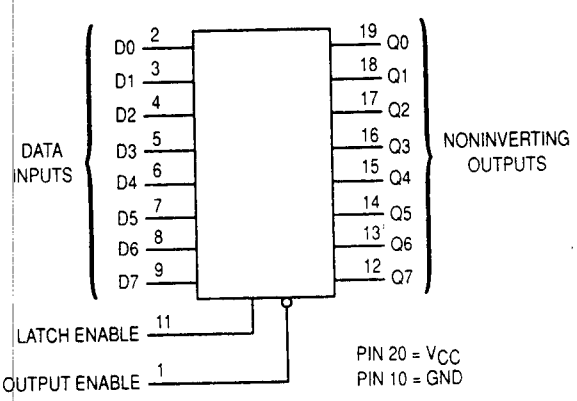
ORDERING INFORMATION

MC74HCTXXXAN	Plastic
MC74HCTXXXADW	SOIC

PIN ASSIGNMENT



LOGIC DIAGRAM



Design Criteria	Value	Units
Internal Gate Count*	58.5	ea
Internal Gate Propagation Delay	1.5	ns
Internal Gate Power Dissipation	5.0	µW
Speed Power Product	0.0075	pJ

* Equivalent to a two–input NAND gate.

FUNCTION TABLE

Inputs			Output
Output Enable	Latch Enable	D	Q
L	H	H	H
L	H	L	L
L	L	X	No Change
H	X	X	Z

X = Don't Care
Z = High Impedance

Octal 3-State Noninverting Bus Transceiver

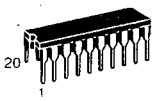
High–Performance Silicon–Gate CMOS

MC54/74HC245A

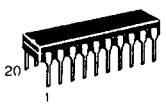
The MC54/74HC245A is identical in pinout to the LS245. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC245A is a 3–state noninverting transceiver that is used for 2–way asynchronous communication between data buses. The device has an active–low Output Enable pin, which is used to place the I/O ports into high–impedance states. The Direction control determines whether data flows from A to B or from B to A.

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 308 FETs or 77 Equivalent Gates



J SUFFIX
CERAMIC PACKAGE
CASE 732–03



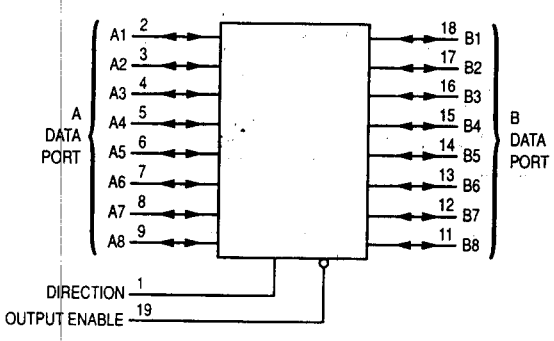
N SUFFIX
PLASTIC PACKAGE
CASE 738–03

DW SUFFIX
SOIC PACKAGE
CASE 751D–04

ORDERING INFORMATION

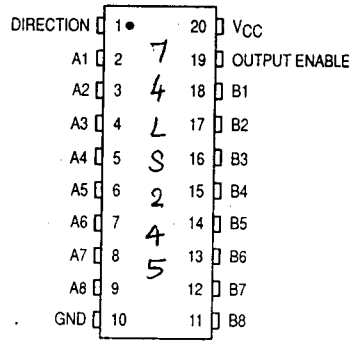
MC54HCXXXAJ	Ceramic
MC74HCXXXAN	Plastic
MC74HCXXXADW	SOIC

LOGIC DIAGRAM



PIN 10 = GND
PIN 20 = V_{CC}

PIN ASSIGNMENT



FUNCTION TABLE

Control Inputs		
Output Enable	Direction	Operation
L	L	Data Transmitted from Bus B to Bus A
L	H	Data Transmitted from Bus A to Bus B
H	X	Buses Isolated (High–Impedance State)

X = don't care

256 Bit/1K 5.0V CMOS Serial EEPROM

FEATURES

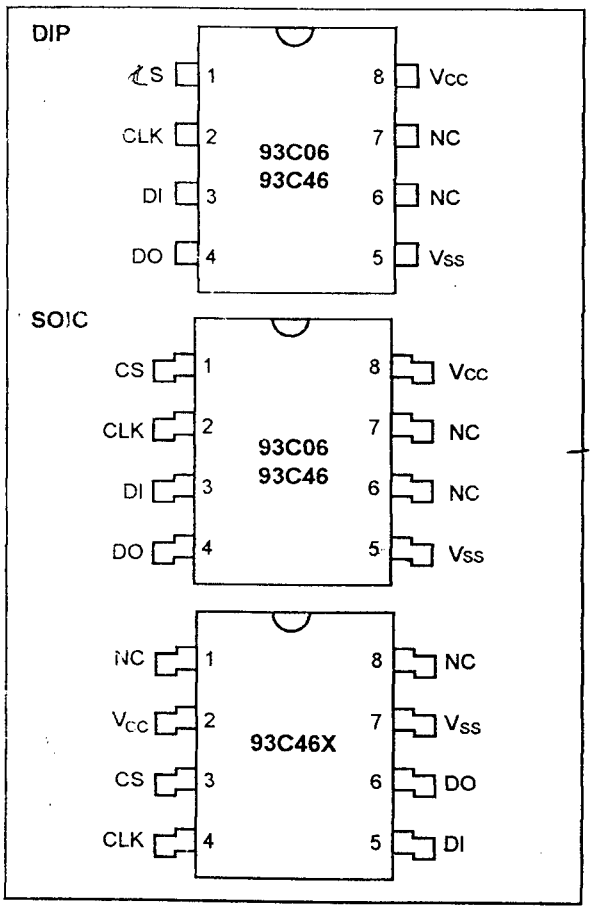
- Low power CMOS technology
- 16 bit memory organization
  - 16 X 16 bit organization (93C06)
  - 64 x 16 bit organization (93C46)
- Single 5 volt only operation
- Self-timed ERASE and WRITE cycles
- Automatic ERASE before WRITE
- Power on/off data protection circuitry
- 1,000,000 ERASE/WRITE cycles guaranteed
- Data Retention > 200 years
- 8-pin DIP or SOIC package
- Available for extended temperature ranges:
  - Commercial: 0 C to +70 C
  - Industrial: -40 C to +85 C
  - Automotive: -40 C to +125 C
- 2 ms program cycle time

DESCRIPTION

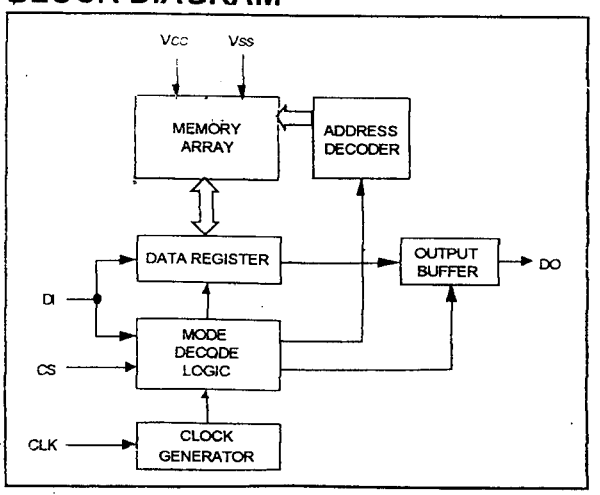
The Microchip Technology Inc. 93C06/46 family of Serial Electrically Erasable PROMs are configured in a x16 organization. Advanced CMOS technology makes these devices ideal for low-power non-volatile memory applications. The 93C06/46 is available in the standard 8-pin DIP and surface mount SOIC packages. The 93C46X comes as SOIC only.

These devices offer fast (1 ms) byte write and extended (-40 C to +125 C) temperature operation. It is recommended that all other applications use Microchip's 93LC46.

PACKAGE TYPE



BLOCK DIAGRAM



INSTRUCTIONS OF LCD MODULE:

Instruction	Code										Description	Execute Time (max.)
	RS	R/W	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0		
Clear Display	0	0	0	0	0	0	0	0	0	1	Clears all display and returns the cursor to the home position (Address 0).	1.64mS
Cursor At Home	0	0	0	0	0	0	0	0	1	*	Returns the cursor to the home position (Address 0). Also returns the display being shifted to the original position. DD RAM contents remain unchanged.	1.64mS
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets the cursor move direction and specifies or not to shift the display. These operations are performed during data write and read.	40μS
Display On/Off Control	0	0	0	0	0	0	1	D	C	B	Sets ON/OFF of all display (D) cursor ON/OFF (C), and blink of cursor position character (B).	40μS
Cursor/Display Shift	0	0	0	0	0	1	S/C	R/L	*	*	Moves the cursor and shifts the display without changing DD RAM contents.	40μS
Function Set	0	0	0	0	1	DL	N	F	*	*	Sets interface data length (DL) number of display lines (L) and character font (F).	40μS
CG RAM Address Set	0	0	0	1	ACG						Sets the CG RAM address. CG RAM data is sent and received after this setting.	40μS
DD RAM Address Set	0	0	1	ADD							Sets the DD RAM address. DD RAM data is sent and received after this setting	40μS
Busy Flag/ Address Read	0	1	BF	AC							Reads Busy flag (BF) indicating internal operation is being performed and reads address counter contents.	40μS
CG RAM/DD RAM Data Write	1	0	WRITE DATA								Writes data into DD RAM or CG RAM.	40μS
CG RAM/DD RAM Data Read	1	1	READ DATA								Reads data from DD RAM or CG RAM.	40μS

NOTE:

Code	Description	Execute Time (max.)
I/D = 1: Increment I/D = 0: Decrement S = 1: With display shift S/C = 1: Display shift S/C = 0: Cursor movement R/L = 1: Shift to the right R/L = 0: Shift to the left DL = 1: 8-bit DL = 0: 4-bit N = 1: 2 lines N = 0: 1 line F = 1: 5 x 10 dots F = 0: 5 x 7 dots BF = 1: Internal operation is being performed. BF = 0: Instruction acceptable.	DD RAM: Display Data RAM CG RAM: Character Generator RAM ACG: CG RAM Address ADD: DD RAM Address Corresponds to cursor address. AC: Address Counter, used for both DD RAM and CG RAM * : Invalid	fcp or fosc = 250 kHz However, when frequency changes, execution time also changes. Ex. When fcp or fosc = 270 kHz, $40\mu S \times \frac{250}{270} = 37\mu S$

NOTE: For details in program, refer to the User's Manual which is separately provided.

Lower 4 bit \ Upper 4 bit	0000	0010	0011	0100	0101	0110	0111	1010	1011	1100	1101	1110	1111
×××0000	CG RAM (1)												
×××0001	(2)												
×××0010	(3)												
×××0011	(4)												
×××0100	(5)												
×××0101	(6)												
×××0110	(7)												
×××0111	(8)												
×××1000	(1)												
×××1001	(2)												
×××1010	(3)												
×××1011	(4)												
×××1100	(5)												
×××1101	(6)												
×××1110	(7)												
×××1111	(8)												

* CG RAM: Character pattern area which can freely be rewritten by program.