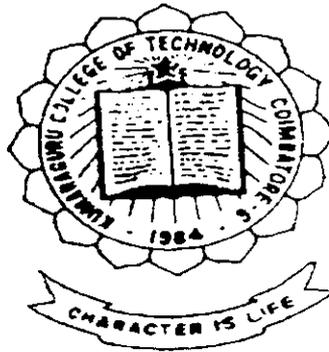


DATA ACQUISITION THROUGH TELEPHONE

PROJECT REPORT (1999 – 2000)

P-1364



SUBMITTED BY

P. MAHESHWARI

R. ARUN PRASAD

K. SELVANAYAKI

C.V. BHARANIDHARAN

UNDER THE GUIDANCE OF

PROF. M. RAMASAMY, M.E., (PH.D)

HOD, ECE

J. NARAYAN KUMAR

MD, AL SYSTEMS

DEPARTMENT OF
ELECTRONICS AND COMMUNICATION ENGINEERING
KUMARAGURU COLLEGE OF TECHNOLOGY,

COIMBATORE – 641 006.

105, 3rd Street,
Tatabad,
Coimbatore – 641 012.

Ph.: 0422-493960
Fax: 0422-213849
E-mail: also@vsnl.com

TO WHOMSOEVER IT MAY CONCERN

This is to certify that the following final year B.E (Electronics & Communication Engineering) students of Kumaraguru College of Technology, Coimbatore have worked on their project entitled "DATA ACQUISITION THROUGH TELEPHONE" in our Organisation.

The students are

P. Maheshwari
R. Arun Prasad
K. Selvanayagi
C.V. Bharanidharan

During this period their attendance and conduct were found to be good. We wish them the very best in their endeavor.

For AL SYSTEMS,

J. Narayan Kumar

Date: _____

We thank our beloved Principal Dr. K.K. Padmanabhan BSc.(Engg),Mtech,PhD for his constant encouragement

We thank our Head of the Department and our project guide Prof.M.RAMASAMY, M.E.(PhD), who has always guided us with his ever valuable suggestions and had led us his fullest support during the progress of our project. He had always been ready to clear our skeptics.

We would like to thank our class advisor MR.S.GOVINDARAJU, M.E. and all the staff members of ECE department for their constant support in our endeavor.

Our sincere thanks to MR. J. NARAYAN KUMAR, B.E. Managing Partner AL Systems. and Mrs. Santhamani, for providing the necessary infrastructure and guidance for our project.

Finally, thanks to all our friends who contributed in our project. especially K.Ashok Babu, for his valuable ideas.

“Data Acquisition through Telephone” aims in acquisition of data stored in the text format in the computer through telephone lines.

The system hardware and software are designed based on the telephone standards. The circuit designed here is capable of detecting the ring and the get the Dual Tone Multiple Frequency signals, decode it and forward it to the computer through the computer's parallel I/O port.

The codes written in 'C' constantly monitors the data in the status register of the parallel port and stores it in a file. The codes written in Visual Basic reads the data from the file and accordingly runs an application. A DTMF telephone set situated in any remote area is used to send commands through the telephone exchange to the circuit to access various files from the attached computer terminal.

CONTENTS

1. INTRODUCTION	1
2. ALL ABOUT TELEPHONE	
2.1 <i>Inside the Telephone</i>	3
2.2 <i>Signaling</i>	5
3. INPUT INTERFACE CIRCUITORY	
3.1 <i>Switching System</i>	8
3.2 <i>Ring Detection Circuitory</i>	10
3.3 <i>DTMF Decoder</i>	10
4. OUTPUT INTERFACE CIRCUITORY	13
5. HARDWARE DESCRIPTION	
5.1 <i>MCT2E</i>	16
5.2 <i>DTMF Receiver</i>	20
5.3 <i>MC34114</i>	32
5.4 <i>74LS244</i>	47
6. PARALLEL PORT	
6.1 <i>Introduction</i>	51
6.2 <i>Parallel Port Registers</i>	51
6.3 <i>Specifications</i>	54

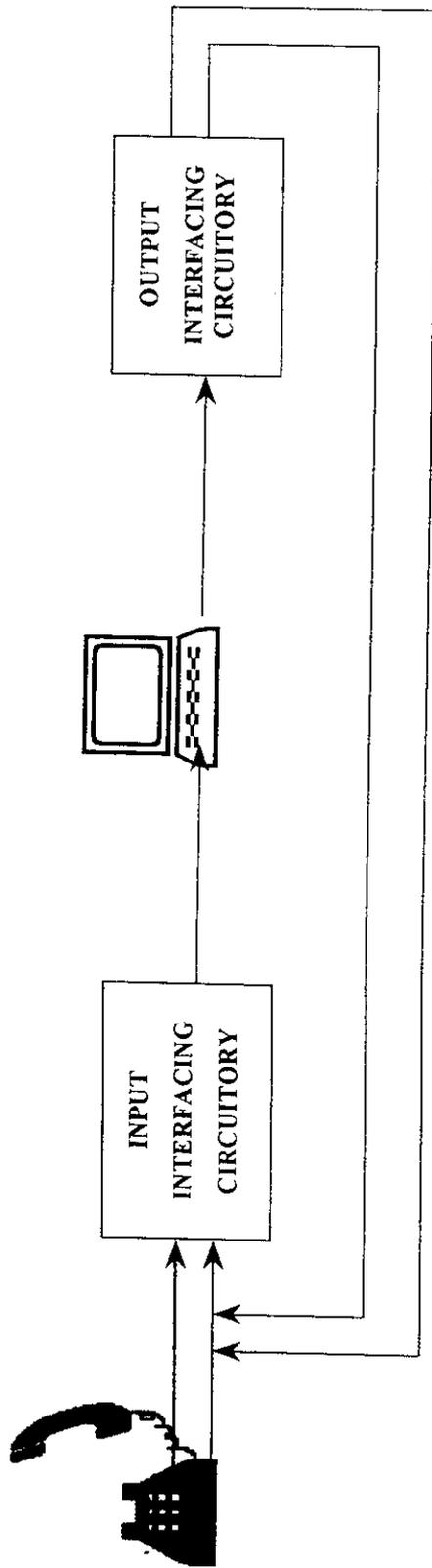
7. SCHEMATIC & PCB LAYOUT.....	55
8. SOFTWARE	
8.1 <i>Algorithm.....</i>	59
8.2 <i>Flowchart.....</i>	60
8.3 <i>Visual Basic Codes.</i>	63
8.4 <i>'C' Codes.....</i>	67
9. FUTURE DEVELOPMENT.....	71
10. CONCLUSION.....	72
11. BIBLIOGRAPHY.....	73

The data in a computer can be accessed only when he is in the place where the computer is located or he can do it with a computer is connected to a network to which the computer from which data has to be accessed is connected. Without a computer accessing of data residing in the computer is not possible. We have made this possible in our project

The Aim of the project is to get the data stored in the personal computer from a place anywhere in the world where there is a telephone. As there is no place without a telephone, we conclude that you can get data from anywhere in the world. Several other features are added to the project.

The control signals from the telephone lines are transferred to the computer with the help of the input interfacing circuitry. The input interfacing circuitry gets activated by the ringing current that come in the telephone lines. Then control signals are decoded and transferred to the personal computer. The computer then makes an analysis of the control information and according to the commands offered it sends the data. The data is then interfaced with the telephone lines through output interfacing circuitry

BLOCK DIAGRAM



2.1 INSIDE THE TELEPHONE:

Handset houses a transmitter and a receiver. There is a four-wire circuit in the handset, two wires for the transmit and two wires for the receive. Each side of the function has its own two wire electrical circuit at this point. Once the wires are run from the handset to the base of the telephone, two wires go into set. Actually, these wires meet up with the whole network of cross connect inside the set. Transmit wire is connected inside the set to the dial pad, which is an addressing mechanism.

Hook switch is the portion of the set that actually gets the dial tone from Telephone Company or when we through with the call, gives the dial tone. In reality, an electrical wiring circuit is physically connected from the telephone company office to our telephone circuit. Using a group of tones that fall into spectrum of voice frequency, the tone dialer has a set of buttons that will sent out frequency based tones instead of electrical pulses

The touch-tones are actually Dual-Tone Multiple Frequency (DTMF) set. Each of the numbers are represented on the dial pad have both x and y matrix or cross-point. The dual tone arrangement would get away with the usage of only half of the generators needed to represent the same number of digits. When a number is pressed two separate tones are generated and sent to the Central Office simultaneously. Each number on the dial pad has its own distinct set of dual tones, so the system recognizes each as a discrete number. This allows for quicker dialing, due to the fact that the tones are generated 23 pulses per sec (PPS), much quicker than the rotary set. The calls setup time is reduced to 6 – 10 sec. Tip and Ring is a phrase that describes the two wires that are connected to the telephone set from the outside world.

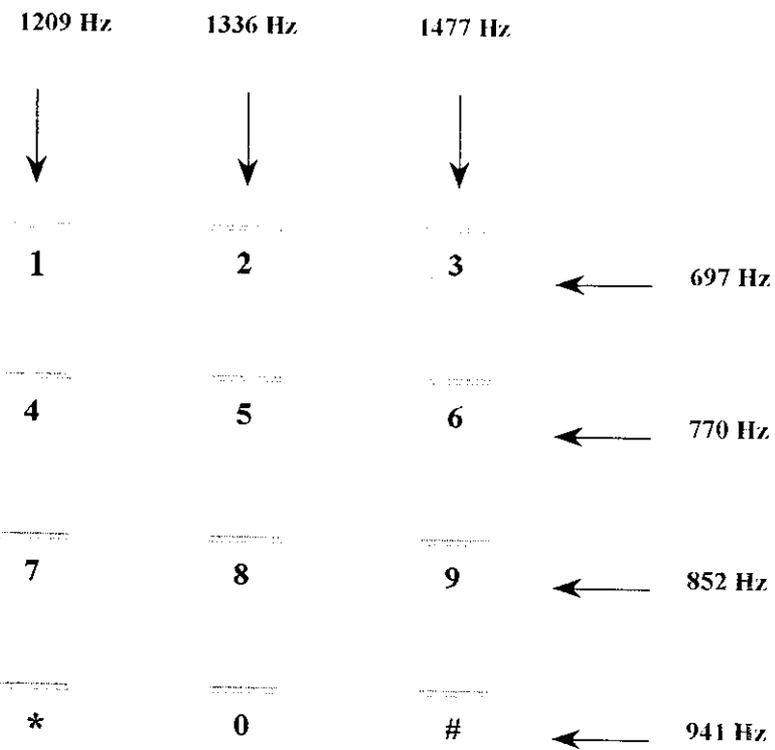


Fig . 2.1 - MULTI-FREQUENCY PUSHBUTTON DIALING PAD

2.2 SIGNALING :

The interchange of signaling information can be illustrated with the help of a typical call connection sequence in Indian Network. The circled number in Fig. 2.2 correspond to the steps listed below:

-  *A request for originating a call is initiated when the calling subscriber lifts the handset*
-  *The exchange sends dial-tone to the calling subscriber to indicate to him to Start dialing.*
-  *The called number (address) is transmitter to the exchange when the calling Subscriber dials the desired digits.*
 - *Ring-back tone, if the called subscriber is free.*
 - *Busy tone, if the called subscriber is busy.*
 - *Recorded message, if provision exists, for non-completion of call due to some other constraint.*
-  *The called subscriber indicates acceptance of the incoming call by lifting the handset*
-  *The exchange recognizing the acceptance terminates the ringing current and the ring-back tone and establishes a connection between the calling and the called subscribers.*

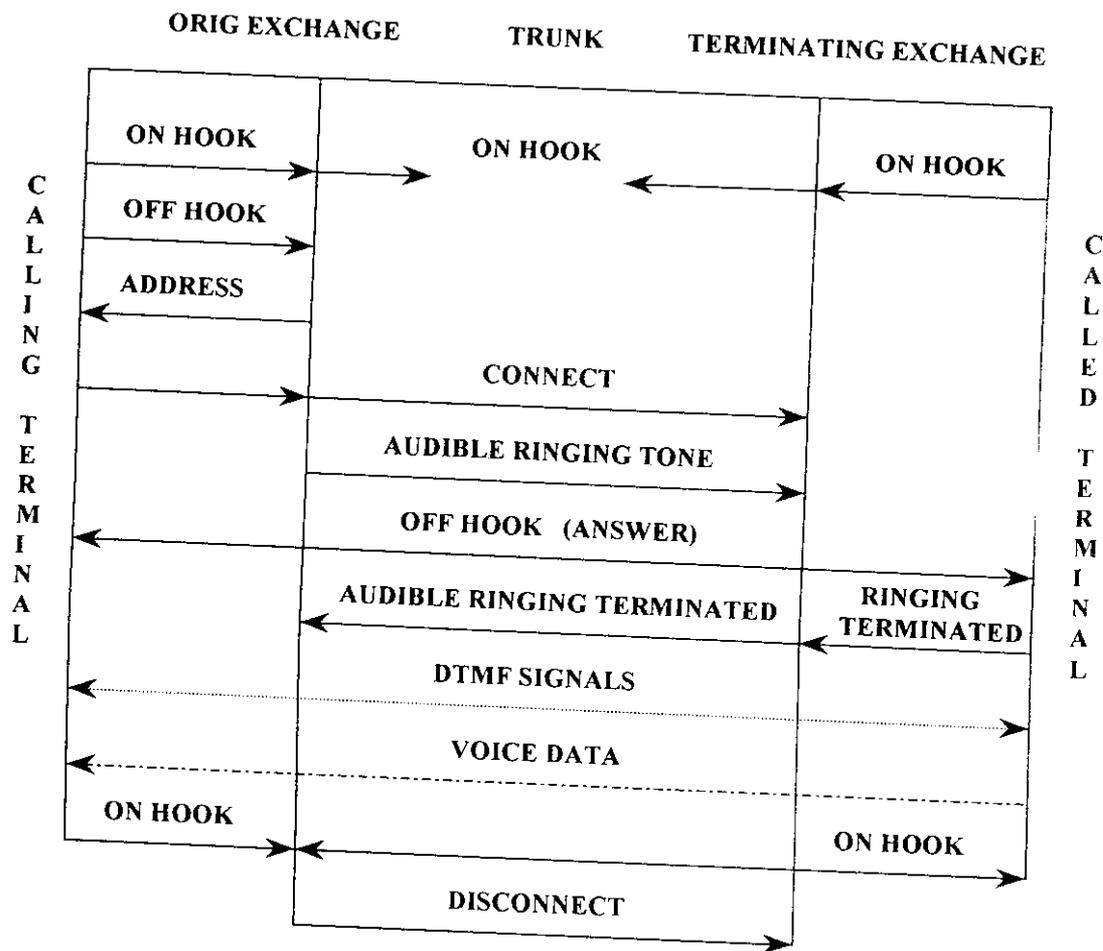


Fig . 2.2 – SIGNAL FLOW

-  *The control information from the caller end is transferred to the called terminal by the use of DTMF signals.*
-  *The DTMF signals are decoded in the called end and is converted into a form that can be sent to the computer*
-  *The computer processes the bits and reads the data stored in the computer*
-  *The data is then transmitted to the caller*

INTRODUCTION :

Tip and Ring lines are initially connected to the Ring detection circuit. The ringing voltage is fed to the ring detection circuitry which performs the function of rectifying the voltage and isolating the rest of the circuitry from the telephone lines. Each ring is represented using a 5V pulse which is fed to the parallel port of the computer. Computer after a certain number of counts will give control information to the switching system. In response to the control signal given by the computer the switching system connects Tip and Ring lines to the DTMF decoder. The control signals coming via the telephone lines are decoded and the decoded bits are fed to the parallel port of the computer. Depending on the control information provided the computer does a specific action like giving you the data stored in a specific file in the computer's harddisk.

The various blocks in the input interfacing circuitry is explained below :

3.1 SWITCHING SYSTEM :

A switching transistor and a relay performs the function of the switching system. When a low is given to the transistor, it is in the cutoff mode and a ground is not available to the supply to energize the relay and so the Tip and Ring lines are connected to the ring detection circuitry. When a high is given to the base of the transistor, it goes to the saturation mode and thus providing a ground to the supply of the relay. This energizes the relay coil and Tip and Ring lines are connected to the decoder circuitry

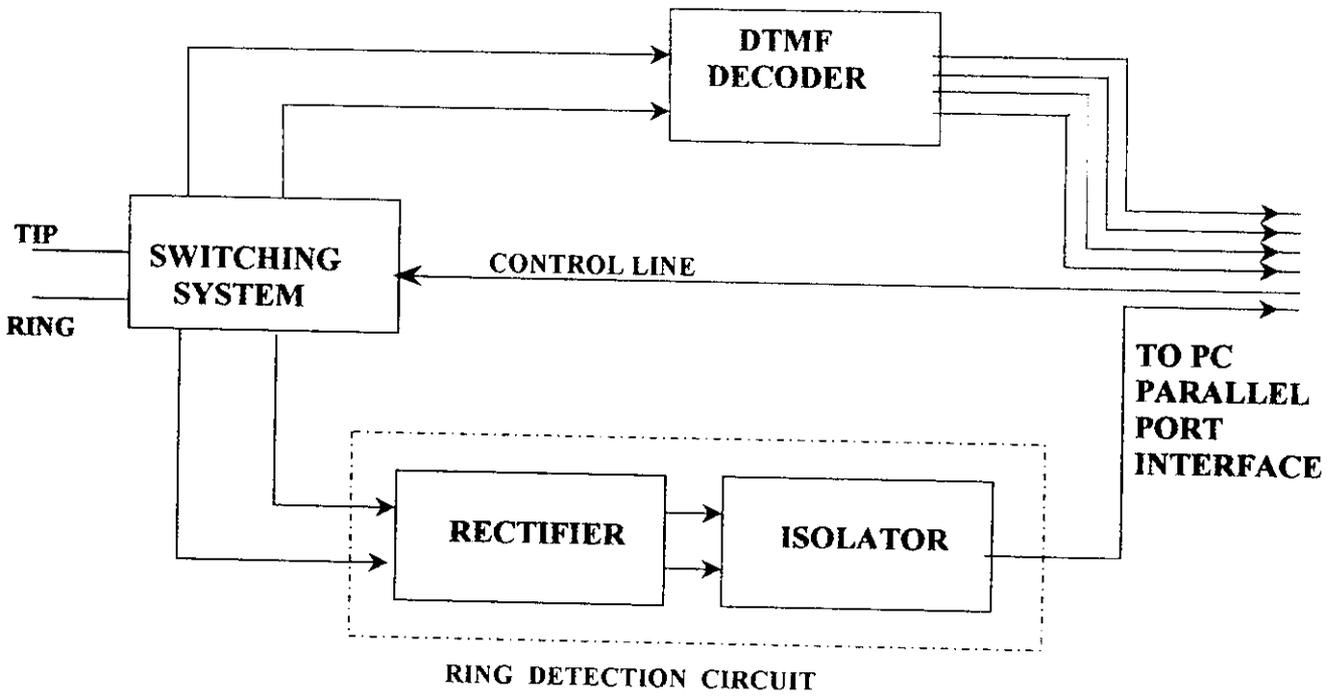


Fig 3.1 INPUT INTERFACING CIRCUITORY

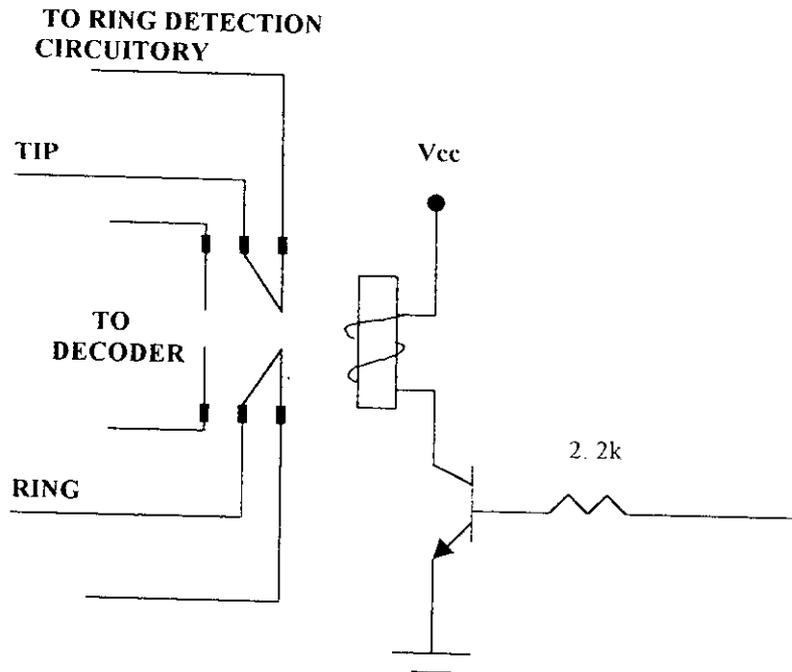


Fig. 3.2 Switching System

3.2 RING DETECTION CIRCUITORY :

The rectification process is done using a bridge rectifier. The output voltage of the bridge rectifier is held constant using a zener diode. The output voltage is reduced by using a low value of resistance that is put in parallel to the zener diode. The resultant voltage is then fed to the first two pins of the opto-isolator (MCT2E). The output of the opto-isolator will be 0.6 V down the collector voltage, i.e , the voltage at the pin 5. The voltage across 1 and 2 points is around 65V to 75V. The voltage across the points 3 and 4 is 1.5V. The voltage at the pin 4 of the opto-isolator is 3.5V and voltage at the pin 6 is 4.5V

3.3 DTMF DECODER:

The DTMF signals are fed to the decoder. These are signals with specific frequencies which is detected by the decoder. The external components helps us to control the guard adjust time and the time for recognition of the signals. The std pin gives an indication of the valid signal recognition. The four output pins at Q1, Q2, Q3, Q4 gives the decoded bits indicating the DTMF signal received.



P-1364

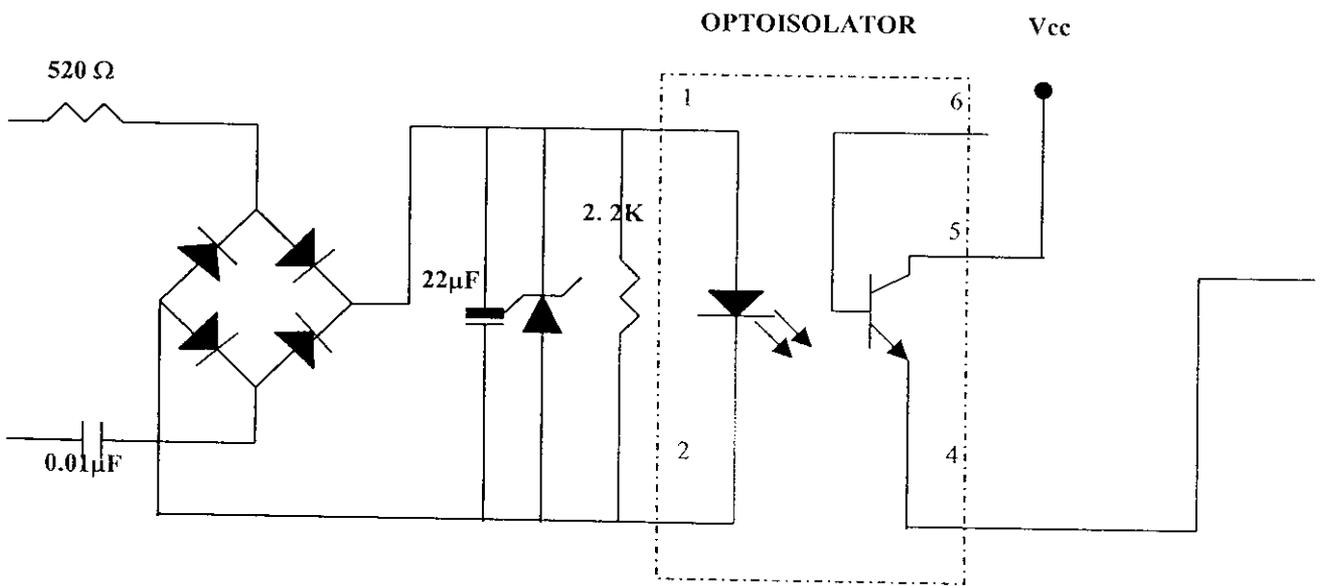


Fig 3.3 RING DETECTION CIRCUIT

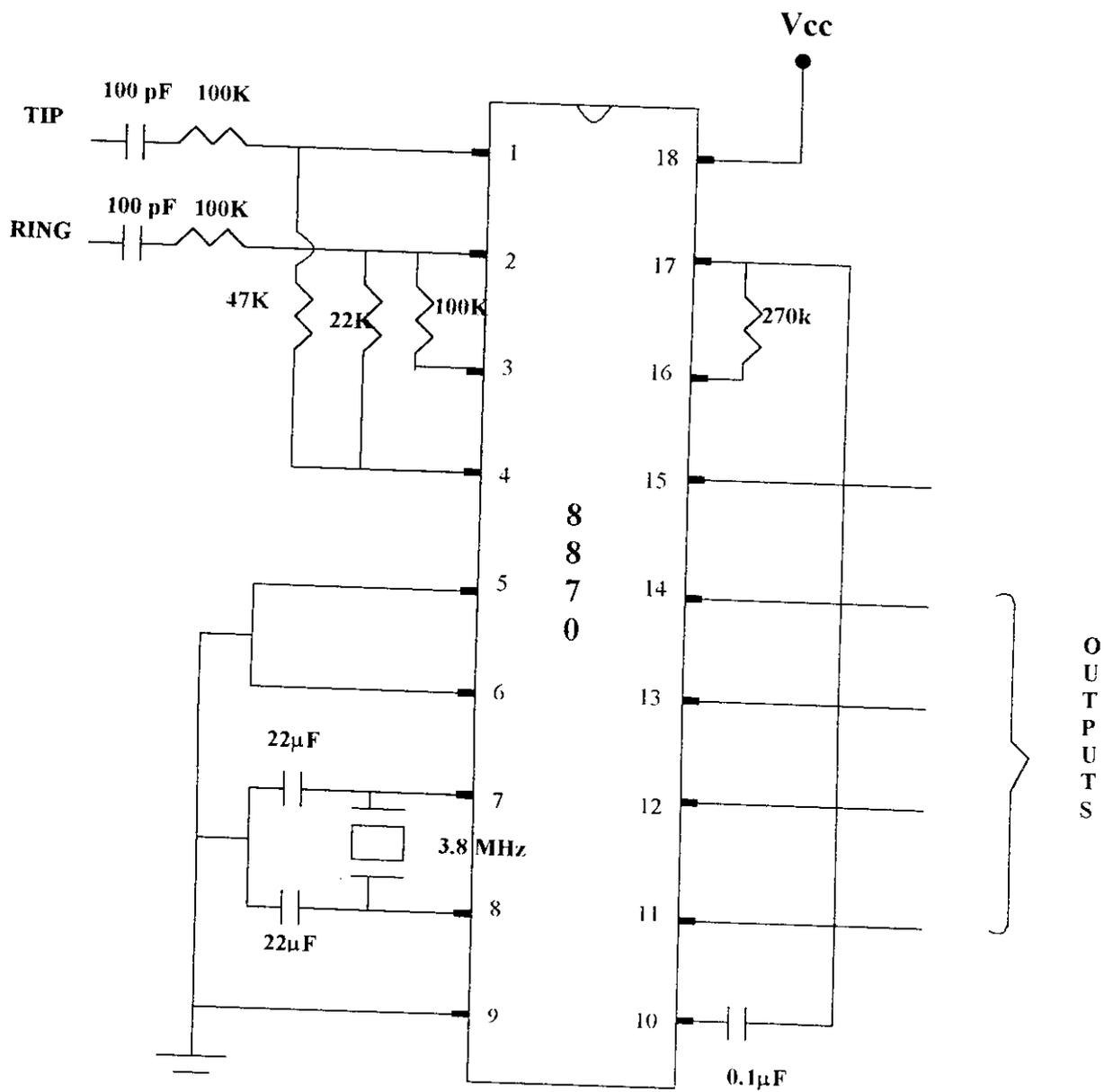
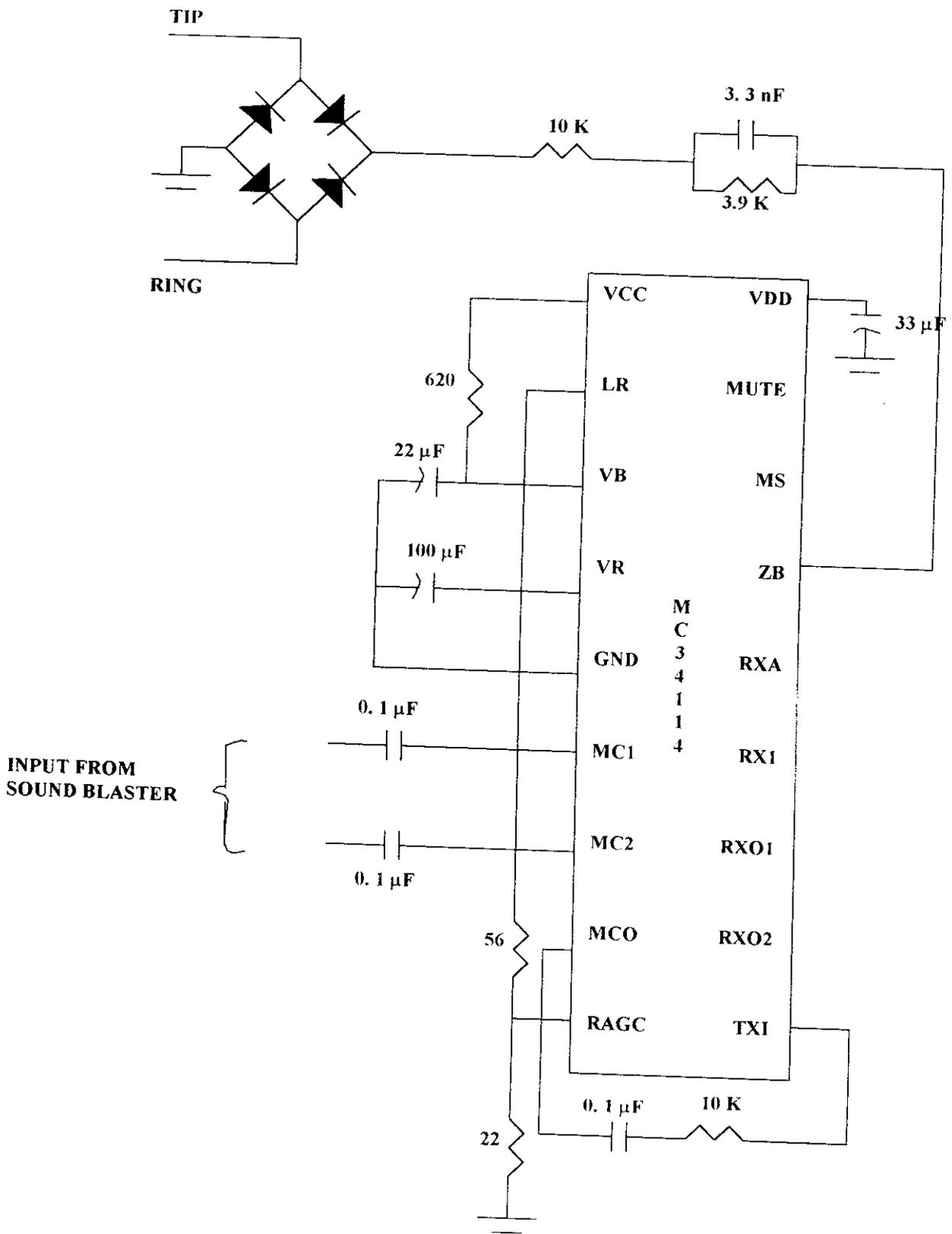


Fig 3.4 DTMF DECODER CIRCUIT

The output circuitry has to perform the following jobs :

- *It provides impedance matching between sound blaster and the telephone lines*
- *It provides the necessary gain to the input*
- *It protects the sound blaster from the high DC voltage available in the telephone lines*

These jobs can be accomplished using a single IC , MC34114



DAT

This chapter provides the hardware description of the following Ics :

❖ *MCT2E , OPTICAL ISOLATOR*

❖ *8870 , DTMF RECEIVER*

❖ *MC34114, MONOLITHIC TELEPHONE SPEECH NETWORK*

❖ *74LS244 , TRISTATE BUFFER*

5.1 MCT2E

It consists of Gallium arsenide infrared emitting diode optically coupled to silicon phototransistor detector

5.1.1 MAXIMUM RATINGS :

RATING	SYMBOL	VALUE	UNIT
--------	--------	-------	------

INPUT LED

Reverse Voltage	V_R	3	volts
Forward Current – Continuous	I_F	60	mA
LED Power Dissipation @ $T = 25\text{ C}$	P_D	120	mW
Derate above 25 C		1.41	mW/C

OUTPUT TRANSISTOR

Collector – Emitter voltage	V_{CEO}	30	Volts
Emitter – Collector Voltage	V_{ECO}	7	Volts
Collector – Base Voltage	V_{CBO}	70	Volts
Collector Current – Continuous	I_C	150	mA
Detector Power Dissipation @ $T = 25\text{ C}$	P_D	150	mW
Derate above 25 C		1.76	mW/C

TOTAL DEVICE

Isolation surge voltage	V_{iso}	7500	$V_{ac(pk)}$
Total Device Power Dissipation ($T = 25\text{ C}$)	P_D	250	mW
Above 25 C		2.94	mW/C

5.1.2 PIN DESCRIPTIONS :

PIN NUMBER	DESCRIPTION
1	LED Anode
2	LED Cathode
3	No Connection
4	Emitter
5	Collector
6	Base

5.1.3 ELECTRICAL CHARACTERISTICS :

CHARACTERISTICS	SYMBOL	MIN	TYP	MAX	UNITS
-----------------	--------	-----	-----	-----	-------

INPUT LED

<i>Forward Voltage</i>	V_F	-	1.23	-	Volts
<i>Reverse Leakage Current</i>	I_R	-	.01	10	μA
<i>Capacitance</i>	C_J	-	18	-	pF

OUTPUT TRANSISTOR

Collector – Emitter Dark Current	I_{CEO}	-	1	50	nA
Collector – Base Dark Current	I_{CBO}	-	0.2	20	nA
Collector – Emitter Breakdown Voltage	$V_{(BR)CEO}$	30	45	-	volts
Collector – Base Breakdown Voltage	$V_{(BR)CEO}$	70	100	-	volts
Emitter – Collector Breakdown Voltage	$V_{(BR)ECO}$	7	7	8	volts
DC Current gain	h_{FE}	-	500	-	-
Collector – Emitter Capacitance	C_{CE}	-	7	-	pF
Collector – Base Capacitance	C_{CB}	-	19	-	pF
Emitter – Base Capacitance	C_{EB}	-	9	-	pF

COUPLED

Output Collector Current	I_C	2	7	-	mA
Collector – Emitter Saturation Voltage	$V_{CE(sat)}$	-	0.19	0.4	volts
Turn – On – Time	t_{on}	-	2.8	-	μs
Turn – off – Time	t_{off}	-	4,5	-	μs
Rise Time	t_r	-	1.2	-	μs
Fall Time	t_f	-	1.3	-	μs
Isolation Voltage	V_{ISO}	7500	-	-	Vac(pk)
Isolation Resistance	R_{ISO}	1011	-	-	Ω
Isolation Capacitance	C_{ISO}	-	0.2	-	pF

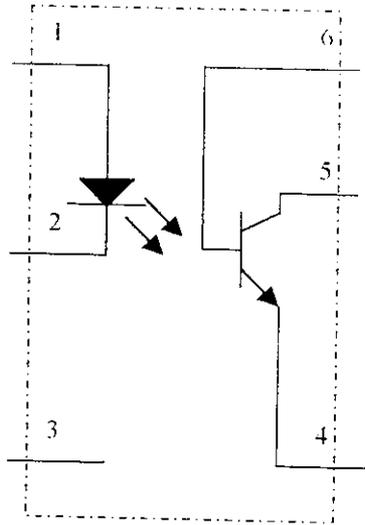


Fig. – 5.1.1 – Pin Diagram

INPUT PULSE

OUTPUT PULSE

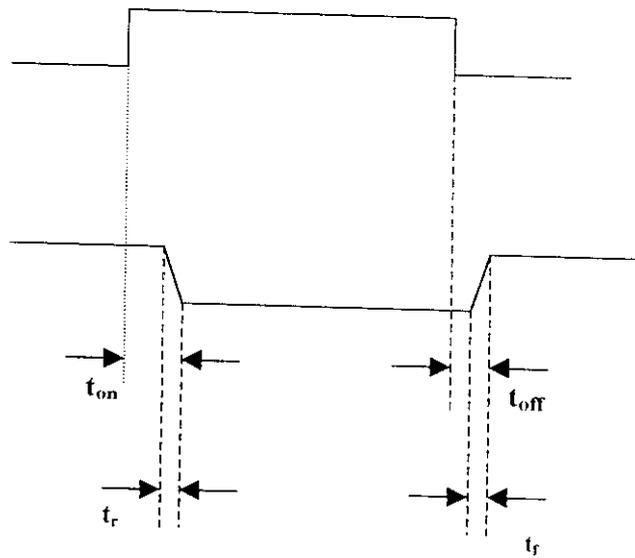


Fig. – 5.1.2 – Pulse Response

5.2 DTMF RECEIVER

5.2.1 INTRODUCTION:

The Teltone M-8870 is a full DTMF Receiver that integrates both bandsplit filter and decoder functions into a single 18-pin DIP or SOIC package. Manufactured using CMOS process technology, the M-8870 offers low power consumption (35mW max) and precise data handling. Its filter section uses switched capacitor technology for both the high and low group filters and for dial tone rejection. Its decoder uses digital counting techniques to detect and decode all 16 DTMF tone pairs into a 4-bit code. External component count is minimized by provision of an on-chip differential input amplifier, clock generator, and latched tri-state interface bus. Minimal external components required include a low-cost 3.579545 MHz color burst crystal, a timing resistor, and a timing capacitor.

5.2.2 FEATURES:

- *Low power consumption*
- *Adjustable acquisition and release times*
- *Central office quality and performance*
- *Inexpensive 3.58 MHz time base*
- *Single 5V power supply*
- *Dial tone suppression*

5.2.3 FUNCTIONAL DESCRIPTION:

M-8870 operating functions include a bandsplit filter that separates the high and low tones of the received pair, and a digital decoder that verifies both the frequency and duration of the received tones before passing the resulting 4-bit code to the output bus.

5.2.4 FILTER:

Applying the dual-tone signal to the inputs of two 6th order switched capacitor bandpass filters with bandwidths that correspond to the bands enclosing the low and high group tones separates the low and high group tones. The filter also incorporates notches at 350Hz and 440Hz, providing excellent dial tone rejection. Each filter output is followed by a single-order switched capacitor section that smoothes the signals prior to limiting. High-gain comparators provided with hysteresis to prevent detection of unwanted low-level signals and noise perform signal limiting. The comparator outputs provide full-rail logic swings at the frequencies of the incoming tones.

5.2.5 DECODER:

The M-8870 decoder uses a digital counting technique to determine the frequencies of the limited tones and to verify that they correspond to standard DTMF frequencies. A complex averaging algorithm is used to protect against tone simulation by extraneous signal (such as voice) while tolerating small frequency variations. The algorithm ensures an optimum combination of immunity to talk-off

and tolerance to interfering signals (third tones) and noise. When the detector recognizes the simultaneous presence of two valid tones (known as “signal condition”), it raises the Early Steering flag (Est). Any subsequent loss of signal condition will cause Est to fall.

5.2.6 STEERING CIRCUIT:

Before a decoded tone pair is registered, the receiver checks for valid signal duration (referred as “character-recognition-condition”). This check is performed by an experimental RC time constant driven by Est. A logic high on Est causes V_C to rise as the capacitor discharges. Provided that signal condition is maintained (Est remains high) for the validation period (t_{GTF}), V_C reaches the threshold (V_{TS}) of the steering logic to register the tone pair, thus latching its corresponding 4-bit code into the output latch. At this point, the GT output is activated and drives V_C to V_{DD} . GT continues to drive high as long as Est remains high. Finally, after a short delay to allow the output latch to settle, the “delayed steering” output flag (StD) goes high, signaling that a received tone pair has been registered. The contents of the output latch are made available on the 4-bit output bus by raising the three-state control input (OE) to a logic high. The steering circuit works in reverse to validate the interdigit pause between signals. Thus, as well as rejecting signals too short to be considered valid, the receiver will tolerate signal interruptions (dropouts) too short to be considered a valid pause. This capability, together with the ability to select the steering time constants externally, allows the designer to tailor performance to meet a wide variety of system requirements.

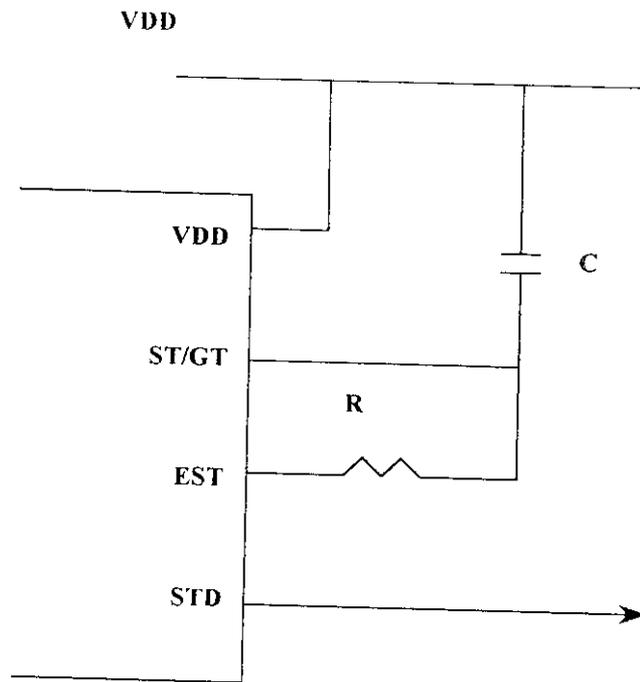


Fig 5.2.1 STEERING CIRCUIT

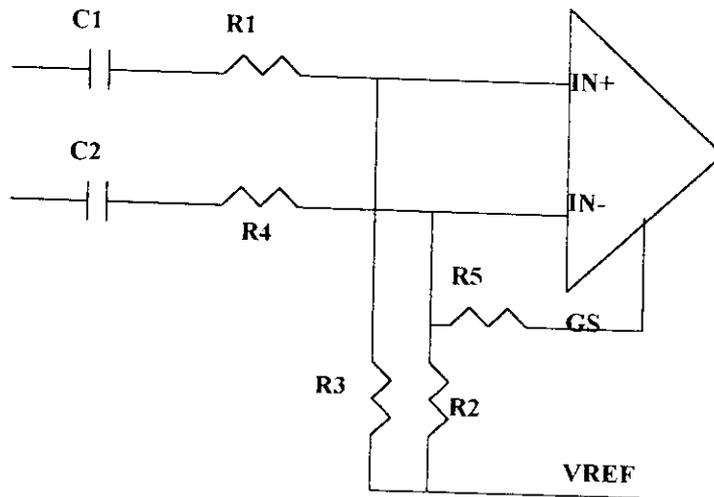


Fig 5.2.2 DIFFERENTIAL INPUT CONFIGURATION

5.2.7 GUARD ADJUSTMENT:

Where independent selection of signal duration and interdigit pause are not required, the simple steering circuit is applicable. Component values are chosen according to the formula:

$$t_{REC} = t_{DP} + t_{GTP}$$

$$t_{GTP} \sim 0.67 RC$$

The value of t_{DP} is a parameter of the device and t_{REC} is the minimum signal duration to be recognized by the receiver. A value for C of $0.1\mu F$ is recommended for most applications, leaving R to be selected by the designer. For example, a suitable value of R for a t_{REC} of 40ms would be $300 K\Omega$. The timing requirements for most telecommunication applications are satisfied with this circuit. Different steering arrangements may be used to select independently the guard times for tone-present (t_{GTP}) and tone-absent (t_{GTA}). This may be necessary to meet system specifications that place both accept and reject limits on both tone duration and interdigit pause.

Guard time adjustment also allows the designer to tailor system parameters such as talk-off and noise immunity. Increasing t_{REC} improves talk-off performance, since it reduces the probability that tones simulated by speech will maintain signal condition long enough to be registered. On the other hand, a relatively short t_{REC} with a long t_{DO} would be appropriate for extremely noisy environments where fast acquisition time and immunity to dropouts would be required. Design information for guard time adjustment is shown in Fig. 5.2.1

5.2.8 INPUT CONFIGURATION:

The input arrangement of the M-8870 provides a differential input operational amplifier as well as a bias source (V_{REF}) to bias the inputs at mid-rail. Provision is made for connection of a feedback resistor to the op-amp output (GS) for gain adjustment.

In a single-ended configuration, the input pins are connected to give a single ended input with the op-amp connected for unity gain and V_{REF} biasing the input at $1/2V_{DD}$. Fig 5.2.2 shows the differential configuration, which permits gain adjustment with the feedback resistor R_5 .

5.2.9 DTMF CLOCK CIRCUIT:

The internal clock circuit is completed with the addition of a standard 3.579545 MHz television color burst crystal. The crystal can be connected to a single M-8870 or to a series of M-8870s by coupling the oscillator output of each M-8870 through a 30pF capacitor to the oscillator input of the next M-8870.

5.2.10 PIN FEATURES:

PIN	NAME	DESCRIPTION	
1	IN+	Non-Inverting input	
2	IN-	Inverting input	
3	GS	Gain select, gives access to output of front-end amplifier for connection of feedback resistor.	
4	V _{REF}	Reference voltage output (nominally V _{DD} /2). May be used to bias the inputs at mid-rail.	
5	V _{SS}	Negative power supply (normally connected to 0V)	
6	V _{SS}	Negative power supply (normally connected to 0V)	
7	OSC1	Clock input	3.579545 MHz crystal connected between these pins completes the internal oscillator
8	OSC2	Clock input	
9	V _{SS}	Negative power supply (normally connected to 0V)	
10	OE	Three-state output enable (input). Logic high enables the outputs Q1-Q4. Internal pull up.	
11-14	Q1, Q2, Q3, Q4	Three-state data outputs. When enabled by OE, provides the code corresponding to the last valid tone pair received.	
15	StD	Delayed steering output. Presents a logic high when a received tone pair has been registered and the output latch is updated. Returns to logic low when the voltage on St/GT falls below V _{TSI} .	
16	Est	Early steering output. Presents a logic high immediately when the digital algorithm detects a recognizable tone pair (signal condition). Any momentary loss of signal condition will cause Est to return to a logic low.	
17	St/GT	Steering input/guard time output (bi-directional). A voltage greater than V _{TSI} detected at St causes the device to register the detected tone pair and update the output latch. A voltage less than V _{TSI} frees the device to accept a new tone pair. The GT output acts to reset the external steering time constant and its state is a function of Est and the voltage on St.	
18	V _{DD}	Positive power supply (Normally connected to +5V).	

5.2.11 ABSOLUTE MAXIMUM RATINGS:

PARAMETER	SYMBOL	VALUE
Power supply voltage ($V_{DD}-V_{SS}$)	V_{DD}	6.0V max
Voltage on any pin	V_{dc}	$V_{SS}-0.3V, V_{DD}+0.3$
Current on any pin	I_{DD}	10mA max
Operating temperature	T_A	-40°C to +85°C
Storage temperature	T_S	-65°C to +150°C

5.2.12 TONE DECODING:

F _{LOW}	F _{HIGH}	KEY(REF.)	OE	Q4	Q3	Q2	Q1
697	1209	1	H	0	0	0	1
697	1336	2	H	0	0	1	0
697	1477	3	H	0	0	1	1
770	1209	4	H	0	1	0	0
770	1336	5	H	0	1	0	1
770	1477	6	H	0	1	1	0
852	1209	7	H	0	1	1	1
852	1336	8	H	1	0	0	0
852	1477	9	H	1	0	0	1
941	1209	0	H	1	0	1	0
941	1336	*	H	1	0	1	1
941	1477	#	H	1	1	0	0
697	1633	A	H	1	1	0	1
770	1633	B	H	1	1	1	0
852	1633	C	H	1	1	1	1
941	1633	D	H	0	0	0	0
ANY	ANY	ANY	L	Z	Z	Z	Z

L = LOGIC LOW, H = LOGIC HIGH, Z= HIGH IMPEDANCE

5.2.13 DC CHARACTERISTICS:

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Operating supply voltage	V_{DD}	4.75		5.25	V
Operating supply current	I_{DD}		3.0	7.0	mA
Standby supply current	I_{DDQ}			100	μA
Power consumption	P_O		15	35	mW
Low level input voltage	V_{IL}			1.5	V
High level input voltage	V_{IH}	3.5			V
Input leakage current	I_{IH}/I_{IL}		0.1		μA
Pull-up(source) current on OE	I_{SO}		6.5	15.0	μA
Input impedance, signal inputs 1,2	R_{IN}	8	10		$M\Omega$
Steering threshold voltage	V_{TST}	2.2		2.5	V
Low level output voltage	V_{OL}			0.03	V
High level output voltage	V_{OH}	4.97			V
Output low(sink) current	I_{OL}		2.5		MA
Output high(source) current	I_{OH}	1.0.40	0.8		MA
Output voltage V_{REF}	V_{REF}	2.4		2.7	V
Output Resistance V_{REF}	R_{OR}		10		$K\Omega$

1. dBm = decibels above or below a reference over of 1 mW into a 600 ohm load.
2. Digit sequence consists of all 16 DTMF tones.
3. Tone duration = 40ms. Tone pause = 40ms.
4. Nominal DTMF frequencies are used, measured at GS.
5. Both tones in the composite signal have an equal amplitude.
6. Bandwidth limited (0 to 3KHz) Gaussian noise.
7. The precise dial tone frequencies are (350 and 440 Hz) 2%.

8. For an error rate of better than 1 in 10,000.
 9. Referenced to lowest level frequency component in DTMF signal.
 10. Minimum signal acceptance level is measured with specified maximum frequency deviation.
 11. Input pins defined as $IN+$, $IN-$ and OE .
 12. External voltage source used to bias V_{REF}
- This parameter also applies to a third tone injected onto the power supply

5.2.14 OPERATING CHARACTERISTICS – GAIN SETTING AMPLIFIER

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Input Leakage current	I_N		100		nA
Input resistance	R_{IN}	4			MΩ
Input offset voltage	V_{OS}		25		mV
Power supply rejection	PSRR	50			dB
Common mode rejection	CMRR	55			dB
DC open loop voltage gain	A_{VOL}	60			dB
Open loop unity gain bandwidth	F_C	1.2	1.5		MHz
Output voltage swing	V_O	3.5			V_{P-P}
Tolerable capacitive load(GS)	C_L			100	PF
Tolerable resistive load (GS)	R_L			50	KΩ
Common mode range	V_{CM}	2.5			V_{P-P}

5.2.15 AC SPECIFICATIONS:

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Valid input signal (each tone of composite signal)		-29		+1	dBm	1,2,3,4,5,8
		27.5		869	mVRMS	
Positive twist accept				10	dB	2,3,4,8
Negative twist accept				10	dB	
Frequency deviation accept limit				$\bar{n}1.5\%$ +2Hz	Nom.	2,3,5,8,10
Frequency deviation reject limit		3.5%			Nom.	2,3,5
Third tone tolerance		-25	-16		dB	2,3,4,5,8,9,13
Noise tolerance			-12		dB	2,3,4,5,6,8,9
Dial tone tolerance		+18	+22		dB	2,3,4,5,7,8,9
Tone present detection time	t_{DP}	5	8	14	ms	
Tone absent detection time	t_{DA}	0.5	3	8.5	ms	
Minimum tone duration accept	t_{REC}			40	ms	
Maximum tone duration reject	t_{REC}	20			ms	
Minimum inter-digit pause accept	t_{ID}			40	ms	
Maximum inter-digit reject	t_{DO}	20			ms	
Propagation delay(St to Q)	t_{PQ}		6	11	μ S	OE = VDD
Propagation delay(ST to Std)	t_{PSID}		9	16	μ S	
Input data setup(Q to Std)	t_{QSID}		4.0		μ S	
Propagation delay(OE to Q), enable	t_{PTE}		50	60	ns	RL=10k Ω ,CL=50pF
Propagation delay (OE to Q), disable	t_{PTD}		300		ns	
Crystal clock frequency	f_{CLK}	3.5759	3.579 5	3.5831	MHz	
Clock output(OSC2), capacitive load	C_{LO}				pF	

5.2.16 APPLICATIONS:

- *Telephone switch equipment*
- *Mobile radio*
- *Remote control*
- *Remote data entry*
- *Paging Systems*
- *Personal Computers*
- *Telephone Answering Machines*
- *Credit Card Systems*

5.3 MC34114

5.3.1 INTRODUCTION:

The MC34114 is a monolithic integrated telephone speech network designed to replace the bulky magnetic hybrid circuit of the telephone set. The MS34114 incorporates the necessary functions of the transmit amplification, receive amplification, and side tone control, each with externally adjustable gain. Loop length equalization varies the gain based on the loop current. The microphone amplifier has a balanced, differential input stage designed to reduce radio frequency interference problems. A MUTE input mutes the microphone and receive amplifiers during dialing. A regulated output voltage is provided for biasing of the microphone and a separate output voltage powers the external dialer, microprocessor, or the other circuitry. The MC34114 is designed to operate at minimum of 1.2 volts, making party line operation possible.

A circuit using MC34114 can be made with Bell Telephone, British Telecom(BT) , and NTT (Nippon Telegraph & Telephone) standards. It is available in a standard 18-pin DIP, and a 20-pin SOIC package.

5.3.2 FEATURES :

- 📞 *Operation down to 1.2 volts*
- 📞 *External adjustable transmit, receive, and sidetone gains*
- 📞 *Differential Microphone amplifier input minimizes RFI susceptibility*
- 📞 *Transmit, receive, and sidetone equalization on both voice and DTMF signals*
- 📞 *Regulated 1.7 volts output for biasing microphone*
- 📞 *Regulated 3.3 volts output for powering external dialer or MPU*
- 📞 *Microphone and receive amplifiers muted during dialing*
- 📞 *Differential receive amplifier output eliminates coupling capacitor*
- 📞 *Operates with receiver impedance of 50Ω and higher*
- 📞 *Complies with NT, Bell Telephone and BT standards*

			VDD
VCC	1	18	MUTE
LR	2	17	MS
VB	3	16	ZD
VR	4	15	RXA
GND	5	14	RXI
MC1	6	13	RXO1
MC2	7	12	RXO2
MC0	8	11	TXI
RAGC	9	10	

Fig 5.3.1 Pin Description

5.3.3 PIN DESCRIPTIONS :

SYMBOL	DESCRIPTIONS
V_{CC}	<i>Power supply pin for the IC. Supply voltage is derived from loop current. Transmit amplifier output operates on this pin</i>
LR	<i>Resistors at this pin set DC characteristics of the circuit. The majority of the loop current flows through the resistors. Other characteristics for individual regulatory agencies</i>
V_B	<i>A Resistor or an appropriate network connected from this pin to V_{CC} sets the terminal impedance</i>
V_R	<i>A 1.1 volt regulated output which can be used to bias the microphone. Additionally the voltage powers a portion of the internal circuitry.</i>
GND	<i>Ground pin for the entire IC. This should not be confused with earth ground.</i>
MC1	<i>Inverting differential input to the microphone amplifier. Input impedance is typically 20 kΩ</i>
MC2	<i>Non-inverting input to the microphone amplifier. Input impedance is typically 20 kΩ</i>
MC0	<i>Microphone amplifier output. Amplifier's gain is fixed at 30dB</i>
RAGC	<i>Loop current sensing output. The voltage at this pin, determined by the loop current and a resistor operates loop length equalization circuit</i>
TXI	<i>Input to the transmit amplifier from the microphone amplifier, DTMF source and other sources. Input impedance ~ 1.0 kΩ</i>
RXO2	<i>Receive amplifier non-inverting differential output. Current capability</i>

	<i>of the receiver typically set at ± 3.0 mA peak</i>
<i>RXOI</i>	<i>Receive amplifier inverting differential output. Current capability of the receiver typically ± 3.0 mA peak</i>
<i>RXI</i>	<i>Summing input to the receive amplifier. This is an AC virtual ground</i>
<i>RXA</i>	<i>Summed outputs of the receive current amplifier, sidetone amplifier and an AGC point. Normally connected to the receive amplifier input through a capacitor</i>
<i>ZB</i>	<i>Input to the receive current amplifier. A balanced network is connected between this pin and VCC. The network affects the receive level and sidetone performance. Input impedance is $\sim 500\Omega$ in series with the diode.</i>
<i>MS</i>	<i>Mode select input. A logic '1' sets the IC for pulse dialing. A logic '0' sets the IC for tone dialing. Effective only if MUTE IS AT LOGIC '0'. Input impedance is $\sim 60K\Omega$.</i>
<i>MUTE</i>	<i>Mute input. A logic '1' sets normal speech mode. A logic '0' mutes the microphone and receives amplifiers and allows MS to be functional. Input impedance is $\sim 60 K\Omega$ referenced to VDD. An internal fixed delay of 11mS minimizes the clicks in the receiver when returning to speech mode.</i>
<i>V_{DD}</i>	<i>A regulated 3.3volt output for an external dialer. Output source current capability is 1.0 mA in speech mode, 2.5 mA in tone dialing mode.</i>

5.3.4 FUNCTIONAL DESCRIPTION :

The MC34114 is a speech network which provides the hybrid function and DC loop current interface of a telephone and is meant to connect TIP and RING through a polarity guard bridge. The transmit, receive, and sidetone gains are externally adjustable, and additionally, line length compensation varies the gain with the variations in the loop current. The microphone amplifier employs a differential input to minimize RFI susceptibility.

The loop current interface portion determines the DC voltage versus current characteristics, and provides the required regulated voltages for internal and external use.

The dialer interface provides three modes of operation :

- *speech (non-dialing)*
- *pulse dialing*
- *tone (DTMF) dialing.*

When switching among the modes, some parameters are changed in order to optimize the circuit operation for that mode.

The DC voltage at V_{CC} is determined by the level shift from V_{CC} to LR plus the voltage across resistors. I_{cc} is internal bias current required by the MC34114, normally in the range of 10mA. I_{cc} can be reduced, if necessary in consistent with the transmit and receive signal requirements.

The following table summarizes the changes in parameters to optimize operation :

<i>FUNCTION</i>	<i>SPEECH</i>	<i>PULSE</i>	<i>TONE</i>
<i>LR Level shift</i>	<i>2.8 V</i>	<i>2.8 V</i>	<i>3.8 V</i>
<i>V_{DD}</i> <i>Current capability</i>	<i>1.0 mA</i>	<i>2.5 mA</i>	<i>2.5 mA</i>
<i>Microphone</i> <i>Amplifier</i>	<i>functional</i>	<i>Muted</i>	<i>Muted</i>
<i>Receive amplifier</i>	<i>Switched out</i>	<i>Switched in</i>	<i>Switched in</i>

5.3.5 DC LINE INTERFACE:

The DC line interface circuit sets the DC voltage characteristics with respect to loop current. In speech and pulse dialing modes current source II is off, and the level shift is due to Q1's base-emitter drop, 1.0 volt across the 20K resistor, and the voltage across R1, which varies with VCC from 0.15 volts to 1.0 volt. When the loop current coming in from Tip and Ring exceeds the I_{cc} requirement, the excess current flows through Q1, R2 and R3 to set the slope of the V-I characteristics for the circuit.

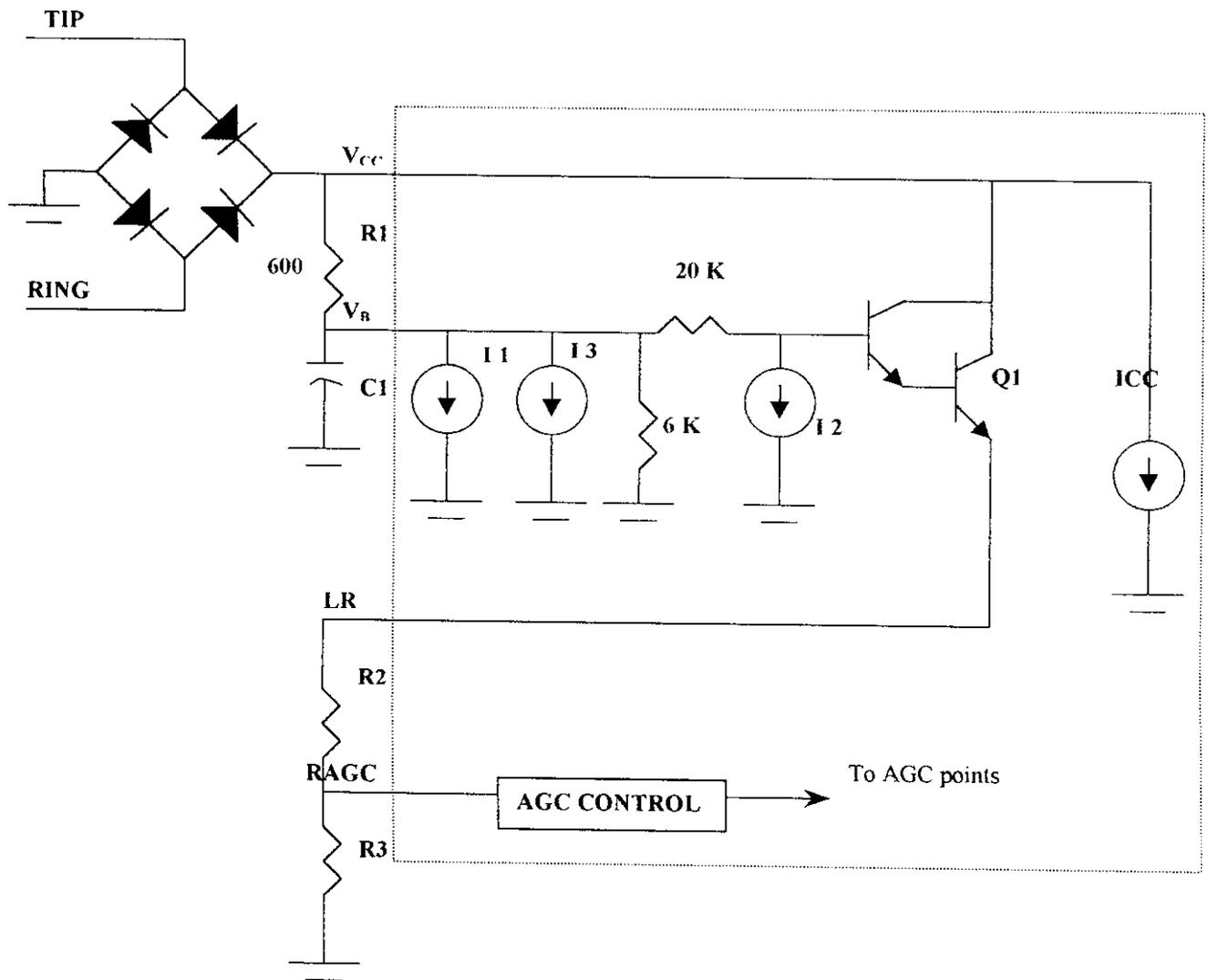


Fig. 5.3.2 DC LINE INTERFACE EQUIVALENT

In the tone dialing mode, current source I1 is on, drawing an additional 1.7 mA through R1, increasing the level shift by ~ 1.0 volts. This feature ensures that, at low loop currents, sufficient voltage is present at Vcc for DTMF signals, and that the V_{dd} regulator supplies sufficient voltage to the external dialer. The I_{cc} current increases by ~ 1.3 mA in this mode. R1 must be kept in the range of 100 to 1800Ω. If it is too large, insufficient current will flow into V_B to bias up the circuit. If it is too small, insufficient filtering at V_B unless C1 is increased accordingly. Speech signals must be well filtered from V_B .

The voltage across R3 determines the operation of the AGC circuit. As the voltage at RAGC increases from 0.4v to 1.2 v, the AGC control varies the current gain of the two AGC points from 1.0 to 0.5, thereby reducing the gains of the transmit and receive paths by 6.0dB.

The values of R2 and R3 can be varied as required to comply with various regulatory agencies; to compensate for the additional circuitry powered by the loop current or to change the starting point of the AGC function. If the AGC is not used, pin 9 should be ground for high gains or V_R for low gains.

5.3.6 VOLTAGE REGULATORS :

The MC341114 has two internal voltage regulators that are used to power both internal and external circuitry. The voltage regulator provides 1.7 volts at maximum current of 500μA. This output is normally used to set the DC bias into

TX1 pin and to bias the electret microphone. V_R will be typically $\sim 300\text{mV}$ less than when V_{cc} is below 2.0 volts.

The V_{dd} regulator provides 3.3 V at a maximum of 1.0mA at the speech mode, 2.5mA in pulse or tone dialing modes. It is normally used to power external dialer, and other associated circuitry. V_{dd} is $\sim 0.5\text{V}$ less than V_{cc} until V_{dd} regulates. It is a shunt type regulator, which automatically switches to high impedance mode when V_{cc} falls below 1.4 V. This prevents excessive battery drain in the event a memory sustaining battery is used with a external dialer. Leakage current is typically $.02\mu\text{A}$ with an applied voltage of upto 6V at V_{dd} with pin 17 open or at V_{dd} . If pin 17 is at ground a current of several micro-amps will flow into V_{dd} and out of pin 17

5.3.7 MICROPHONE AMPLIFIER :

The microphone amplifier has a differential input, single ended output and a fixed gain of + 30 dB. The output is in phase with MC2 and out of phase with MC1. The inputs have nominal impedance of $20\text{K}\Omega$ and are matched to provide a high common mode rejection. To provide a high CMRR against unwanted signals induced in the microphone leads, the microphone should be biased with two equal value resistors.

The output has a DC bias voltage of 1.1 V ($V_{cc} > 3.0\text{ V}$) and nominally swing $2.0\text{ V}_{p,p}$. The output impedance is $\sim 270\Omega$, and has a peak current capability of $\sim 600\mu\text{A}$ for 5% THD. When the MC 34114 is switched to either dialing mode, the microphone amplifier is muted by $\sim 70\text{dB}$, effectively disabling the microphone. The DC voltage at MCO is 80 mV when muted.

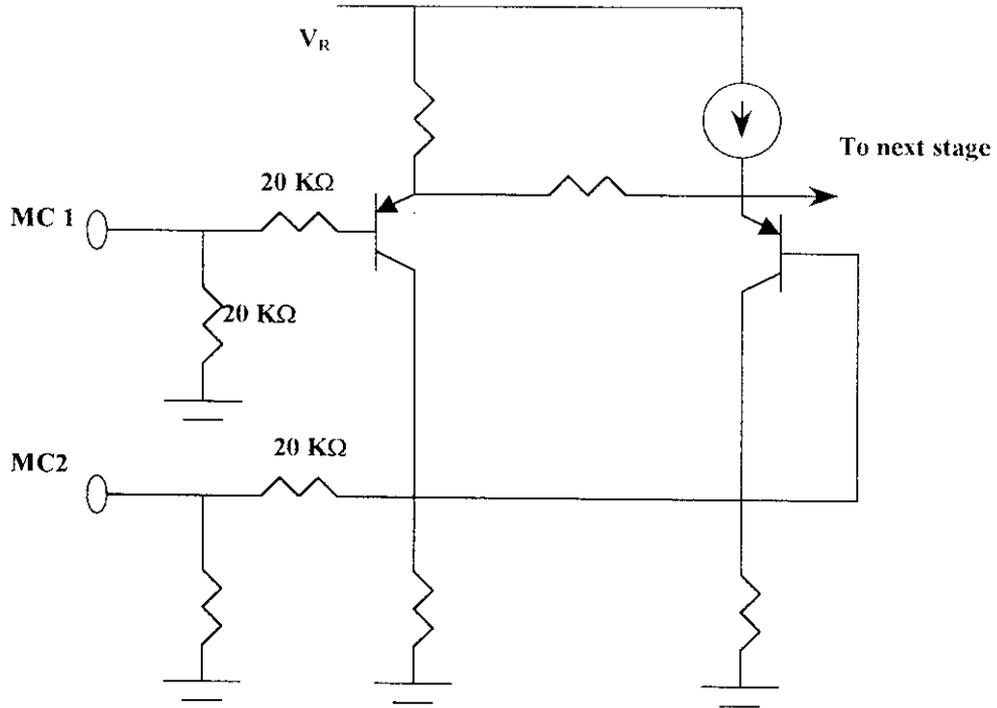


Fig .5.3.3 INPUT STAGE

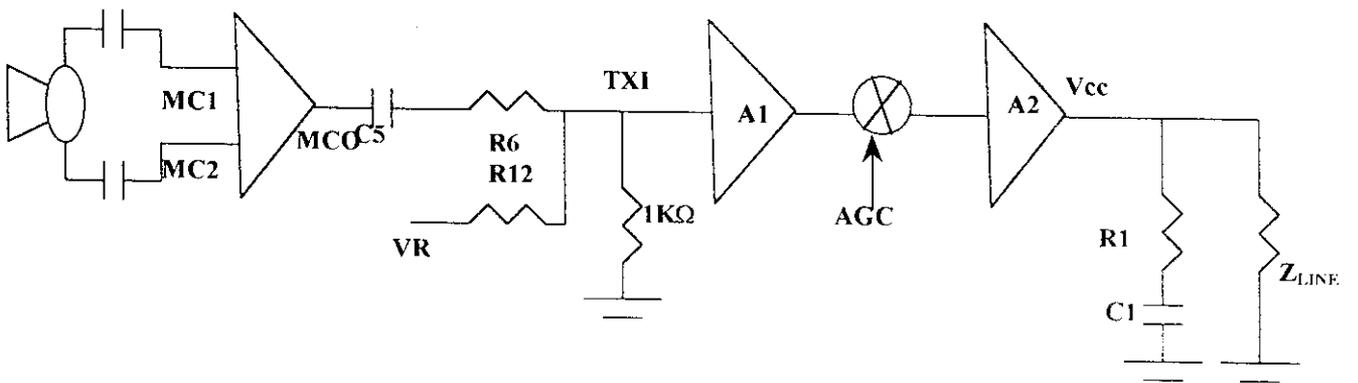


Fig. 5.3.4 TRANSMIT PATH

5.3.8 TRANSMIT PATH :

The AC transmit path consist of components as shown in the fig. The voltage output at MCO is converted to a current into TXI by C5, R6 and TXI's 1.0 k input impedance. A1 and A2 are current amplifiers with a combined gain of 100. The AGC point has current gain of 1.0 at low loop currents, and decreases to 0.5 as loop current increases. Therefore the current gain from TXI to V_{cc} varies from 100 to 50 as loop current is increased. The resulting output at V_{cc} acts on R1 and line impedance to generate a voltage signal at V_{cc} and consequently, at Tip and Ring. At low loop currents, the gain is $\sim 84V/V$ and decreases to 42 V/V at higher loop currents.

For more precise calculations, considerations should be given to the effects of C5, R12 and R7 and C10 and ZB network. The cumulative effects of these additional components is ~ 1.5 dB. The voltage signal at V_{cc} is out of phase with that of at TXI and in phase with that at MC1. The maximum available voltage swing at V_{cc} is a function of impedance at V_{cc} , the DC bias current at A2's output, and the V_{cc} DC voltage. A2's bias current i_d determined by the bias current through R12, which is gained up by A1, A2 and AGC point.

5.3.9 RECEIVE PATH :

The AC receive path consists of the components shown in the Fig.6.5 R1, typically 600Ω , provides AC termination for the signals coming in Tip and Ring. The receive signal creates an AC current through the ZB network and 500Ω

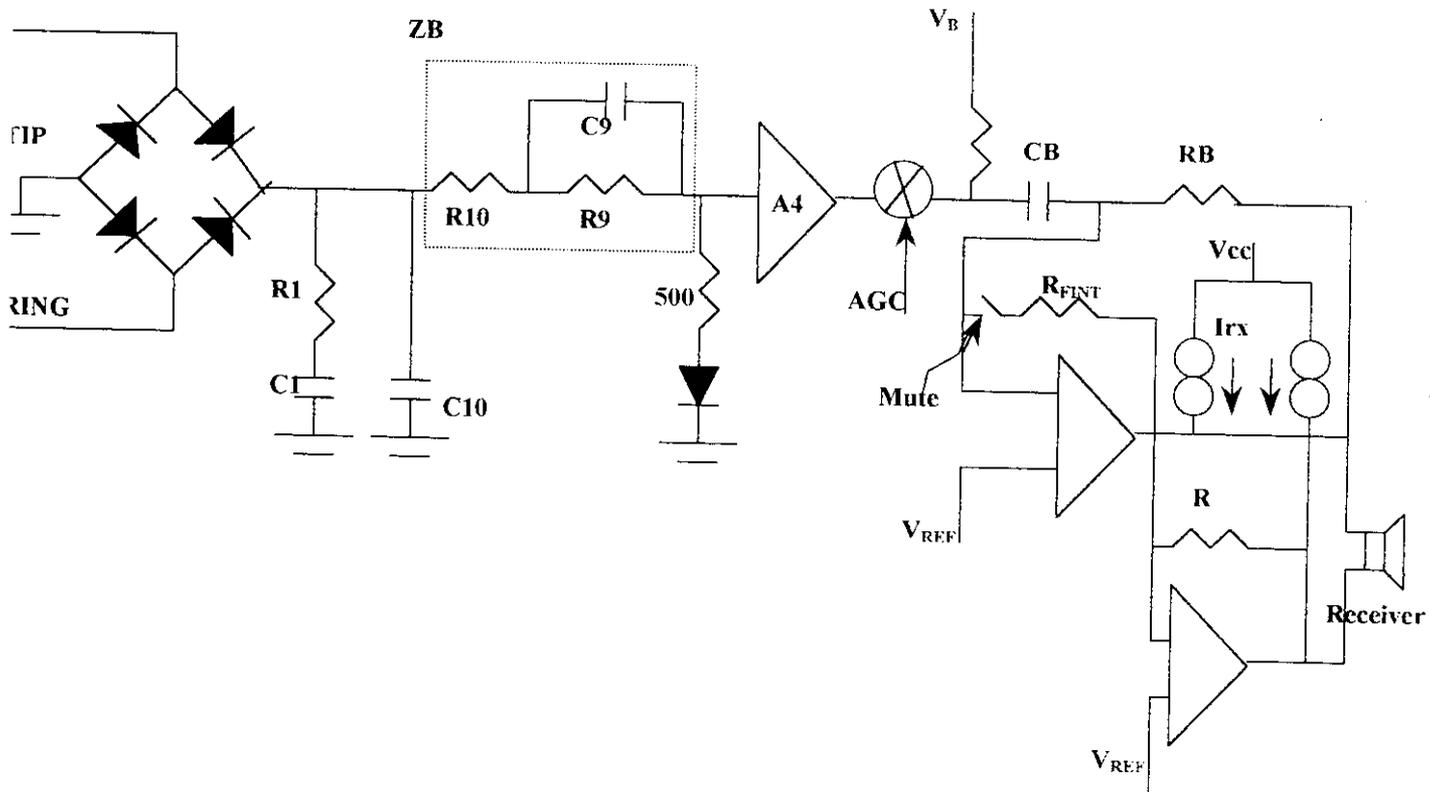


Fig. 5.3.5 RECEIVE PATH

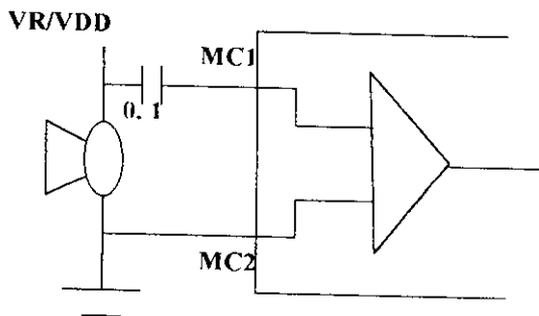


Fig 5.3.6 Terminal Microphone

resistor at the ZB pin. A4 reduces the current by $\frac{1}{2}$, and feeds it through the AGC point, which has a gain of 1.0 at low currents. The AGC gain is reduced to 0.5 as loop current increases. The AGC current out of the AGC point feeds through C8 to RXI, the receive amps summing node. The voltage swing at RXO1 is then determined by the current through C8 and the R8 feedback resistor. The second op-amp is internally configured for inverting unity gain. C9 provides a phase shift to aid sidetone calculation, and C8 can be selected to provide low frequency roll off. High frequency roll off can be obtained by adding a feedback capacitor across R8.

When MC34114 is switched to either dialing mode, the receive gain is muted by the switching in of the internal feedback resistor, typically 1.0 K Ω . The effective feedback resistor for the amplifier is now the parallel combination of R8 and R_{FINT}. The internal resistor is switched in coincident with Mute switching low. However Mute is switched high, a delay occurs before the internal resistor is switched out. This feature prevents dialing transients from being heard as loud clicks in the receiver. The DC bias voltages at RXI, RXO1 and RXO2 is ~ 0.65 volts. The bias current at RXI is ~ 50 nA into the pin. The maximum voltage swing at RXO1 and RXO2 is a function of the receiver impedance.

5.3.10 SIDETONE CANCELLATION :

Sidetone cancellation is provided by the current amplifier which generates a current representative of the transmit signal to cancel the reflected sidetone signal coming in through ZB and A4. To achieve perfect cancellation, it is necessary that $ZB \sim 500\Omega$. Z_{LINE} is the AV impedance of the line. The reactive components of the line's impedance can be compensated by making the ZB network

comparatively reactive. The capacitor C9 provides a phase shift to compensate for the phase shift created by the phone line.

The MC 34114 is designed for use with electret microphones, although dynamic microphones can be used. Carbon microphones are not recommended, as they require considerable bias current, which is not available from MC34114 regulators. When using an electret microphone, which requires more than 1.7 volts, but less than 1.0mA for bias, it can be biased from V_{dd} instead. If three terminal electret microphone is used, it should be connected to MC 34114.

5.3.11 EMI SUSCEPTIBILITY :

Potential EMI susceptibility problems should be addressed early in the electrical and mechanical design of the telephone. EMI may enter the circuit through Tip and Ring, through the microphone wiring, or through any of the PC board traces. The most sensitive pins on the MC34114 are microphone amplifier inputs. Board traces to these pins should be kept short, and associated components should preferably be physically close to the pins. TXI, RXI and ZB should also be considered sensitive to EMI signals.

The microphone wires within the handset cord can act as an antenna, and pick up nearby radio stations. If this is a problem in the final design, adding RF filters to the PC Board where the wires attach to the board can generally reduce the problem.

5.4 74LS244

5.4.1 INTRODUCTION:

It is a octal buffer and a line driver to be employed as memory address drivers, clock drivers and bus-oriented transmitters /receivers

5.4.2 FEATURES:

- *Hysteresis at inputs to improve noise margin*
- *Tri-state outputs drive bus line or buffer memory address registers*
- *Input clamp diodes limit high speed termination effects*

5.4.3 TRUTH TABLE :

INPUTS		OUTPUTS
1G,2G	D	
L	L	L
L	H	H
H	X	Z

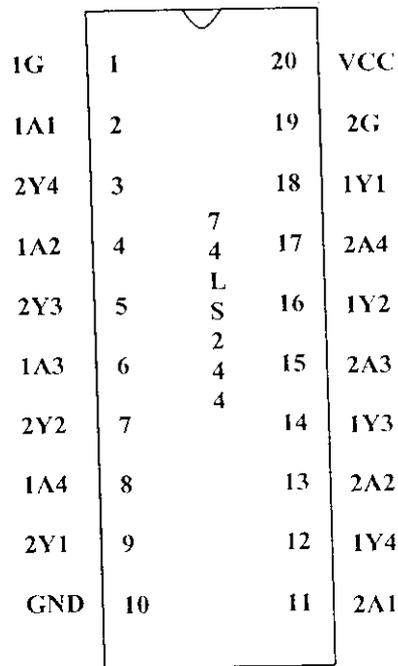


Fig . 5.4.1- Pin Diagram

5.4.4 OPERATING RANGE :

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}	4.75	5.0	5.25	volts
Operating ambient temperature	T_A	0	25	70	volts
Output Current – High	I_{OH}	-	-	15	mA
Output Current – Low	I_{OL}	-	-	24	mA

5.4.5 DC CHARACTERISTICS :

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}	20	-	-	volts
Input Low Voltage	V_{IL}	-	-	0.8	volts
Output High Voltage	V_{OH}	2.4	3.4	-	volts
Output Low Voltage	V_{OL}	-	0.35	-	volts
Input High Current	I_{IH}	-	-	-0.2	mA
Input Low Current	I_{IL}	-	-	20	mA
Output High Current	I_{OH}	-	-	27	mA
Output Low Current	I_{OL}	-	-	46	mA

5.4.6 AC CHARACTERISTICS :

PARAMETER	SYMBOL	TYP	MAX	UNITS
<i>Propagation Delay , Data to Output</i>	t_{PLH}	12	18	<i>nsec</i>
<i>Propagation Delay , Data to Output</i>	t_{PHL}	12	18	<i>nsec</i>
<i>Output Enable Time to High Level</i>	t_{PZH}	15	23	<i>nsec</i>
<i>Output Enable Time to Low Level</i>	t_{PZL}	20	30	<i>nsec</i>
<i>Output Disable Time from Low Level</i>	t_{PLZ}	15	25	<i>nsec</i>
<i>Output Disable Time from High Level</i>	t_{PHZ}	10	18	<i>nsec</i>

6.1 INTRODUCTION:

The parallel portion of the computer makes possible attachment of various devices that accept eight bits of parallel data at standard TTL levels. The rear of the adapter has a 25-pin, D-shell connector.

6.2 PARALLEL PORT REGISTERS:

6.2.1 DATA LATCH (HEX X78, X7C)

Writing to this address causes data to be stored in the printer's data buffer. Reading this address sends the contents of the printer's data buffer to the system microprocessor.

6.2.2 PRINTER CONTROLS (HEX X7A, X7E)

Printer control signals are stored at this address to be read by the system microprocessor. The following are bit definitions for this byte.

Bit	7	<i>Not used</i>
Bit	6	<i>Not used</i>
Bit	5	<i>Not used</i>
Bit	4	<i>+ IRQ Enable – A 1 in this position allows an interrupt to occur when ‘-ACK’ changes from true to false</i>
Bit	3	<i>+ SLCT IN – A 1 in this bit position selects the printer.</i>
Bit	2	<i>- INIT – A 0 starts the printer.</i>

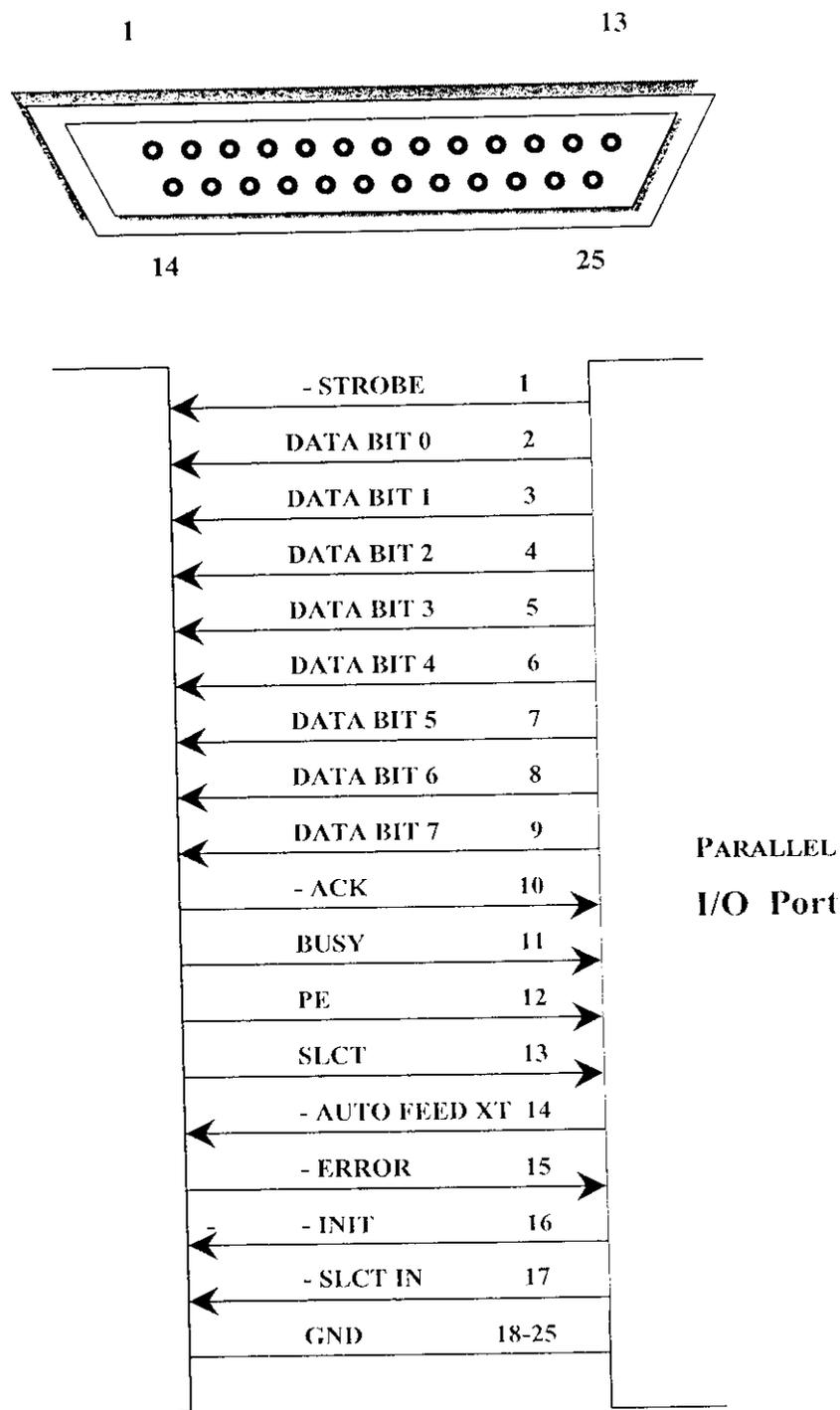
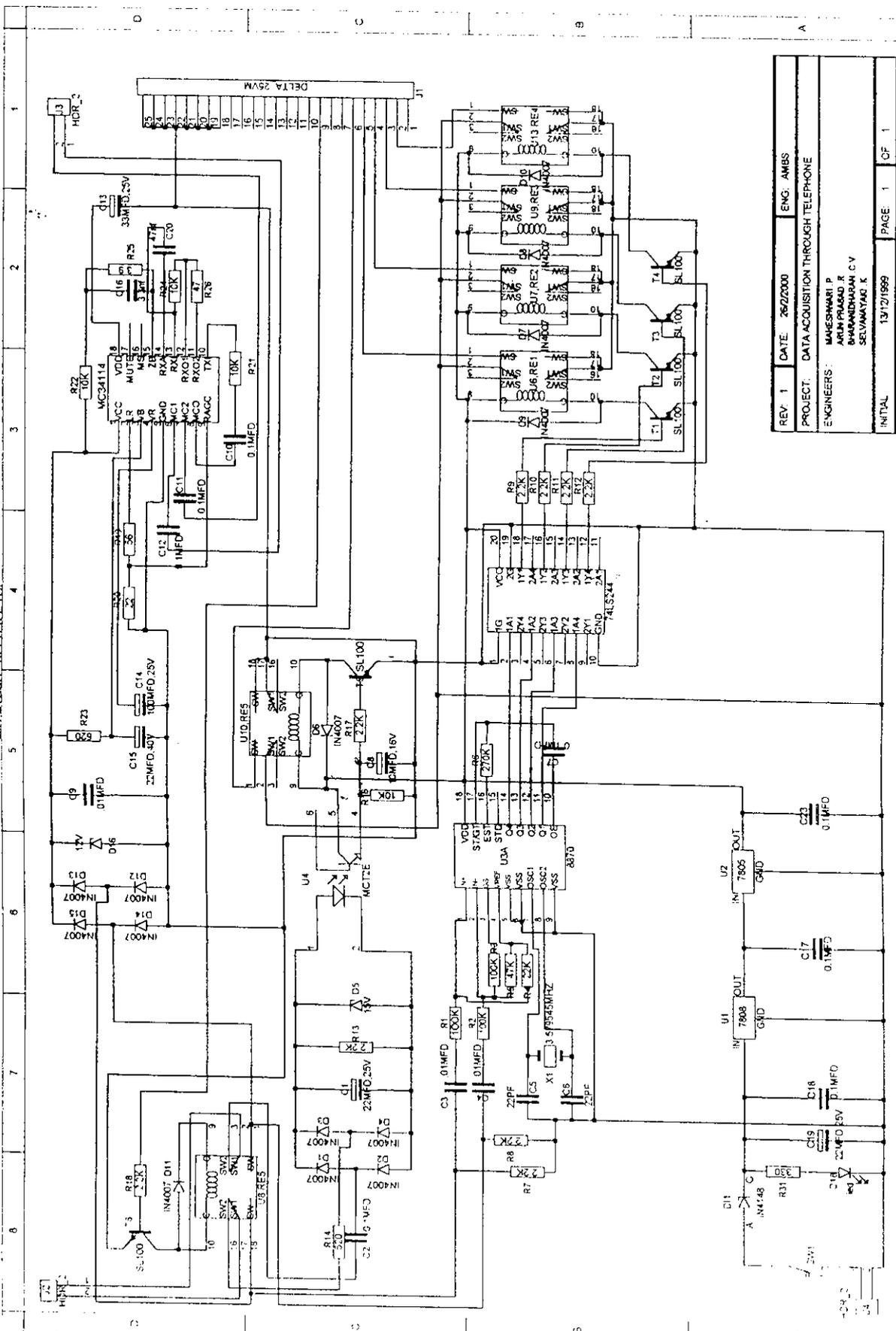


Fig . 6.1 – Parrallet Port Signals

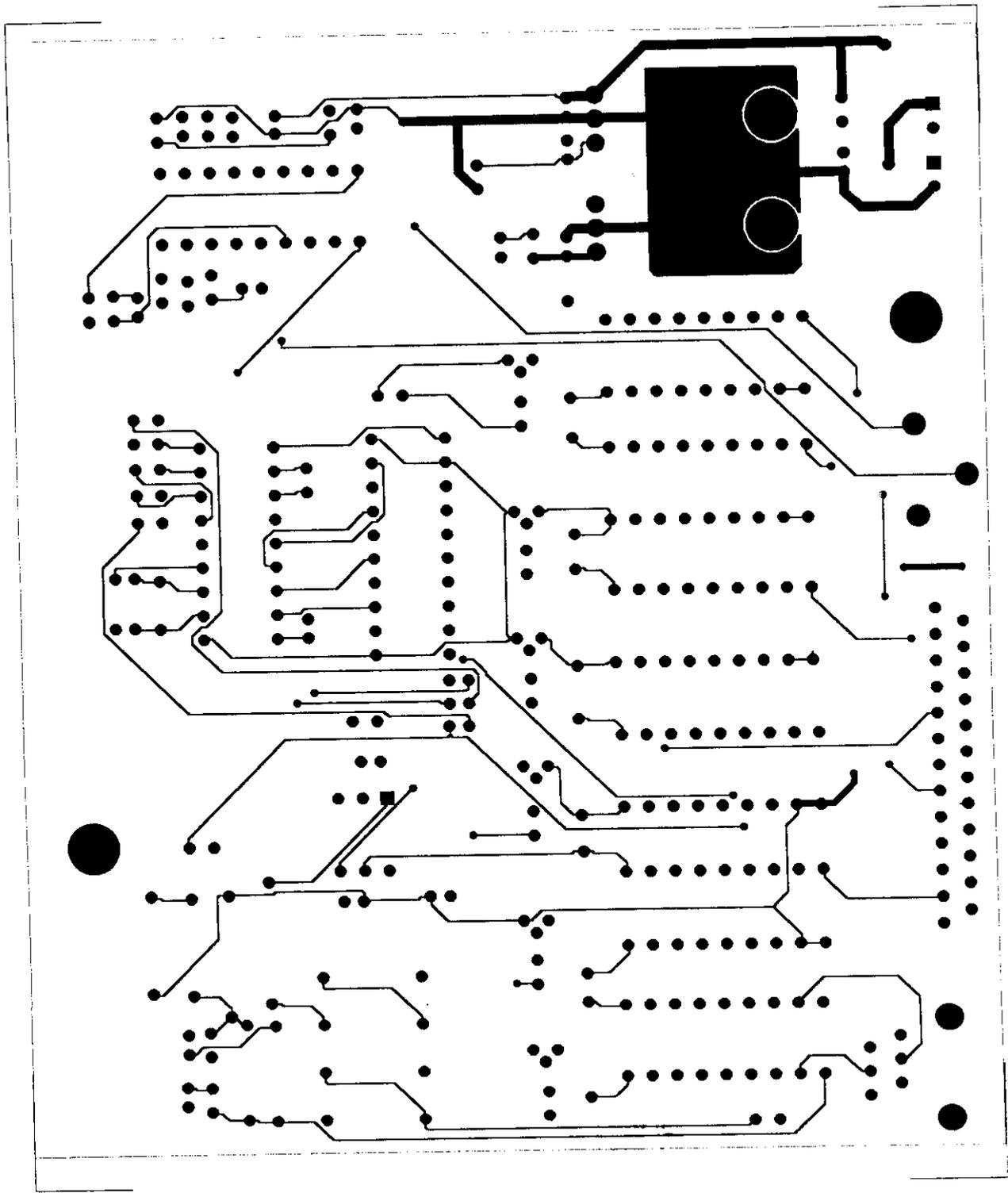
6.3 SPECIFICATIONS:

PARAMETER	RATINGS
<i>Sink Current</i>	<i>24mA (MAX)</i>
<i>Source Current</i>	<i>-2.6mA (Max)</i>
<i>High Level output voltage</i>	<i>2.4Vdc (Max)</i>
<i>Low Level output voltage</i>	<i>0.5Vdc (Max)</i>



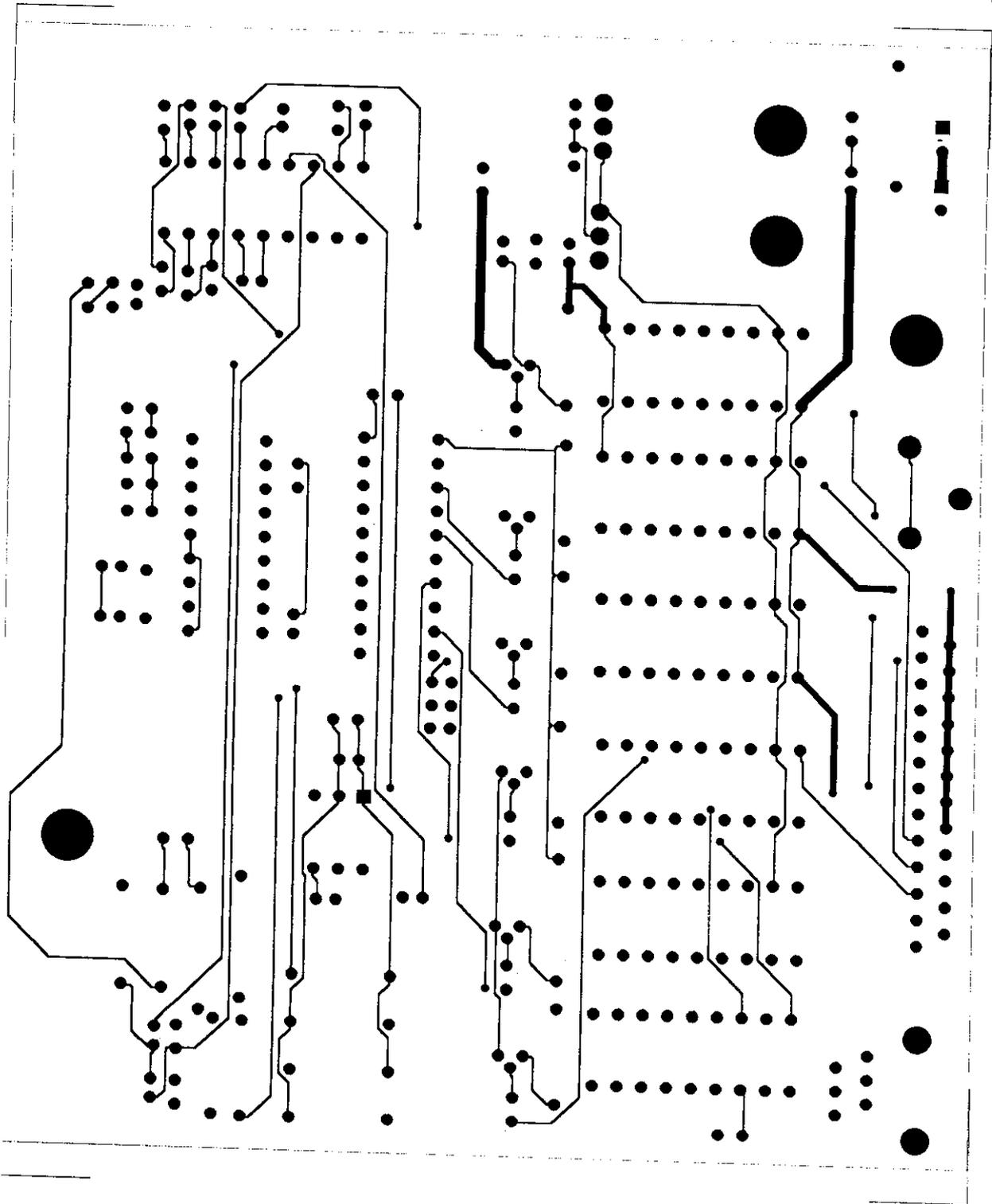


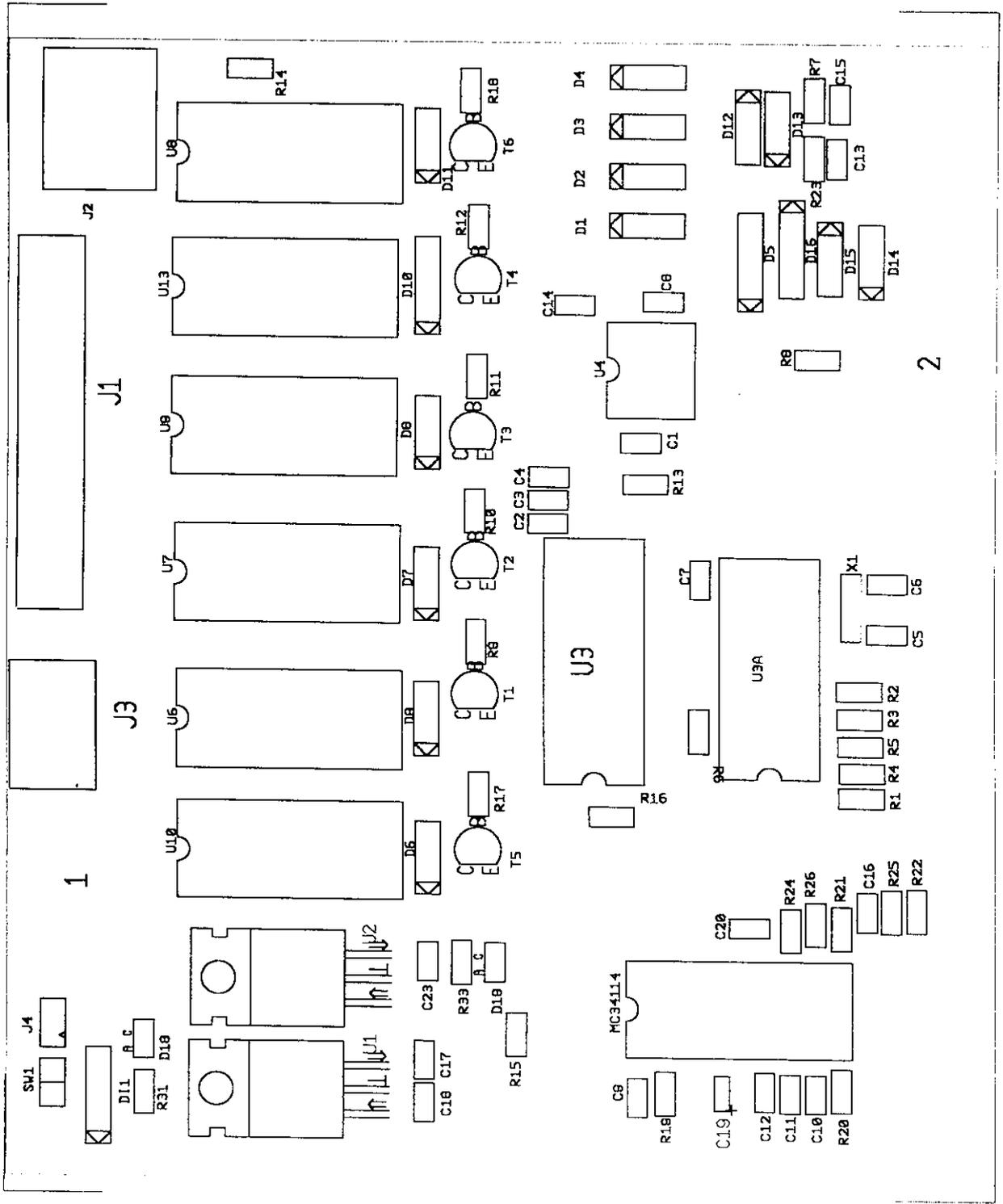
ULT Board
Pcb Layout





U. Thoma
PCB Design





REV. 1.0
 1 1 1 1 1 1

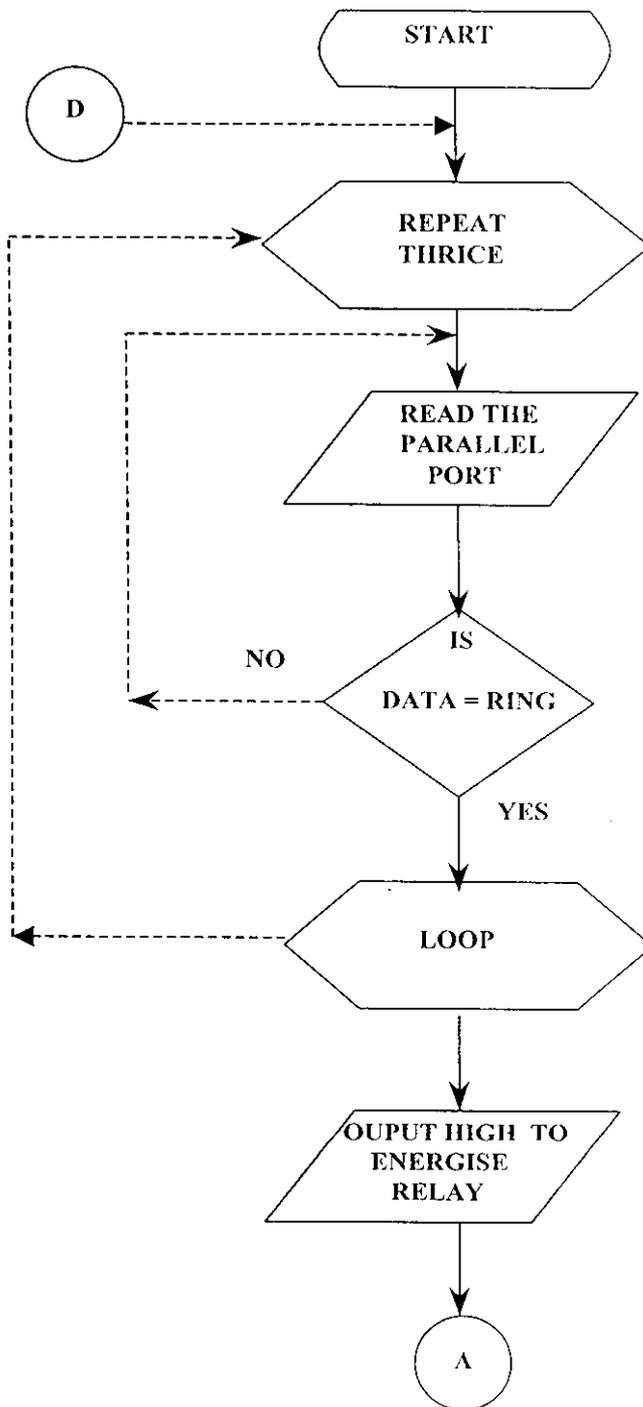


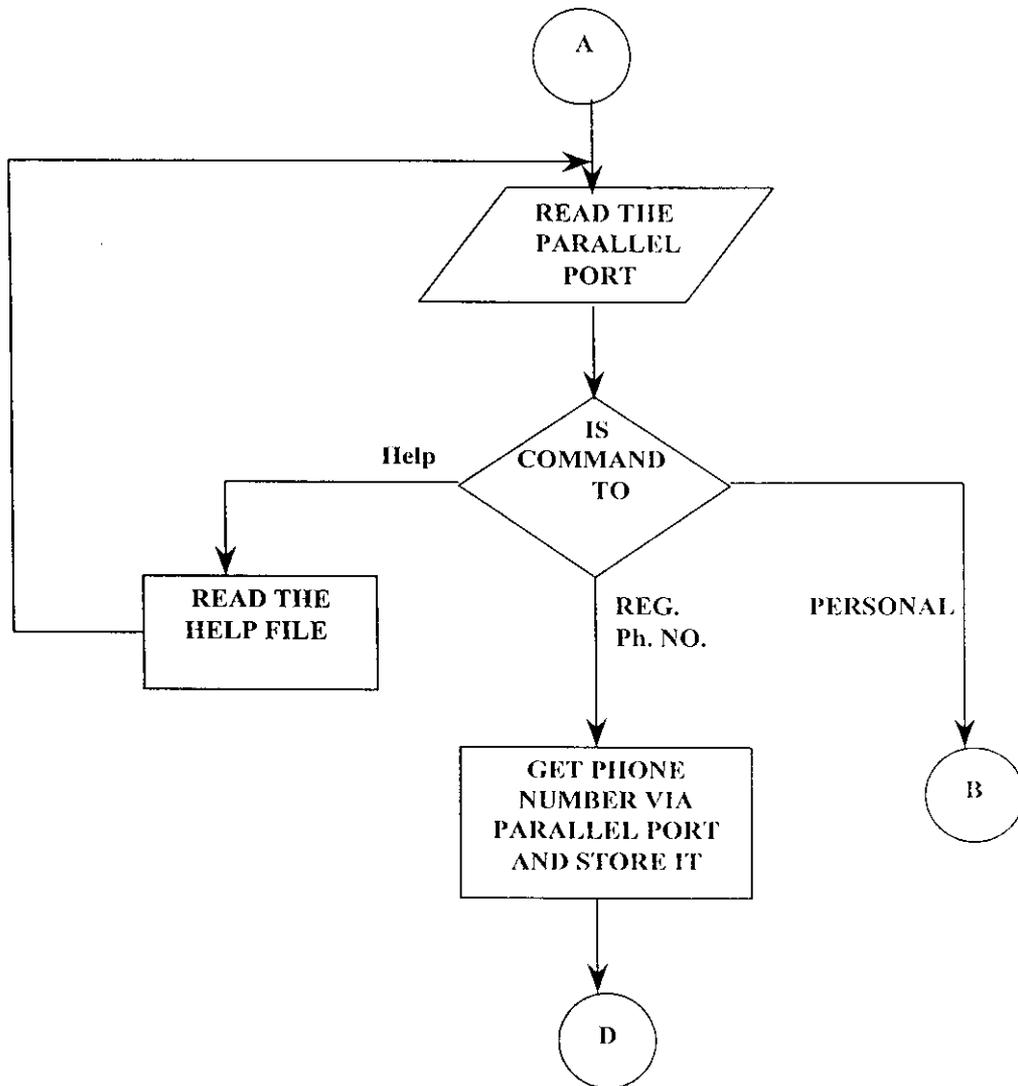
Scale: 1:1 (PCB)
 Scale: 1:50 (ROTATED)
 Date: 01/25/95, 0:00 (mm)

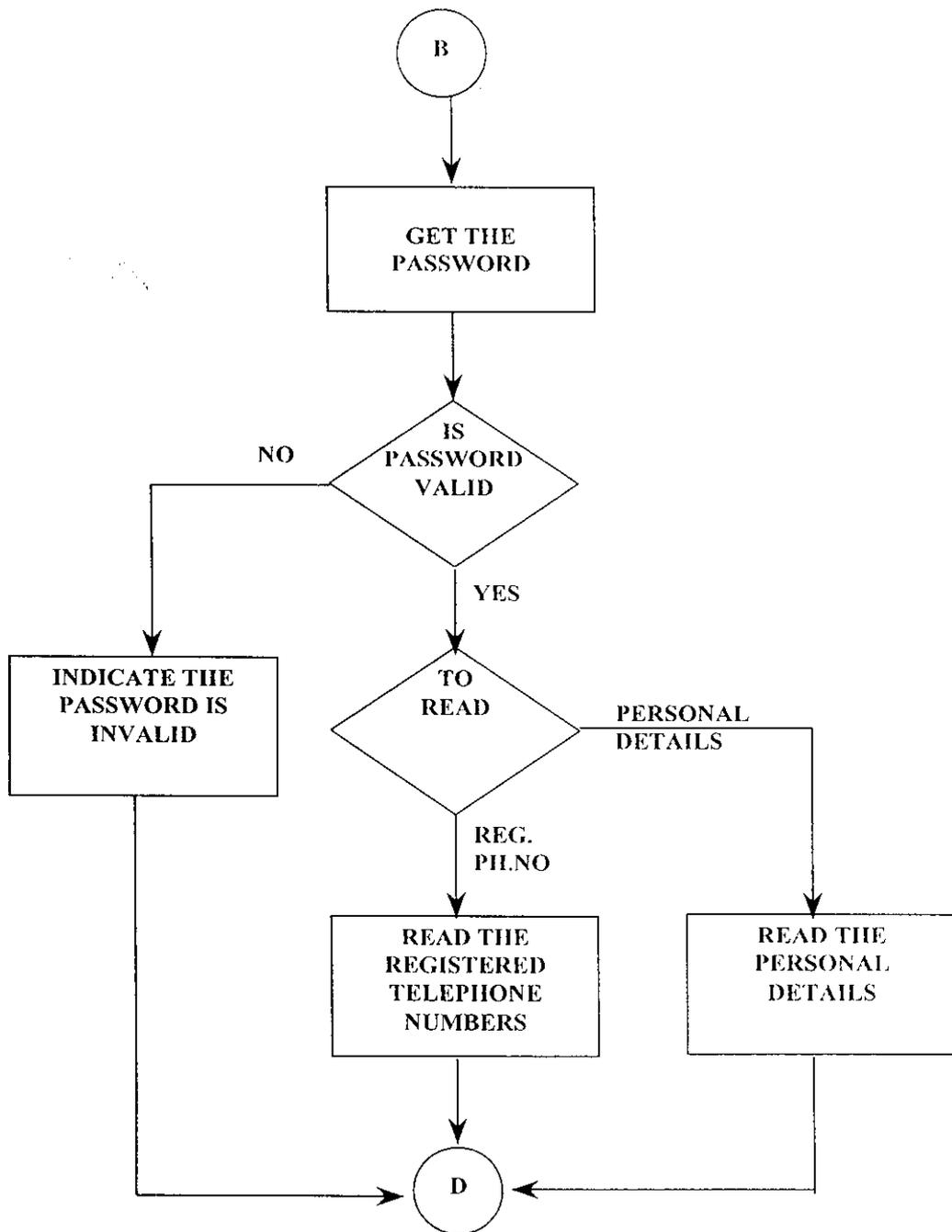
8.1 ALGORITHM:

- *Read the Status Register of the parallel I/O port.*
- *Repeat the above step until a data corresponding to a ring pulse is read.*
- *Repeat the above 2 steps for specified number of ring counts.*
- *Energize the relay (to release the hook switch) by sending a high pulse through the data register.*
- *Get the command from the user, through the status register of the parallel I/O port.*
- *Repeat the above step until a valid command is received.*
- *If the command is to get help, activate the help file and again get the command.*
- *If the command is to register the caller phone number, get the phone number through the parallel I/O port and store it in a file.*
- *If the command is to read the personal data, enter the password and activate the file containing personal details.*
- *If the command is to read the registered phone number, enter the password and activate the file containing phone numbers.*

8.2 FLOW CHART :







8.3 VISUAL BASIC CODES:

```
Private Sub Form_Load()  
Dim DATA As String  
5   Open "C:\DAT\RING.TXT" For Output As #1  
    Print #1, 0  
    Close #1  
    For ring = 1 To 3  
10      X = Shell("C:\DAT\RING.EXE", 0)  
        I = 3  
        GoSub 1000  
        Open "C:\DAT\RING.TXT" For Input As #1  
        Line Input #1, DATA  
        Close #1  
        If DATA = "8" Then GoTo 10  
    Next ring  
    X = Shell("C:\DAT\RELAYON.EXE", 0)  
    X = Shell("READPLEASE.EXE C:\DAT\WELCOME.TXT", 0)  
    I = 15  
    GoSub 1000  
20   Beep  
    I = 2  
    GoSub 1000  
    X = Shell("C:\DAT\RING.EXE", 0)  
    I = 2  
    GoSub 1000
```

```

Open "C:\DAT\COMMAND.TXT" For Input As #1
Line Input #1, DATA
Close #1
If DATA = "1" Then
    X = Shell("READPLEASE C:\DAT\HELP.TXT", 0)
    I = 15
    GoSub 1000
    GoTo 20
End If
If DATA = "2" Then
    X = Shell("READPLEASE.EXE C:\DAT\HELP.TXT", 0)
    I = 3
    GoSub 1000
    30 Beep
    I = 2
    GoSub 1000
    X = Shell("C:\DAT\PHONENO.EXE", 0)
    I = 2
    GoSub 1000
    Open "C:\DAT\RING.TXT" For Input As #1
    Line Input #1, DATA
    Close #1
    If DATA <> "10" Then GoTo 30
End If
If DATA = "3" Then
    GoSub 2000
    X = Shell("READPLEASE C:\DAT\PERSONAL.TXT", 0)

```

```

End If
If DATA = "4" Then
    GoSub 2000
    X = Shell("READPLEASE.EXE C:\DAT\PHONENO.TXT", 0)
End If
I = 15
GoSub 1000
40 X = Shell("READPLEASE.EXE C:\DAT\THANKYOU.TXT", 0)
X = Shell("C:\DAT\RELAYOFF.EXE")
GoTo 5
1000 PAUSETIME = 1
START = Timer
Do While Timer < START + PAUSETIME
Loop
Return
2000
    Beep
    I = 2
    GoSub 1000
    X = Shell("C:\DAT\RING.EXE", 0)
    I = 2
    GoSub 1000
    Open "C:\DAT\COMMAND.TXT" For Input As #1
    Line Input #1, DATA
    Close #1
    If DATA <> "9" Then GoTo 50
    Beep

```

```
I = 2
GoSub 1000
X = Shell("C:\DAT\RING.EXE", 0)
I = 2
GoSub 1000
Open "C:\DAT\COMMAND.TXT" For Input As #1
Line Input #1, DATA
Close #1
If DATA <> "9" Then GoTo 50
Return
50 X = Shell("READPLEASE.EXE C:\DAT\ERROR.TXT", 0)
I = 10
GoSub 1000
GoTo 40
```

8.4 C CODES

8.4.1 RING.CPP

```
#include <stdio.h>
#include <dos.h>
#include <conio.h>

void main()
{
    int ring, data ;
    FILE *start;
    outportb(0x379,0);
    ring = inportb(0x379);
    data = ring & 8;
    start = fopen ("c:\dat\ring.txt", "w");
    fprintf(start, "%d", data);
    fclose(start);
    data = ring & 240;
    start = fopen ("c:\dat\ring.txt", "w");
    fprintf(start, "%d", data);
    fclose(start);
}
```

8.4.2 PHONENO.CPP

```
# include <stdio.h>
# include <dos.h>
# include <conio.h>

void main()
{
    int data;
    FILE *command;
    data = inportb(0x378);
    data = data & 240;
    switch(data)
    {
        case(48) :    data = 1;
                    break;
        case(240) :  data = 2;
                    break;
        case(176) :  data = 3;
                    break;
        case(80) :   data = 4;
                    break;
        case(16) :   data = 5;
                    break;
        case(208) :  data = 6;
```

8.4.3 RELAYON.CPP

```
# include <dos.h>

void main()
{
    outportb(0x378,128);
}
```

8.4.4 RELAYOFF.CPP

```
# include <dos.h>

void main()
{
    outportb(0x378,0);
}
```

The following points suggests the further development of our project :

✘ Making the software to be a fully window based application

✘ Increasing the number of facilities provided like

- A Facsimile facility can be incorporated by receiving the fax number from the user and the WinFax application can be used to a send the fax.*
- Providing access to email*

✘ Accessing of any file from the computer through voice recognition

✘ Recording the message of the caller

Computer - Telephone line interfacing has been achieved using Input Interfacing circuitry, which accepts data and control information which are send through telephone lines. It then sends them to the computer in a form acceptable by the Parallel I/O port in the computer. These informations are recognized by the software and the necessary actions are taken.

All Hardware and Software sections are tested and verified, individually and combined.

-  **Stanley Shell.** *'The PC Data Handbook'*, BPB Publications,
New Delhi First Indian Edition ,1992.
-  **Tom Mc Govern** *'Data Communications Concepts & Applications'*,
BPB Publications , IFBN Edition.
-  *'Fast and LS TTL Data Book'*, Literature Distribution Center,
Fourth Edition 1989.
-  *'PC/AT' Technical Reference' Personal Computer Hardware Reference*
Library, First Edition 1984.
-  **Garewith** *'Teach yourself Visual Basic 5.0'* ,TechMedia Publications