PAYLOAD INDICATOR

PROJECT REPORT

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IN PARTIAL FULFILMENT OF THE REQUIREMENTS

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Department of Electronics & Communication Engineering

Kumaraguru College of Technology

Coimbatore-641006.

KUMARAGURU COLLEGE OF TECHNOLOGY

COIMBATORE – 641 006

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

CERTIFICATE

This is to certify that this project entitled

PAYLOAD INDICATOR

has been submitted by

Ms/Mr. .....

In partial fulfillment of the requirements for the award of the degree of Bachelor of Engineering in Electronics and Communication Engineering Branch of Bharathiar University, Coimbatore – 641 046 during the Academic year 2002-2003

..... (Guide)

..... (Head of the Department)

Certified that the candidate was examined by us in the project work.

Viva-Voce examination held on .....

University Register Number

.....

..... (Internal Examiner)

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HRD/PROJ/2003
13-March-2003

TO WHOMSOEVER IT MAY CONCERN

This is to certify that the following final year BE (ECE) students of Kumaraguru College of Technology - Coimbatore, have undergone project work in our organisation;

1. **Mr. S. HARIHARAN**
2. **Mr. S. SAKTHIVEL MANIKANDAN**
3. **Ms. S. SUBASHINI**

P-1387

The details are:

- Project Title : PAY LOAD INDICATOR
- Period of project : May 2002 to March 2003
- Department : Product Development Engineering (Electronics)

During this period their performance, attendance and conduct were **Good.**

We wish them the very best for a bright future.

ANTHONY THIYAGARAJAN
Dy. MANAGER - HRD

DEDICATED

TO OUR

BELOVED PARENTS

AND FRIENDS

ACKNOWLEGEMENT

ACKNOWLEDGEMENT

Any teamwork requires the wholehearted contribution of not only the team members, but also of the people who guide and support the work. In this regard, on the successful completion of our project we would like to express our heart felt gratitude to a few people.

To begin with we express our deep sense of gratitude to our principal, **Dr. K.K. Padmanabhan, B.Sc (Engg), M.Tech, Ph.D**, for having provided the necessary facilities to carry out this project successfully.

We would like to convey our sincere thanks to our guide and head of the Department of **Electronics and Communication Engg, Prof. Muthuraman Ramasamy, M.E, FIE, MIEEE (USA), MISTE, MBMESI, C. Engg. (I)** for his excellent motivation and guidance.

We are indebted to our guide **Prof. S. Govindaraju M.E**, for his effort in taking valuable time out to help whenever we needed. We also express our heartfelt thanks to **Mr. G.C. Thiyagarajan M.E, Lecturer,** ECE Department for his valuable assistance.

SYNOPSIS

SYNOPSIS

In most of the automobiles at present the dashboard consists of speedometer, odometer, temperature, pressure and fuel gauges. There is no provision to indicate the load on the vehicle. The load on the vehicle is measured in a weighbridge.

The project 'PAYLOAD INDICATOR' found success in solving this problem. In this project the load on the vehicle is sensed and displayed on the vehicle's dashboard.

Load cell is used as weight sensor. Two are fixed at the beam of the vehicle.. One is to sense the front-end load and other is to sense the rear end load. Load cell converts the weight into an electrical signal. This signal is amplified and processed in a microcontroller and is converted into a weight value. This weight value is sent to the dashboard through RS-232 cable. Then weight is displayed on a Liquid Crystal Display on the dashboard.

The objective of the project was achieved and tested and verified in the company successfully.

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CONTENTS

1. INTRODUCTION

Today we have stepped into the 21st century. So, our science and technology should be abreast with the fast growing world. Load on the present automobiles on Indian roads is measured in a weighbridge.

Electronic manufacturing is the fastest growing segment of the manufacturing world. Electromechanical and mechanical devices are being replaced by electronic devices at a fast rate. The emphasis on quality is matched with the expectations that electronic goods will be manufactured with ever increasing capability at even lower cost.

Microcontroller based design has many advantages such as it is flexible, development time is less and also cost is less. This project uses PIC 16f73 microcontroller and load cell as weight sensor. Depending on the load on the vehicle the pressure exerted on the load cell varies and this causes a variation in the resistance of the gauge. By applying an input to the load cell the output varies proportional to the weight. After processing the signal in the microcontroller weight value is displayed in the Liquid Crystal Display.

2. VEHICLE WEIGHING SYSTEMS

There are many weighing systems at present. Systems can be categorized into one of the following: -

- Portable wheel or axle weighers
- On-board weighing system
- Single axle weighbridge
- Full length plate weighbridge
- Part length weighbridge

2.1 Portable Wheel Axle Weigher:

This is probably the most versatile method of weighing as in theory it should be possible to weigh any wheeled vehicle, anywhere, anytime. However the more axles a vehicles has, the more units one needs to weigh it correctly and the more time it may take to do this. It is also easier to cause weight transfer with this type of equipment. For two axled vehicles, for 'off site'/'away from base' weighing, or where the weighing demands are not particularly high, this is probably the most cost-effective method of all.

2.2 On Board Weighing:

The advantage of these systems are that they are installed either as Original Equipment or After Market products, and adds functionality to vehicle information. Increasingly these systems are becoming compatible with Satellite and GPS technology to enable drivers and fleet managers to control the weights of their vehicles. Since these systems are on-board, they cannot give either axle or gross vehicle weights as they can only register weights that are 'above' them, although these elements can be easily set. Each vehicle requiring to be weighed has to have a system fitted and this can prove costly for multi-vehicle operations.

2.3 Single Axle Weighbridge:

With the exception of the two axled vehicles mentioned above, this type of weighbridge provides the easiest and quickest method of obtaining axle weights of all types of road vehicles. Most single axle weighbridges can be operated either statically (stop and go), or dynamically (in motion) which gives the best results when weighing large vehicles with self compensating suspension systems. The most important factor when considering installation of an axle weighbridge is the suitability of the site, which must be firm, flat

and level for at least one vehicle length, either side of the weighbridge platform if reasonable results are to obtained. The risk of weight transfer during the weighing will be the determining factor in levels of accuracy, irrespective of the inherent accuracy of the weighbridge.

2.4 Full Length Plate Weighbridge:

This type of weighbridge gives the highest levels of accuracy for gross vehicle weights and may be tested and stamped for trade use. Plate weighbridges are usually 15 or 18 metres long with capacities ranging from 50 to 100 tonnes, thus they can accommodate even the largest road vehicle. However they are quite expensive and installation costs can add considerably to the final price. A plate weighbridges can be used to obtain individual axle weights provided it is pit mounted (not surface mounted) and that the roadway adjacent to the weighbridge is firm, flat and level.

2.5 Part Length Weighbridge:

These weighbridges are usually 3 or 4 metres long and are most frequently found on farms where they are used to weigh agricultural tractor and trailer combinations. They are essentially a compromise between a full length and an axle weighbridge, and should cost less than the full-length weighbridge. Part length weighbridges can be used to obtain tractor and trailer bogie weights of large articulated trucks and also individual axle weights of other road vehicles provided (as in the case of full weighbridges) that the adjacent roadway is firm, flat and level.

3. SYSTEM DESCRIPTION

3.1 BLOCK DIAGRAM:

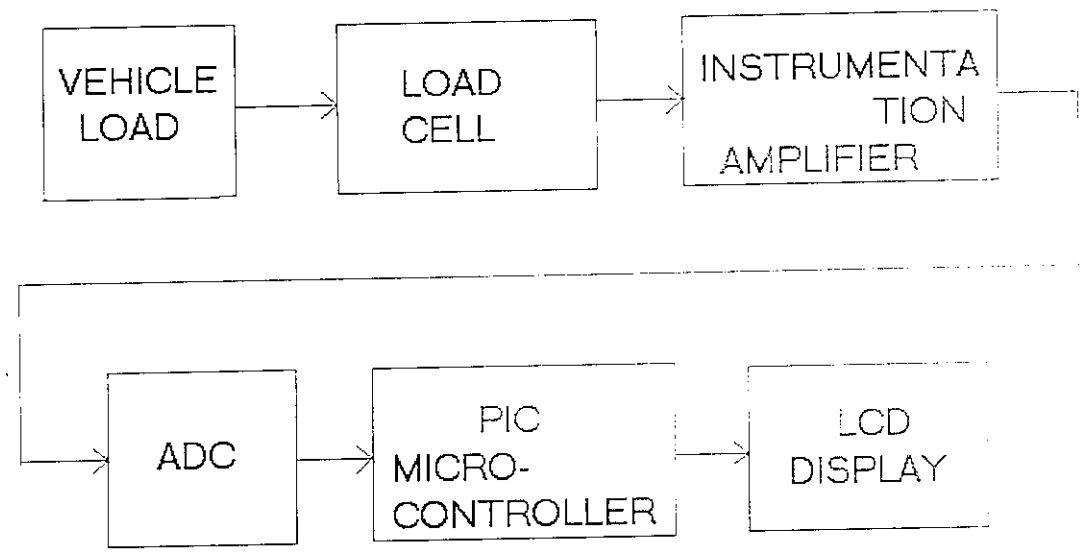


Figure (3.1)

3.2 DESCRIPTION:

Load cell:

Load cell is nothing but a sensor, which senses the weight of the object which is to be weighed. This is actually a force transducer, converts the weight in to electrical signal. This is made of strain gages on which object is placed. Due to the weight a pressure is created which compress the strain gage makes the resistance variations. This resistance variation is converted into an electrical signal by applying an input to the load cell. This is in the range of milli volts.

Instrumentation amplifier:

The output range of load cell is in the order of very few milli volts. In order to process succeeding sections it should be of voltage range. To make it, we need an amplifier section where the input is in the order of milli volts and the output is in volts. The best choice among the available is instrumentation amplifier. Because it has high gain accuracy, high CMMR, high gain stability with low temperature coefficient, low dc offset, and low output impedance.

Analog to digital conversion:

The amplified analog signal is converted into digital signal here. Even though an analog signal represents a real physical parameter with accuracy, it is difficult to process, store or transmit the analog signal with out introducing considerable error because of superimposition of noise. Therefore, for processing, transmission and storage purposes, it is often convenient to express these variables in digital form. It reduces noise and gives better accuracy.

Micro controller:

This is the section where all the processing works are carried out. By testing and experimental results look up table is formed. For a particular value of voltage there is a particular value of weight. This is in hexadecimal format. Then it is converted in to decimal format and given to display section.

LCD display:

This is fixed at the Dash Board of the vehicle where the load of the vehicle is displayed.

4. SENSOR DESCRIPTION

System Components:

In contemporary control applications, weighing systems are used in both static and dynamic applications some systems are technologically advanced, interfacing with computers for data base integration and using microprocessor based techniques to proportion material inputs and feed rates. To send the weight information to computers, signal conditioners are utilized to permit direct communication from the load cell via conversion of the load cell's analog signal to a digital signal.

An entire system can be constructed from five basic modules. They are:

- Load cells.
- Cable.
- Junction box (summing up the load cell signals up to one output).
- Instrumentation (indicators, signal conditioners, etc).
- Peripheral equipment (printers, scoreboards, etc.).

Load Cell:

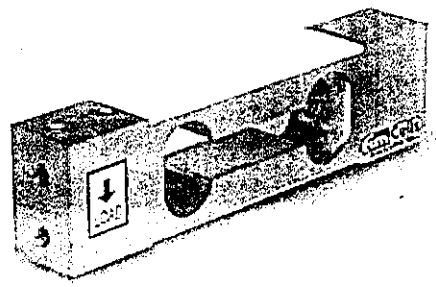
A load cell is classified as a force transducer. This device converts force or weight in to an electrical signal. It is utilized in nearly every electronic

weighing system. The strain gage is the heart of a load cell. A strain gage is a device that changes resistance when it is stressed. The gages are developed from an ultra thin heat-treated metallic foil and are chemically bonded to a thin dielectric layer. "Gage patches" are then mounted to the strain element with specially formulated adhesives. The precise positioning of the gage, the mounting procedure, and the materials used all have a measurable effect on overall performance of the load cell.

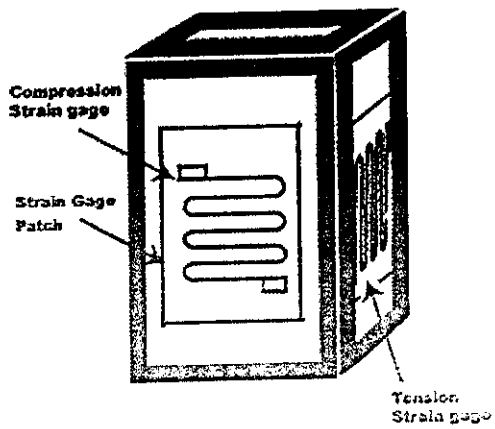
Each gage patch consists of one or more fine wires cemented to the surface of a beam, ring, or more fine wires cemented to the surface of a beam, ring, or column

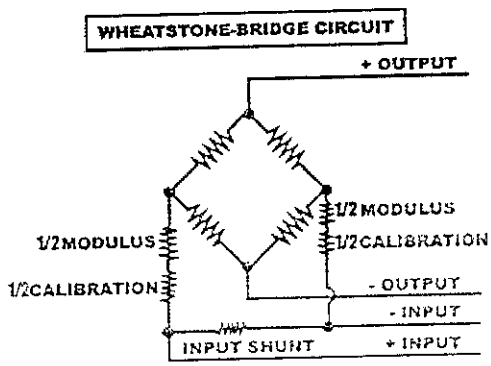
(the strain element) with in a load cell. As the surface to which the gage is attached becomes strained, the wires stretch or compress changing their resistance proportional to the applied load. One or more strain gages are used in the making of a load cell.

Multiple strain gages are connected to create the four legs of a Wheatstone bridge configuration. When an input voltage is applied to the bridge, the output becomes a voltage proportional to the force on the cell. This output can be amplified and processed by conventional electrical instrumentation.



Structure:


Compression
Strain gage
Strain Gage
Patch
Tension
Strain gage


WHEATSTONE-BRIDGE CIRCUIT
+ OUTPUT
1/2 MODULUS
1/2 CALIBRATION
1/2MODULUS
1/2CALIBRATION
- OUTPUT
- INPUT
INPUT SHUNT
+ INPUT

5. INSTRUMENTATION AMPLIFIER

In many applications of signal measurement it is necessary to measure a small signal that sits on top of a slowly varying background that is much larger. The signal would be in the order of few milli volts and hence need amplification for processing it. In our project the output from the load cell will be in the order of few milli volts and hence for processing it with a microcontroller we go for amplifier stage.

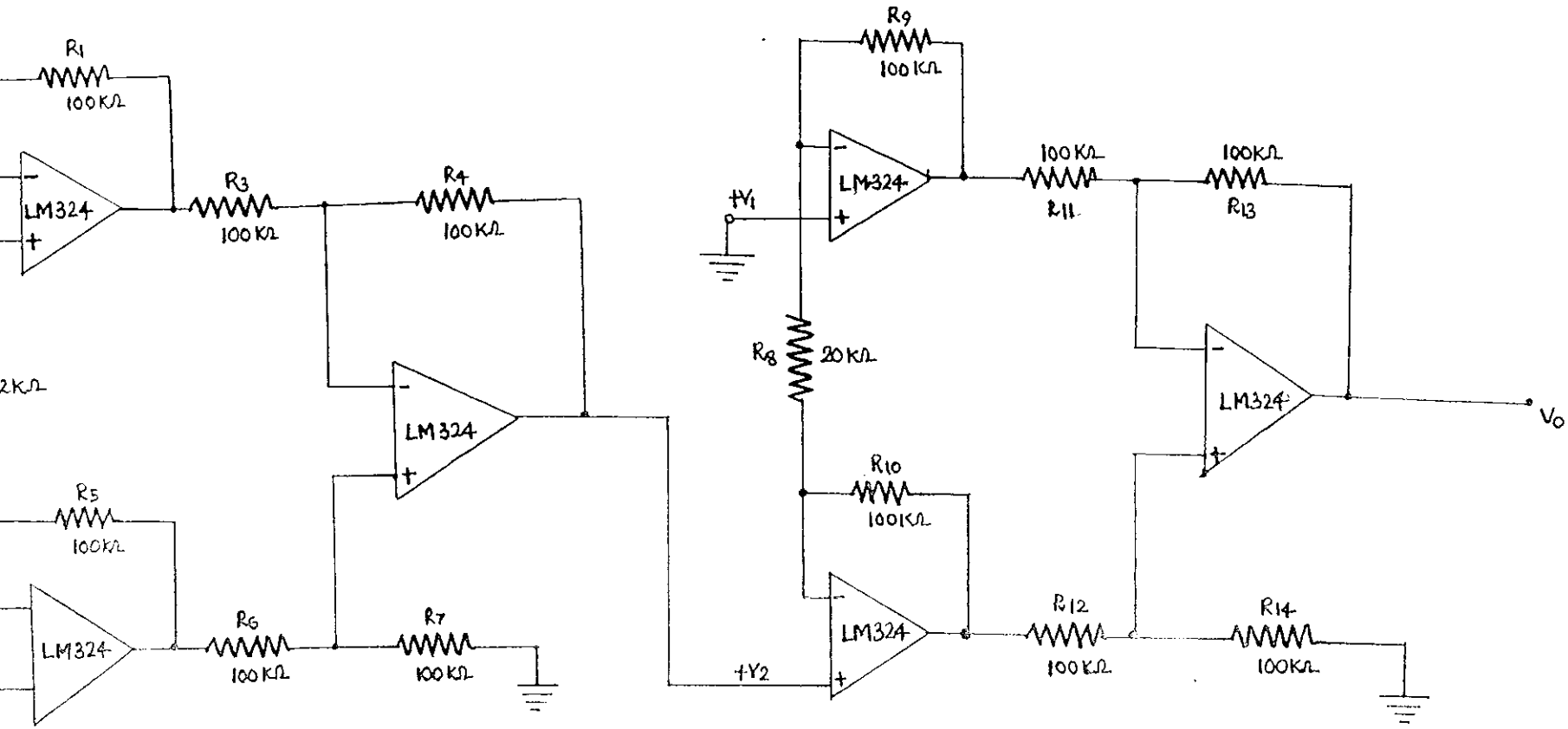
Why not ordinary amplifier?

When the input signal is very small and the gain, which has to be achieved, is large we go for multiple amplifier stages. In doing so the amplifier feedback path plays a vital role that is a part of output is feedback to the input and an oscillatory effect is produced. To avoid these undesired effects we go for high gain stability instrumentation amplifier.

Requirement:

The output from the Load Cell varies from 0 to 50 milli volts. Hence we require a gain of 1000 to make the upper limit 5V.

- First Amplifier stage Gain G1 = 100
- Second Amplifier stage Gain G2 = 10
- Overall Gain G = G1 x G2


R1
100KΩ
LM324
R3
100KΩ
R4
100KΩ
2KΩ
LM324
R5
100KΩ
LM324
R6
100KΩ
R7
100KΩ
R9
100KΩ
+V1
LM324
100KΩ
R11
100KΩ
R13
R8
20KΩ
LM324
Vo
R10
100KΩ
+V2
LM324
R12
100KΩ
R14
100KΩ

DESIGN:

- Gain of a Non-inverting amplifier is (1 + R2/R1)
- Gain of a Inverting amplifier is - R2/R1

where R1 -----> Input Resistance

R2 -----> Feedback Resistance

- The voltage at the (+) input terminal of op-amp A_3 is R2V1'/(R+R2)
- The voltage at the (-) input terminal of op-amp A3 is V2'

Using Superposition Theorem, we have,

$$V0 = -(R2/R1)\,V2' + (1+R2/R1)(R2\,V1'/R1 + R2)$$

$$= R2/R1\,(V1' - V2')$$

- Since, no current flows into op-amp, the current I flowing (upwards) in R is I = (V1 – V2)/r and passes through the resistor R'.

$$V1' = R'I + V1 = R'/R\,(V1 - V2) + V1$$

$$V2' = -R'I + V2 = -R'/R\,(V1 - V2) + V2$$

Putting the values of V1' and V2' in Equation 1, we obtain,

$$V0 = R2/R1\,[2R'/R\,(V1 - V2) + (V1 - V2)]$$

Or

$$V0 = R2/R1\,(1 + 2R'/R)(V1 - V2)$$

Using a variable resistance R we can vary the difference gain of this instrumentation amplifier.

Features:

- ❖ High Gain Accuracy
- ❖ High CMRR
- ❖ High Gain Stability with low Temperature Coefficient
- ❖ Low DC Offset
- ❖ Low Output Impedance
- ❖ No Oscillatory effect

The differential input single-ended output instrumentation amplifier is one of the most versatile signal processing amplifiers available. It is used for precision amplification of differential dc or ac signals while rejecting large values of common mode noise. By using integrated circuits, a high level of performance is obtained at minimum cost.

To obtain good input characteristics, two voltage followers buffer the input signal. The input impedance of the op-amp should be high. This high of an input impedance provides two benefits: it allows the instrumentation amplifier to be used with high source resistances and still have low error and it allows the source resistances to be unbalanced by over 10,000X with no degradation in common mode rejection. The followers drive a balanced differential amplifier, as shown in Figure 5. 1, which provides gain and rejects the common mode voltage.

CHAPTER 6

MICROCONTROLLER UNIT

6. MICROCONTROLLER UNIT:

This is the unit where all the signal processing is done. The Microcontroller that is used for this project is PIC16F73 which is a 28 pin CMOS FLASH microcontroller.

6.1 FEATURES:

High Performance RISC CPU:

- Harvard Architecture
- Only 35 single word instructions to learn
- All single cycle instructions except for program branches which are two-cycle
- Operating speed: DC - 20 MHz clock input

  DC - 200 ns instruction cycle
- Up to 8K x 14 words of FLASH Program Memory,

  Up to 368 x 8 bytes of Data Memory (RAM)
- Pinout compatible to the PIC16C73B/74B/76/77
- Pinout compatible to the PIC16F873/874/876/877
- Interrupt capability (up to 12 sources)
- Eight level deep hardware stack
- Direct, Indirect and Relative Addressing modes
- Processor read access to program memory

Special Microcontroller Features:

- Power-on Reset (POR)
- Power-up Timer (PWRT) and
- Oscillator Start-up Timer (OST)
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- Programmable code protection
- Power saving SLEEP mode
- Selectable oscillator options
- In-Circuit Serial Programming (ICSP) via two pins

Peripheral Features:

- Timer0: 8-bit timer/counter with 8-bit prescaler
- Timer1: 16-bit timer/counter with prescaler, can be incremented during SLEEP via external crystal/clock
- Timer2: 8-bit timer/counter with 8-bit period register, prescaler and postscaler
- Two Capture, Compare, PWM modules
  - Capture is 16-bit, max. resolution is 12.5 ns
  - Compare is 16-bit, max. resolution is 200 ns

- PWM max. resolution is 10-bit

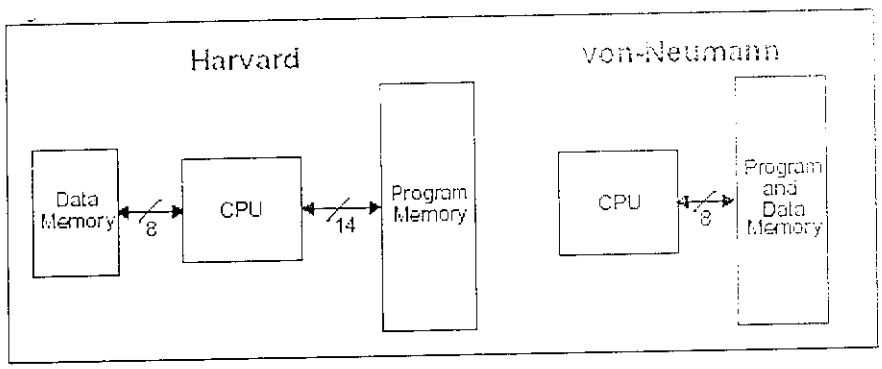
- 8-bit, up to 8-channel Analog-to-Digital converter
- Synchronous Serial Port (SSP) with SPI (Master mode) and I 2 C (Slave)
- Universal Synchronous Asynchronous Receiver Transmitter (USART/SCI)
- Parallel Slave Port (PSP), 8-bits wide with external RD, WR and CS controls (40/44-pin only)
- Brown-out detection circuitry for Brown-out Reset (BOR)

CMOS Technology:

- Low power, high speed CMOS FLASH technology
- Fully static design
- Wide operating voltage range: 2.0V to 5.5V
- High Sink/Source Current: 25mA
- Industrial temperature range
- Low power consumption:
  - < 2 mA typical @ 5V, 4 MHz
  - 20 μA typical @ 3V, 32 kHz
  - < 1 μA typical standby current

6.2 HARVARD ARCHITECTURE:

Harvard architecture has the program memory and data memory as separate memories and is accessed from separate buses. This improves bandwidth over traditional von Neumann architecture in which program and data are fetched from the same memory using the same bus. To execute an instruction, a von Neumann machine must make one or more (generally more) accesses across the 8-bit bus to fetch the instruction. Then data may need to be fetched, operated on, and possibly written. As can be seen from this description, that bus can be extremely congested. While with a Harvard architecture, the instruction is fetched in a single instruction cycle (all 14-bits). While the program memory is being accessed, the data memory is on an independent bus and can be read and written. These separated buses allow one instruction to execute while the next instruction is fetched. A comparison of Harvard vs. von-Neumann architectures is shown in Figure below.



6.3 MEMORY ORGANISATION:

In PIC16F73 'F' signifies that it has flash memory. So we will see some information about flash memories.

Flash Memory:

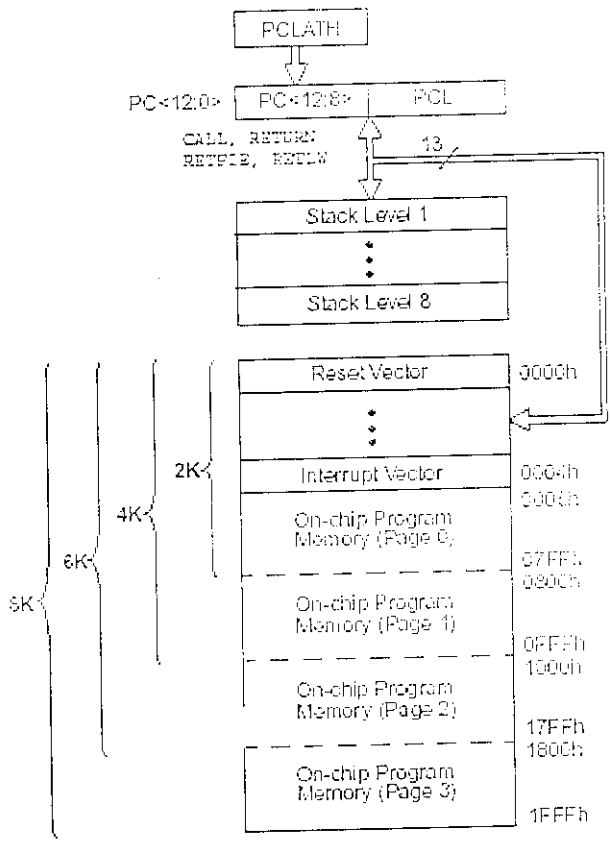
The Flash Memory is a variation of EE-PROM but the difference between the Flash Memory and EE-PROM is in the erasure procedure. The EE-PROM can be erased at a register level, but the flash memory must be erased either in its entirety or at the sector (block) level. These memory chips can be erased and programmed at least a million times. These chips are suitable for also the low-power systems.

There are two memory blocks in the PIC16F73 Microcontroller. The Program Memory and Data Memory have separate buses so that concurrent access can occur. The Program Memory can be read internally by user code.

Program Memory Organization:

The PIC16F73 device has a 13-bit program counter capable of addressing an 8K word x 14-bit program memory. The PIC16F73 device has 4K words. The program memory maps for PIC16F73 device is shown in Figure below. Accessing a location above the physically implemented address will cause a wraparound. The RESET Vector is at 0000h and the Interrupt Vector is at 0004h.

Architectural Program Memory Map and Stack



Programming Memory Paging:

PIC 16F7X devices are capable of addressing a continuous 8K-word block of program memory. The CALL and GOTO instruction provided only 11 bits of address to allow branching within any 2K program memory page. When during a CALL as GOTO instruction the upper 2 bits of the address are provided by PCLATH <4:3> when doing a CALL or GOTO instruction, the user must ensure that the page select bits are programmed so that the desired program memory page in addressed. If a return from a CALL instruction (or interrupted) in executed, the entire 13 bit PC in Popped off the stack. Therefore, manipulation of the PCLATH <4:3> bits are not required for the RETURN instructions (which POPs the address from the stack)

Data Memory Organization:

The Data Memory is partitioned into multiple banks, which contain the General Purpose Registers and the Special Function Registers. Bits RP1 (STATUS<6>) and RP0 (STATUS<5>) are the bank select bits. Each bank extends up to 7Fh (128 bytes). The lower locations of each bank are reserved for the Special Function Registers. Above the Special Function Regis-ters are General Purpose Registers, implemented as static RAM. All

implemented banks contain Special Function Registers. Some frequently used Special Function Registers from one bank may be mirrored in another bank for code reduction and quicker access.

RP1:RP0	BANK
00	0
01	1
10	2
11	3

6.4 REGISTERS:

General Purpose Registers:

The General Purpose Registers area in the Microcontroller is dedicated for defining the user defined registers. To access this General Purpose Register area, the user can address them using FSR or address them directly in the program. In our program for display, we have used the indirect accessing method as it simplifies the programming when large lookup tables are present in the program.

Special Function Registers:

The Special Function Registers are registers used by the CPU and peripheral modules for controlling the desired operation of the device. These registers are implemented as static RAM. The Special Function Registers can be classified into two sets: core (CPU) and peripheral. In our project some of the SFR's that we have used are:

1. STATUS Register
2. ADCON Register
3. ADRES Register
4. PORTA & TRISA Register
5. PORTB & TRISB Register
6. PORTC & TRISC Register

7. PIR1 Register

8. TXSTA, TXREG, RCSTA, RCREG, SPBRG

The description of the STATUS Register is given below and details of other SFR's will be given in subsequent sections.

STATUS Register:

The STATUS register contains the arithmetic status of the ALU, the RESET status and the bank select bits for data memory. The STATUS register can be the destination for any instruction, as with any other register. If the STATUS register is the destination for an instruction that affects the Z, DC, or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the TO and PD bits are not writable, therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, CLRF STATUS will clear the upper three bits and set the Z bit. This leaves the STATUS register as 000u uluu (where u = unchanged). Therefore, that only BCF, BSF, SWAPF and MOVWF instructions are used to alter the STATUS register, because these instructions do not affect the Z, C, or DC bits from the STATUS register.

Indirect Addressing, INDF and FSR Registers:

The INDF register is not a physical register. Addressing the INDF register will cause indirect addressing. Indirect addressing is possible by using the INDF register. Any instruction using the INDF register actually accesses the register pointed to by the File Select Register, FSR. Reading the INDF register itself indirectly (FSR = '0') will read 00h. Writing to the INDF register indirectly results in a no operation (although status bits may be affected).

I/O Ports:

There are 3 I/O ports in PIC16F73 microcontroller. Some of the pins for the I/O ports are multiplexed with an alternate function for the peripheral features on the device. In general, when a peripheral is enabled, that pin may not be used as a general purpose I/O pin.

PORTA and the TRISA Register:

PORTA is a 6-bit wide, bi-directional port. The corresponding data direction register is TRISA. Setting a TRISA bit (= '1') will make the corresponding PORTA pin an input (i.e., put the corresponding output driver in a Hi-Impedance mode). Clearing a TRISA bit (= '0') will make the corresponding PORTA pin an output (i.e., put the contents of the output

latch on the selected pin). Reading the PORTA register reads the status of the pins, whereas writing to it will write to the port latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read, the value is modified and then written to the port data latch. All PORTA pins have TTL input levels and full CMOS output drivers. Other PORTA pins are multiplexed with analog inputs and analog VREF input. In our project the PORTA 0 pin has been used as an analog input pin. Some PORTA pins have been also been used to send commands to the display unit. The operation of each pin is selected by clearing/setting the control bits in the ADCON1 register (A/D Control Register1).

The TRISA register controls the direction of the RA pins, even when they are being used as analog inputs. The user must ensure the bits in the TRISA register are maintained set, when using them as analog inputs.

PORTB and the TRISB Register:

PORTB is an 8-bit wide, bi-directional port. The corresponding data direction register is TRISB. Setting a TRISB bit (='1') will make the corresponding PORTB pin an input (i.e., put the corresponding output driver in a Hi-Impedance mode). Clearing a TRISB bit (= '0') will make the

corresponding PORTB pin an output (i.e., put the contents of the output latch on the selected pin). Each of the PORTB pins has a weak internal pull-up. A single control bit can turn on all the pull-ups. This is per-formed by clearing bit RBPU (OPTION_REG<7>). The weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on a Power-on Reset.

Four of the PORTB pins (RB7:RB4) have an interrupt-on-change feature. Only pins configured as inputs can cause this interrupt to Occur (i.e., any RB7:RB4 pin configured as an output is excluded from the interrupt-on-change comparison). The input pins (of RB7:RB4) are compared with the old value latched on the last read of PORTB. The "mismatch" outputs of RB7:RB4 are ORed together to generate the RB Port Change Interrupt with flag bit RBIF (INTCON<0>).

PORTC and the TRISC Register:

PORTC is an 8-bit wide, bi-directional port. The corresponding data direction register is TRISC. Setting a

TRISC bit (= '1') will make the corresponding PORTC pin an input (i.e., put the corresponding output driver in a Hi-Impedance mode). Clearing a TRISC bit (= '0') will make the corresponding PORTC pin an output (i.e., put the

contents of the output latch on the selected pin). PORTC is multiplexed with several peripheral functions. PORTC pins have Schmitt Trigger input buffers. When enabling peripheral functions, care should be taken in defining TRIS bits for each PORTC pin. Some peripherals override the TRIS bit to make a pin an output, while other peripherals override the TRIS bit to make a pin an input. Since the TRIS bit override is in effect while the peripheral is enabled, read-modify-write instructions (BSF, BCF, XORWF) with TRISC as destination should be avoided.

6.5 INSTRUCTION SET SUMMARY:

The PIC 16 instruction set is highly orthogonal and comprised of there basic categories.

- ❖ Byte oriented operation
- ❖ Bit oriented operation
- ❖ Literal and control operation

Each PIC 16 instruction in a 14bit word divided into an op code, which specifies the instruction type and more or operation, which further specify the operation of the instruction. For byte-oriented instructions, 'f' represents a file register designator specifies were the result of the operation is to be placed if 'd' in zero the result is placed in the w register. If 'd' is one, the result is placed in the file register specified in the instruction.

For bit-oriented instructions 'b' represents a bit field designator, which sleets the bit affected by the operation, while 'f' represents the address of the file in which the bit is located. For literal and control operation. 'k' represents an 8 or 11bit constant or literal value. One instruction cycle consists & oscillator periods for an OSC frequency of 4 MHZ. This gives a normal instruction execution time of lines. All instructions are executed within a single instruction cycle, unless a conditional but true or the program contains is changed as a result of an instruction. When this program contains is changed as a result of an instruction. When this occurs the execution takes 2 instruction cycles with the second cycle execution as a NOP. All execution examples use the format 'oxbb' to represent a hexadecimal no, when 'b' signifies a hexadecimal digit.

6.6 ANALOG TO DIGITAL CONVERSION:

The analog-to-digital (A/D) converter module has up to eight analog inputs. The A/D allows conversion of an analog input signal to a corresponding 8-bit digital number. The output of the sample and hold is the input into the converter, which generates the result via successive approximation. The analog reference voltage is software selectable to either the device's positive supply voltage (VDD) or the voltage level on the VREF pin. The A/D converter has a unique feature of being able to operate while the device is in SLEEP mode.

The A/D module has three registers. These registers are:

- A/D Result Register (ADRES)
- A/D Control Register0 (ADCON0)
- A/D Control Register1 (ADCON1)
  - The ADCON0 register controls the operation of the A/D module.
  - The ADCON1 register configures the functions of the port pins.

The I/O pins can be configured as analog inputs (one I/O can also be a voltage reference) or as digital I/O.

8-bit A/D Block Diagram

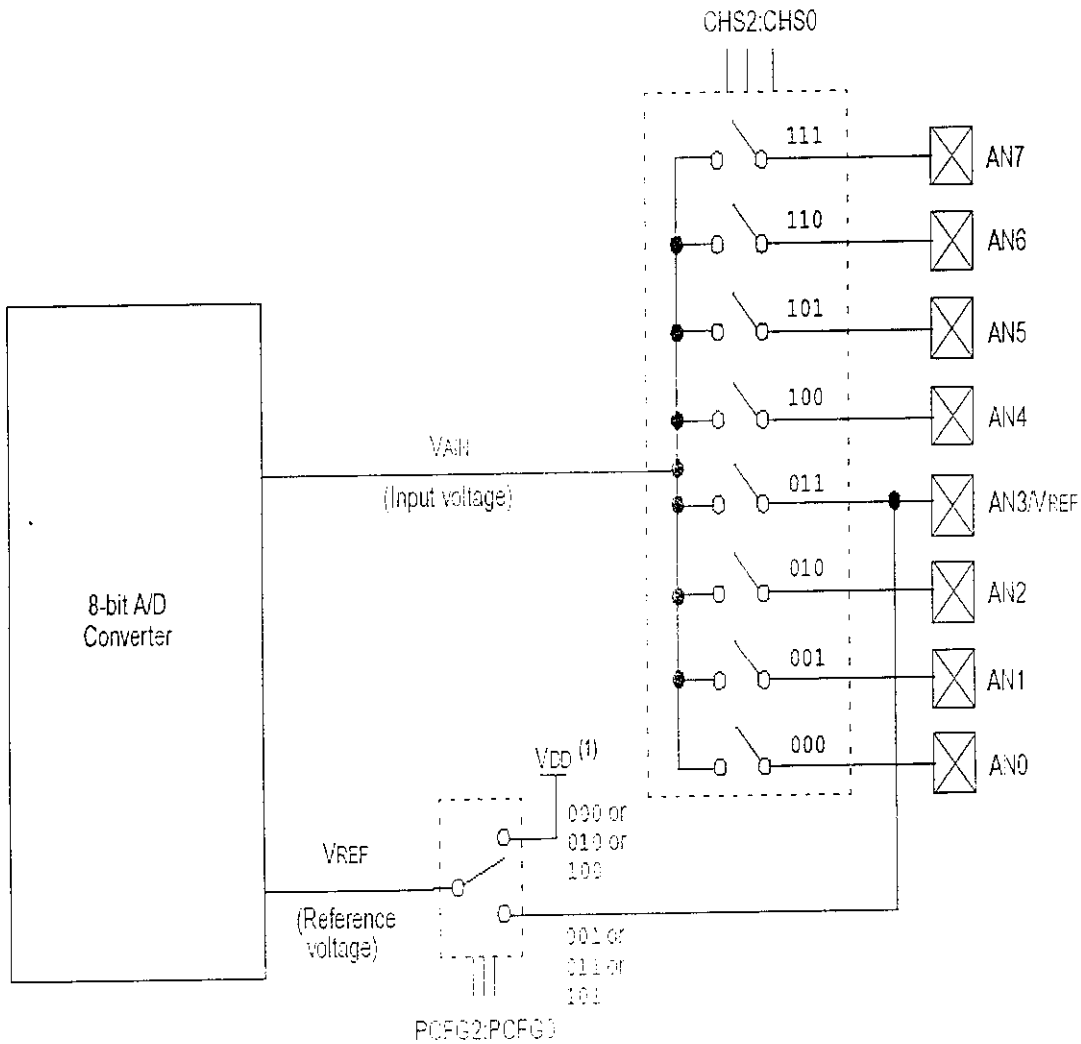


Figure (6.6.1)

Operation:

When the A/D conversion is complete, the result is loaded into the ADRES register, the GO/DONE bit (ADCON0<2>) is cleared, and A/D interrupt flag bit, ADIF, is set. After the A/D module has been configured as desired, the selected channel must be acquired before the conversion is started. The analog input channels must have their corresponding TRIS bits selected as an input.

After this acquisition time has elapsed the A/D conversion can be started. The following steps should be followed for doing an A/D conversion:

1. Configure the A/D module:

   - Configure analog pins / voltage reference / and digital I/O (ADCON1)
   - Select A/D input channel (ADCON0)
   - Select A/D conversion clock (ADCON0)
   - Turn on A/D module (ADCON0)

2. Configure A/D interrupt (if desired):

   - Clear the ADIF bit
   - Set the ADIE bit
   - Set the GIE bit

3. Wait the required acquisition time.

4. Start conversion:

- Set the GO/DONE bit (ADCON0)

5. Wait for A/D conversion to complete, by either:

- Polling for the GO/DONE bit to be cleared

OR

- Waiting for the A/D interrupt

6. Read A/D Result register (ADRES), clear the ADIF bit, if required.

7. For next conversion, go to step 1 or step 2 as required. The A/D conversion time per bit is defined as TAD. A minimum wait of 2TAD is required before next acquisition starts.

Figure 6.6.2 shows the conversion sequence, and the terms that are used. Acquisition time is the time that the A/D module's holding capacitor is connected to the external voltage level. Then there is the conversion time of 10 TAD, which is started when the GO bit is set. The sum of these two times is the sampling time. There is a minimum acquisition time to ensure that the holding capacitor is charged to a level that will give the desired accuracy for the A/D conversion.

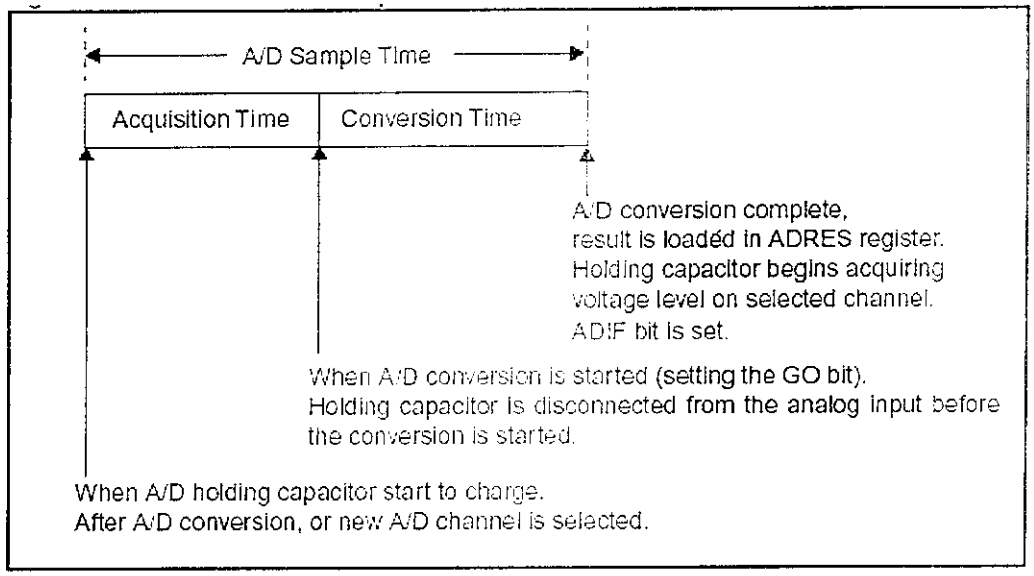


Figure (6.6.2)

Transfer Function:

The ideal transfer function of the A/D converter is as follows: the first transition occurs when the analog input voltage (VAIN) is 1 LSb (or Analog VREF / 256) (Figure 6.6.3).

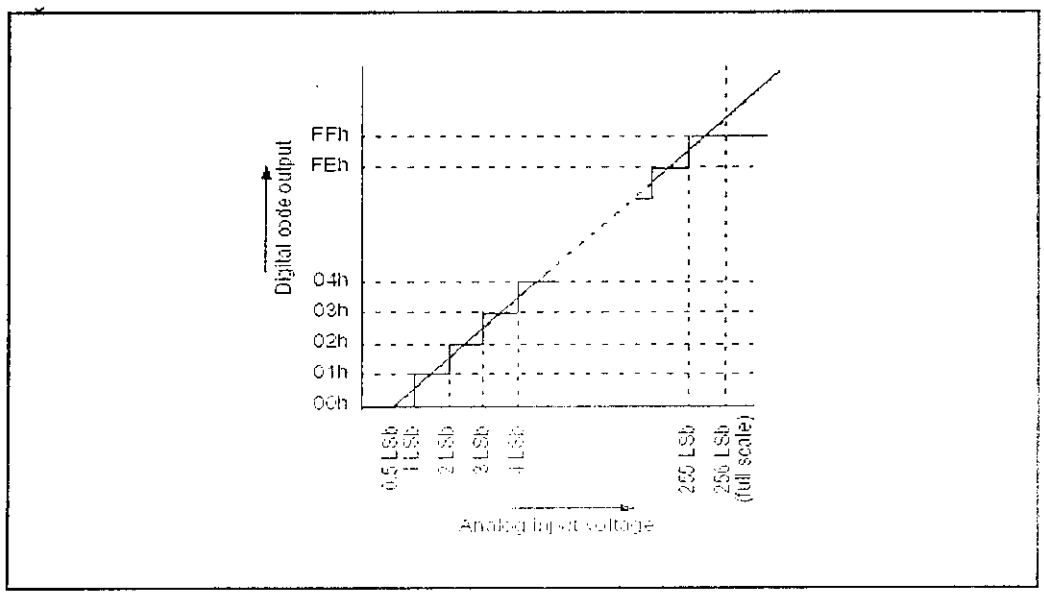


Figure (6.6.3)

Purpose:

The analog output from the load cell is amplified and given to the microcontroller for processing. To process the information in microcontroller it has to be converted into digital form. So we need an analog-to-digital converter. Pic 16f73 has an integrated ADC module. The conversion can be established by simple software codes.

- ✓ Amplified analog signal from front wheel sensor is given to channel 0 of Pic 16f73 (2).
- ✓ Amplified analog signal from the rear wheel sensor is given to channel 0 of Pic 16f73 (1).
- ✓ Both analog signals are converted into digital data using software codes.

6. 7 USART:

The Universal Synchronous Asynchronous Receiver Transmitter (USART) module is one of the two serial I/O modules (other is the SSP module). The USART is also known as a Serial Communications Interface or SCI. The USART can be configured as a full duplex asynchronous system that can communicate with peripheral devices such as CRT terminals and personal computers, or it can be configured as a half duplex synchronous system that can communicate with peripheral devices such as A/D or D/A integrated circuits, Serial EEPROMs etc.

The USART can be configured in the following modes:

- Asynchronous (full duplex)
- Synchronous - Master (half duplex)
- Synchronous - Slave (half duplex)

USART Baud Rate Generator (BRG)

The BRG supports both the Asynchronous and Synchronous modes of the USART. It is a dedicated 8-bit baud rate generator. The SPBRG register controls the period of a free running 8-bit timer. In asynchronous mode bit BRGH (TXSTA<2>) also controls the baud rate. In synchronous mode bit BRGH is ignored. Table shows the formula for computation of the baud rate for different USART modes which only apply in master mode (internal clock). Given the desired baud rate and Fosc, the nearest integer value for the SPBRG register can be calculated using the formula in Table, where X equals the value in the SPBRG register (0 to 255). From this, the error in baud rate can be determined.

Table: Baud Rate Formula

SYNC	BRGH = 0 (Low Speed)	BRGH = 1 (High Speed)
0	(Asynchronous) Baud Rate = Fosc/(64(X+1))	Baud Rate= Fosc/(16(X+1))
1	(Synchronous) Baud Rate = Fosc/(4(X+1))	NA

X = value in SPBRG (0 to 255)

USART Asynchronous Mode:

In this mode, the USART uses standard nonreturn-to-zero (NRZ) format (one start bit, eight or nine data bits and one stop bit). The most common data format is 8-bits. An on-chip dedicated 8-bit baud rate generator can be used to derive standard baud rate frequencies from the oscillator. The USART transmits and receives the LSb first. The USART's transmitter and receiver are functionally independent but use the same data format and baud rate. The baud rate generator produces a clock either x16 or x64 of the bit shift rate, depending on the BRGH bit (TXSTA<2>). Parity is not supported by the hardware, but can be implemented in software (stored as the ninth data bit). Asynchronous mode is stopped during SLEEP.

Asynchronous mode is selected by clearing the SYNC bit (TXSTA<4>).

The USART Asynchronous module consists of the following important elements:

- Baud Rate Generator
- Sampling Circuit
- Asynchronous Transmitter
- Asynchronous Receiver

USART Asynchronous Transmitter

The USART transmitter block diagram is shown in Figure 6.7.1. The heart of the transmitter is the transmit (serial) shift register (TSR). The shift register obtains its data from the read/write transmit buffer, TXREG. The TXREG register is loaded with data in software. The TSR register is not loaded until the STOP bit has been transmitted from the previous load. As soon as the STOP bit is transmitted, the TSR is loaded with new data from the TXREG register (if available). Once the TXREG register transfers the data to the TSR register (occurs in one TCY), the TXREG register is empty and the TXIF flag bit is set. This interrupt can be enabled/disabled by setting/clearing the TXIE enable bit. The TXIF flag bit will be set regardless of the state of the TXIE enable bit and cannot be cleared in software. It will reset only when new data is loaded into the TXREG register.

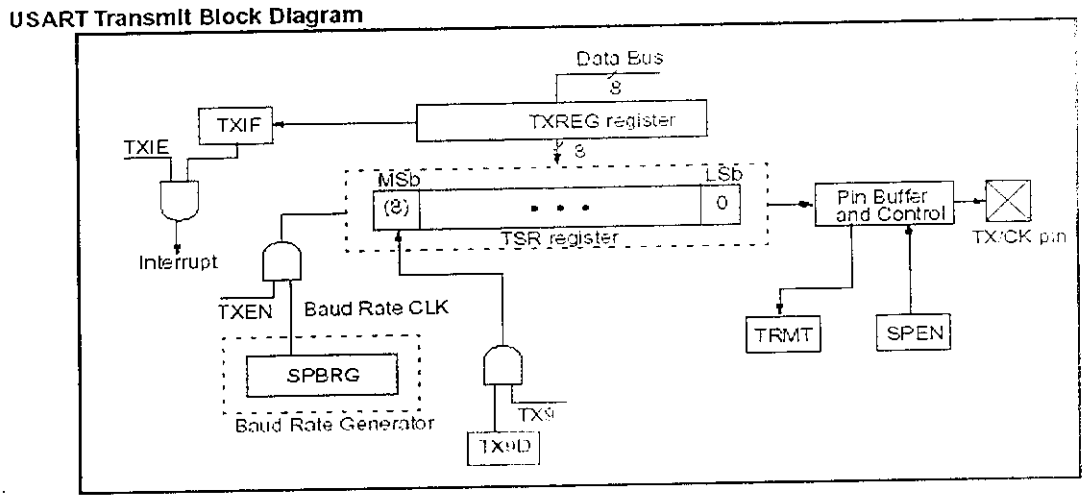


Figure (6.7.1)

Steps to follow when setting up a Asynchronous Transmission:

1. Initialize the SPBRG register for the appropriate baud rate. If a high-speed baud rate is desired, set the BRGH bit.

2. Enable the asynchronous serial port by clearing the SYNC bit and setting the SPEN bit.

3. If interrupts are desired, then set the TXIE, GIE and PEIE bits.

4. If 9-bit transmission is desired, then set the TX9 bit.

5. Enable the transmission by setting the TXEN bit, which will also set the TXIF bit.

6. If 9-bit transmission is selected, the ninth bit should be loaded in the TX9D bit.

7. Load data to the TXREG register (starts transmission).

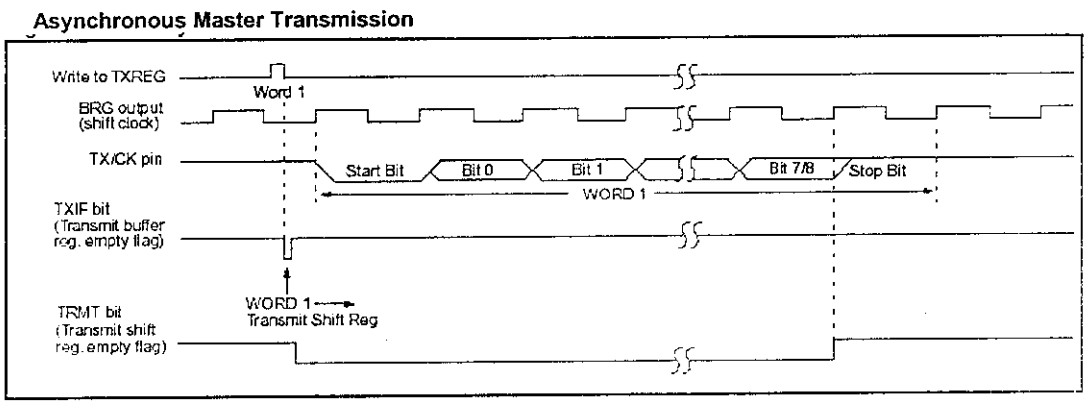


Figure (6.7.2)

USART Asynchronous Receiver

The receiver block diagram is shown in the Figure 6.7.3. The data is received on the RX/DT pin and drives the data recovery block. The data recovery block is actually a high speed shifter operating at x16 times the baud rate, whereas the main receive serial shifter operates at the bit rate or at FOSC. Once Asynchronous mode is selected, reception is enabled by setting the CREN bit (RCSTA<4>).

The heart of the receiver is the receive (serial) shift register (RSR). After sampling the RX/TX pin for the STOP bit, the received data in the RSR is transferred to the RCREG register (if it is empty). If the transfer is complete, the RCIF flag bit is set. The actual interrupt can be enabled/disabled by setting/clearing the RCIE enable bit. The RCIF flag bit is a read only bit which is cleared by the hardware. It is cleared when the RCREG register has been read and is empty. The RCREG is a double buffered register, i.e. it is a two deep FIFO. It is possible for two bytes of data to be received and transferred to the RCREG FIFO and a third byte begin shifting to the RSR register.

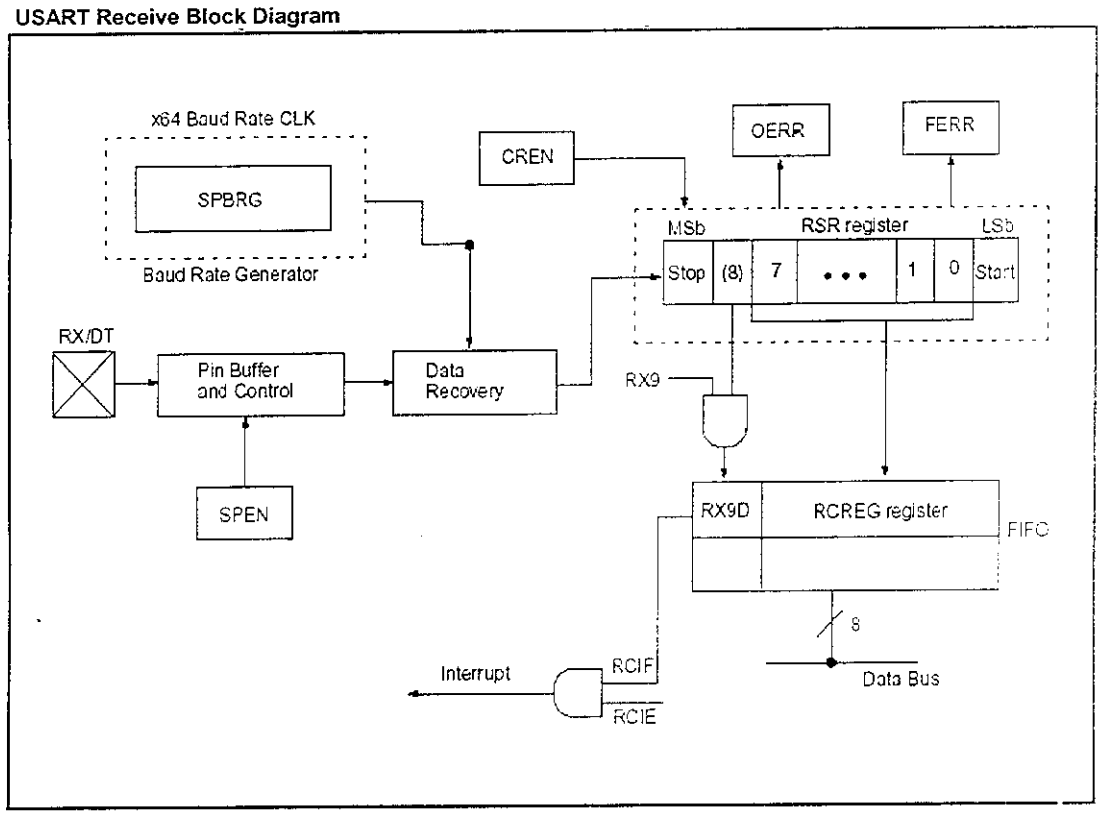


Figure (6.7.3)

Steps to follow when setting up an Asynchronous Reception:

1. Initialize the SPBRG register for the appropriate baud rate. If a high speed baud rate is desired, set bit BRGH.

2. Enable the asynchronous serial port by clearing the SYNC bit, and setting the SPEN bit.

3. If interrupts are desired, then set the RCIE, GIE and PEIE bits.

4. If 9-bit reception is desired, then set the RX9 bit.

5. Enable the reception by setting the CREN bit.

6. The RCIF flag bit will be set when reception is complete and an interrupt will be generated if the RCIE bit was set.

7. Read the RCSTA register to get the ninth bit (if enabled) and determine if any error occurred during reception.

8. Read the 8-bit received data by reading the RCREG register.

9. If any error occurred, clear the error by clearing the CREN bit.

. Asynchronous Reception

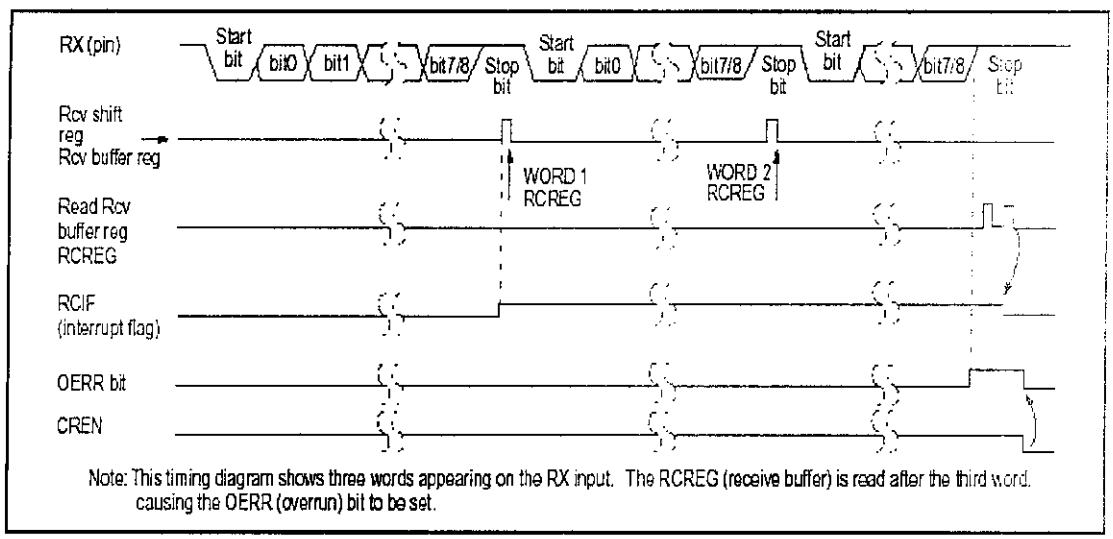


Figure (6.7.4)

Sampling:

The data on the RX/DT pin is sampled three times by a majority detect circuit to determine if a high or a low level is present at the RX pin. Figure 6.7.5 shows the waveform for the sampling circuit. The sampling operates the same regardless of the state of the BRGH bit; only the source of the x16 clock is different.

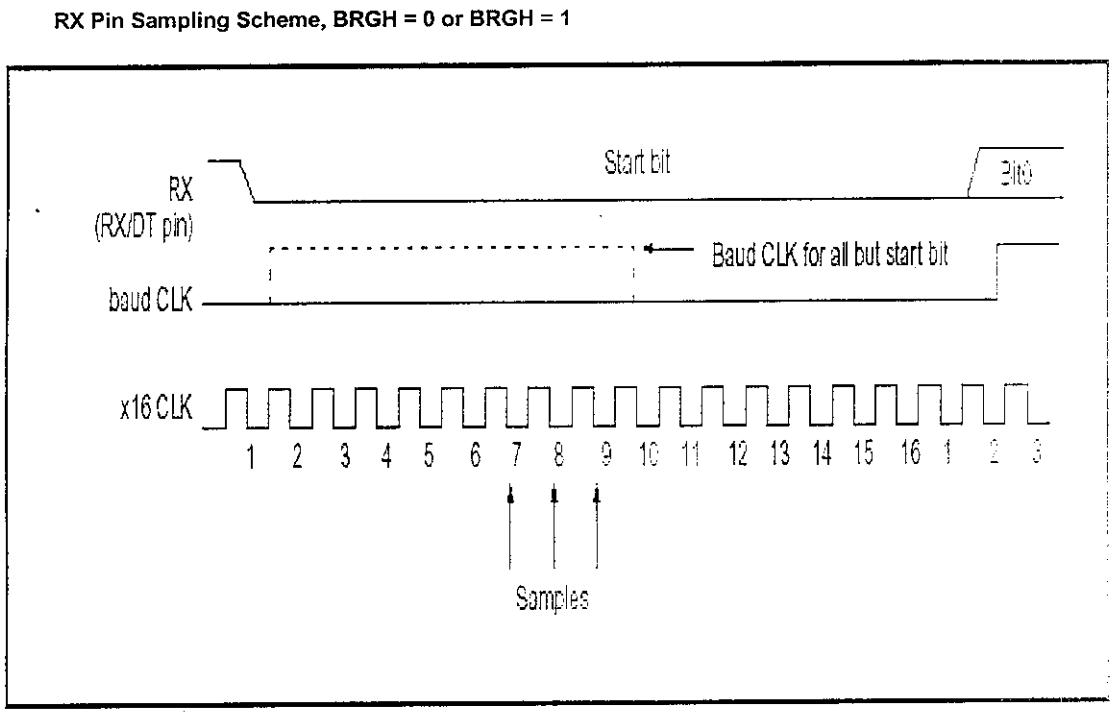


Figure (6.7.5)

Purpose:

By processing the signal from the load cell in the microcontroller we arrive at the weight value. This weight value (rear end) is sent to front-end microcontroller through serial communication by the in built USART module in the Pic16f73. The TTL level is converted into RS-232 level by line drivers and sent through the RS-232 cable. At the receiving end line receivers are used to convert the RS-232 level back into TTL level. Then the USART module of the receiving microcontroller receives data. MAX 232 can be used as dual transmitter and receiver.

- ✓ USART module of Pic16f73 (1) transmits the rear end weight to Pic16f73 (2).
- ✓ USART module of Pic16f73 (2) receives the data from Pic16f73 (1) and the microcontroller processes the data to find the total load on the vehicle.
- ✓ USART module of Pic16f73 (2) transmits this total weight to Pic16f73 (3)

7. MAX 232

RS 232 DRIVERS/RECEIVERS

General Description:

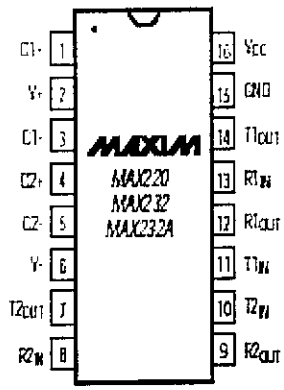
MAX 231 belongs to the maxim family in which the line drivers/receivers are intended for all RS 232 and V.28/V.24 communications interface and in particular for those applications where +/- 12 volts is not available. Since nearly all RS 232 applications need both line drivers and receivers, the family includes both receivers and drivers in one package. Both receivers and line drivers meet all EIA RS 232 and CCIT V.28 specifications. The MAX 232 consists of three sections, the transmitters, the receivers and the charge pump DC-DC voltage converters.

Features:

- Operates from single 5 volts supply
- Meets all RS 232C and V.28 specifications
- Multiple drivers and receivers
- On board DC-DC converter
- +/- 9 volts output swing with 5 volt supply

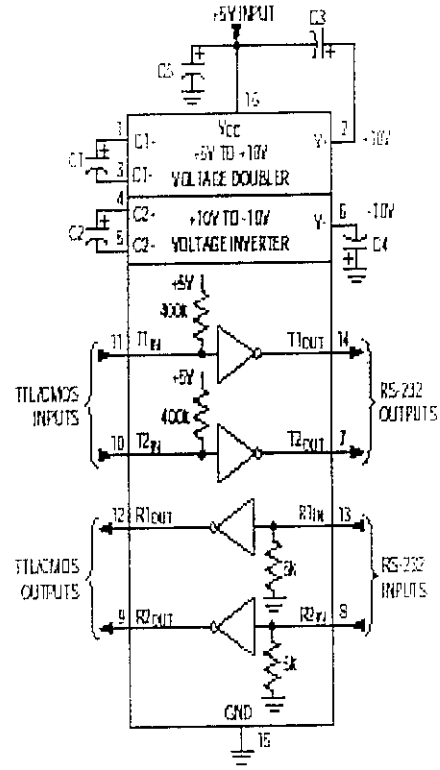
- Low power shut down < 1 microamps
- 3 state TTL/CMOS receiver output
- +/- 30 volts receiver input levels

TOP VIEW



DIP/SO

CAPACITANCE (µF)					
DEVICE	C1	C2	C3	C4	C5
MAX220	4.7	4.7	10	10	4.7
MAX232	1.0	1.0	1.0	1.0	1.0
MAX232A	0.1	0.1	0.1	0.1	0.1



DUAL CHARGE PUMP VOLTAGE CONVERTER:

The RS 232 drivers/receivers have on board charge pump voltage converters, which converts the +/- 5 volts, Input power to the +/- -10 volts needed to generate the RS 232 output levels. Two charge pump voltage converters perform this +/- 5 volts to +/- 10 volts conversion. The first users capacitors C1 to double the +5 volts to +10 volts, storing the +10 volts on the V output filter capacitor C3.The second charge pump voltage converter uses capacitor C2 to invert the +10 volts to –10 volts, storing the –10 volts on the V output filter capacitor C4.A small amount of power may be drawn from the +10 volts and –10 volts output to power external circuitry.

DRIVER (TRANSMITTER) SECTION :

The transmitters or the line drivers are inverting level translators, which convert the CMOS/TTL input levels to RS 232 or V.28 voltage levels. With +5 volt Vcc, the typical output voltage swing is +/-9 volts when loaded with a nominal 5 Kilo ohms input resistance of an RS 232 receiver. The output swing is guaranteed to meet the RS 232/V.28 specifications of +/-5 volts minimum output swing under the worst case conditions of all transmitters during the 3 Kilo ohms minimum allowable

load impedence Vcc=4.5 volts and maximum operating ambient temperature.

The input thresholds are both CMOS/TTL compatible, with a logic threshold of about 25% of Vcc. The inputs of unused driver section can be left unconnected, an internal 400 Kilo ohms input pull-up resistor to Vcc will pull the inputs high, forcing the unused transmitter outputs low. The input pull-up resistors source about 12 microamps and the driver inputs should be driven high or open circuited to minimize power supply current in the slow down mode.

When in the low power shut down mode, the driver outputs are turned off and their leakage current is less than 1 microamp with driver output pulled to ground. The driver output leakage remains less than 1 microamps even if the transmitter output is back driven between 0 volts and Vcc-+6 volts. Below -.5 volts the transmitter is diode clamped to ground with 1 Kilo ohm series impedance. The transmitter is also zener clamped to approximately Vcc +6 volts, with a series impedence of 1 Kilo ohm. As required by RS 232 and V.28 the slew rate is limited to less than 30 volts/microseconds. This limits the maximum usable baud rate to 19200 bauds.

RECEIVER SECTION:

All but the MAX 230 and MAX 234 contain RS 232/V.28receivers.These receivers convert the +5volts to +15volts RS 232 signals to 5 volts TTL/CMOS outputs.

Since the RS232 C /V.28 specifications define a voltage level greater than +3 volts as a zero, the receiver are inverting . These receivers are able to respond to both RS232C/V.28levels and TTL level inputs. The receivers are protected against input over voltage upto +30 volts.

The lower threshold has a guaranteed value of .8 volts. This value is important in the sense that the receiver will have a logic one output if the receiver is not being driven. This is because the equipment containing the line driver is turned off or disconnected if the connecting cable has an open circuit or short circuit. In the other words the receiver implements type1 interpretation of fault conditions. While or even a -3 volts receiver threshold would not give proper indication on the control lines such as DTR and DSR. The receiver on the other hand has a full .8 volts noise margin for detecting the power down or the cable connected states.

The receiver has a hysteresis of approximately of .5 volts with a minimum guaranteed hysteresis 200mv.This aids is obtaining clean output

transitions even with slow rise and fall line input signals with moderate amount of noise and ringing. The propagation delays of the receivers are 350ns for negative going input signals and 650ns for positive going input signals.

Purpose:

The signal from each load cell is in the order of few millivolts. So it has to be amplified and processed with a microcontroller at that point. The processed data is sent to the microcontroller that drives the LCD at the Dash Board through a RS 232 cable. For TTL to RS 232 level conversion and RS 232 to TTL level conversion MAX 232 is used.

CHAPTER 8

POWER SUPPLY

8. POWER SUPPLY

For any hardware circuit to work power is needed. The power supply construction should be simple and satisfy the circuit requirement.

The power supply circuit consists of:

- A dc voltage of 12-17V from the battery
- A regulator which regulates the high voltage to a constant 5V

Battery voltage:

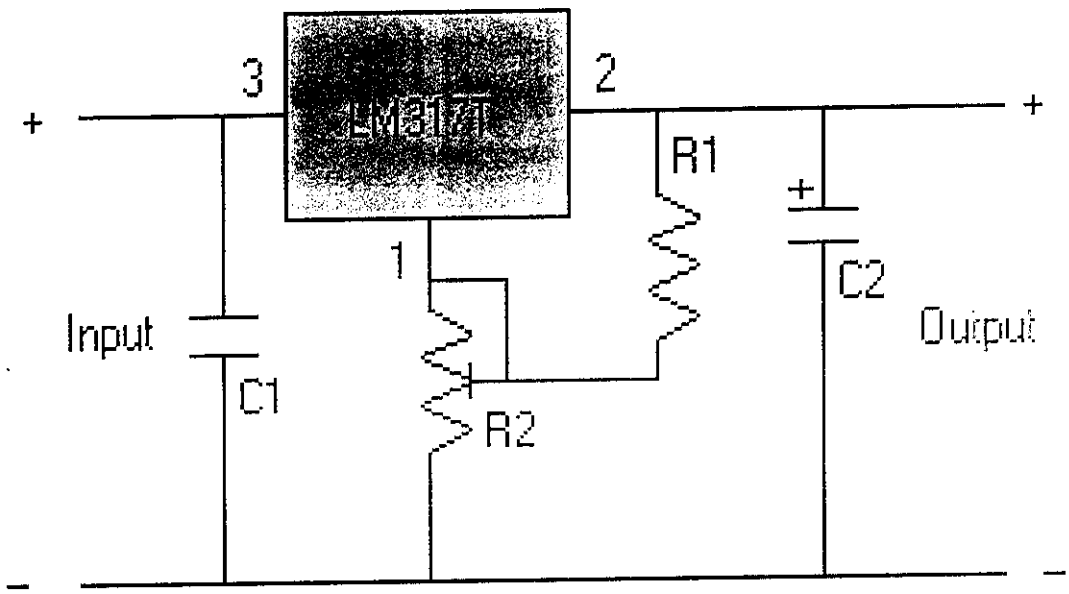
The dc supply from the battery is about 12-17V. Since the microcontroller requires only 5V for its operation, the voltage is regulated to 5V.

Regulator:

The function of a voltage regulator is to provide a stable DC voltage independent of the load current, temperature and ac voltage variations. It is in this stage the battery voltage is reduced to a stable DC voltage of 5V.

LM317:

The voltage regulator used in our power supply is the adjustable voltage regulator LM317. This is used to provide 5V to the Microcontroller, serial communication line driver (MAX232), and the Liquid Crystal Display.



Components Used:

Capacitors	C1	0.01 microfarad	
	C2	1 microfarad	
Resistors		R1	240 ohm
		R2	720 ohm

For the LM317:

- R2 = (192 x Vout) - 240, where R2 in ohms, Vout is in volts and must be at between 1.2 V and 35 V.
- Vin should be at least 2.5V greater than Vout. Select a wall adapter with a voltage at least 2.5 V greater than your regulated output at full load
- Maximum output current is 1 A. Use proper heat sink for LM317 if it has to dissipate more than 1W.
- The tab of the LM317 is connected to the center pin.

LM317 is an adjustable 3-terminal positive voltage regulator capable of supplying in excess of 1.5V to 37V output range. They are exceptionally easy to use and require only two external resistors to set the output voltage. Further both line and load regulation are better than standard fixed voltage regulators. In addition to higher performance than fixed voltage regulators, it offers full overload protection available in the IC. Included on the chip are current limit, thermal overload protection and safe area protection. All overload protection circuit remains fully functional even if the adjustable terminal is disconnected.

Features:

- Adjustable output down to 1.2V
- Guaranteed 1% output voltage tolerance
- Guaranteed 1.5A output current
- Line regulation typically 0.01%/V
- Load regulation typically 0.3%
- Current limit constant with temperature
- 100% electrical burn-in
- Eliminates the need to stock many voltages
- Standard 3-lead transistor package
- 80 dB ripple rejection
- Output is short-circuit protected

Normally, no capacitors are needed unless the device is situated far from the input filter capacitors in which case, an input bypass is needed.

An optional output capacitor can be added to improve transient response. The adjustable terminal can be bypassed to achieve very high ripple rejection ratios, which are difficult to achieve with standard three terminal regulators.

Besides replacing fixed regulator, it is useful in a wide variety of other applications. Since the regulator is floating and sees only the input to output

differential voltage, supplies of several hundred volts can be regulated as long as the maximum input to output differential is not exceeded. Also, it makes an especially simple adjustable switching regulator, programmable output regulator, or by connecting a fixed resistor between the adjustment pin and output.

Some Notes:

- Lm117 can be used as a precision current regulator.
- Supplies with electronic shutdown can be achieved by clamping the adjustment terminal to ground, which programs the output to 1.2V where most loads draw little current.
- For applications requiring greater output current LM150 series (3A) and LM138 series (5A) can be used.
- For the negative complement LM137 can be used.

9. LIQUID CRYSTAL DISPLAY:

Introduction:

Liquid crystal displays (LCDs) have materials, which combine the properties of both liquids and crystals. Rather than having a melting point, they have a temperature range within which the molecules are almost as mobile as they would be in a liquid, but are grouped together in an ordered form similar to a crystal.

An LCD consists of two glass panels, with the liquids crystal material sandwitched in between them. The inner surface of the glass plates are coated with transparent electrodes which define the character, symbols or patterns to be displayed polymeric layers are present in between the electrodes and the liquid crystal, which makes the liquid crystal molecules to maintain a defined orientation angle.

One each polarisers are pasted outside the two glass panels. These polarisers would rotate the light rays passing though them to a definite angle, in a particular direction. When the LCD is in the off state, light rays are rotated by the two polarisers and the liquid crystal, such that the light rays

come out of the LCD without any orientation and hence the LCD appears transparent.

When sufficient voltage is applied to the electrodes, the liquid crystal molecules would be aligned in a specific direction. The light rays passing through the LCD would be rotated by the polarisers, which would result in activating/highlighting the desired characters.

We use the LAMPEX LCD displays in the display unit of the project. LAMPEX has emerged as the single largest manufacturer and exporter in India for Liquid Crystal Displays (LCDs) and Liquid Crystal Modules (LCMs) of high contrast Twisted Neumatic(TN) and Super Twisted Neumatic (STN) with optional features of LED Backlighting and other configurations to exacting standards with outstanding quality, reliability and ensuring optimum performance at a very competitive prices. Alphanumeric Dot Matrix Liquid Crystal Display (LCD) modules consist of specialty Controllers with in-built Character ROM having standard ASCII Character set and Japanese Character set.

Power Supply:

The power supply should be of the +5V, with maximum allowable transients of 10mV. To achieve a better / suitable contrast for the display, the voltage at pin 3 should be adjusted properly.

A module should not be inserted or removed from a live circuit. The ground terminal of the power supply must be isolated properly so that no voltage is induced in it. The module should be isolated from the other circuits, so that stray voltages are not induced, which could cause a flickering display.

Hardware:

Develop a uniquely decoded "E' strobe pulse, active high, to accompany each module transaction. Address or control lines can be assigned to drive the RS and R/W inputs.

Mounting:

- Cover the display surface with a transparent protective plate, to protect the polarizer.
- Don't touch the display surface with bare hands or any hard materials. This will stain the display area and degrade the insulation between terminals.
- Do not use organic solvents to clean the display panel as these may adversely affect tape or with absorbent cotton and pertroleum benzene.

- The processing or even a light deformation of the claws of the metal frame will have effect on the connection of the output signal and cause an abnormal display.
- Do not damage or modify the pattern wiring, or drill attachment holes in the PCB. When assembling the module into another equipment , the space between the module and the fitting plate should have enough height, to avoid causing stress to the module surface.
- Make sure that there is enough space behind the module, to dissipate the heat generated by the ICs while functioning for longer durations.
- When cleaning by a vacuum cleaner, do not bring the sucking mouth near the module. Static electricity of the electrically powered driver or the vacuum cleaner may destroy the module.

Environmental Precautions:

Operate the LCD module under the relative condition of 40 C and 50% relative humidity. Lower temperature can cause retardation of the blinking speed of the display, while higher temperature makes the overall display discolor. When the temperature gets to be within the normal limits, the

display will be normal. Polarization degradation, bubble generation or polarizer peel-off may occur with high temperature and humidity.

TROUBLE SHOOTING:

Improper Character Display:

When the characters to be displayed are missing between, the data read / write is too fast. A slower interfacing would rectify this problem.

When uncertainty is there in the start of the first characters other than the specified ones are rewritten, check the initialization and the software routine.

In a multi-line display, if the display of characters in the subsequent lines doesn't take place properly, check the DD RAM addresses set for the corresponding display lines.

When it is unable to display data, even though it is present in the DD RAM, either the display on/off flag is in the off stage or the display shift function is not set properly. When the display shift is done simultaneous with the data write operation, the data may not be visible on the display.

If a character not found in the font table is displayed or a character is missing, the CG ROM is faulty and the controller IC has to be changed.

Functional Description of the Controller IC :

The interfacing of the Microcontroller can be done only by having knowledge of the different Registers of the Lampex LCD controller.

The controller IC has two 8 bit registers, an instruction register (IR) and a data Register (DR). The IR stores the instruction codes and address information for display data RAM (DD RAM) and character generator RAM (CG RAM). The IR can be written, but not read by the microcontroller.

BUSY FLAG:

When the busy flag is 1, the controller is in the internal operation mode, and the next instruction will not be accepted. When RS=0 and R/W=1, the busy flag is output to DB7. The next instruction must be written after ensuring that the busy flag is 0.

DISPLAY DATA RAM (DD RAM):

The characters to be displayed are written into the display data RAM (DD RAM), in the form of 8 bit character codes present in the character font table.

CHARACTER GENERATOR RAM (CG RAM):

In the character generator RAM, the user can rewrite character patterns by program. For 5*7 dots, seven character patterns can be written.

Interfacing the Microcontroller to Lampex LCD Module:

The Lampex LCD module is interfaced with the PIC microcontroller through 4-bit mode. In our interfacing procedure, a proper delay is given in passing the parameters to the LCD and the procedure of checking the Busy flag is not used. Apart from the data pins used in the interface, the three most important pins used in the LCD are:

a) R/W

b) RS

c) EN

R/W (Read/Write):

The R/W pin is the 5th pin the Lampex LCD. Whenever we have to pass the data to LCD this pin is to be enabled. In case of writing the R/W=0 and in case we read the BUSY flag R/W=1

RS (Register Select):

The RS is the 4th pin of the LCD. Whenever RS is asserted low, then the instruction Register is selected. When RS is asserted high, then the data Register is selected.

EN (Enable):

The EN is the 6th pin of the LCD. Only if this pin is asserted high, the data or command is passed from the microcontroller to the LCD and after passing the required information it is asserted low.

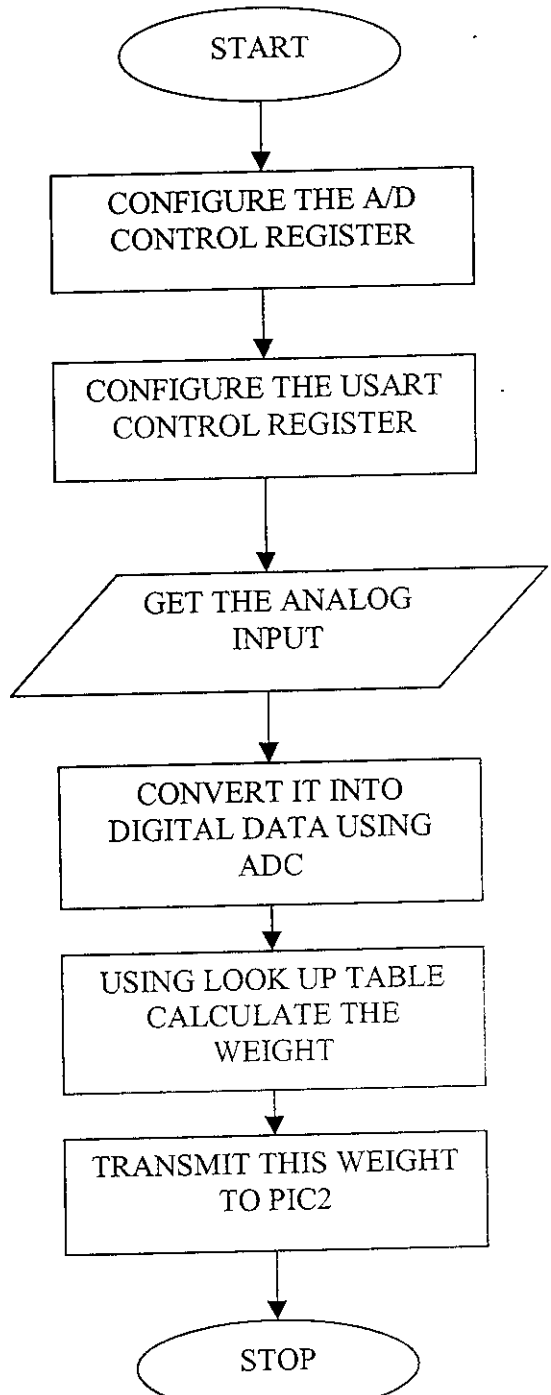
Connections:

1. Port A (RA0 – RA3) of the 16F73 (pins 2 – 5) act as output port. This Port A is connected with the data pins (DB4 – DB7) of the LCD module (pins 11-14).
2. The 1st pin of the LCD module is grounded.
3. The 2nd pin of the LCD module is connected to +5V power supply.
4. The 3rd pin of the LCD module is connected to be variable pin of the potentiometer (20k ohm preset) for contrast control.
5. The 2nd pin of the portC (RC2) is connected to the 5th pin of the LCD module which is for Register select (RS).
6. The 5th pin of the portA (RA5) is connected to the 4th pin of the LCD module which is for Read / Write (R/W).
7. The 0th pin of the portC (RC0) is connected to the 6th pin of the LCD module which is for Enable (EN).
8. The 15th pin is given +5V and 16th pin of the LCD module is grounded and it provides the backlit display.

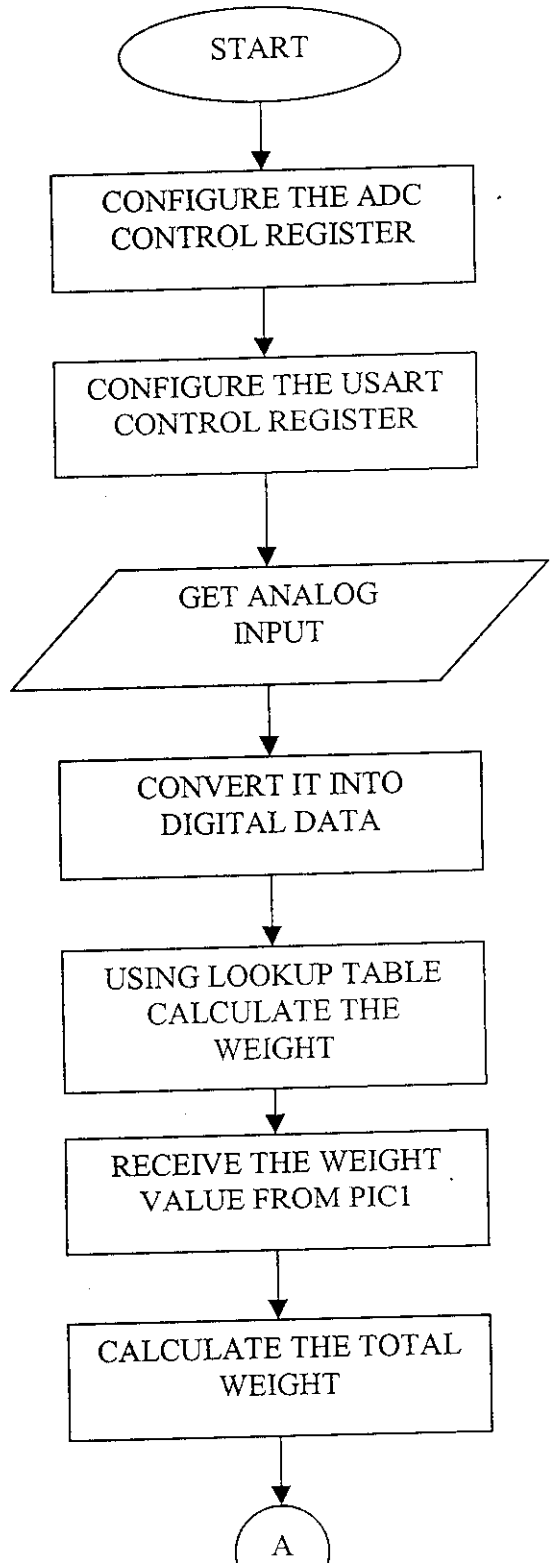
10. SOFTWARE DESCRIPTION:

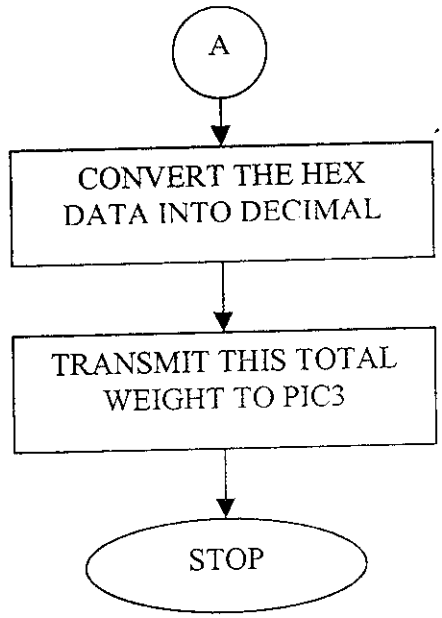
10.1 FLOWCHART:

REAR END WEIGHT TRANSMISSION:

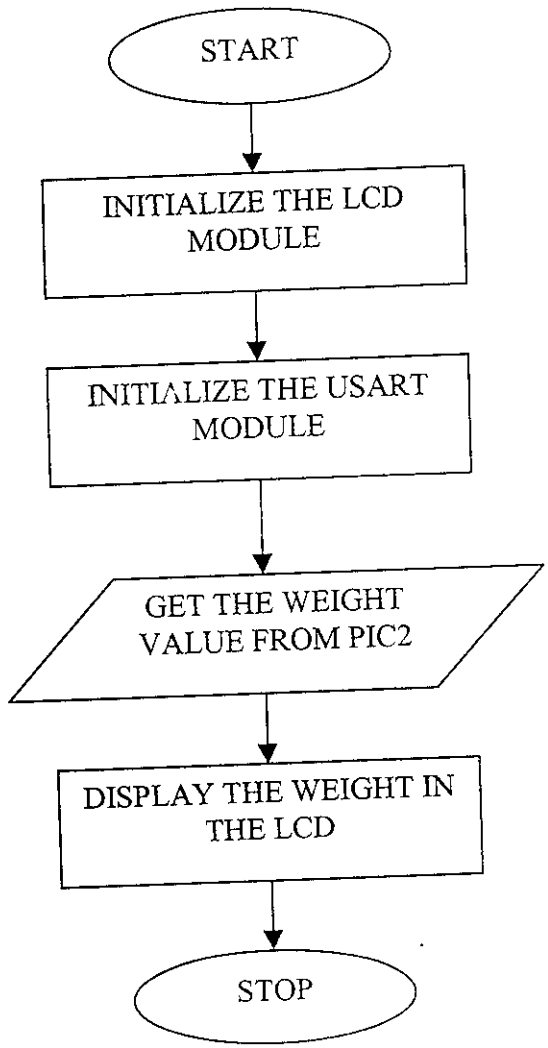


FRONT END WEIGHT TRANSMISSION

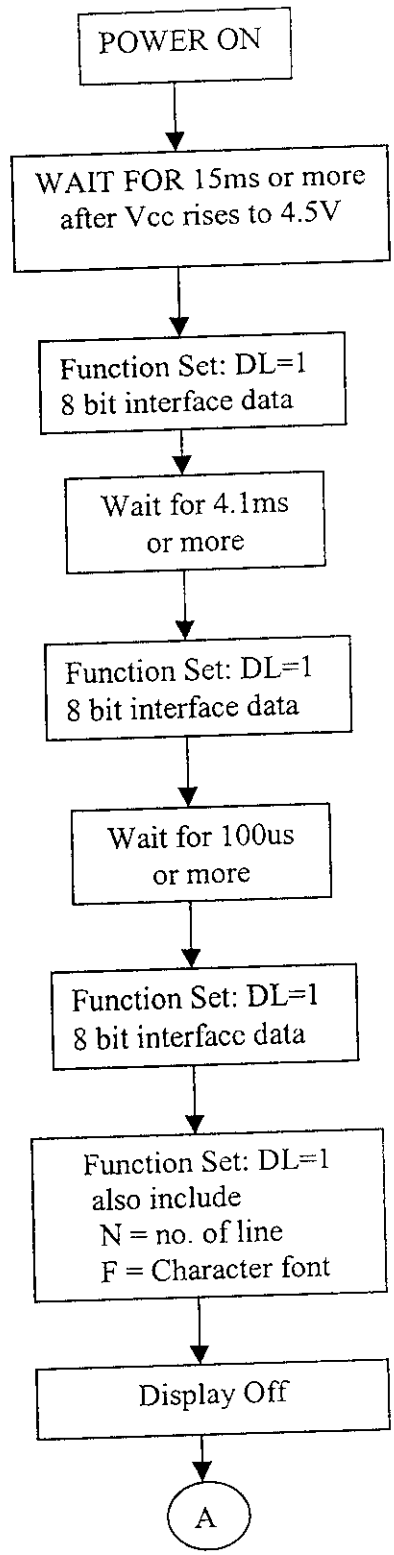


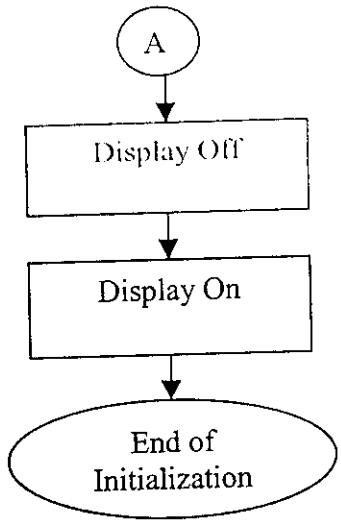

A
CONVERT THE HEX DATA INTO DECIMAL
TRANSMIT THIS TOTAL WEIGHT TO PIC3
STOP

WEIGHT DISPLAY ON LCD

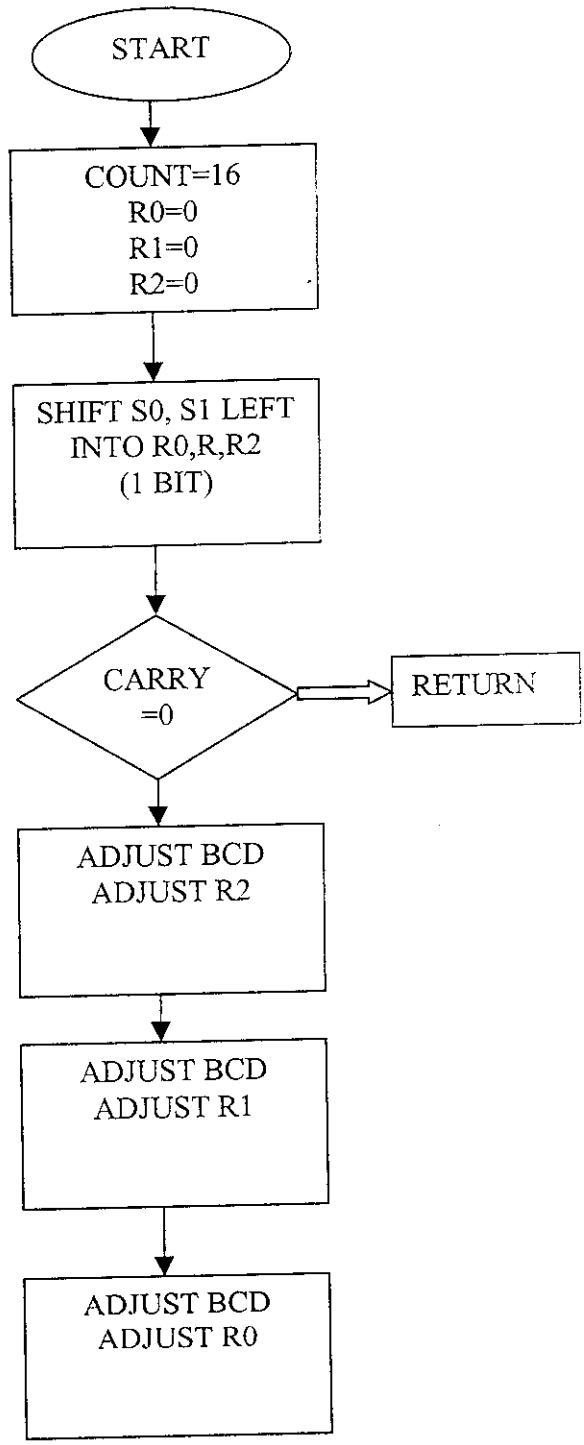


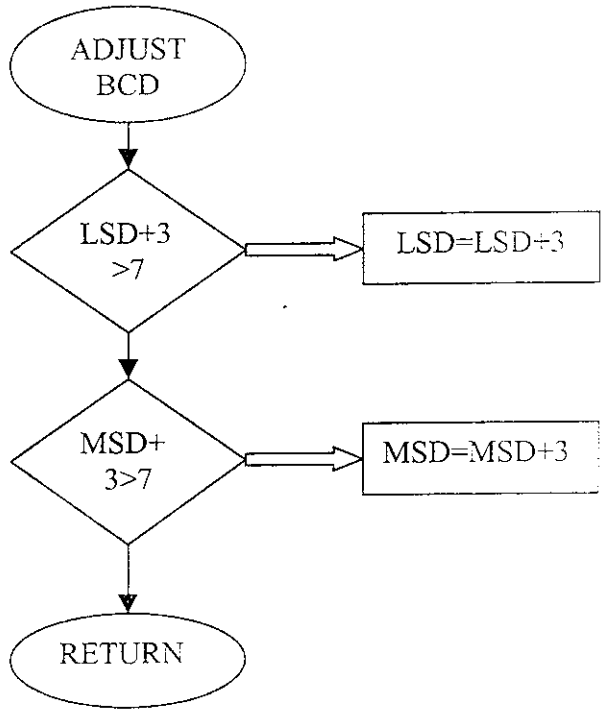
LCD DRIVING


POWER ON
WAIT FOR 15ms or more after Vcc rises to 4.5V
Function Set: DL=1 8 bit interface data
Wait for 4.1ms or more
Function Set: DL=1 8 bit interface data
Wait for 100us or more
Function Set: DL=1 8 bit interface data
Function Set: DL=1 also include N = no. of line F = Character font
Display Off
A


A
Display Off
Display On
End of
Initialization

HEXADECIMAL TO DECIMAL




ADJUST
BCD
LSD+3
>7
LSD=LSD+3
MSD+
3>7
MSD=MSD+3
RETURN

10.2 SOFTWARE CODING

For Pic16F73 (1):

```
      LIST P=P16F73
      INCLUDE "P16F73.INC"

;*****************************************************
;*******PROGRAM FOR TRANSMISSION OF REAR END LOAD
;*****************************************************

#DEFINE     BANK0       BCF STATUS,RP0
#DEFINE     BANK1       BSF STATUS,RP0

      CBLOCK      0X20

C1
C2
C3
W_TEMP
STATUS_TEMP1
Temp
COUNT
WEIGHT
RESULT1
RESULT2
COUN
COUNT1
COUNT2
TEMP1
TEMP2
TEMP3
TEMP4

      ENDC


      ORG   0X00
      CALL INIT_PORT
      GOTO ONE


;*****************************************************
;INTERRUPT SERVICE ROUTINE
;*****************************************************

      ORG   0X04
      MOVWF W_TEMP                  ; save off current W register
                                      contents
      MOVF  STATUS,W                ; move status register into W
                                      register
```

```
      MOVWF STATUS_TEMP1              ; save off contents of STATUS
                                        register

      CALL  ATOD1
      BANK0                           ; ensure file register bank set to 0
      MOVF    STATUS_TEMP1,W          ; retrieve copy of STATUS register
      MOVWF       STATUS              ; restore pre-isr STATUS register
                                        contents

      SWAPF W_TEMP,F
      SWAPF W_TEMP,W                  ; restore pre-isr W register
                                        contents
      RETFIE                          ; return from interrupt

;**************END OF INTERRUPT ROUTINE*********************


;************ MAIN PROGRAM *********************************

INIT_PORT
      BANK1
      BSF   TRISA,0
      BSF   TRISA,1
      CLRF  TRISB
      CLRF  TRISC
      CLRF  ADCON1
      CLRF  PIE1



DEL   MOVLW       D'1'          ;5MS DELAY
      MOVWF       C3
      MOVLW       0X90          ;5MS DELAY
      MOVWF       C2
      MOVLW       0XFF
      MOVWF       C1
      DECFSZ      C1,1
      GOTO  $-1
      DECFSZ      C2,1
      GOTO  $-5
      DECFSZ      C3,1
      GOTO  $-9
      RETURN



ONE   CALL  MAIN


LOOP1

ATOD1 BANK1
      CLRF  ADCON1
      BANK0
      MOVLW B'10000001'
      MOVWF ADCON0
```

```
      NOP
      NOP

      BSF   ADCON0,2
      BTFSS       PIR1,ADIF
      GOTO  $-1
      BCF   PIR1,ADIF

      MOVF  ADRES,0
      MOVWF COUNT
;INITIALISATION
      MOVLW 0x32
      MOVWF WEIGHT
      MOVLW 0x00
      MOVWF RESULT1
      MOVWF RESULT2
      BCF   STATUS,Z
      BCF   STATUS,C

;WEIGHT ROUTINE
;CHECKING FOR 0 0A LEVELS
      MOVF  COUNT,0
      SUBLW 0x0A
      BTFSC STATUS,C
      GOTO  Lo1
      MOVLW       0x0A
      SUBWF COUNT,1
      MOVLW 0x64
      MOVWF RESULT1


;MULTIPLICATION


J1    MOVF  RESULT1,0
      ADDWF WEIGHT,0
      MOVWF RESULT1
      BTFSS STATUS,C
      GOTO  LOP1
      MOVLW 0x01
      BCF   STATUS,C
      ADDWF RESULT2,1
LOP1  DECFSZ      COUNT,1
      GOTO  J1
      GOTO  L2
Lo1   MOVLW 0x64
      MOVWF RESULT1
L2    NOP
      CALL  MAIN
      GOTO  LOOP1

MAIN

;USART
;INITIALISATION
      BANKSEL TXSTA
```

```
        MOVWF TXSTA
        MOVLW 0x0C
        MOVWF SPBRG ;9600 BAUD RATE



;TRANSMIT
        BANKSEL     PIR1
U1      BTFSS PIR1,TXIF
        GOTO  U2
        MOVF  RESULT1,0
        MOVWF TXREG
        CALL DEL
U2      BTFSS PIR1,TXIF
        GOTO  U2
        MOVF  RESULT2,0
        MOVWF TXREG
        CALL DEL
        RETURN
        END
```

For Pic16F73 (2):

```
      LIST P=P16F73
      INCLUDE "P16F73.INC"

;*****************************************************
;*******PROGRAM FOR TRANSMISSION OF TOTAL LOAD
;*****************************************************

#DEFINE     BANK0       BCF STATUS,RP0
#DEFINE     BANK1       BSF STATUS,RP0


      CBLOCK      0X20

C1
C2
C3
W_TEMP
STATUS_TEMP1
Temp
COUNT
WEIGHT
RESULT1
RESULT2
COUN
COUNT1
COUNT2
TEMP1
TEMP2
TEMP3
TEMP4
REGI1
REGI2
RES1
RES2

      ENDC


      ORG   0X00
      CALL  INIT_PORT
      GOTO ONE

;*****************************************************
;INTERRUPT SERVICE ROUTINE
;*****************************************************


      ORG   0X04
      MOVWF W_TEMP                    ; save off current W register
                                        contents
      MOVF  STATUS,W                  ; move status register into W
                                        register
```

```
     MOVWF STATUS_TEMP1              ; save off contents of STATUS
                                       register

     CALL  ATOD1
     CALL  USAR                      ; ensure file register bank set to 0
     BANK0                           ; retrieve copy of STATUS register
     MOVF  STATUS_TEMP1              ; restore pre-isr STATUS register
     MOVWF STATUS                      contents

     SWAPF W_TEMP,F
     SWAPF W_TEMP,W                  ; restore pre-isr W register
                                       contents
     RETFIE                          ; return from interrupt

;***************END OF INTERRUPT ROUTINE*********************


;************* MAIN PROGRAM ********************************

INIT_PORT
      BANK1
      BSF   TRISA,0
      CLRF  TRISB
      CLRF  TRISC
      CLRF  ADCON1
      CLRF  PIE1



DEL   MOVLW       D'1'          ;5MS DELAY
      MOVWF       C3
      MOVLW       0X90          ;5MS DELAY
      MOVWF       C2
      MOVLW       0XFF
      MOVWF       C1
      DECFSZ      C1,1
      GOTO  $-1
      DECFSZ      C2,1
      GOTO  $-5
      DECFSZ      C3,1
      GOTO  $-9
      RETURN


ONE   CALL  MAIN


LOOP1


ATOD1 BANK1
      CLRF  ADCON1
      BANK0
      MOVLW B'10001001'
      MOVWF ADCON0
```

```
      NOP
      NOP

      BSF   ADCON0,2
      BTFSS PIR1,ADIF
      GOTO  $-1
      BCF   PIR1,ADIF

      MOVF  ADRES,0
      MOVWF COUNT
;INITIALISATION
      MOVLW 0x32
      MOVWF WEIGHT
      MOVLW 0x00
      MOVWF RESULT1
      MOVWF RESULT2
      BCF   STATUS,Z
      BCF   STATUS,C


;CHECKING FOR 0-0A LEVELS
      MOVF  COUNT,0
      SUBLW 0x0A
      BTFSC STATUS,C
      GOTO  Lo1
      MOVLW       0x0A
      SUBWF COUNT,1
      MOVLW 0x64
      MOVWF RESULT1


;MULTIPLICATION


J1    MOVF  RESULT1,0
      ADDWF WEIGHT,0
      MOVWF RESULT1
      BTFSS STATUS,C
      GOTO  LOP1
      MOVLW 0x01
      BCF   STATUS,C
      ADDWF RESULT2,1
LOP1  DECFSZ COUNT,1
      GOTO  J1
      GOTO  L2
Lo1   MOVLW 0x64
      MOVWF RESULT1
L2    NOP

USAR
;USART
;INITIALISATION
      BANKSEL TXSTA
      MOVLW B'00100000'
      MOVWF TXSTA
      MOVLW 0x0C
```

```
      MOVWF SPBRG ;9600 BAUD RATE
      BANKSEL     RCSTA
      MOVLW B'10010000'
      MOVWF RCSTA

;RECEIVE

      BANKSEL     PIR1
UR1   BTFSS PIR1,RCIF
      GOTO  UR1
      MOVF  RCREG,0
      BANKSEL     REGI1
      MOVWF REGI1
UR2   BTFSS PIR1,RCIF
      GOTO  UR2
      MOVF  RCREG,0
      BANKSEL     REGI2
      MOVWF REGI2
;TOTAL WEIGHT ROUTINE
      MOVF  RESULT1,0
      ADDWF REGI1,0
      MOVWF RES1
      BTFSS STATUS,C
      GOTO  W1
      MOVLW 0x01
      ADDWF RESULT2,0
      ADDWF REGI2,0
      MOVWF RES2
      GOTO  W2
W1    MOVF  RESULT2,0
      ADDWF REGI2,0
      MOVWF RES2
W2    NOP

;CONVERSION OF HEXADECIMAL TO DECIMAL
      CLRF  0x53
      CLRF  0x54
      CLRF  0x55
      BCF   STATUS,C
      MOVLW 0x10
      MOVWF COUN
      MOVLW 0x51
      MOVWF FSR
      MOVF  RES1,0
      MOVWF INDF
      INCF  FSR,1
      MOVF  RES2,0
      MOVWF INDF
L1    MOVLW 0x05
      MOVWF COUNT1
      MOVLW 0x03
      MOVWF COUNT2
      MOVLW 0x51
      MOVWF FSR
J2    RLF   INDF,1
      INCF  FSR,1
```

```
        GOTO  J2
        DECFSZ      COUN,0
        GOTO  HH1
        GOTO  HA2
HH1     MOVLW 0x53
        MOVWF FSR
        MOVF  INDF,0
        BTFSS STATUS,C
        GOTO  H1
        GOTO  H2
H1      ANDLW 0x0F
        MOVWF TEMP3
        ADDLW 0x03
        MOVWF TEMP1
        BTFSS TEMP1,3
        GOTO  HAR1
        MOVWF TEMP4
        GOTO  HAR2
HAR1    MOVF  TEMP3,0
        MOVWF TEMP4
HAR2    MOVF  INDF,0
        ANDLW 0xF0
        MOVWF TEMP3
        ADDLW 0x30
        MOVWF TEMP1
        BTFSS TEMP1,7
        GOTO  HAR3
        GOTO  HAR4
HAR3    MOVF  TEMP3,0
HAR4    ADDWF TEMP4,0
        MOVWF INDF
        INCF  FSR,1
        MOVF  INDF,0
        DECFSZ COUNT2,1
        GOTO  H1
H2      DECFSZ COUN,1
        GOTO  L1
        GOTO  HA2
HA2     NOP
        CALL  MAIN
        GOTO  LOOP1

MAIN

;USART
;INITIALISATION
        BANKSEL TXSTA
        MOVLW B'00100000'
        MOVWF TXSTA
        MOVLW 0x0C
        MOVWF SPBRG ;9600 BAUD RATE


;TRANSMIT
        BANKSEL     PIR1
U1      BTFSS PIR1,TXIF
        GOTO  U2
```

```
        MOVF   RES1,0
        MOVWF  TXREG
        CALL   DEL
U2      BTFSS  PIR1,TXIF
        GOTO   U2
        MOVF   RES2,0
        MOVWF  TXREG
        CALL   DEL
        RETURN
        END
```

For Pic16F73 (3):

```
      LIST P=P16F73
      INCLUDE "P16F73.INC"



;REGISTERS
DATACONT      EQU  0x30
DELCONT1      EQU  0x31
DELCONT2      EQU  0x32
TEMP1         EQU  0x33
REGI1         EQU  0x34
REGI2         EQU  0x35


      ORG   0X00
      CALL  USAR



LOOP1

USAR
;USART
;INITIALISATION
      BANKSEL     TXSTA
      MOVLW       B'00100000'
      MOVWF       TXSTA
      MOVLW       0x0C
      MOVWF       SPBRG ;9600 BAUD RATE
      BANKSEL     RCSTA
      MOVLW       B'10010000'
      MOVWF       RCSTA

;RECEIVE

      BANKSEL     PIR1
UR1   BTFSS       PIR1,RCIF
      GOTO        UR1
      MOVF        RCREG,0
      BANKSEL     REGI1
      MOVWF       REGI1
UR2   BTFSS       PIR1,RCIF
      GOTO        UR2
      MOVF        RCREG,0
      BANKSEL     REGI2
      MOVWF       REGI2
      CALL        MAIN
      GOTO        LOOP1
```

```
MAIN

;DATA
      MOVF        REGI2,W
      ADDLW       0x30
      MOVWF       0x40
      MOVF        REGI1,W
      ADDLW       0x30
      MOVWF       0x41
      MOVLW       'T'
      MOVWF       0x42
      MOVLW       'O'
      MOVWF       0x43
      MOVLW       'N'
      MOVWF       0x44

;Power_up Delay
      CALL        POWDEL

;INITIALISE THE PORTS
;CONFIGURING BOTH PORTS AS OUTPUTS
      MOVLW       B'00000000'
      MOVWF       TRISA
      MOVWF       TRISC
;SETTING THE PORTS TO INITIAL VALUES
      BCF         STATUS,RP0
      MOVLW       0x00
      MOVWF       PORTA
      MOVWF       PORTC

      BCF         PORTC,2
      BCF         PORTA,5
      BCF         PORTC,0
;FUNCTION SET
      BCF         STATUS,RP0
      BCF         PORTA,0
      BCF         PORTA,1
      MOVLW       B'00110100'
      MOVWF  PORTB
      BSF         PORTA,2
      CALL        DELAY
      BCF          PORTA,2
;FUNCTION SET
      BCF         STATUS,RP0
      MOVLW       B'00101000'
      MOVWF       TEMP1
      SWAPF       TEMP1,W
      ANDLW       0x0F
      MOVWF       PORTA
      BSF         PORTC,0
      BCF         PORTC,0
      MOVF        TEMP1,0
      ANDLW       0x0F
      MOVWF       PORTA
      BSF         PORTC,0
      CALL        DELAY
```

```
;FUNCTION SET
      BCF         STATUS,RP0
      MOVLW       B'00101000'
      MOVWF       TEMP1
      SWAPF       TEMP1,W
      ANDLW       0x0F
      MOVWF       PORTA
      BSF         PORTC,0
      BCF         PORTC,0
      MOVF        TEMP1,0
      ANDLW       0x0F
      MOVWF       PORTA
      BSF         PORTC,0
      CALL        DELAY
      BCF         PORTC,0
;FUNCTION SET
      BCF         STATUS,RP0
      MOVLW       B'00101000'
      MOVWF       TEMP1
      SWAPF       TEMP1,W
      ANDLW       0x0F
      MOVWF       PORTA
      BSF         PORTC,0
      BCF         PORTC,0
      MOVF        TEMP1,0
      ANDLW       0x0F
      MOVWF       PORTA
      BSF         PORTC,0
      CALL        DELAY
      BCF         PORTC,0
;DISPLAY ON
      BCF         STATUS,RP0
      MOVLW       B'00001111'
      MOVWF       TEMP1
      SWAPF       TEMP1,W
      ANDLW       0x0F
      MOVWF       PORTA
      BSF         PORTC,0
      BCF         PORTC,0
      MOVF        TEMP1,0
      ANDLW       0x0F
      MOVWF       PORTA
      BSF         PORTC,0
      CALL        DELAY
      BCF         PORTC,0
;CURSOR SHIFT
      BCF         STATUS,RP0
      MOVLW       B'00010000'
      MOVWF       TEMP1
      SWAPF       TEMP1,W
      ANDLW       0x0F
      MOVWF       PORTA
      BSF         PORTC,0
      BCF         PORTC,0
      MOVF        TEMP1,0
      ANDLW       0x0F
      MOVWF       PORTA
```

```
      BSF         PORTC,0
      CALL        DELAY
      BCF         PORTC,0
;MOVE CURSOR
      BCF         STATUS,RP0
      MOVLW       B'00010100'
      MOVWF       TEMP1
      SWAPF       TEMP1,W
      ANDLW       0x0F
      MOVWF       PORTA
      BSF         PORTC,0
      BCF         PORTC,0
      MOVF        TEMP1,0
      ANDLW       0x0F
      MOVWF       PORTA
      BSF         PORTC,0
      CALL        DELAY
      BCF         PORTC,0

;DATA DISPLAY
      MOVLW       0x05
      MOVWF       DATACONT
      MOVLW       0x40
      MOVWF       FSR
LOOP1 BSF         PORTC,2
      BCF         PORTA,5
      MOVF        INDF,W
      MOVWF       TEMP1
      SWAPF       TEMP1,W
      ANDLW       0x0F
      MOVWF       PORTA
      BSF         PORTC,0
      BCF         PORTC,0
      MOVF        TEMP1,0
      ANDLW       0x0F
      MOVWF       PORTA
      BSF         PORTC,0
      CALL        DELAY
      BCF         PORTC,0
      INCF        FSR,F
      DECFSZ      DATACONT,F
      GOTO        LOOP1
      RETURN
Delays
;  Power-up Delay of 15.0102 ms
POWDEL MOVLW      0x27
       MOVWF      DELCONT1
LOOP3  MOVLW      0xFF
       MOVWF       DELCONT2
LOOP2  DECFSZ     DELCONT2,F
       GOTO       LOOP2
       DECFSZ     DELCONT1,F
       GOTO       LOOP2
         RETURN
;Common Delay of 1.1334 ms
DELAY  MOVLW      0x03
       MOVWF      DELCONT1
```

```
LOOP5   MOVLW       0xFF
        MOVWF       DELCONT2
LOOP4   DECFSZ       DELCONT2,F
          GOTO      LOOP4
          DECFSZ    DELCONT1,F
          GOTO      LOOP5
          RETURN


         END
```

CONCLUSION

11. CONCLUSION

The project 'PAYLOAD INDICATOR' is designed for use in all vehicles. The Payload Indicator is a low cost device suitable for Indian conditions. It serves as an easy means of indicating the load on the vehicle. It benefits the driver of the vehicle to keep track of the load on the vehicle and adjust himself to various traffic conditions to prevent accidents. The resolution of the displayed data can be varied by simple software routines. The Payload indicator is designed in such a way that facilities available at present can be expanded.

Future Improvements:

- An EPROM may be employed in the circuit to make this project a load indicator as well as recorder.
- Switches may be employed to select the range in which the weight should be displayed in LCD.

BIBLIOGRAPHY

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APPENDIX

PIC16F7X

FLASH Memory Programming Specification

This document includes the programming specifications for the following devices:

- PIC16F73
- PIC16F74
- PIC16F76
- PIC16F77

1.0 PROGRAMMING THE PIC16F7X

The PIC16F7X is programmed using a serial method. The Serial mode allows the PIC16F7X to be programmed while in the users' system, allowing for increased design flexibility. This programming specification applies to PIC16F7X devices in all packages.

1.1 Hardware Requirements

The PIC16F7X requires two programmable power supplies, one for VDD (2.0 V to 5.5 V) and the other for VPP of 12.75 V to 13.25 V. Both supplies should have a minimum resolution of 0.25 V.

1.2 Programming Mode

The Programming mode for the PIC16F7X allows programming of user program memory, special locations used for ID, and the configuration word.

Pin Diagram

PDIP, SOIC

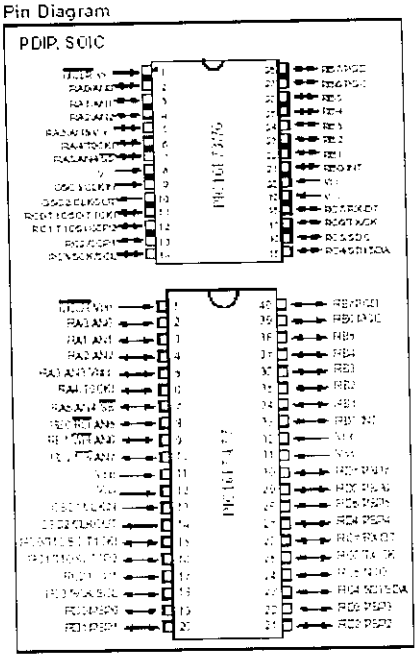


TABLE 1-1: PIN DESCRIPTIONS (DURING PROGRAMMING): PIC16F7X

Pin Name	During Programming		
	Function	Pin Type	Pin Description
RB6/PGC	CLOCK	I	Clock Input
RB7/PGD	DATA	I/O	Data Input/Output
MCLR/VPP	VTEST MODE	P	Program Mode Select
VDD	VDD	P	Power Supply
VSS	VSS	P	Ground

Legend: I = Input, O = Output, P = Power

2.0 PROGRAM MODE ENTRY

2.1 User Program Memory Map

The user memory space extends from 0x0000 to 0x1FFF (8 K), or 0x0000 to 0x0FFF (4 K). Table 2-1 shows the actual implementation of program memory in the PIC16F7X family. Configuration memory begins at 0x2000, and continues to 0x3FFF. The PC will increment from 0x0000 to 0x1FFF and wrap to 0x0000, 0x2000 to 0x3FFF and wrap around to 0x2000 (not to 0x0000).

Once in configuration memory, the highest bit of the PC stays a '1', thus always pointing to the configuration memory. The only way to point to program memory is to reset the part and reenter Program/Verify mode, as described in Section 2.3.

Configuration memory is selected when the PC points to any address in the range of 0x2000-0x201F; however, only locations 0x2000 through 0x2007 are implemented. Addressing locations beyond 0x201F will access program memory (see Figure 2-1).

TABLE 2-1: IMPLEMENTATION OF PROGRAM MEMORY IN THE PIC16F7X FAMILY

Device	Program Memory Size
PIC16F73	0x0000 – 0x0FFF (4K)
PIC16F74	0x0000 – 0x0FFF (4K)
PIC16F76	0x0000 – 0x1FFF (8K)
PIC16F77	0x0000 – 0x1FFF (8K)

2.2 ID Locations

A user may store identification information (ID) in four ID locations mapped to [0x2000:0x2003]. It is recommended that each ID location word is written as '11 1111 1000 bbbb' where 'bbbb' is ID information. The ID locations can be read after code protection is enabled.

To understand the program memory read mechanism after code protection is enabled, refer to Section 4.0. Table 4-1 shows specific calculations and behavior for each of the PIC16F7X devices.

5.0 PROGRAM/VERIFY MODE ELECTRICAL CHARACTERISTICS

5.1 AC/DC Characteristics

TABLE 5-1: TIMING REQUIREMENTS FOR PROGRAM/VERIFY MODE

Standard Operating Conditions (unless otherwise stated) Operating Temperature: +10°C ≤ TA ≤ +40°C Operating Voltage: 4.5 V ≤ VDD ≤ 5.5 V						
Characteristics	Sym	Min	Typ	Max	Units	Conditions/Comments
General						
VDD level for read and verification	VDD	2.0		5.5	V	
VDD level for programming and erasing	VDDP	4.75		5.25	V	
High voltage on MCLR for chip erase and program write operations	VPP	12.75		13.25	V	Note 1, 2
MCLR rise time (VSS to VPP) for Test mode entry	TVHHR			1.0	µs	
(RB6, RB7) input high level	VIH1	0.8 VDD			V	Schmitt Trigger input
(RB6, RB7) input low level	VIL1	0.2 VDD			V	Schmitt Trigger input
Serial Program/Verify						
Data in setup time before clock↓	T_{setl}	100			ns	
Data in hold time after clock↓	T_{hld1}	100			ns	
Data input not driven to next clock input (delay required between command/data or command/command)	T_{dly1}	1.0			µs	
Delay between clock↓ to clock↑ of next command or data	T_{dly2}	1.0			µs	
Clock↑ to data out valid (during read data)	T_{dly3}	200			ns	
Erase cycle time	T_{era}	30			ms	Note 3
Programming cycle time	T_{prog}	1	—	3[4]	ms	

Note 1: VPP should be current limited to about 100 mA.
2: VPP must remain above VDDP + 4.0 V to remain in Programming mode, while not actually erasing or programming.
3: The chip erase is self-timed.
4: T_{prog} is expected to be reduced to 1 mS max.

21.2 Control Registers

Register 21-1: ADCON0 Register

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/$\overline{\text{DONE}}$	Resv	ADON
bit 7							bit 0

bit 7:6 **ADCS1:ADCS0**: A/D Conversion Clock Select bits
00 = FOSC/2
01 = FOSC/8
10 = FOSC/32
11 = FRC (clock derived from the internal A/D RC oscillator)

bit 5:3 **CHS2:CHS0**: Analog Channel Select bits
000 = channel 0, (AN0)
001 = channel 1, (AN1)
010 = channel 2, (AN2)
011 = channel 3, (AN3)
100 = channel 4, (AN4)
101 = channel 5, (AN5)
110 = channel 6, (AN6)
111 = channel 7, (AN7)

Note: For devices that do not implement the full 8 A/D channels, the unimplemented selections are reserved. Do not select any unimplemented channels.

bit 2 **GO/$\overline{\text{DONE}}$**: A/D Conversion Status bit

When ADON = 1

1 = A/D conversion in progress
(Setting this bit starts the A/D conversion. This bit is automatically cleared by hardware when the A/D conversion is complete)

0 = A/D conversion not in progress

bit 1 **Reserved**: Always maintain this bit cleared.

bit 0 **ADON**: A/D On bit

1 = A/D converter module is operating
0 = A/D converter module is shutoff and consumes no operating current

Legend		
R = Readable bit	W = Writable bit	
U = Unimplemented bit, read as '0'		- n = Value at POR reset

Register 21-2: ADCON1 Register

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	PCFG2	PCFG1	PCFG0
bit 7							bit 0

bit 7:3 **Unimplemented:** Read as '0'

bit 2:0 **PCFG2:PCFG0:** A/D Port Configuration Control bits

PCFG2:PCFG0	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0
000	A	A	A	A	A	A	A	A
001	A	A	A	A	VREF	A	A	A
010	D	D	D	A	A	A	A	A
011	D	D	A	A	VREF	A	A	A
100	D	D	D	D	A	D	A	A
101	D	D	D	D	VREF	D	A	A
11x	D	D	D	D	D	D	D	D

A = Analog input D = Digital I/O

Note: When AN3 is selected as VREF, the A/D reference is the voltage on the AN3 pin. When AN3 is selected as an analog input (A), then the voltage reference for the A/D is the device VDD.

Legend	
R = Readable bit	W = Writable bit
U = Unimplemented bit, read as '0'	- n = Value at POR reset

Note 1: On any device reset, the Port pins multiplexed with analog functions (ANx) are forced to be an analog input.

21.4 A/D Acquisition Requirements

For the A/D converter to meet its specified accuracy, the charge holding capacitor (CHOLD) must be allowed to fully charge to the input channel voltage level. The analog input model is shown in Figure 21-3. The source impedance (*RS*) and the internal sampling switch (*RSS*) impedance directly affect the time required to charge the capacitor CHOLD. The sampling switch (*RSS*) impedance varies over the device voltage (VDD) (Figure 21-3). The maximum recommended impedance for analog sources is 10 kΩ. After the analog input channel is selected (changed), the acquisition must be done before the conversion can be started.

To calculate the minimum acquisition time, Equation 21-1 may be used. This equation assumes that 1/2 LSb error is used (512 steps for the A/D). The 1/2 LSb error is the maximum error allowed for the A/D to meet its specified resolution.

Equation 21-1: Acquisition Time

$$TACQ = \text{Amplifier Settling Time} + \text{Holding Capacitor Charging Time} + \text{Temperature Coefficient}$$
$$TACQ = TAMP + TC + TCOFF$$

Equation 21-2: A/D Minimum Charging Time

$$VHOLD = (VREF - (VREF/512)) \cdot (1 - e^{-Tc/(CHOLD(RIC + RSS + RS))})$$
or
$$Tc = -(51.2\ pF)(1\ k\Omega + RSS + RS)\ln(1/511)$$

Example 21-1 shows the calculation of the minimum required acquisition time TACQ. This calculation is based on the following system assumptions.

Rs	=	10 kΩ
Conversion Error	=	1/2 LSb
VDD	=	5V @ Rss = 7 kΩ (see graph in Figure 21-3)
Temperature	=	50°C (system max.)
VHOLD	=	0V @ time = 0

Example 21-1: Calculating the Minimum Required Acquisition Time

$$TACQ = TAMP + TC + TCOFF$$
$$TACQ = 5\ \mu s + Tc + [(Temp - 25\ °C)(0.05\ \mu s/°C)]$$
$$Tc = -CHOLD(RIC + RSS + RS)\ln(1/512)$$
$$-51.2\ pF(1\ k\Omega + 7\ k\Omega + 10\ k\Omega)\ln(0.0020)$$
$$-51.2\ pF(18\ k\Omega)\ln(0.0020)$$
$$-0.921\ \mu s(-6.2146)$$
$$5.724\ \mu s$$
$$TACQ = 5\ \mu s + 5.724\ \mu s + [(50\ °C - 25\ °C)(0.05\ \mu s/°C)]$$
$$10.724\ \mu s + 1.25\ \mu s$$
$$11.974\ \mu s$$

18.2 Control Registers

Register 18-1: TXSTA: Transmit Status and Control Register

R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R-1	R/W-0
CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D
bit 7							bit 0

bit 7 **CSRC**: Clock Source Select bit
Asynchronous mode
Don't care

Synchronous mode
1 = Master mode (Clock generated internally from BRG)
0 = Slave mode (Clock from external source)

bit 6 **TX9**: 9-bit Transmit Enable bit
1 = Selects 9-bit transmission
0 = Selects 8-bit transmission

bit 5 **TXEN**: Transmit Enable bit
1 = Transmit enabled
0 = Transmit disabled

Note: SREN/CREN overrides TXEN in SYNC mode.

bit 4 **SYNC**: USART Mode Select bit
1 = Synchronous mode
0 = Asynchronous mode

bit 3 **Unimplemented**: Read as '0'

bit 2 **BRGH**: High Baud Rate Select bit
Asynchronous mode
1 = High speed
0 = Low speed

Synchronous mode
Unused in this mode

bit 1 **TRMT**: Transmit Shift Register Status bit
1 = TSR empty
0 = TSR full

bit 0 **TX9D**: 9th bit of transmit data. Can be parity bit.

Legend		
R = Readable bit	W = Writable bit	
U = Unimplemented bit, read as '0'		- n = Value at POR reset

Register 18-2: RCSTA: Receive Status and Control Register

R/W-0	R/W-0	R/W-0	R/W-0	U-0	R-0	R-0	R-0
SPEN	RX9	SREN	CREN	—	FERR	OERR	RX9D
bit 7							bit 0

bit 7 **SPEN**: Serial Port Enable bit
1 = Serial port enabled (Configures RX/DT and TX/CK pins as serial port pins)
0 = Serial port disabled

bit 6 **RX9**: 9-bit Receive Enable bit
1 = Selects 9-bit reception
0 = Selects 8-bit reception

bit 5 **SREN**: Single Receive Enable bit
Asynchronous mode
Don't care

Synchronous mode - master
1 = Enables single receive
0 = Disables single receive
This bit is cleared after reception is complete.

Synchronous mode - slave
Unused in this mode

bit 4 **CREN**: Continuous Receive Enable bit
Asynchronous mode
1 = Enables continuous receive
0 = Disables continuous receive

Synchronous mode
1 = Enables continuous receive until enable bit CREN is cleared (CREN overrides SREN)
0 = Disables continuous receive

bit 3 **Unimplemented**: Read as '0'

bit 2 **FERR**: Framing Error bit
1 = Framing error (Can be updated by reading RCREG register and receive next valid byte)
0 = No framing error

bit 1 **OERR**: Overrun Error bit
1 = Overrun error (Can be cleared by clearing bit CREN)
0 = No overrun error

bit 0 **RX9D**: 9th bit of received data, can be parity bit.

Legend		
R = Readable bit	W = Writable bit	
U = Unimplemented bit, read as '0'		- n = Value at POR reset

Table 18-3: Baud Rates for Synchronous Mode

BAUD RATE (Kbps)	Fosc = 20 MHz			16 MHz			10 MHz			7.15909 MHz		
	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)
0.3	NA	-	-	NA	-	-	NA	-	-	NA	-	-
1.2	NA	-	-	NA	-	-	NA	-	-	NA	-	-
2.4	NA	-	-	NA	-	-	NA	-	-	NA	-	-
9.6	NA	-	-	NA	-	-	9.766	+1.73	255	9.622	+0.23	185
19.2	19.53	+1.73	255	19.23	+0.16	207	19.23	+0.16	129	19.24	+0.23	92
76.8	76.92	+0.16	64	76.92	+0.16	51	75.76	-1.36	32	77.82	+1.32	22
96	96.15	+0.16	51	95.24	0.79	41	96.15	+0.16	25	94.20	1.88	18
300	294.1	-1.96	16	307.69	+2.56	12	312.5	+4.17	7	298.3	0.57	5
500	500	0	9	500	0	7	500	0	4	NA		
HIGH	5000	-	0	4000	-	0	2500	-	0	1789.8		0
LOW	19.53	-	255	15.625	-	255	9.766	-	255	6.991	-	255

BAUD RATE (Kbps)	Fosc = 5.0688 MHz			4 MHz			3.579545 MHz			1 MHz			32.768 kHz		
	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)
0.3	NA	-	-	NA	-	-	NA	-	-	NA	-	-	0.303	+1.14	26
1.2	NA	-	-	NA	-	-	NA	-	-	1.202	+0.16	207	1.170	2.48	6
2.4	NA	-	-	NA	-	-	NA	-	-	2.404	+0.16	103	NA	-	-
9.6	9.6	0	131	9.615	+0.16	103	9.622	+0.23	92	9.615	+0.16	25	NA		
19.2	19.2	0	65	19.231	+0.16	51	19.04	0.83	46	19.23	+0.16	12	NA		
76.8	79.2	+3.13	15	76.923	+0.16	12	74.57	2.90	11	83.34	+8.51	2	NA		
96	97.48	+1.54	12	100	+4.17	9	99.43	+3.57	8	NA	-	-	NA		
300	316.8	+5.60	3	NA	-	-	298.3	0.57	2	NA	-	-	NA		
500	NA	-	-	NA	-	-	NA	-	-	NA	-	-	NA		
HIGH	1267	-	0	1000	-	0	894.9	-	0	250	-	0	8.192		0
LOW	4.950	-	255	3.906	-	255	3.496	-	255	0.9766	-	255	0.032	-	255

Table 18-4: Baud Rates for Asynchronous Mode (BRGH = 0)

BAUD RATE (Kbps)	Fosc = 20 MHz			16 MHz			10 MHz			7.15909 MHz		
	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)
0.3	NA	-	-	NA	-	-	NA	-	-	NA	-	-
1.2	1.221	+1.73	255	1.202	+0.16	207	1.202	+0.16	129	1.203	+0.23	92
2.4	2.404	+0.16	129	2.404	+0.16	103	2.404	+0.16	64	2.380	-0.83	46
9.6	9.469	-1.36	32	9.615	+0.16	25	9.766	+1.73	15	9.322	-2.90	11
19.2	19.53	+1.73	15	19.23	+0.16	12	19.53	+1.73	7	18.64	-2.90	5
76.8	78.13	+1.73	3	83.33	+8.51	2	78.13	+1.73	1	NA	-	-
96	104.2	+8.51	2	NA	-	-	NA	-	-	NA	-	-
300	312.5	+4.17	0	NA	-	-	NA			NA		-
500	NA	-	-	NA	-	-	NA	-	-	NA		
HIGH	312.5		0	250		0	156.3		0	111.9		0
LOW	1.221		255	0.977		255	0.6104		255	0.437		255

BAUD RATE (Kbps)	Fosc = 5.0688 MHz			4 MHz			3.579545 MHz			1 MHz			32.768 kHz		
	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)
0.3	0.31	+3.13	255	0.3005	-0.17	207	0.301	+0.23	185	0.300	+0.16	51	0.255	14.67	1
1.2	1.2	0	65	1.202	+1.67	51	1.190	-0.83	46	1.202	+0.16	12	NA		
2.4	2.4	0	32	2.404	+1.67	25	2.432	+1.32	22	2.232	-6.99	6	NA		
9.6	9.9	+3.13	7	NA	-	-	9.322	-2.90	5	NA			NA		
19.2	19.8	+3.13	3	NA		-	18.64	-2.90	2	NA			NA		
76.8	79.2	+3.13	0	NA			NA			NA			NA		
96	NA	-	-	NA	-	-	NA	-		NA			NA		
300	NA	-	-	NA	-	-	NA	-	-	NA			NA		
500	NA	-	-	NA	-	-	NA			NA			NA		
HIGH	79.2	-	0	62.500	-	0	55.93	-	0	15.63		0	2.512		0
LOW	0.3094	-	255	0.245	-	255	0.2186	-	255	0.0610		255	0.0020	-	255

Table 18-5: Baud Rates for Asynchronous Mode (BRGH = 1)

BAUD RATE (Kbps)	Fosc = 20 MHz			16 MHz			10 MHz			7.15909 MHz		
	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)
9.6	9.615	+0.16	129	9.615	+0.16	103	9.615	+0.16	64	9.520	-0.83	46
19.2	19.230	+0.16	64	19.230	+0.16	51	18.939	-1.36	32	19.454	+1.32	22
38.4	37.878	-1.36	32	38.461	+0.16	25	39.062	+1.7	15	37.286	-2.90	11
57.6	56.818	-1.36	21	58.823	+2.12	16	56.818	-1.36	10	55.930	-2.90	7
115.2	113.636	-1.36	10	111.111	-3.55	8	125	+8.51	4	111.860	-2.90	3
250	250	0	4	250	0	3	NA			NA		
625	625	0	1	NA	-	-	625	0	0	NA		
1250	1250	0	0	NA	-	-	NA	-	-	NA	-	-

BAUD RATE (Kbps)	Fosc = 5.0688 MHz			4 MHz			3.579545 MHz			1 MHz			32.768 kHz		
	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)
9.6	9.6	0	32	NA	-	-	9.727	+1.32	22	8.928	-6.99	6	NA	-	-
19.2	18.645	-2.94	16	1.202	+0.17	207	18.643	-2.90	11	20.833	+8.51	2	NA		
38.4	39.6	+3.12	7	2.403	+0.13	103	37.286	-2.90	5	31.25	-18.61	1	NA		
57.6	52.8	-8.33	5	9.615	+0.16	25	55.930	-2.90	3	62.5	+8.51	0	NA		
115.2	105.6	-8.33	2	19.231	+0.16	12	111.860	-2.90	1	NA			NA		
250	NA	-		NA		-	223.721	-10.51	0	NA			NA		
625	NA	-	-	NA		-	NA	-	-	NA			NA		-
1250	NA	-	-	NA	-	-	NA	-	-	NA			NA		

May 1997

National Semiconductor

LM117/LM317A/LM317
3-Terminal Adjustable Regulator

General Description

The LM117 series of adjustable 3-terminal positive voltage regulators is capable of supplying in excess of 1.5A over a 1.2V to 37V output range. They are exceptionally easy to use and require only two external resistors to set the output voltage. Further, both line and load regulation are better than standard fixed regulators. Also, the LM117 is packaged in standard transistor packages which are easily mounted and handled.

In addition to higher performance than fixed regulators, the LM117 series offers full overload protection available only in IC's. Included on the chip are current limit, thermal overload protection and safe area protection. All overload protection circuitry remains fully functional even if the adjustment terminal is disconnected.

Normally, no capacitors are needed unless the device is situated more than 6 inches from the input filter capacitors in which case an input bypass is needed. An optional output capacitor can be added to improve transient response. The adjustment terminal can be bypassed to achieve very high ripple rejection ratios which are difficult to achieve with standard 3-terminal regulators.

Besides replacing fixed regulators, the LM117 is useful in a wide variety of other applications. Since the regulator is "floating" and sees only the input-to-output differential voltage, supplies of several hundred volts can be regulated as long as the maximum input to output differential is not exceeded, i.e., avoid short-circuiting the output.

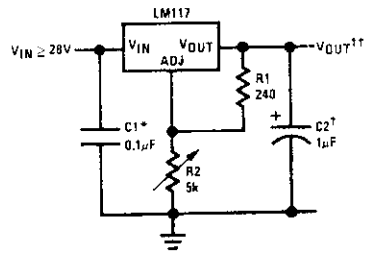
Also, it makes an especially simple adjustable switching regulator, a programmable output regulator, or by connecting a fixed resistor between the adjustment pin and output, the LM117 can be used as a precision current regulator. Supplies with electronic shutdown can be achieved by clamping the adjustment terminal to ground which programs the output to 1.2V where most loads draw little current.

For applications requiring greater output current, see LM150 series (3A) and LM138 series (5A) data sheets. For the negative complement, see LM137 series data sheet.

Features

- Guaranteed 1% output voltage tolerance (LM317A)
- Guaranteed max. 0.01%/V line regulation (LM317A)
- Guaranteed max. 0.3% load regulation (LM117)
- Guaranteed 1.5A output current
- Adjustable output down to 1.2V
- Current limit constant with temperature
- P+ Product Enhancement tested
- 80 dB ripple rejection
- Output is short-circuit protected

Typical Applications



DS009063-1

Full output current not available at high input-output voltages

*Needed if device is more than 6 inches from filter capacitors.

†Optional—improves transient response. Output capacitors in the range of 1 μF to 1000 μF of aluminum or tantalum electrolytic are commonly used to provide improved output impedance and rejection of transients.

$$\text{††}V_{OUT} = 1.25V\left(1 + \frac{R2}{R1}\right) + I_{ADJ}(R_2)$$

LM117 Series Packages and Power Capability

Part Number Suffix	Package	Rated Power Dissipation	Design Load Current
K	TO-3	20W	1.5A
H	TO-39	2W	0.5A
T	TO-220	20W	1.5A
E	LCC	2W	0.5A
S	TO-263	4W	1.5A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Power Dissipation	Internally Limited
Input-Output Voltage Differential	+40V, −0.3V
Storage Temperature	−65°C to +150°C
Lead Temperature	
Metal Package (Soldering, 10 seconds)	300°C
Plastic Package (Soldering, 4 seconds)	260°C
ESD Tolerance (Note 5)	3 kV

Operating Temperature Range

LM117	$-55°C \le T_J \le +150°C$
LM317A	$-40°C \le T_J \le +125°C$
LM317	$0°C \le T_J \le +125°C$

Preconditioning

Thermal Limit Burn-In	All Devices 100%

Electrical Characteristics (Note 3)

Specifications with standard type face are for $T_J = 25°C$, and those with **boldface type** apply over **full Operating Temperature Range**. Unless otherwise specified, $V_{IN} - V_{OUT} = 5V$, and $I_{OUT} = 10$ mA.

Parameter	Conditions	LM117 (Note 2)			Units
		Min	Typ	Max	
Reference Voltage					V
	$3V \le (V_{IN} - V_{OUT}) \le 40V$, $10 mA \le I_{OUT} \le I_{MAX}$, $P \le P_{MAX}$	1.20	1.25	1.30	V
Line Regulation	$3V \le (V_{IN} - V_{OUT}) \le 40V$ (Note 4)		0.01	0.02	%/V
			0.02	0.05	%/V
Load Regulation	$10 mA \le I_{OUT} \le I_{MAX}$ (Note 4)		0.1	0.3	%
			0.3	1	%
Thermal Regulation	20 ms Pulse		0.03	0.07	%/W
Adjustment Pin Current			50	100	μA
Adjustment Pin Current Change	$10 mA \le I_{OUT} \le I_{MAX}$, $3V \le (V_{IN} - V_{OUT}) \le 40V$		0.2	5	μA
Temperature Stability	$T_{MIN} \le T_J \le T_{MAX}$		1		%
Minimum Load Current	$(V_{IN} - V_{OUT}) = 40V$		3.5	5	mA
Current Limit	$(V_{IN} - V_{OUT}) \le 15V$				
	K Package	1.5	2.2	3.4	A
	H, K Packages	0.5	0.8	1.8	A
	$(V_{IN} - V_{OUT}) = 40V$				
	K Package	0.3	0.4		A
	H, K Packages	0.15	0.2		A
RMS Output Noise, % of V_{OUT}	$10 Hz \le f \le 10 kHz$		0.003		%
Ripple Rejection Ratio	$V_{OUT} = 10V$, f = 120 Hz, $C_{ADJ} = 0$ μF		65		dB
	$V_{OUT} = 10V$, f = 120 Hz, $C_{ADJ} = 10$ μF	66	80		dB
Long-Term Stability	$T_J = 125°C$, 1000 hrs		0.3	1	%
Thermal Resistance, Junction-to-Case	K Package		2.3	3	°C/W
	H Package		12	15	°C/W
	E Package				°C/W
Thermal Resistance, Junction-to-Ambient (No Heat Sink)	K Package		35		°C/W
	H Package		140		°C/W
	E Package				°C/W

Electrical Characteristics (Note 3)

Specifications with standard type face are for T_J = 25°C, and those with **boldface type** apply over **full Operating Temperature Range**. Unless otherwise specified, $V_{IN} - V_{OUT}$ = 5V, and I_{OUT} = 10 mA.

Parameter	Conditions	LM317A			LM317			Units
		Min	Typ	Max	Min	Typ	Max	
Reference Voltage		1.238	1.250	1.262				V
	3V ≤ ($V_{IN} - V_{OUT}$) ≤ 40V, 10 mA ≤ I_{OUT} ≤ I_{MAX}, P ≤ P_{MAX}	**1.225**	**1.250**	**1.270**	**1.20**	**1.25**	**1.30**	V
Line Regulation	3V ≤ ($V_{IN} - V_{OUT}$) ≤ 40V (Note 4)		0.005	0.01		0.01	0.04	%/V
			0.01	**0.02**		**0.02**	**0.07**	%/V
Load Regulation	10 mA ≤ I_{OUT} ≤ I_{MAX} (Note 4)		0.1	0.5		0.1	0.5	%
			0.3	**1**		**0.3**	**1.5**	%
Thermal Regulation	20 ms Pulse		0.04	0.07		0.04	0.07	%/W
Adjustment Pin Current			50	100		50	100	µA
Adjustment Pin Current Change	10 mA ≤ I_{OUT} ≤ I_{MAX} 3V ≤ ($V_{IN} - V_{OUT}$) ≤ 40V		0.2	5		0.2	5	µA
Temperature Stability	$T_{MIN} \le T_J \le T_{MAX}$		1			1		%
Minimum Load Current	($V_{IN} - V_{OUT}$) = 40V		3.5	10		3.5	10	mA
Current Limit	($V_{IN} - V_{OUT}$) ≤ 15V							
	K, T, S Packages	1.5	2.2	3.4	1.5	2.2	3.4	A
	H Package	0.5	0.8	1.8	0.5	0.8	1.8	A
	($V_{IN} - V_{OUT}$) = 40V							
	K, T, S Packages	0.15	0.4		0.15	0.4		A
	H Package	0.075	0.2		0.075	0.2		A
RMS Output Noise, % of V_{OUT}	10 Hz ≤ f ≤ 10 kHz		0.003			0.003		%
Ripple Rejection Ratio	V_{OUT} = 10V, f = 120 Hz, C_{ADJ} = 0 µF		65			65		dB
	V_{OUT} = 10V, f = 120 Hz, C_{ADJ} = 10 µF	66	80		66	80		dB
Long-Term Stability	T_J = 125°C, 1000 hrs		0.3	1		0.3	1	%
Thermal Resistance, Junction-to-Case	K Package					2.3	3	°C/W
	H Package		12	15		12	15	°C/W
	T Package		4	5		4		°C/W
Thermal Resistance, Junction-to-Ambient (No Heat Sink)	K Package		35			35		°C/W
	H Package		140			140		°C/W
	T Package		50			50		°C/W
	S Package (Note 6)		50			50		°C/W

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 2: Refer to RETS117H drawing for the LM117H, or the RETS117K for the LM117K military specifications.

Note 3: Although power dissipation is internally limited, these specifications are applicable for maximum power dissipations of 2W for the TO-39 and 20W for the TO-3, TO-220, and TO-263. I_{MAX} is 1.5A for the TO-3, TO-220, and TO-263 packages and 0.5A for the TO-39 package. All limits (i.e., the numbers in the Min. and Max. columns) are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 4: Regulation is measured at a constant junction temperature, using pulse testing with a low duty cycle. Changes in output voltage due to heating effects are covered under the specifications for thermal regulation.

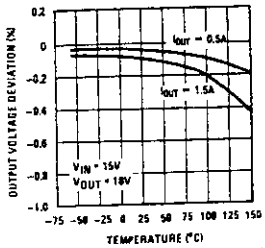
Note 5: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 6: If the TO-263 package is used, the thermal resistance can be reduced by increasing the PC board copper area thermally connected to the package: Using 0.5 square inches of copper area, θ_{JA} is 50°C/W; with 1 square inch of copper area, θ_{JA} is 37°C/W; and with 1.6 or more square inches of copper area, θ_{JA} is 32°C/W.

Typical Performance Characteristics

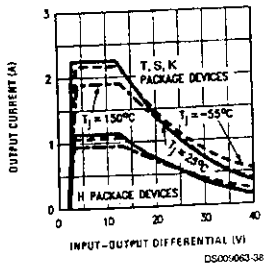
Output Capacitor = 0 µF unless otherwise noted

Load Regulation



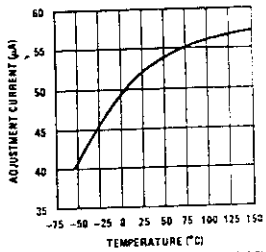
DS009063-37

Current Limit



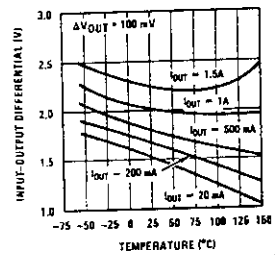
DS009063-38

Adjustment Current



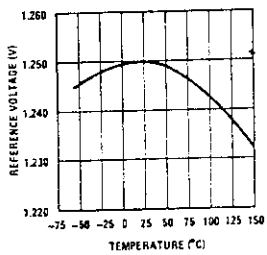
DS009063-39

Dropout Voltage



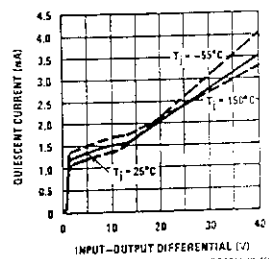
DS009063-40

Temperature Stability



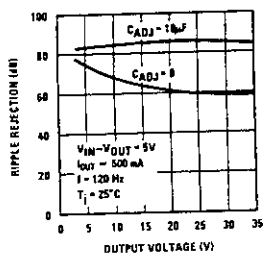
DS009063-41

Minimum Operating Current



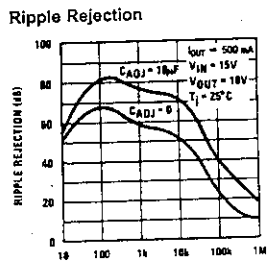
DS009063-42

Ripple Rejection



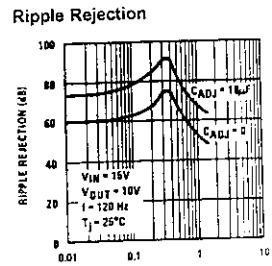
DS009063-43

Ripple Rejection



DS009063-44

Ripple Rejection



DS009063-45

National Semiconductor

December 1994

LM124/LM224/LM324/LM2902
Low Power Quad Operational Amplifiers

General Description

The LM124 series consists of four independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, DC gain blocks and all the conventional op amp circuits which now can be more easily implemented in single power supply systems. For example, the LM124 series can be directly operated off of the standard +5V power supply voltage which is used in digital systems and will easily provide the required interface electronics without requiring the additional ±15V power supplies.

Unique Characteristics

- In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage
- The unity gain cross frequency is temperature compensated
- The input bias current is also temperature compensated

Advantages

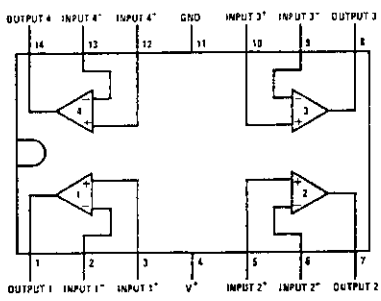
- Eliminates need for dual supplies
- Four internally compensated op amps in a single package
- Allows directly sensing near GND and V_{OUT} also goes to GND
- Compatible with all forms of logic
- Power drain suitable for battery operation

Features

- Internally frequency compensated for unity gain
- Large DC voltage gain 100 dB
- Wide bandwidth (unity gain) 1 MHz
  (temperature compensated)
- Wide power supply range:
  Single supply 3V to 32V
  or dual supplies ±1.5V to ±16V
- Very low supply current drain (700 μA)—essentially independent of supply voltage
- Low input biasing current 45 nA
  (temperature compensated)
- Low input offset voltage 2 mV
  and offset current 5 nA
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Large output voltage swing 0V to V^+ − 1.5V

Connection Diagram

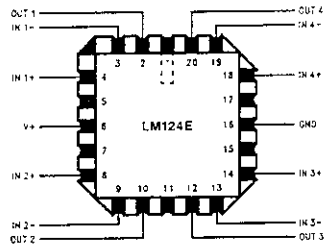
Dual-In-Line Package



TL/H/9299–1

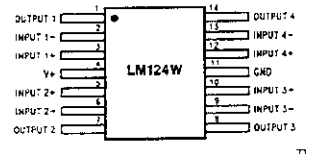
Top View

Order Number LM124J, LM124AJ, LM124J/883, LM124AJ/883*, LM224J, LM224AJ, LM324J, LM324M, LM324AM, LM2902M, LM324N, LM324AN or LM2902N**
See NS Package Number J14A, M14A or N14A



TL/H/9299–32

Order Number LM124AE/883 or LM124E/883
See NS Package Number E20A



TL/H/9299–33

Order Number LM124AW/883 or LM124W/883
See NS Package Number W14B

*LM124A available per JM38510/11006
**LM124 available per JM38510/11005

RRD-B30M115/Printed in U. S. A.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

(Note 9)

	LM124/LM224/LM324 LM124A/LM224A/LM324A	LM2902
Supply Voltage, V^+	32V	26V
Differential Input Voltage	32V	26V
Input Voltage	−0.3V to +32V	−0.3V to +26V
Input Current (V_{IN} < −0.3V) (Note 3)	50 mA	50 mA
Power Dissipation (Note 1)		
Molded DIP	1130 mW	1130 mW
Cavity DIP	1260 mW	1260 mW
Small Outline Package	800 mW	800 mW
Output Short-Circuit to GND (One Amplifier) (Note 2) $V^+ \leq 15V$ and $T_A = 25°C$	Continuous	Continuous
Operating Temperature Range		−40°C to +85°C
LM324/LM324A	0°C to +70°C	
LM224/LM224A	−25°C to +85°C	
LM124/LM124A	−55°C to +125°C	

	LM124/LM224/LM324 LM124A/LM224A/LM324A	LM2902
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	260°C	260°C
Soldering Information		
Dual-In-Line Package		
Soldering (10 seconds)	260°C	260°C
Small Outline Package		
Vapor Phase (60 seconds)	215°C	215°C
Infrared (15 seconds)	220°C	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD Tolerance (Note 10)	250V	250V

Electrical Characteristics $V^+ = +5.0V$, (Note 4), unless otherwise stated

Parameter	Conditions	LM124A			LM224A			LM324A			LM124/LM224			LM324			LM2902			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	(Note 5) $T_A = 25°C$		1	2		1	3		2	3		2	5		2	7		2	7	mV
Input Bias Current (Note 6)	$I_{IN(+)}$ or $I_{IN(-)}$, $V_{CM} = 0V$, $T_A = 25°C$		20	50		40	80		45	100		45	150		45	250		45	250	nA
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, $V_{CM} = 0V$, $T_A = 25°C$		2	10		2	15		5	30		3	30		5	50		5	50	nA
Input Common-Mode Voltage Range (Note 7)	$V^+ = 30V$, (LM2902, $V^+ = 26V$), $T_A = 25°C$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	V
Supply Current	Over Full Temperature Range $R_L = \infty$ On All Op Amps $V^+ = 30V$ (LM2902 $V^+ = 26V$)		1.5	3		1.5	3		1.5	3		1.5	3		1.5	3		1.5	3	mA
	$V^+ = 5V$		0.7	1.2		0.7	1.2		0.7	1.2		0.7	1.2		0.7	1.2		0.7	1.2	
Large Signal Voltage Gain	$V^+ = 15V$, $R_L \geq 2 k\Omega$, ($V_O = 1V$ to $11V$), $T_A = 25°C$	50	100		50	100		25	100		50	100		25	100		25	100		V/mV
Common-Mode Rejection Ratio	DC, $V_{CM} = 0V$ to $V^+ - 1.5V$, $T_A = 25°C$	70	85		70	85		65	85		70	85		65	85		50	70		dB
Power Supply Rejection Ratio	$V^+ = 5V$ to $30V$ (LM2902, $V^+ = 5V$ to $26V$), $T_A = 25°C$	65	100		65	100		65	100		65	100		65	100		50	100		dB

Electrical Characteristics $V^+ = +5.0V$ (Note 4) unless otherwise stated (Continued)

Parameter		Conditions		LM124A			LM224A			LM324A			LM124/LM224			LM324			LM2902			Units
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Amplifier-to-Amplifier Coupling (Note 8)		f = 1 kHz to 20 kHz, $T_A = 25°C$ (Input Referred)			−120			−120			−120			−120			−120			−120		dB
Output Current	Source	$V_{IN}^+ = 1V$, $V_{IN}^- = 0V$, $V^+ = 15V$, $V_O = 2V$, $T_A = 25°C$		20	40		20	40		20	40		20	40		20	40		20	40		mA
	Sink	$V_{IN}^- = 1V$, $V_{IN}^+ = 0V$, $V^+ = 15V$, $V_O = 2V$, $T_A = 25°C$		10	20		10	20		10	20		10	20		10	20		10	20		mA
		$V_{IN}^- = 1V$, $V_{IN}^+ = 0V$, $V^+ = 15V$, $V_O = 200$ mV, $T_A = 25°C$		12	50		12	50		12	50		12	50		12	50		12	50		µA
Short Circuit to Ground		(Note 2) $V^+ = 15V$, $T_A = 25°C$			40	60		40	60		40	60		40	60		40	60		40	60	mA
Input Offset Voltage		(Note 5)				4			4			5			7			9			10	mV
Input Offset Voltage Drift		$R_S = 0\Omega$			7	20		7	20		7	30		7			7			7		µV/°C
Input Offset Current		$I_{IN(+)} - I_{IN(-)}$, $V_{CM} = 0V$				30			30			75			100			150		45	200	nA
Input Offset Current Drift		$R_S = 0\Omega$			10	200		10	200		10	300		10			10			10		pA/°C
Input Bias Current		$I_{IN(+)}$ or $I_{IN(-)}$			40	100		40	100		40	200		40	300		40	500		40	500	nA
Input Common-Mode Voltage Range (Note 7)		$V^+ = +30V$ (LM2902, $V^+ = 26V$)		0		$V^+ - 2$	0		$V^+ - 2$	0		$V^+ - 2$	0		$V^+ - 2$	0		$V^+ - 2$	0		$V^+ - 2$	V
Large Signal Voltage Gain		$V^+ = +15V$ (V_O Swing = 1V to 11V) $R_L \geq 2\ k\Omega$		25			25			15			25			15			15			V/mV
Output Voltage Swing	V_{OH}	$V^+ = 30V$ (LM2902, $V^+ = 26V$)	$R_L = 2\ k\Omega$	26			26			26			26			26			22			V
			$R_L = 10\ k\Omega$	27	28		27	28		27	28		27	28		27	28		23	24		
	V_{OL}	$V^+ = 5V$, $R_L = 10\ k\Omega$			5	20		5	20		5	20		5	20		5	20		5	100	mV

Electrical Characteristics $V^+ = +5.0V$ (Note 4) unless otherwise stated (Continued)

Parameter		Conditions		LM124A			LM224A			LM324A			LM124/LM224			LM324			LM2902			Units
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output Current	Source	$V_O = 2V$	$V_{IN}^+ = +1V$, $V_{IN}^- = 0V$, $V^+ = 15V$	10	20		10	20		10	20		10	20		10	20		10	20		mA
	Sink		$V_{IN}^- = +1V$, $V_{IN}^+ = 0V$, $V^+ = 15V$	10	15		5	8		5	8		5	8		5	8		5	8		

Note 1: For operating at high temperatures, the LM324/LM324A/LM2902 must be derated based on a +125°C maximum junction temperature and a thermal resistance of 88°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM224/LM224A and LM124/LM124A can be derated based on a +150°C maximum junction temperature. The dissipation is the total of all four amplifiers—use external resistors, where possible, to allow the amplifier to saturate of to reduce the power which is dissipated in the integrated circuit.

Note 2: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 40 mA independent of the magnitude of V^+. At values of supply voltage in excess of +15V, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

Note 3: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the op amps to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than −0.3V (at 25°C).

Note 4: These specifications are limited to $-55°C \le T_A \le +125°C$ for the LM124/LM124A. With the LM224/LM224A, all temperature specifications are limited to $-25°C \le T_A \le +85°C$, the LM324/LM324A temperature specifications are limited to $0°C \le T_A \le +70°C$, and the LM2902 specifications are limited to $-40°C \le T_A \le +65°C$.

Note 5: $V_O \cong 1.4V$, $R_S = 0\Omega$ with V^+ from 5V to 30V; and over the full input common-mode range (0V to $V^+ - 1.5V$) for LM2902, V^+ from 5V to 26V.

Note 6: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.

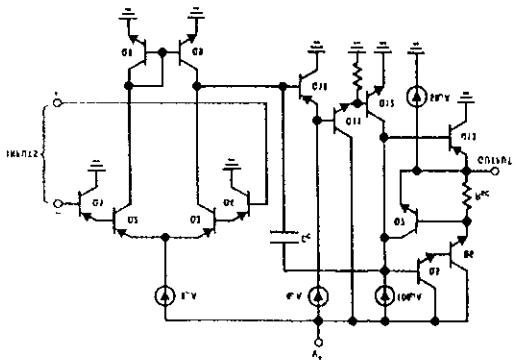
Note 7: The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V (at 25°C). The upper end of the common-mode voltage range is $V^+ - 1.5V$ (at 25°C), but either or both inputs can go to +32V without damage (+26V for LM2902), independent of the magnitude of V^+.

Note 8: Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitance increases at higher frequencies.

Note 9: Refer to RETS124AX for LM124A military specifications and refer to RETS124X for LM124 military specifications.

Note 10: Human body model, 1.5 kΩ in series with 100 pF.

Schematic Diagram (Each Amplifier)



TL/H/9299–2

19-4323; Rev 7b; 11/07

MAXIM

+5V-Powered, Multichannel RS-232 Drivers/Receivers

General Description

The MAX220–MAX249 family of line drivers/receivers is intended for all EIA/TIA-232E and V.28/V.24 communications interfaces, particularly applications where ±12V is not available.

These parts are especially useful in battery-powered systems, since their low-power shutdown mode reduces power dissipation to less than 5µW. The MAX225, MAX233, MAX235, and MAX245/MAX246/MAX247 use no external components and are recommended for applications where printed circuit board space is critical.

Applications

Portable Computers

Low-Power Modems

Interface Translation

Battery-Powered RS-232 Systems

Multi-Drop RS-232 Networks

Features

Superior to Bipolar

- **Operate from Single +5V Power Supply (+5V and +12V—MAX231/MAX239)**
- **Low-Power Receive Mode in Shutdown (MAX223/MAX242)**
- **Meet All EIA/TIA-232E and V.28 Specifications**
- **Multiple Drivers and Receivers**
- **3-State Driver and Receiver Outputs**
- **Open-Line Detection (MAX243)**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX220CPE	0°C to +70°C	16 Plastic DIP
MAX220CSE	0°C to +70°C	16 Narrow SO
MAX220CWE	0°C to +70°C	16 Wide SO
MAX220C/D	0°C to +70°C	Dice*
MAX220EPE	-40°C to +85°C	16 Plastic DIP
MAX220ESE	-40°C to +85°C	16 Narrow SO
MAX220EWE	-40°C to +85°C	16 Wide SO
MAX220EJE	-40°C to +85°C	16 CERDIP
MAX220MJE	-55°C to +125°C	16 CERDIP

Ordering Information continued at end of data sheet.

**Contact factory for dice specifications.*

Selection Table

Part Number	Power Supply (V)	No. of RS-232 Drivers/Rx	No. of Ext. Caps	Nominal Cap. Value (µF)	SHDN & Three-State	Rx Active in SHDN	Data Rate (kbps)	Features
MAX220	+5	2/2	4	4.7/10	No	—	120	Ultra-low-power, industry-standard pinout
MAX222	+5	2/2	4	0.1	Yes	—	200	Low-power shutdown
MAX223 (MAX213)	+5	4/5	4	1.0 (0.1)	Yes	✓	120	MAX241 and receivers active in shutdown
MAX225	+5	5/5	0	—	Yes	✓	120	Available in SO
MAX230 (MAX200)	+5	5/0	4	1.0 (0.1)	Yes	—	120	5 drivers with shutdown
MAX231 (MAX201)	+5 and +7.5 to +13.2	2/2	2	1.0 (0.1)	No	—	120	Standard +5/+12V or battery supplies; same functions as MAX232
MAX232 (MAX202)	+5	2/2	4	1.0 (0.1)	No	—	120 (64)	Industry standard
MAX232A	+5	2/2	4	0.1	No	—	200	Higher slew rate, small caps
MAX233 (MAX203)	+5	2/2	0	—	No	—	120	No external caps
MAX233A	+5	2/2	0	—	No	—	200	No external caps, high slew rate
MAX234 (MAX204)	+5	4/0	4	1.0 (0.1)	No	—	120	Replaces 1488
MAX235 (MAX205)	+5	5/5	0	—	Yes	—	120	No external caps
MAX236 (MAX206)	+5	4/3	4	1.0 (0.1)	Yes	—	120	Shutdown, three state
MAX237 (MAX207)	+5	5/3	4	1.0 (0.1)	No	—	120	Complements IBM PC serial port
MAX238 (MAX208)	+5	4/4	4	1.0 (0.1)	No	—	120	Replaces 1488 and 1489
MAX239 (MAX209)	+5 and +7.5 to +13.2	3/5	2	1.0 (0.1)	No	—	120	Standard +5/+12V or battery supplies; single-package solution for IBM PC serial port
MAX240	+5	5/5	4	1.0	Yes	-	120	DIP or flatpack package
MAX241 (MAX211)	+5	4/5	4	1.0 (0.1)	Yes	-	120	Complete IBM PC serial port
MAX242	+5	2/2	4	0.1	Yes	✓	200	Separate shutdown and enable
MAX243	+5	2/2	4	0.1	No	—	200	Open-line detection simplifies mouse
MAX244	+5	8/10	4	1.0	No	—	120	High slew rate
MAX245	+5	8/10	0	-	Yes	✓	120	High slew rate, int. caps, two shutdown modes
MAX246	+5	8/10	0	—	Yes	✓	120	High slew rate, int. caps, three shutdown modes
MAX247	+5	8/9	0	—	Yes	✓	120	High slew rate, int. caps, nine shutdown modes
MAX248	+5	8/8	4	1.0	Yes	✓	120	High slew rate, selective half-shutdown
MAX249	+5	6/10	4	1.0	Yes	✓	120	Available in quad flatpack package

ABSOLUTE MAXIMUM RATINGS—MAX220/222/232A/233A/242/243

Supply Voltage (V_{CC}) ..... -0.3V to +6V
Input Voltages
T_{IN} ..... -0.3V to (V_{CC} + 0.3V)
R_{IN} ..... ±30V
T_{OUT} (Note 1) ..... ±15V
Output Voltages
T_{OUT} ..... ±15V
R_{OUT} ..... -0.3V to (V_{CC} + 0.3V)
Driver/Receiver Output Short Circuited to GND ..... Continuous
Continuous Power Dissipation (T_A = +70°C)
16-Pin Plastic DIP (derate 10.53mW/°C above +70°C) ... 842mW
18-Pin Plastic DIP (derate 11.11mW/°C above +70°C) ... 889mW
20-Pin Plastic DIP (derate 8.00mW/°C above +70°C) ... 440mW
16-Pin Narrow SO (derate 8.70mW/°C above +70°C) ... 696mW
16-Pin Wide SO (derate 9.52mW/°C above +70°C) ... 762mW
18-Pin Wide SO (derate 9.52mW/°C above +70°C) ... 762mW
20-Pin Wide SO (derate 10.00mW/°C above +70°C) ... 800mW
20-Pin SSOP (derate 8.00mW/°C above +70°C) ... 640mW
16-Pin CERDIP (derate 10.00mW/°C above +70°C) ... 800mW
18-Pin CERDIP (derate 10.53mW/°C above +70°C) ... 842mW
Operating Temperature Ranges
MAX2_ _AC_ _, MAX2_ _C_ _ ..... 0°C to +70°C
MAX2_ _AE_ _, MAX2_ _E_ _ ..... -40°C to +85°C
MAX2_ _AM_ _, MAX2_ _M_ _ ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

Note 1: Input voltage measured with T_{OUT} in high-impedance state, $\overline{SHDN}$ or V_{CC} = 0V.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—MAX220/222/232A/233A/242/243

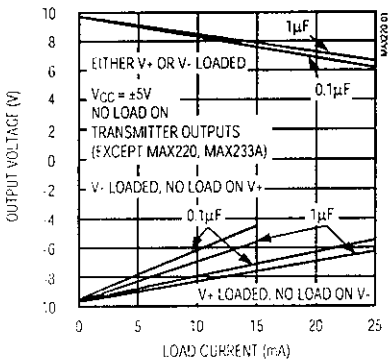
(V_{CC} = +5V ±10%, C1–C4 = 0.1µF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
RS-232 TRANSMITTERS						
Output Voltage Swing	All transmitter outputs loaded with 3kΩ to GND		±5	±8		V
Input Logic Threshold Low				1.4	0.8	V
Input Logic Threshold High			2	1.4		V
Logic Pull-Up/Input Current	Normal operation			5	40	µA
	$\overline{SHDN}$ = 0V, MAX222/242, shutdown			±0.01	±1	
Output Leakage Current	V_{CC} = 5.5V, $\overline{SHDN}$ = 0V, V_{OUT} = ±15V, MAX222/242			±0.01	±10	µA
	V_{CC} = $\overline{SHDN}$ = 0V, V_{OUT} = ±15V			±0.01	±10	
Data Rate	All except MAX220, normal operation			200	116	kbits/sec
	MAX220			22	20	
Transmitter Output Resistance	V_{CC} = V+ = V- = 0V, V_{OUT} = ±2V		300	10M		Ω
Output Short-Circuit Current	V_{OUT} = 0V			±7	±22	mA
RS-232 RECEIVERS						
RS-232 Input Voltage Operating Range					±30	V
RS-232 Input Threshold Low	V_{CC} = 5V	All except MAX243 $R2_{IN}$	0.8	1.3		V
		MAX243 $R2_{IN}$ (Note 2)	-3			
RS-232 Input Threshold High	V_{CC} = 5V	All except MAX243 $R2_{IN}$		1.8	2.4	V
		MAX243 $R2_{IN}$ (Note 2)		-0.5	-0.1	
RS-232 Input Hysteresis	All except MAX243, V_{CC} = 5V, no hysteresis in shdn.		0.2	0.5	1	V
	MAX243			1		
RS-232 Input Resistance			3	5	7	kΩ
TTL/CMOS Output Voltage Low	I_{OUT} = 3.2mA			0.2	0.4	V
TTL/CMOS Output Voltage High	I_{OUT} = -1.0mA		3.5	V_{CC} - 0.2		V
TTL/CMOS Output Short-Circuit Current	Sourcing V_{OUT} = GND		-2	-10		mA
	Shrinking V_{OUT} = V_{CC}		10	30		
TTL/CMOS Output Leakage Current	$\overline{SHDN}$ = V_{CC} or $\overline{EN}$ = V_{CC} ($\overline{SHDN}$ = 0V for MAX222), 0V ≤ V_{OUT} ≤ V_{CC}			±0.05	±10	µA

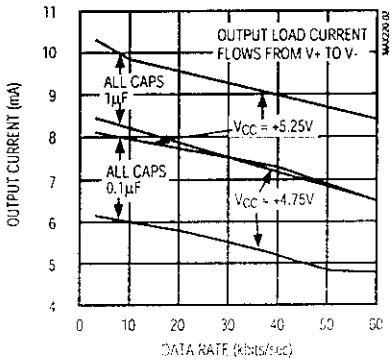
Typical Operating Characteristics

MAX220/MAX222/MAX232A/MAX233A/MAX242/MAX243

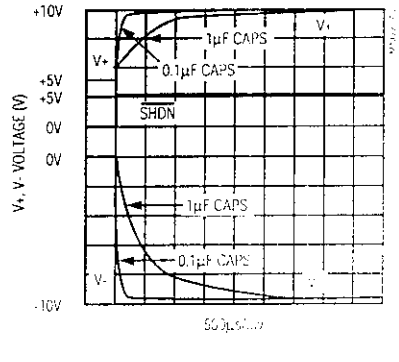
OUTPUT VOLTAGE vs. LOAD CURRENT



AVAILABLE OUTPUT CURRENT vs. DATA RATE



MAX222/MAX242 ON-TIME EXITING SHUTDOWN



LM 324, LM324A

QUADRUPLE OPERATIONAL AMPLIFIERS

- Wide range of supply voltages single supply 3v to 30v (LM 2902 and LM 2902Q 3v to 26v) or Dual supplies
- Low supply current drain independent of supply voltage 0.8 MA typical.
- Common mode input voltage rang include ground allowing direct sensing near ground.
- Low input bias and offset parameters input offset voltage 3MV typical.

  A version 2MV typical.

  Input offset current.... 2NA typical;

  Input bias counts 15 NA typical.

  A version 15 NA typical.
- Differential input voltage range equal to maximum rated supply voltage 32V (26V for LM2902 and LM2902Q)
- Open loop differential voltage amplification 100V / MV typical.
- Internal frequency compensation.

Description:

These devices consist of four independent, high gain frequency compensated operational amplifiers that were designed specifically to operate from a single supply. Over a wide rang of voltages. Operation from split supplies is also possible so long as the difference between the two supplies in 3V to 30V and VCC in at least 1.5V more positive than the input common mode voltage. The low supply counts drain in independent of the magnitude of the supply voltage.

. Application include transaction amplifiers, dc amplification blocks and all the conventional operational amplifier circuits that mow can be more easily implemented in single supply voltage systems, for example the LM124 can be operated directly off of the standard 5V supply that is used in digital systems and will easily provide the required interface electronics without requiring additional ±15v supplies.

The LM324 and LM324 A are characterized four operation from 0° to 70°c.