MICROCONTROLLER BASED MULTIPURPOSE PORTABLE DATA LOGGING SYSTEM WITH PC BASED DATA ANALYSIS

PROJECT REPORT

SUBMITTED BY

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IN PARTIAL FULFILMENT OF THE REQUIREMENTS

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Department of Electronics & Communication Engineering

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COIMBATORE - 641 006.

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CERTIFICATE

TO WHOMSOEVER IT MAY CONCERN

This is to certify that ***R. Sandeep Raja Chidambaram, B. Balamurugan, A. Vivek***, from the Electronics and Communication Engineering Department of Kumaraguru College of Technology have worked on the project titled "***Microcontroller based Multipurpose Portable Data logging Device with PC based Data Analysis***" under the guidance of Mrs. B. Sudha, Senior Project Engineer, during the project tenure year from May, 2002 to March, 2003 as a part of their curriculum for the degree of Bachelor of Engineering in our organization during the academic year 2002- 2003. They have shown a lot of interest and completed the design of the Project and we wish them the very best in all their future endeavors.

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SYNOPSIS

Existence of a field untouched or uninfluenced by microcontrollers is unthinkable and inconvenient. Microcontroller is the hype in the field of electronics and communication. The field of signal acquisition and signal conditioning is no exception to this generalization.

Data logging is imperative in many areas of engineering. Manual methods have become obsolete due to their cumbersome nature. Data logging using microcontrollers and computers are accurate and easier. Software has come into existence that makes this process very simple. One such software used in our project is *KEIL*, a cross-compiler between C and 8051 assembly level programming.

The core of our system features AT89c51 microcontroller, that receives the input involved in logging, stores them in the external RAM 62256 and forwards the stored data to computer via RS 232.The received data are analyzed using LabVIEW.

CONTENTS

1. INTRODUCTION

DATA LOGGING SYSTEM

The simplest way to store data is to record it on paper with either a strip-chart recorder or an x-y plotter. For greater utility data can be digitized and stored in computer files for later data analysis. Many instruments digitize and store data in memory for subsequent transfer to a computer file. The analytical signal can also be digitized and stored to a computer data file using a computer data logging system.

Measurements are done on stand alone instruments of various type oscilloscopes, multimeters, counters etc. However, the need to *record* the measurements and *process* the collected data for *visualization* has become increasingly important. There are several ways in which the data can be exchanged between instruments and a computer. Many instruments have a serial port which can exchange data to and from a computer or another instrument.

Another way to measure signals and transfer the data into a computer is by using a Data logging board. The analog and continuous time signals measured by the sensor and modified by the signal conditioning circuitry must converted into the form a computer can understand. This is what is referred to here as *data logging*.

Our Data logging system consists of a Microcontroller AT89c51, which controls the whole process, ADC 0809 which converts analog input to digital output, RAM IC 62256 which stores the received data that can be retrieved for future analysis.

SERIAL COMMUNICATION

One of the most universal parts of the PC is its serial port. You can connect a mouse, a modem, a printer, a plotter, another PC, dongles, etc. But its usage (both software and hardware) is one of the best-kept secrets for most users, besides that it is not difficult to understand how to connect devices to it and how to program it.

Serial communication is often used either to control or to receive data from an embedded microprocessor. Serial communication is a form of I/O in which the bits of a byte begin transferred appear one after the other in a timed sequence on a single wire. Serial communication has become the standard for inter-computer communication.

Types of serial communications:

There are two basic types of serial communications,

- Synchronous and
- Asynchronous.

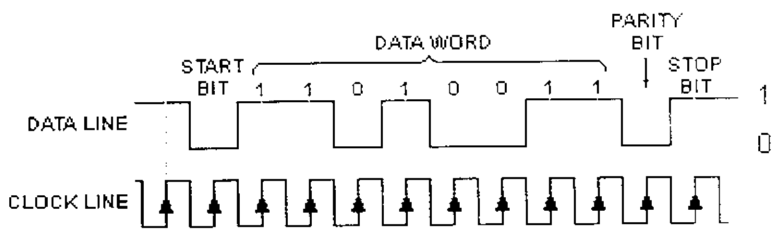
SYNCHRONOUS COMMUNICATION:

With Synchronous communications, the two devices initially synchronize themselves to each other, and then continually send characters to stay in sync. Even when data is not really being sent, a constant flow of bits allows each device to know where the other is at any given time. That is, each character that is sent is either actual data or an idle character. Synchronous communications allows faster data transfer rates than asynchronous methods, because additional bits to mark the beginning and end of each data byte are not required. The serial ports on IBM-style PCs are asynchronous devices and therefore only support asynchronous serial communications.

ASYNCHRONOUS COMMUNICATION:

Asynchronous means "no synchronization", and thus does not require sending and receiving idle characters. However, the beginning and end of each byte of data must be identified by start and stop bits. The start bit indicate when the data byte is about to begin and the stop bit signals when it ends. The requirement to send these additional two bits cause asynchronous communications to be slightly slower than synchronous however it has the advantage that the processor does not have to deal with the additional idle characters.

An asynchronous line that is idle is identified with a value of 1, (also called a mark state). By using this value to indicate that no data is currently being sent, the devices are able to distinguish between an idle state and a disconnected line. When a character is about to be transmitted, a start bit is sent. A start bit has a value of 0, (also called a space state). Thus, when the line switches from a value of 1 to a value of 0, the receiver is alerted that a data character is about to come down the line.



Asynchronous Serial Data Frame

2.1 MICROCONTROLLER-AT89C51

A Micro controller consists of a powerful CPU tightly coupled with memory (RAM, ROM, or EPROM), various Input features such as serial ports, parallel ports, timers/counter, interrupt controller data acquisition interface Analog to Digital converter (ADC), Digital to Analog converter (DAC) everything integrated into a single silicon chip.

It does not mean that any Microcontroller should have all the above said features on chip. Depending on the need and area of application for which it is designed, the on chip features present in it may (or) may not include all the individual section mentioned above.

Any Microcontroller requires memory to store a sequence of instruction making up a program, Parallel port or serial port for communication with an external system timer/counter for control purpose like generating time delay, and rate for the serial port apart from the controlling unit called the Central Processing Unit (CPU).

AT89C51

GENERAL DESCRIPTION:

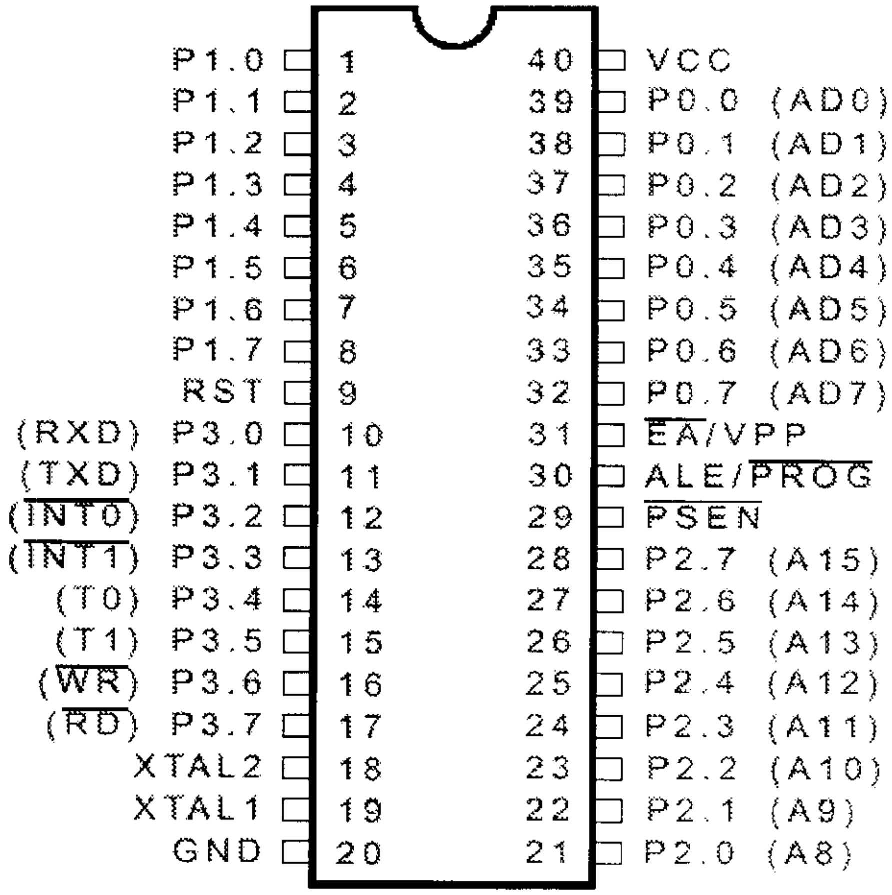
The heart of our data acquisition system is AT89C51 which is a low-power, high-performance CMOS 8-bit microcomputer with 4K bytes of Flash Programmable and Erasable Read Only Memory (EPROM).The device is manufactured using Atmel's high density nonvolatile memory technology and is compatible with the industry standard MCS-51™ instruction set and pin out. The on-chip Flash allows the program memory to be reprogrammed in-system or by a conventional nonvolatile memory programmer.

By combining a versatile 8-bit CPU with Flash on a monolithic chip, the Atmel AT89C51 is a powerful microcomputer which provides a highly flexible and cost effective solution to many embedded control applications.

FEATURES:

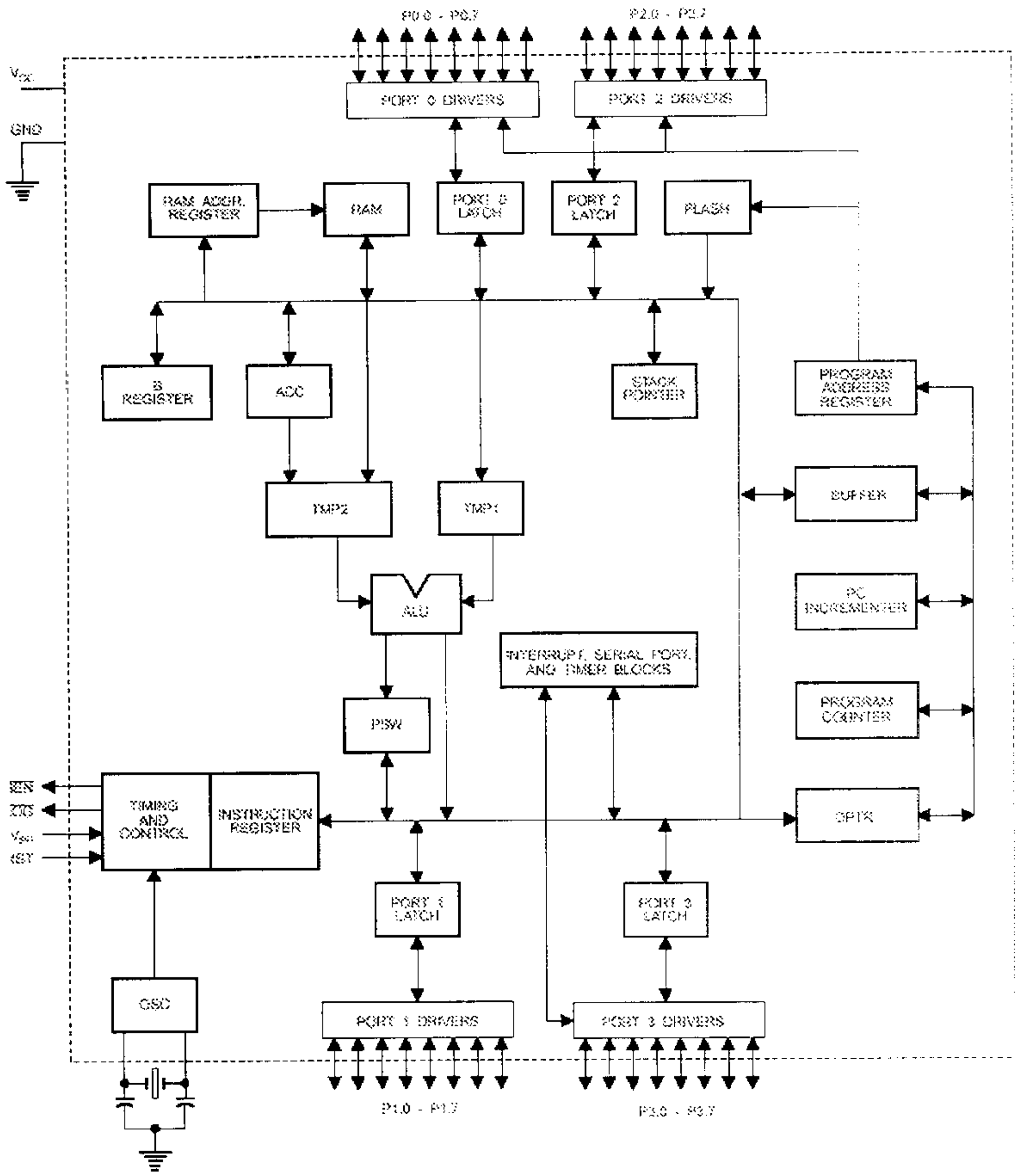
- Compatible with MCS-51™ Products
- 4K Bytes of In-System Reprogrammable Flash Memory
  Endurance: 1,000 Write/Erase Cycles
- Fully Static Operation: 0 Hz to 24 MHz
- Three-Level Program Memory Lock
- 128 x 8-Bit Internal RAM
- 32 Programmable I/O Lines
- Two 16-Bit Timer/Counters
- Six Interrupt Sources
- Programmable Serial Channel
- Low Power Idle and Power Down Modes

PIN DIAGRAM:



The AT89C51 provides the following standard features: 4K bytes of Flash, 128 bytes of RAM, 32 I/O lines, two 16-bit timer/counters, five vector two-level interrupt architecture, a full duplex serial port, on-chip oscillator and clock circuitry. In addition, the AT89C51 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port and interrupt system to continue functioning. The Power down Mode saves the RAM contents but freezes the oscillator disabling all other chip functions until the next hardware reset.

FUNCTIONAL DIAGRAM:



PIN DESCRIPTION:

VCC:

Supply voltage.

GND:

Ground.

PORT 0:

Port 0 is an 8-bit open drain bidirectional I/O port. As an output port each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high impedance inputs.Port0 may also be configured to be the multiplexed low order Address/data bus during accesses to external program and data memory. In this mode P0 has internal pull-ups. Port 0 also receives the code bytes during Flash programming, and outputs the code bytes during program verification. External pull-ups are required during program verification.

PORT 1:

Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (IIL) because of the internal pull-ups. Port 1 also receives the low-order address bytes during Flash programming and verification.

PORT 2:

Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (IIL) because of the internal pull-ups. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that uses 16-bit addresses. In this application it uses strong internal pull-ups when emitting 1s. During accesses to external data memory that uses 8-bit addresses, Port 2 emits the contents of the P2 Special Function Register. Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

PORT 3:

Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (IIL) because of the pull-ups. Port 3 also receives some control signals for Flash programming and verification Port 3 also serves the functions of various special features of the AT89C51 as listed below:

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

RST:

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

ALE/PROG:

Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input (PROG) during Flash programming. In normal operation ALE is emitted at a constant rate of 1/6the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory. If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller.

PSEN:

Program Store Enable is the read strobe to external program memory. When the AT89C51 is executing code from external program memory, PSEN is activated twice each machine cycle, except that two PSEN activations are skipped during each access to external data memory.

EA/VPP:

External Access Enable. EA must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, EA will be internally latched on reset. EA should be strapped to VCC for internal program executions. This pin also receives the 12-volt programming enable voltage (VPP) during Flash programming, for parts that require 12-volt VPP.

XTAL1:

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

XTAL2:

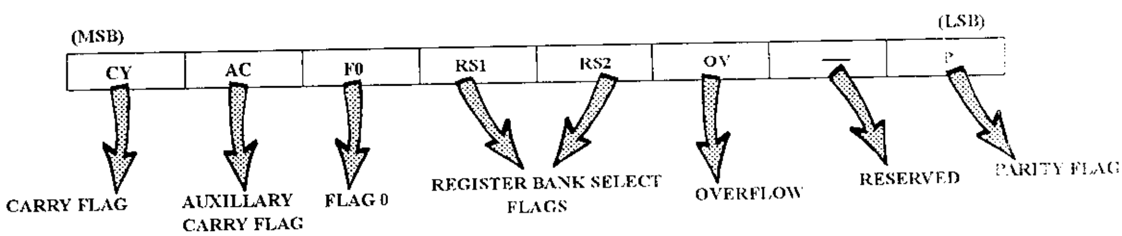
Output from the inverting oscillator amplifier.

CPU TIMING:

All ATMEL flash micro controllers have an on chip oscillator, Which can be used as the clock source for the CPU. To use the on chip oscillator, connect a crystal or ceramic resonator between the XTAL1 and XTAL2 pins of the micro controller, and connect the capacitors to ground. The internal clock generator defines the sequence of states that make up the micro controller machine cycles.

PROGRAM STATUS WORD (PSW):

The program status word register contains the information regarding program status as described in the figure.



PORT OPERATION:

All four ports in the AT89C51 are bi-directional each consists of latch, an output driver, an input buffer. The output drivers of ports and the input buffers of port 0 are used in accesses to external memory. In this application port 0 outputs the lower byte of the external memory address, time multiplexed with the byte being written or read. Port 2outputs the higher byte of external memory address when the address is 16 bit wide. Otherwise the Port 2 pins continue to emit the SFR content.

SERIAL DATA BUFFER:

The serial data buffer is actually two separate registers, a transmit buffer and a receive buffer register. When data is moved to SBUF, it goes to the data buffer where it is held for serial transmission. When data is moved from SBUF, it comes from the receiver.

INTERRUPT STRUCTURE:

This provides five interrupt sources two external interrupts, two timer interrupts and a serial port interrupt. Each of the interrupt sources can be individually enabled or disabled by setting or clearing a bit in the SFR named IE(interrupt enable). All the interrupts can be cleared at once to one of the priority levels by setting or clearing a bit in the SFR named ID. There is also an internal polling sequence that is made use of when interrupt requests of the same priority level occur simultaneously.

IE: Interrupt enables register

EA - ET2 ES ET1 EX1 ET0 EX0

Enable bit = 1 interrupt enabled

Enable bit = 0 disables bit

SYMBOL	POSITION	FUNCTION
EA	IE.7	Global enable /disable all Interrupts. If EA=0, no interrupts Will be Acknowledged. If EA=1, each input source is individually enabled or disabled by setting or clearing its enable bit.
-	IE.6	Undefined/resetted.
ET2	IE.5	Timer 2 enable bit.
ES	IE.4	Serial Port interrupt enable bit.
ET1	IE.3	Timer 1 interrupt enable bit.
EX1	IE.2	External interrupt 1 enable bit.
ET0	IE.1	Timer 0 interrupt enable bit.
EX0	IE.0	External interrupt 0 enable bit.

IP: Interrupt priority register

\- - PT2 PS PT1 PX1 PT0 PX0

Enable bit = 1 interrupt enabled.

Enable bit = 0 disables bit.

SYMBOL	POSITION	FUNCTION
-	IP.7	Reserved
-	IP.6	Reserved
PT2	IP.5	Timer 2 enable bit.
PS	IP.4	Serial Port interrupt enable bit.
PT1	IP.3	Timer 1 interrupt enable bit.
PX1	IP.2	External interrupt 1 enable bit.
PT0	IP.1	Timer 0 interrupt enable bit.
PX0	IP.0	External interrupt 0 enable bit.

TIMER/COUNTERS:

It has two 16 bit timer/counter registers. Timer 0and Timer 1, that can be used as timers or event counters. For each timer/counter register there is a control bit in SFR TMOD that selects the timer/counter function to be "Timer" or "counter".In addition to the timer/counter selection, each timer/counter has four operation modes from which to select, the operating systems 1 and 2 are same for both timer as well as counters. Mode 3 is different. The four operative modes are

i). Mode 0

ii). Mode 1

iii). Mode 2

iv). Mode 3

MEMORY CONFIGURATION:

Memory is an integral part of the microprocessor system. Whileexecuting a program the processor needs to access memory quite requently to read instruction codes and data stored in the memory.

Memory has certain signal requirements to write into and read from its registers. Similarly, microprocessor initiates a set of signals when it wants to read from or write into memory. The required signals are generated using an interfacing circuit.

PROCESSOR SECTION:

This system includes eight data lines (D0 - D7) and other Interfacing lines A0, RD, WR, CLK etc., The RD and WR signals are connected to RD and WR signals of the micro controller. The A0 line of the micro controller is connected to the address line of the micro controller. When A0 line is high the signals are interpreted as control words or status And when its low signals are interpreted as data.

2.2 ADC0809

8-Bit μP Compatible A/D Converters with 8-Channel Multiplexer:

GENERAL DESCRIPTION:

The analog to digital converter we used for our project is ADC0809.The ADC0809 data acquisition component is a monolithic CMOS device with an 8-bit analog-to-digital converter, 8-channel multiplexer and microprocessor compatible control logic. The 8-bit A/D converter uses successive approximation as the conversion technique. The converter features a high impedance chopper stabilized comparator, a 256R voltage divider with analog switch tree and a successive approximation register. The 8-channel multiplexer can directly access any of 8-single-ended analog signals.

The device eliminates the need for external zero and full-scale adjustments. Easy interfacing to microprocessors is provided by the latched and decoded multiplexer address inputs and latched TTL tri-state outputs.

The design of the ADC0809 has been optimized by incorporating the most desirable aspects of several A/D conversion techniques. The ADC0809 offers high speed, high accuracy, minimal temperature dependence, excellent long-term accuracy and repeatability, and consumes minimal power. These features make this device ideally suited to applications from process and machine control to Consumer and automotive applications.

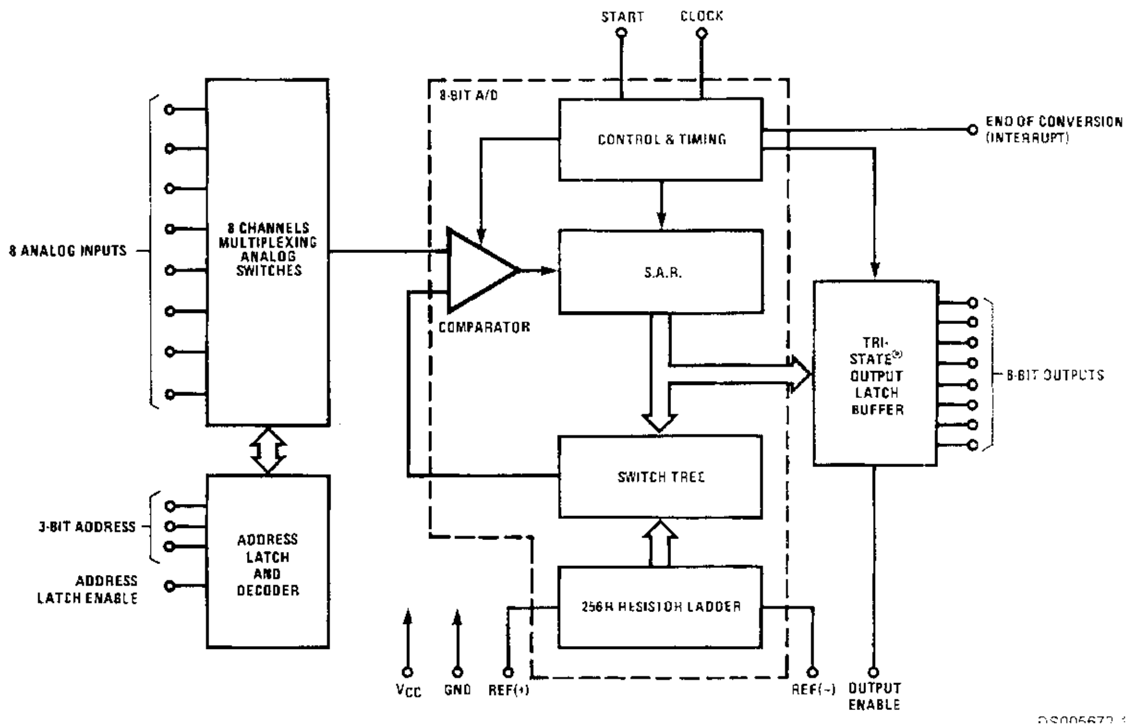
FEATURES:

- Easy interface to all microprocessors
- Operates ratiometrically or with 5 VDC or analog span adjusted Voltage reference
- No zero or full-scale adjust required
- 8-channel multiplexer with address logic
- 0V to 5V input range with single 5V power supply
- Outputs meet TTL voltage level specifications
- Standard hermetic or molded 28-pin DIP package
- 28-pin molded chip carrier package
- ADC0809 equivalent to MM74C949-1

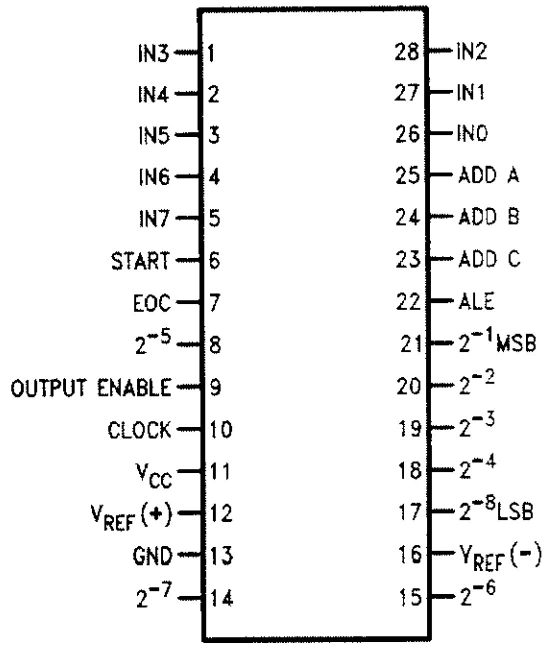
KEY SPECIFICATIONS:

Resolution	8 Bits
Total Unadjusted Error	± 1/2 LSB and ±1 LSB
Single Supply	5 VDC
Low Power	15 mW
Conversion Time	100 μs

BLOCK DIAGRAM:



CONNECTION DIAGRAM:



Dual-In-Line Package

FUNCTIONAL DESCRIPTION:

Multiplexer:

The device contains an 8-channel single-ended analog signal multiplexer. A particular input channel is selected by using the address decoder. Table shows the input states for the address lines to select any channel. The address is latched into the decoder on the low-to-high transition of the address latch enable signal.

TABLE:

SELECTED ANALOG CHANNEL	ADDRESS LINE		
	C	B	A
IN0	L	L	L
IN1	L	L	H
IN2	L	H	L
IN3	L	H	H
IN4	H	L	L
IN5	H	L	H
IN6	H	H	L
IN7	H	H	H

CONVERTER CHARACTERISTICS:

The Converter:

The heart of this single chip data acquisition system is its 8-bit analog-to-digital converter. The converter is designed to give fast, accurate, and repeatable conversions over a wide range of temperatures. The converter is partitioned into 3 major sections:

1. The 256R ladder network,
2. The successive approximation register, and
3. The comparator.

The converter's digital outputs are positive true.

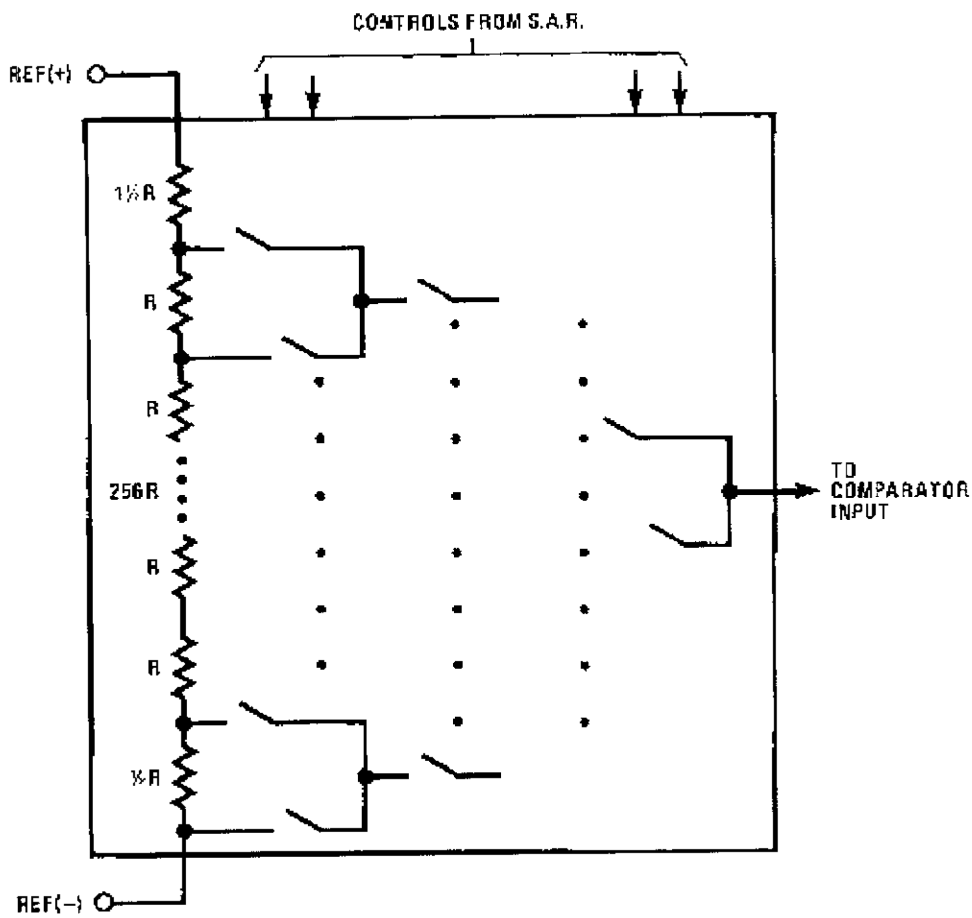
The 256R ladder network approach was chosen over the conventional R/2R ladder because of its inherent monotonicity, which guarantees no missing digital codes. Monotonicity is particularly important in closed loop feedback control systems. A non-monotonic relationship can cause oscillations that will be catastrophic for the system. Additionally, the 256R network does not cause load variations on the reference voltage. The bottom resistor and the top resistor of the ladder network in figures are not the same value as the remainder of the network. The difference in these resistors causes the output characteristic to be symmetrical with the zero and full-scale points of the transfer curve. The first output transition occurs when the analog signal has reached + 1/2 LSB and succeeding output transitions occur every 1 LSB later up to full-scale.

The successive approximation register (SAR) performs 8 iterations to approximate the input voltage. For any SAR type converter, n-iterations are required for an n-bit converter. In the ADC0809, the approximation technique is extended to 8 bits using the 256R network.

The A/D converter's successive approximation register (SAR) is reset on the positive edge of the start conversion (SC) pulse. The conversion is begun on the falling edge of the start conversion pulse. A conversion in process will be interrupted by receipt of a new start conversion pulse. Continuous conversion may be accomplished by tying the end-of-conversion (EOC) output to the SC input. End-of-conversion will go low between 0 and 8 clock pulses after the rising edge of start conversion.

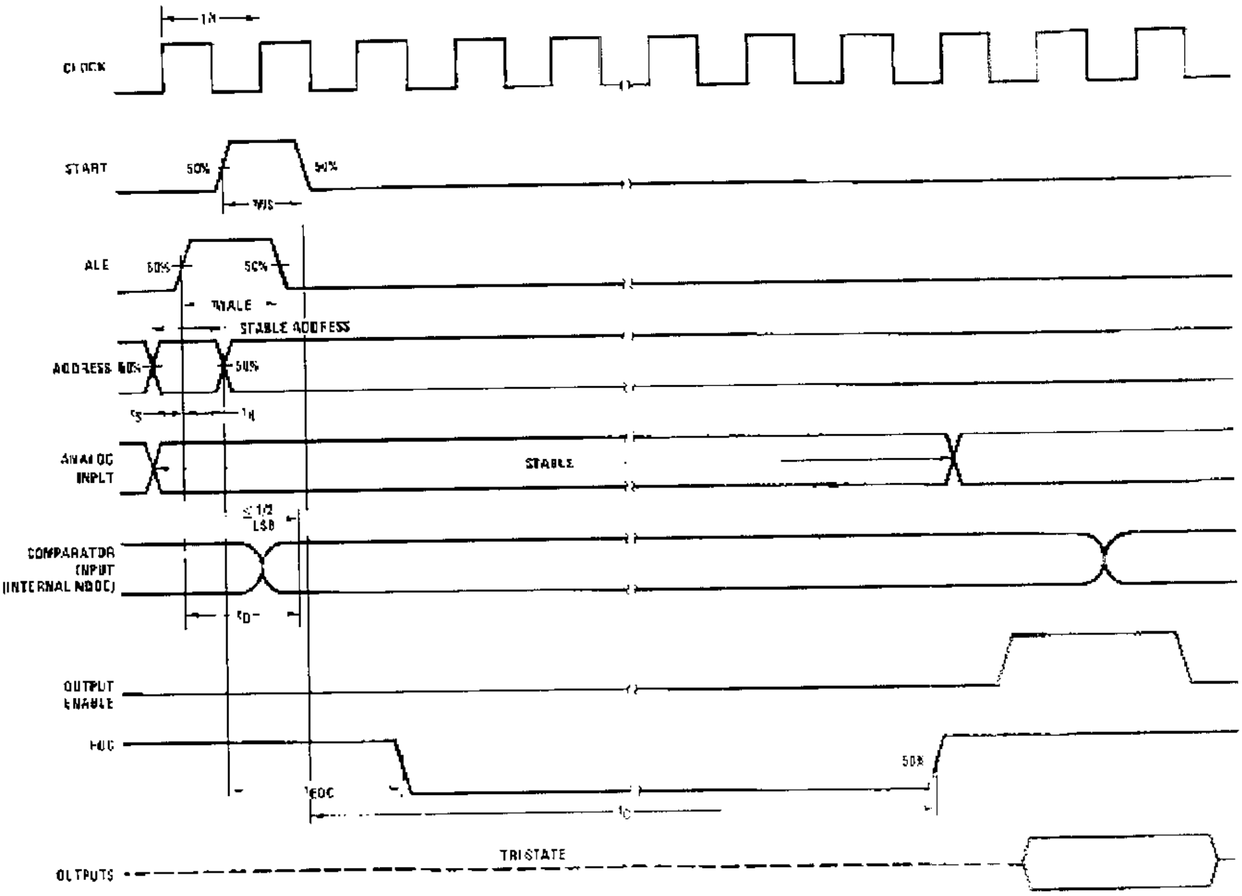
The most important section of the A/D converter is the comparator. It is this section which is responsible for the ultimate accuracy of the entire converter. It is also the comparator drift which has the greatest influence on the repeatability of the device.

FUNCTIONAL DESCRIPTION



Resistor Ladder and Switch Tree

TIMING DIAGRAM:



2.3 UT62256

32k x 8 bit low power CMOS SRAM

GENERAL DESCRIPTION:

The static random access memory (SRAM) used for our project is UT62256.It is a 262,144-bit low power CMOS static random access memory organized as 32,768 words by 8 bits. It is fabricated using high performance, high reliability CMOS technology.

The UT62256 is designed for high-speed and low power application. It is particularly well suited for battery back-up nonvolatile memory application. The UT62256 operates from a single 5Vpower supply and all inputs and outputs are fully TTL compatible.

FEATURES:

- Access time is 35/70ns (max.)
- Low power consumption:

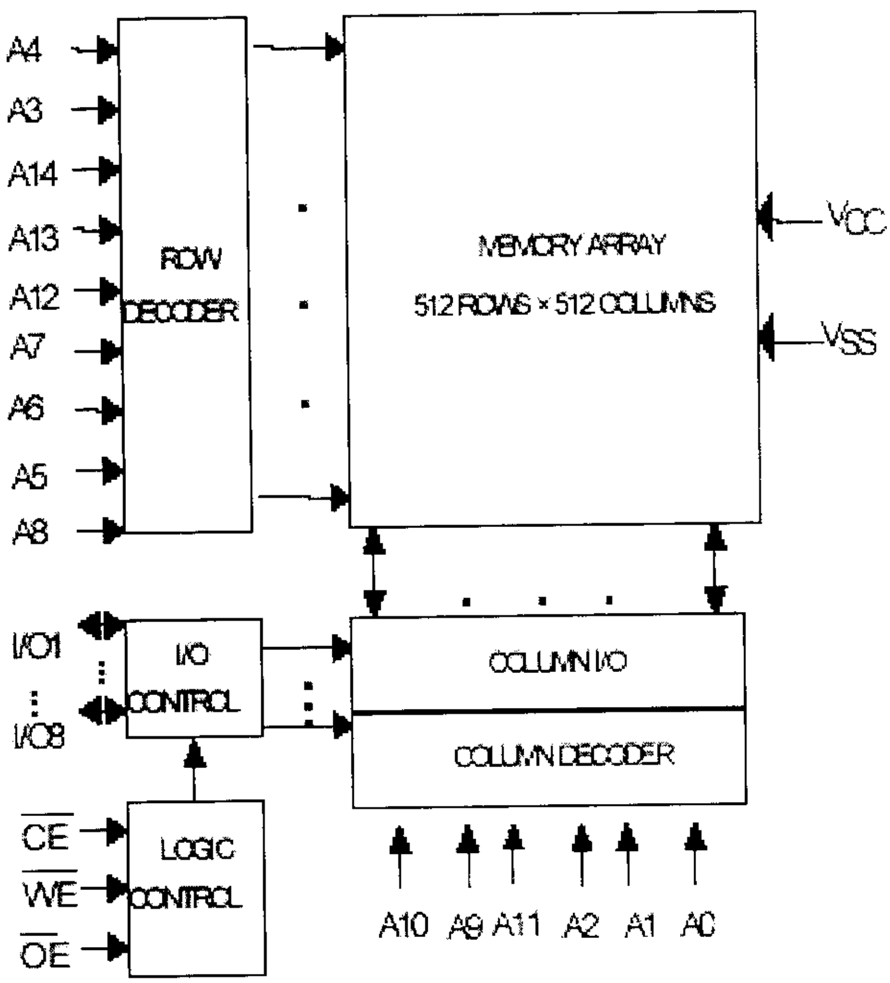
  Operating : 60/40 mA (typical.)

  Standby : 3mA (typical) normal

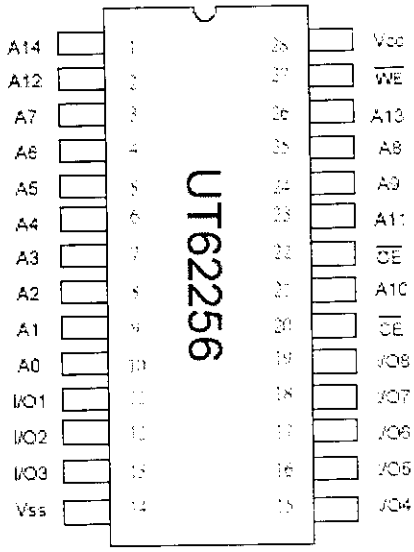
  1μA (typical) LL-version
- Single 5V power supply
- All inputs and outputs are TTL compatible
- Fully static operation
- Three state outputs
- Data retention voltage : 2V (min.)

➢ Package : 28-pin 600 mil PDIP
28-pin 330 mil SOP
28-pin 8x13.4mm STSOP

FUNCTIONAL BLOCK DIAGRAM:



PIN CONFIGURATION:



PIN DESCRIPTION:

SYMBOL	DESCRIPTION
A0 - A14	Address Inputs
I/O1 - I/O8	Data Inputs/Outputs
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
V_{CC}	Power Supply
V_{SS}	Ground

.

TRUTH TABLE:

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O OPERATION	SUPPLY CURRENT
Standby	H	X	X	High - Z	ISB, ISB1
Output Disable	L	H	H	High - Z	I_{CC}
Read	L	L	H	D_{OUT}	I_{CC}
Write	L	X	L	D_{IN}	I_{CC}

2.4. 74HC/HCT573

Octal D-type transparent latch

GENERAL DESCRIPTION:

The 74HC/HCT573 are high speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL).

The 74HC/HCT573 are octal D-type transparent latches featuring separate D-type inputs for each latch and 3-state outputs for bus oriented applications.

A latch enable (LE) input and an output enable (OE) input are common to all latches. The "573" consists of eight D-type transparent latches with 3-state true outputs. When LE is HIGH, data at the Dn inputs enter the latches. In this condition the latches are transparent, i.e. a latch output will change state each time its corresponding D-input changes.

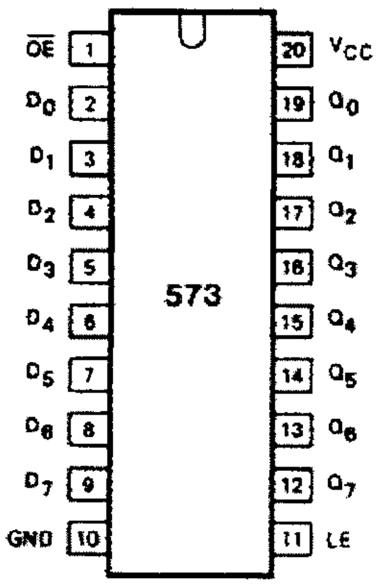
FEATURES:

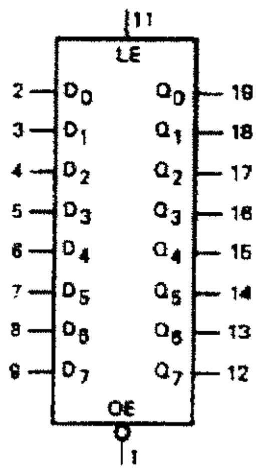
- Inputs and outputs on opposite sides of package allowing easy interface with microprocessors
- Useful as input or output port for microprocessors/ microcomputers
- 3-state non-inverting outputs for bus oriented applications
- Common 3-state output enable input
- Functionally identical to the "563"and "373"
- Output capability: bus driver
- ICC category: MSI

PIN DESCRIPTION

PIN NO	SYMBOL	NAME AND FUNCTION
2,3,4,5,6,7,8, 9	D0 to D7	Data inputs
11	LE	Latch Enable input (active HIGH)
1	OE	3-state Output Enable input (active LOW)
10	GND	Ground (0 V)
19, 18, 17, 16, 15, 14, 13,12	Q0 to Q7	3-state Latch outputs
20	VCC	Positive supply voltage

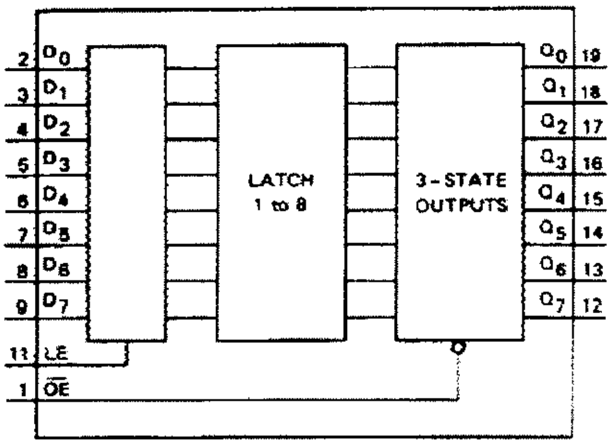
PIN CONFIGURATION:





Logic symbol

FUNCTIONAL DIAGRAM:



When LE is LOW the latches store the information that was present at the D-inputs a set-up time preceding the HIGH-to-LOW transition of LE.When OE is LOW, the contents of the 8 latches are available at the outputs. When OE is HIGH, the outputs go to the high impedance OFF-state. Operation of the OE input does not affect the state of the latches. The "573" is functionally identical to the "563" and "373", but the "563" has inverted outputs and the "373" has a different pin arrangement.

FUNCTIONAL TABLE:

OPERATING MODES	INPUTS			INTERNAL LATCHES	OUTPUTS
	$\overline{OE}$	LE	D_N		Q_0 to Q_7
enable and read register (transparent mode)	L L	H H	L H	L H	L H
latch and read register	L L	L L	l h	L H	L H
latch register and disable outputs	H H	L L	l h	L H	Z Z

2.5. MAX 232

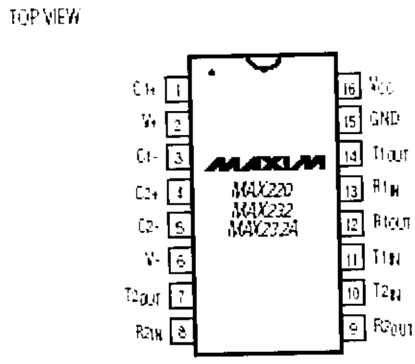
RS 232 drivers/receivers:

GENERAL DESCRIPTION:

Max 231 belongs to maxim family in which the line drivers/receivers are intended for all RS 232 communications interface and in particular for those applications where ±12 volt is not available. Since nearly all RS 232 applications need both line drivers and receivers, the family includes both receivers and the line drivers (transmitters) meet all EIA RS 232 specifications. The MAX 232 consists of three sections –the transmitter, the receiver and the charge pump DC-DC voltage converters.

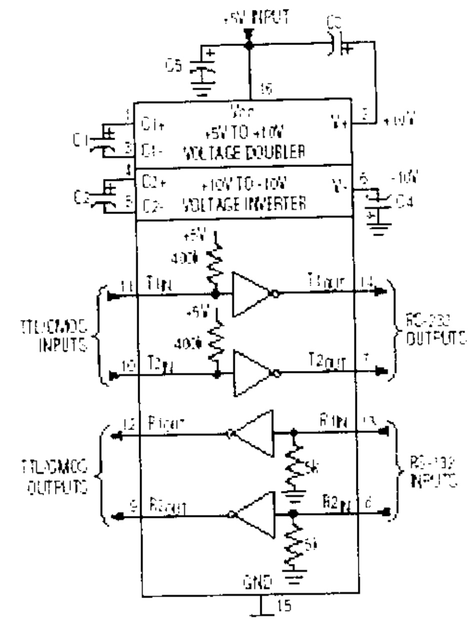
FEATURES:

- Operates from single 5 volts supply
- Meets all RS 232c and V.28 specifications
- Multiple drivers and receivers
- On board DC-DC converters
- ±9volts outputs swing with 5 volts supply
- Low power shut down < 1 μA (typical)
- Three state TTL/CMOS receivers outputs
- ±30 volts receiver input levels



DIP/SO

CAPACITANCE (μF)					
DEVICE	C1	C2	C3	C4	C5
MAX220	4.7	4.7	10	10	4.7
MAX232	1.0	1.0	1.0	1.0	1.0
MAX232A	0.1	0.1	0.1	0.1	0.1



DUAL CHARGE PUMP VOLTAGE CONVERTER:

The RS 232 drivers/receivers have on board charge pump voltage converters, which convert the ±5 volts input power to the ±10 volts needed to generate the RS 232 output levels. Two charge pump voltage converters perform this ±5 volt to ±10 volts conversion. The first uses capacitor C1 to double the +5 volts to +10 volts, storing the + 10 volts on the V+ output filter capacitor, C3.The second charge pump voltage converter uses capacitor C2 to invert the +10 volts to -10 volts, storing the -10 volts on the V- output filter capacitor, C4.A small amount of power may be drawn from the +10 volts (V+) and -10 volts (V-) outputs to power external circuitry.

DRIVER (TRANSMITTER) SECTION:

The transmitter or the line drivers are inverting level translators, which convert the CMOS/TTL input levels to RS 232 voltage levels. with +5 volts Vcc, the typical output voltage swing is ±9 volts when loaded with a nominal 5 kΩ input resistance of an RS 232 receiver. The output swing is guaranteed to meet the RS 232 specifications of ±5 volts minimum output swing under the worst case conditions of all transmitters during the 3 kΩ minimum allowable load impedance Vcc=4.5 volts and maximum operating ambient temperature. The open circuit output voltage swing in the transmitter is set to be from V-to V-.

The input thresholds are both CMOS/TTL compatible, with logic thresholds of about 25% of Vcc. The inputs of unused driver section can be left unconnected; an internal 400 kilo ohms input pull up resistor to Vcc will pull the inputs high, forcing the unused transmitter outputs low. The input pull up resistor source about 12 micro amps and the driver inputs should be driven high or open circuited to minimize power supply current in the slow down mode.

When in the low power shut down mode, the driver outputs are turned off and their leakage current is less than 1 micro amp with driver output pulled to ground .the driver output leakage remains less than 1 micro amps even if the transmitter output is back driven between 0 volts and Vcc- +6 volts. Below – 0.5 volts the transmitter is diode clamped to ground with 1kΩ series impedance. The transmitter is also zener clamped to approximately Vcc +6 volts, with a series impedance of 1 kΩ. As required by RS 232, the slew rate is limited to less than 30 volts/microseconds. This limits the maximum usable baud rate to 19200 bauds.

RECEIVER SECTION:

All but the MAX 230 and MAX 234 contain RS 232/V.28 receivers. These receivers convert the + 5 volts to + 15 volts RS 232 signals to 5 volts TTL/CMOS outputs. Since the RS 232c specifications define a voltage level greater than +3 volts as a zero, the receiver are inverting. These receivers are able to respond to both RS 232 levels and TTL level inputs. The receivers are protected against input over voltage upto +30 volts.

The lower threshold has a guaranteed value of 0.8 volts. This value is important in the sense that the receiver will have a logic one output if the receiver is not being driven. This is because the equipment containing the line driver is turned off or disconnected if the connecting cable has an open circuit or short circuit. In the other words the receiver implements type one interpretation of fault conditions. While or even a -3 volts receiver threshold would not give proper indication on the control lines such as DTR and DSR. The receiver on the other hand has a full 0.8 volts noise margin for detecting the power down or the cable connected states.

The receiver has a hysteresis of approximately of 0.5 volts with a minimum guaranteed hysteresis200 milli volts. This aid is obtaining clean output transitions even with slow rise and fall line input signals with moderate amount of noise and ringing. The propagations delays of the receivers are 350 nano seconds for negative going input signals and 650 nano seconds for positive going input signals.

2.6 RS232 STANDARD:

DCE AND DTE:

RS stands for Recommended standard. RS-232 was created for one purpose, to interface between Data Terminal Equipment (DTE) and Data Communications Equipment (DCE) employing serial binary data interchange.

The modems and instruments sending and receiving serial data are referred to as data communication equipment, or DCE, in the standard. The computer at the other end of the cable is referred to as data terminal equipment or DTE. A DTE has a plug and a DCE a socket. So as stated the DTE is the terminal or computer and the DCE is the modem or other communications device.

BAUD RATE:

RS-232 is a point-point communication standard with a maximum specified range of 75 feet. Speeds of over 115 KBaud are possible. High speeds can be problematic at longer distances but low speeds are quite reliable, even at several times the specified maximum range.

VOLTAGE LEVELS:

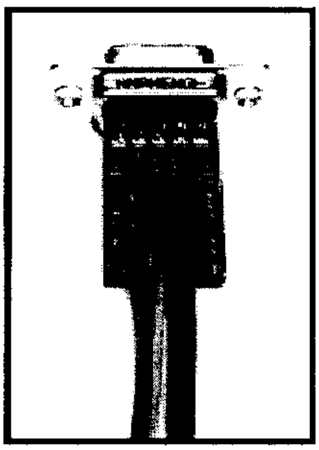
The standard specifies the output levels as being **-5 to -15 Volts for logical 1** and **+5 to +15 Volts for logical 0**, and the input levels as being **-3 to -15 Volts for logical 1** and **+3 to +15 Volts for logical 0**. Signaling is done using a minimum of 3 Lines (TXD, RXD, GND) and uses ±12VDC to represent the logic levels 0 and 1.The term TTL stand for Transistor-

Transistor Logic and refers to digital logic devices that use 0 and +5 Volts to represent the logic levels 0 and1 respectively. The RS-232 Driver allows a device designed for TTL signals (such as a microcontroller) to safely communicate with one designed for true RS-232 levels.

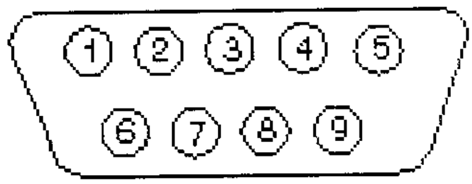
PIN DESCRIPTION:

Pin Name	Abbr.	Pin #	DCE	DTE
Data Carrier Detect	DCD	1	Output	Input
Receive Data	RXD	2	Output	Input
Transmit Data	TXD	3	Input	Output
Data Ground	GND	5		
Data Set Ready	DSR	6	Output	Input
Request To Send	RTS	7	Input	Output
Clear To Send	CTS	8	Output	Input
Ring Indicator	RI	9	Output	Input

RS 232 9-PIN CONNECTOR:



Wired configuration



TXD Transmitted Data:

Outgoing Data to a DCE. This is the serial encoded data sent from a computer to a modem to be transmitted over the telephone line.

RXD Received Data:

Incoming Data from a DCE. This is the serial encoded data received by a computer from a modem which has in turn received it over the telephone line.

DSR Data Set Ready:

Incoming handshaking signal. This should be set true by a modem whenever it is powered on. It can be read by the computer to determine that the modem is on line.

DTR Data Terminal Ready:

Outgoing handshaking signal. This should be set true by a computer whenever it is powered on. It can be read by the modem to determine that the computer is on line.

RTS Request to Send:

Outgoing flow control signal. This is set true by a computer when it wishes to transmit data.

CTS Clear To Send:

Incoming flow control signal. This is set true by a modem to allow the computer to transmit data. The standard envisaged that when a computer wished to transmit data it would set its RTS. The local modem would then arbitrate with the distant modem for use of the telephone line. If it succeeded it would set CTS and the computer would transmit data. The distant modem would use its CTS to prevent any transmission by the distant computer.

DCD Data Carrier Detect:

Incoming signal from a modem. This is set true by a modem when it detects the data carrier signal on the telephone line.

2.7. LM35

Precision Centigrade Temperature Sensors

GENERAL DESCRIPTION:

The Parameter we used for our data logging system for demonstration is temperature.LM35 series are precision integrated-circuit temperature sensors, whose output voltage is linearly proportional to the Celsius (Centigrade) temperature. The LM35 thus has an advantage over linear temperature sensors calibrated in° Kelvin, as the user is not required to subtract a large constant voltage from its output to obtain convenient Centigrade scaling.

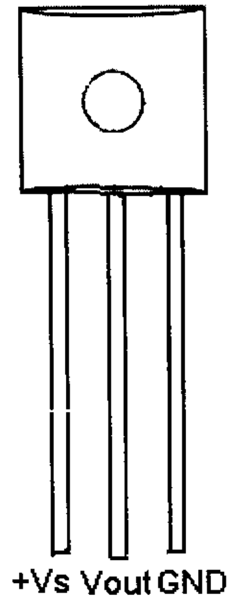
The LM35 does not require any external calibration or trimming to provide typical accuracies of ± 1 /4 °Cat room temperature and ± 3 /4 °C over a full -55 to +150°Ctemperature range. Low cost is assured by trimming and calibration at the wafer level. TheLM35'slowoutputimpedance, linear output, and precise inherent calibration make interfacing to readout or control circuitry especially easy. It can be used with single power supplies, or with plus and minus supplies. As it draws only 60 μA from its supply, it has very low self-heating, less than 0.1°C in still air.

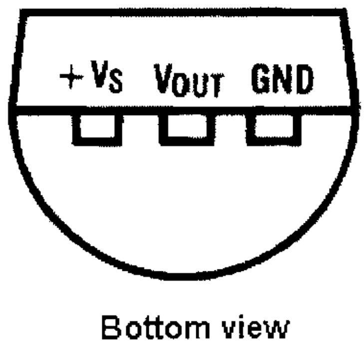
The LM35 is rated to operate over a -55° to +150°C temperature range, while the LM35C is rated for a -40° to +110°C range (-10°with improved accuracy). The LM35 series is available pack-aged in hermetic TO-46 transistor packages, while theLM35C, LM35CA, and LM35D are also available in the plastic TO-92 transistor package. The LM35D is also available in an 8-lead surface mount small outline package and a plastic TO-220 package.

FEATURES:

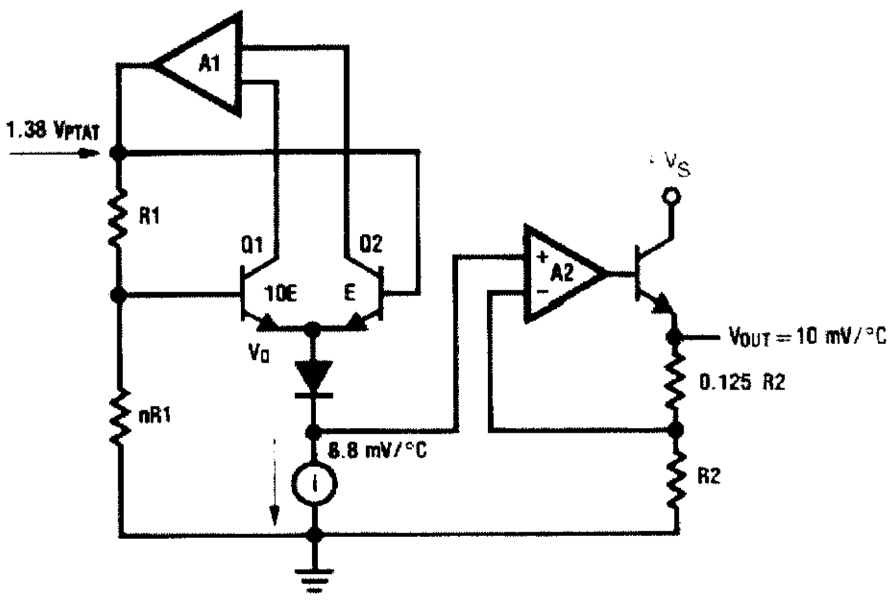
- Calibrated directly in ° Celsius (Centigrade)
- Linear + 10.0 mV/°C scale factor
- 0.5°C accuracy guarantee able (at +25°C)
- Rated for full -55° to +150°C range
- Suitable for remote applications
- Low cost due to wafer-level trimming
- Operates from 4 to 30 volts
- Less than 60 μA current drain
- Low self-heating, 0.08°C in still air
- Nonlinearity only ± 1 /4 °C typical
- Low impedance output, 0.1 W for 1 mA load

PIN DIAGRAM:





BLOCK DIAGRAM:



2.8. LM308 OPERATIONAL AMPLIFIER

GENERAL DESCRIPTION:

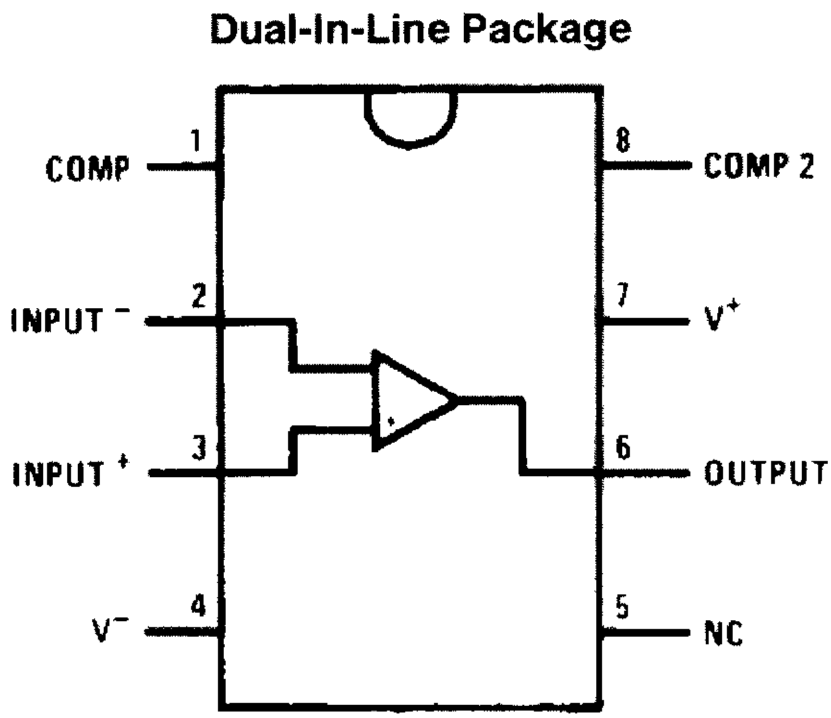
The output from the sensor needs to be amplified by a factor of 2.The LM308 series are precision operational amplifiers which meets this specification. They are amplifiers having specifications a factor of ten better than FET amplifiers over a -55°C to+125°C temperature range. The devices operate with supply voltages from ±2V to ±20V and have sufficient supply rejection to use unregulated supplies.

The low current error of the LM108 series makes possible many designs those are not practical with conventional amplifiers. In fact, it operates from 10 MΩ source resistances, introducing less error than devices like the 709 with 10 kΩ sources. Integrators with drifts less than 500 μV/second analog time delays in excess of one hour can be made using capacitors no larger than 1 μF. The LM308 is guaranteed from 0°C to+70°C.

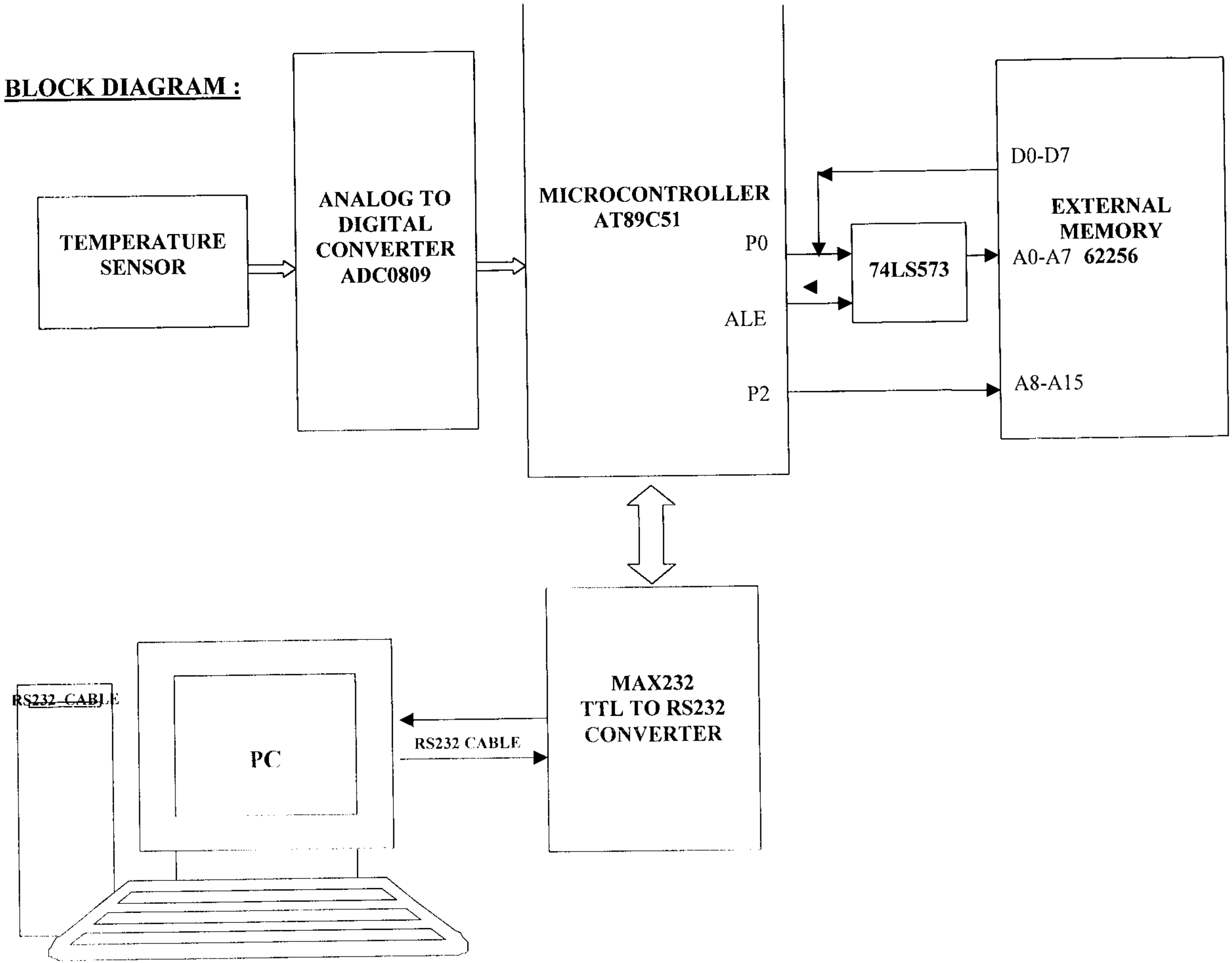
FEATURES:

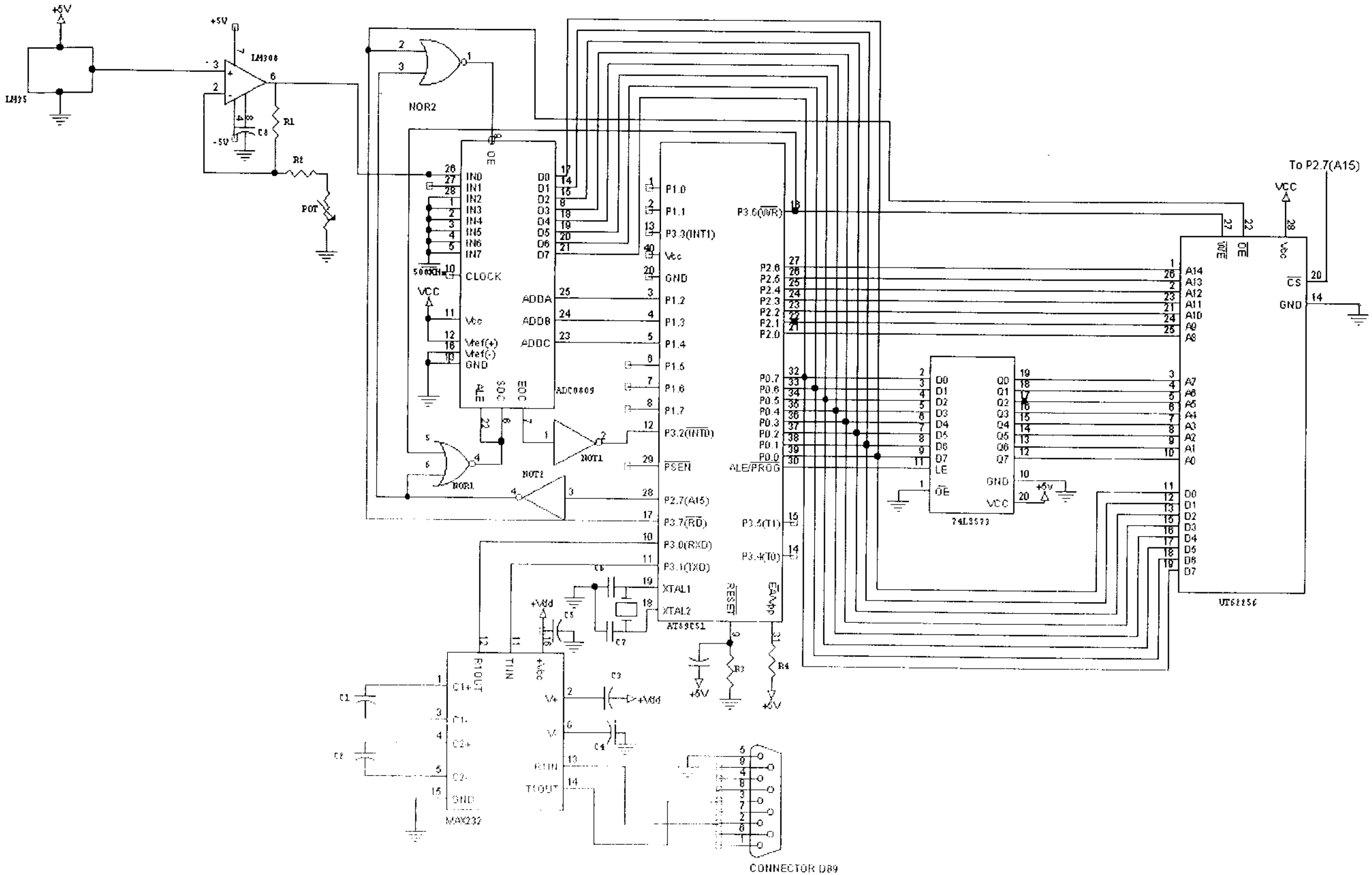
- Maximum input bias current of 3.0 nA over temperature
- Offset current less than 400 pA over temperature
- Supply current of only 300 μA, even in saturation
- Guaranteed drift characteristics

CONNECTION DIAGRAM:



BLOCK DIAGRAM :




LM35
LM308
R1
R2
POT
C8
NOR2
NOR1
NOT1
NOT2
ADC0809
AT89C51
74LS373
UT62256
MAX232
CONNECTOR D89
To P2.7(A15)
C1
C2
C3
C4
C5
C6
C7
R3
R4

IMPLEMENTATION

The main purpose of this project is to collect the data from any type of sensor for certain duration of time and is stored in an external RAM and later being retrieved for analysis purpose. The working and major connections to be given for each component are described briefly as follows:

LM 35:

The LM35 is an integrated-circuit temperature sensor. It can be glued or cemented to a surface and its temperature will be within about 0.01°C of the surface temperature. When +5 volts is given to the Vs pin and the GND pin grounded, LM35 starts to sense the surrounding temperature and produces the corresponding output in voltage, from the Vout pin. Usually the voltages will be in milli-volts. This output should be fed to an amplifier before being given to the ADC.

LM398:

The LM308 is a precision operational amplifier having a factor of ten better than FET amplifiers over a -55C to+125C temperature range.The low current error of the LM108 series makes possible many designs those are not practical with conventional amplifiers. It has been designed in such a way that it amplifies the given input by a factor of 2. This output is now fed to the ADC.

ADC0809:

The output of the op-amp is fed to one of the 8-input channels of the ADC. The selection of the input channel depends upon the three pins ADD A, ADD B, ADD C. These pins are given to the port pins (P1.2, P1.3, and P1.4, as in our case). In our project, the interfacing between ADC and microcontroller is done by memory-mapping, i.e., ADC is assigned an address (for e.g. 8000), whenever this address is called the ADC becomes selected. We had designed an astable multivibrator of 500 KHz using 555 timer which is given as the clock input .Moreover the +Vref is given as +5Volts and -Vref as GND. The output from the WR pulse and A15 of the controller are given as inputs to a NOR gate whose output is fed to both ALE and SOC. Whenever an EOC(End Of Conversion)signal it is fed as external interrupt to the INT0 pin. Also the output from the RD pulse and A15 are given as inputs to another NOR gate whose output is fed to OE (Output Enable).

AT89c51:

Initially the controller is programmed to choose the correct input channel. Then the ADC is called in such a way that WR pulse and A15 are generated .A15 is inverted before being fed as input to the NOR gate. At this particular time, the output of NOR gate becomes high, which is given to the SOC and ALE. Now the start of conversion on the ADC takes place, after the completion of the conversion, an EOC (End Of Conversion) is generated and is given as external interrupt to the INT0 pin, the controller automatically calls the interrupt sub-routine where again the ADC is again called in such a way that RD pulse and A15 are generated, this ultimately makes the output to get enabled and this value is stored in a temporary register called DAT within the controller. Also the time of interval for which the data must be collected can be programmed as our convenience. In this program we had taken the interval to be one minute.

RAM62256:

The interfacing between controller and external RAM is also done by memory mapping. After the data is being put in the temporary register DAT, the external RAM is called by its first location and the data gets moved from DAT to the first location of the RAM and the address pointer gets incremented. Now after one minute, next data is stored in this location and this goes on until the last location comes and stores the data. The latch 573 is used to demuliplex the lower byte address lines and data lines. The ALE pin of the controller is given as latch enable and its output is always enabled. The stored data must be retrieved in a computer through an RS-232 cable, so that these data can be analyzed using LABVIEW.

MAX232:

For the serial communication to take place between controller and PC and RS 232 cable to be connected. But the TTL logic level should be converted into RS232 logic level or vice-versa and hence we use MAX 232. The capacitors are connected for on-board DC-DC converters.

Capacitor C1 - is used to double the +5 volts to +10 volts,

Capacitor C3 - +10 volts is stored on the V+ output filter with the help of C1,

Capacitor C2 - is used to invert the +10 volts to -10 volts,

Capacitor C4 - -10 Volts is stored on the V- output filter.

A small amount of power may be drawn from the +10 volts (V+) and -10 volts (V-) outputs to power external circuitry. The RXD and TXD pin of the controller is connected to the R1OUT and T1IN pins respectively. The R2IN and T2OUT are connected to the corresponding pins of RS 232.

RS232:

RS 232 is used to interface the Data Terminal Equipment (DTE) and Data Communications Equipment (DCE) employing serial binary data interchange. Hence R2IN and T2OUT are connected to the TXD (transmit data) and RXD (receive data). This is now connected to the serial port of the computer

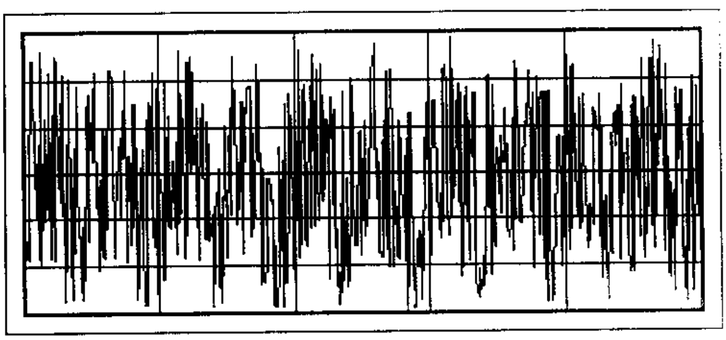
DATA ANALYSIS

Digital signals are everywhere in the world around us. Telephone companies use digital signals to represent the human voice. Radio, TV, and hi-fi sound systems are all gradually converting to the digital domain because of its superior fidelity, noise reduction, and signal processing flexibility. Data is transmitted from satellites to earth ground stations in digital form. NASA's pictures of distant planets and outer space are often processed digitally to remove noise and extract useful information. Economic data, census results, and stock market prices are all available in digital form. Because of the many advantages of digital signal processing, analog signals are also converted to digital form before they are processed with a computer.

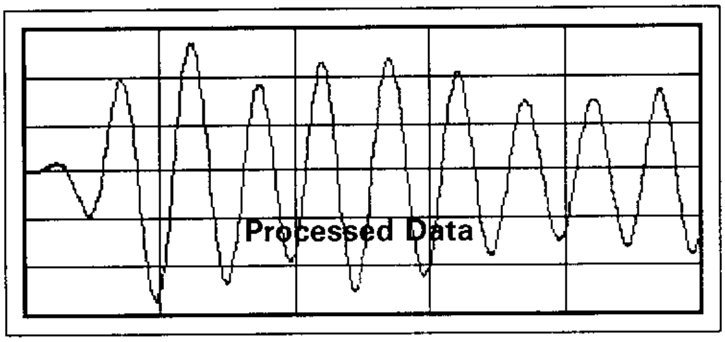
THE IMPORTANCE OF DATA ANALYSIS

The importance of integrating analysis libraries into engineering stations is that the raw data, as shown Figure, does not always immediately convey useful information. Often you must transform the signal, remove noise disturbances, correct for data corrupted by faulty equipment, or compensate for environmental effects, such as temperature and humidity.

Raw Data

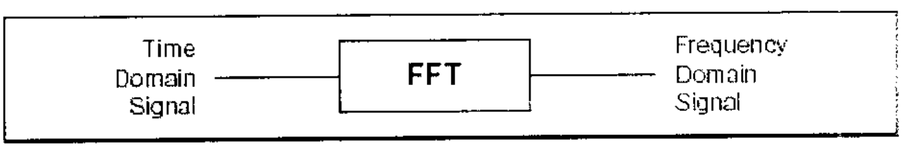


By analyzing and processing the digital data, you can extract the useful information from the noise and present it in a form more comprehensible than the raw data, as shown in Figure .The LabVIEW block diagram programming approach and the extensive set of LabVIEW Measurement Analysis simplify the development of analysis applications. The LabVIEW Measurement Analysis gives you the most recent data analysis techniques that you can wire together.

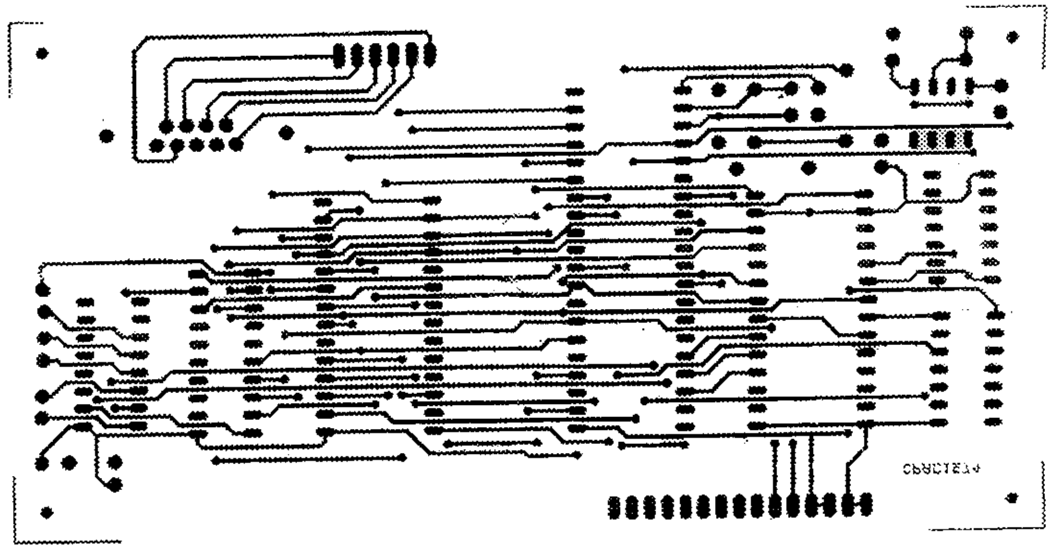


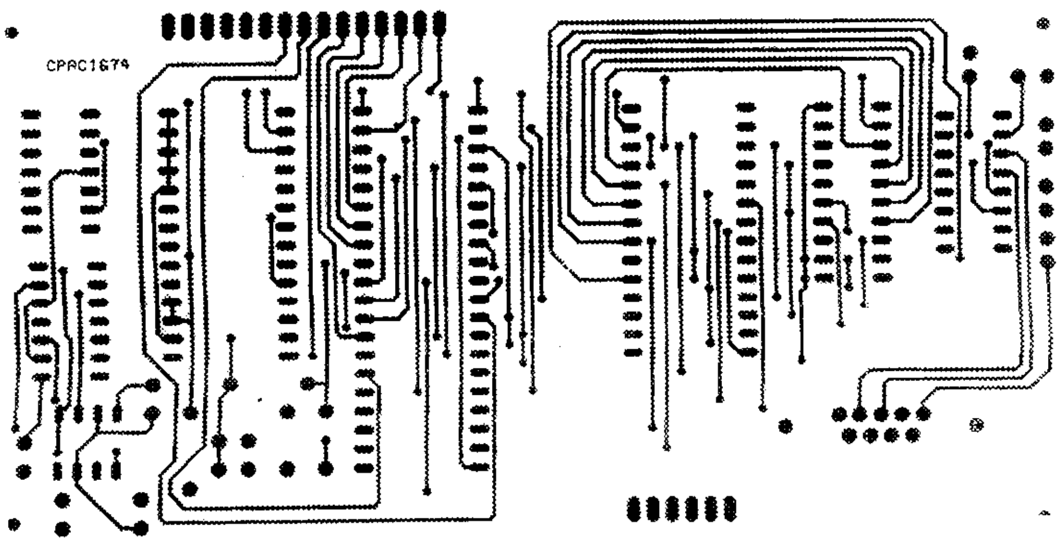
FREQUENCY ANALYSIS:

Fourier's theorem states that any waveform in the time domain can be represented by the weighted sum of sines and cosines. The same waveform can then be represented in the frequency domain as a pair of amplitude and phase values at each component frequency. You can generate any waveform by adding up sine waves, each with a particular amplitude and phase. The Fast Fourier Transform (FFT) is a fast version of the Discrete Fourier Transform (DFT). The DFT transforms digital time domain signals into the digital frequency domain.



3.4 PCB DESIGN





4.1. KEIL SOFTWARE — C*X*51 COMPILER

The C programming language is general-purpose, programming language that provides code efficiency, elements of structured programming, and a rich set of operators. C is not a complex language and is not designed for any one particular area of application. Its generality combined with its absence of restrictions, makes a convenient and effective programming solution for a wide variety of software tasks. Many applications can be solved more easily and efficiently with C than with other more specialized languages.

The **C*x*51** Optimizing C Compiler is a complete implementation of the American National Standards Institute (ANSI) standard for the C language. **C*x*51** is not a universal C compiler adapted for the 8051 target. It is a ground-up implementation dedicated to generating extremely fast and compact code for the8051 microprocessor. **C*x*51** provides you the flexibility of programming in C and the code efficiency and speed of assembly language. The C language on its own is not capable of performing operations (such as input and output) that would normally require intervention from the operating system. Instead, these capabilities are provided as part of the standard library. Because these functions are separate from the language itself, C is especially suited for producing code that is portable across a wide number of platforms. Since **C*x*51** is a cross compiler, some aspects of the C programming language and standard libraries are altered or enhanced to address the peculiarities of an embedded target processor.

4.2. LabVIEW

LabVIEW (**L**aboratory **V**irtual **I**nstrument **E**ngineering **W**orkbench) is a development environment based on graphical programming. LabVIEW uses terminology, icons, and ideas familiar to technicians, scientists, and engineers, and relies on graphical symbols rather than textual language to describe programming actions .In contrast to text-based programming languages, where instructions determine program execution, LabVIEW uses dataflow programming, where the flow of data determines execution.

In LabVIEW, we can build a user interface by using a set of tools and objects. The user interface is known as the front panel. We can then add code using graphical representations of functions to control the front panel objects. The block diagram contains this code. In some ways, the block diagram resembles a flowchart. LabVIEW is integrated fully for communication with hardware such as GPIB, VXI, RS-232, RS-485, and plug-in data acquisition boards. LabVIEW also has built-in libraries for using software standards such as TCP/IP Networking and ActiveX.

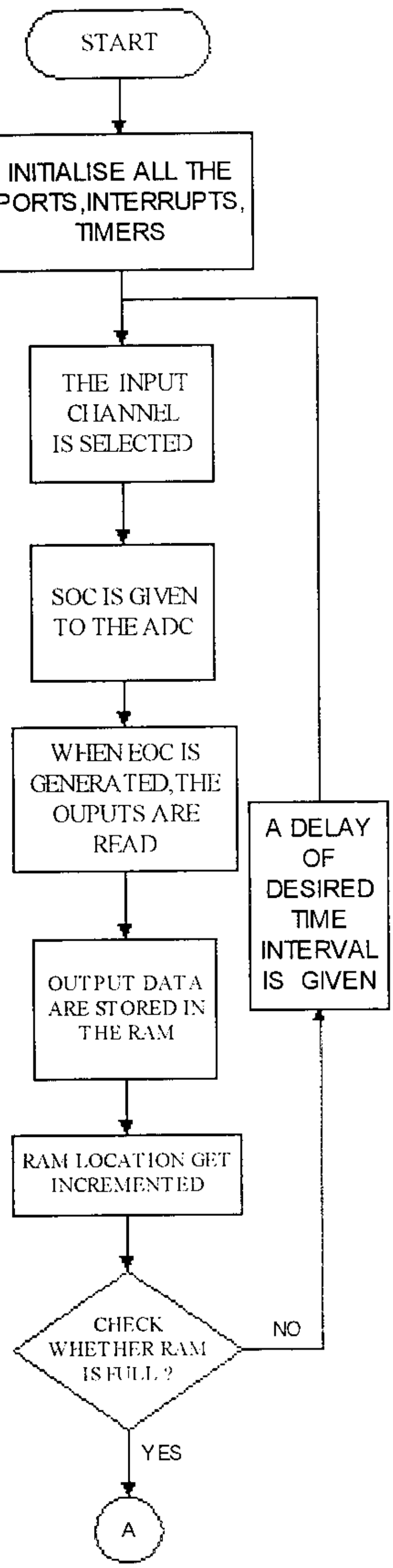
LabVIEW programs are called virtual instruments, or VIs, because their appearance and operation imitate physical instruments, such as oscilloscopes and multimeters. Every VI uses functions that manipulate input from the user interface or other sources and display that information or move it to other files or other computers.

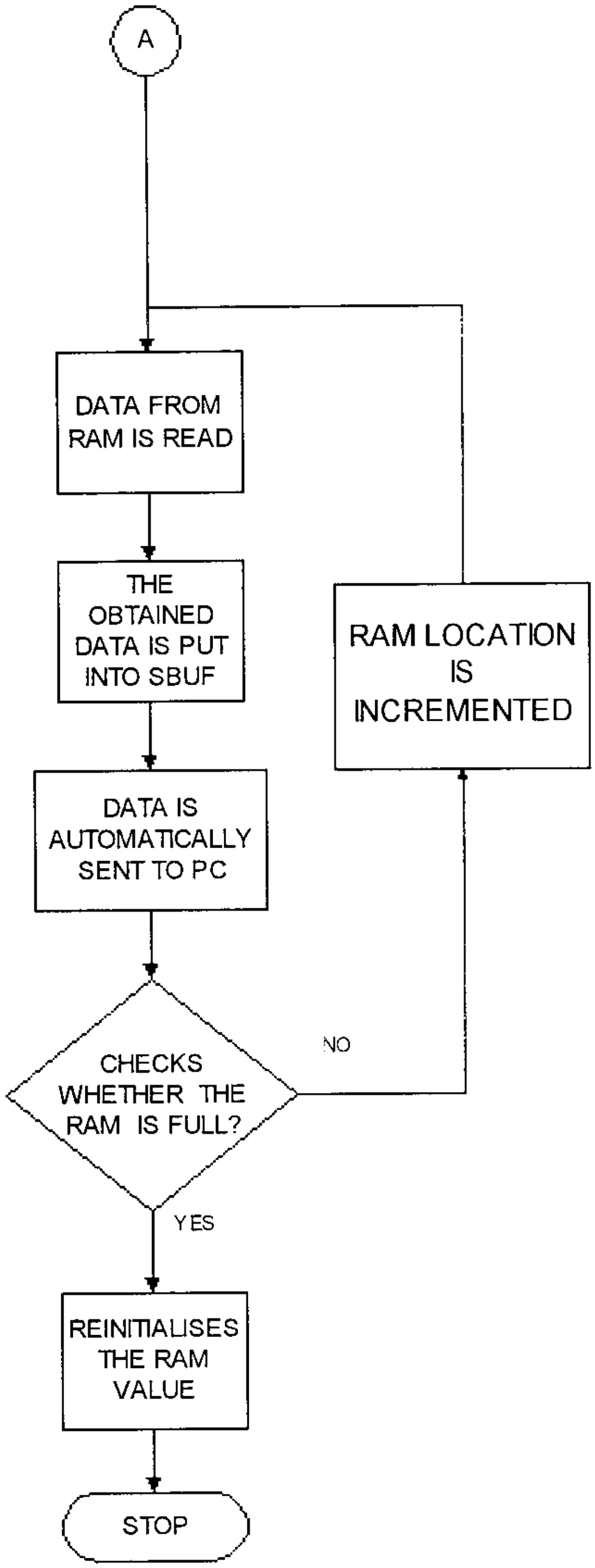
A VI contains the following three components:

- Front panel-Serves as the user interface.

- Block diagram-Contains the graphical source code that defines the functionality of the VI.

- Icon and connector pane-Identifies the VI so that you can use the VI in another VI. A VI within another VI is called a subVI. A subVI corresponds to a subroutine in text-based programming languages.


START
INITIALISE ALL THE PORTS,INTERRUPTS, TIMERS
THE INPUT CHANNEL IS SELECTED
SOC IS GIVEN TO THE ADC
WHEN EOC IS GENERATED,THE OUPUTS ARE READ
OUTPUT DATA ARE STORED IN THE RAM
RAM LOCATION GET INCREMENTED
CHECK WHETHER RAM IS FULL ?
NO
A DELAY OF DESIRED TIME INTERVAL IS GIVEN
YES
A


A
DATA FROM RAM IS READ
THE OBTAINED DATA IS PUT INTO SBUF
DATA IS AUTOMATICALLY SENT TO PC
CHECKS WHETHER THE RAM IS FULL?
NO
RAM LOCATION IS INCREMENTED
YES
REINITIALISES THE RAM VALUE
STOP

5.2 MICROCONTROLLER ALP CODING

```
0x0000    020800    LJMP    C:0800
0x0003    020959    LJMP    extr_interrupt(C:0959)
0x0006    00        NOP
0x0007    00        NOP
0x0008    00        NOP
0x0009    00        NOP
0x000A    00        NOP
0x000B    0209A0    LJMP    Timer0_interrupt(C:09A0)
0x000E    00        NOP

0x0800    787F      MOV     R0,#0x7F
0x0802    E4        CLR     A
0x0803    F6        MOV     @R0,A
0x0804    D8FD      DJNZ    R0,C:0803
0x0806    758120    MOV     SP(0x81),#0x20
0x0809    020847    LJMP    C:0847
0x080C    02088C    LJMP    main(C:088C)
0x080F    E4        CLR     A
0x0810    93        MOVC    A,@A+DPTR
0x0811    A3        INC     DPTR
0x0812    F8        MOV     R0,A
0x0813    E4        CLR     A
0x0814    93        MOVC    A,@A+DPTR
0x0815    A3        INC     DPTR
0x0816    4003      JC      C:081B
0x0818    F6        MOV     @R0,A
0x0819    8001      SJMP    C:081C
0x081B    F2        MOVX    @R0,A
0x081C    08        INC     R0
0x081D    DFF4      DJNZ    R7,C:0813
0x081F    8029      SJMP    C:084A
0x0821    E4        CLR     A
0x0822    93        MOVC    A,@A+DPTR
0x0823    A3        INC     DPTR
0x0824    F8        MOV     R0,A
0x0825    5407      ANL     A,#0x07
0x0827    240C      ADD     A,#dat(0x0C)
0x0829    C8        XCH     A,R0
0x082A    C3        CLR     C
0x082B    33        RLC     A
0x082C    C4        SWAP    A
0x082D    540F      ANL     A,#ct(0x0F)
0x082F    4420      ORL     A,#0x20
0x0831    C8        XCH     A,R0
0x0832    83        MOVC    A,@A+PC
0x0833    4004      JC      C:0839
0x0835    F4        CPL     A
0x0836    56        ANL     A,@R0
0x0837    8001      SJMP    C:083A
0x0839    46        ORL     A,@R0
0x083A    F6        MOV     @R0,A
0x0833    DFE4      DJNZ    R7,C:0821
```

```
0x083D    800B      SJMP    C:084A
0x083F    0102      AJMP    C:0802
0x0841    04        INC     A
0x0842    08        INC     R0
0x0843    102040    JBC     0x24.0,C:0886
0x0846    8090      SJMP    C:07D8
0x0848    09        INC     R1
0x0849    72E4      ORL     C,0xE0.4
0x084B    7E01      MOV     R6,#0x01
0x084D    93        MOVC    A,@A+DPTR
0x084E    60BC      JZ      C:080C
0x0850    A3        INC     DPTR
0x0851    FF        MOV     R7,A
0x0852    543F      ANL     A,#0x3F
0x0854    30E509    JNB     0xE0.5,C:0860
0x0857    541F      ANL     A,#0x1F
0x0859    FE        MOV     R6,A
0x085A    E4        CLR     A
0x085B    93        MOVC    A,@A+DPTR
0x085C    A3        INC     DPTR
0x085D    6001      JZ      C:0860
0x085F    0E        INC     R6
0x0860    CF        XCH     A,R7
0x0861    54C0      ANL     A,#0xC0
0x0863    25E0      ADD     A,ACC(0xE0)
0x0865    60A8      JZ      C:080F
0x0867    40B8      JC      C:0821
0x0869    E4        CLR     A
0x086A    93        MOVC    A,@A+DPTR
0x086B    A3        INC     DPTR
0x086C    FA        MOV     R2,A
0x086D    E4        CLR     A
0x086E    93        MOVC    A,@A+DPTR
0x086F    A3        INC     DPTR
0x0870    F8        MOV     R0,A
0x0871    E4        CLR     A
0x0872    93        MOVC    A,@A+DPTR
0x0873    A3        INC     DPTR
0x0874    C8        XCH     A,R0
0x0875    C582      XCH     A,DPL(0x82)
0x0877    C8        XCH     A,R0
0x0878    CA        XCH     A,R2
0x0879    C583      XCH     A,DPH(0x83)
0x087B    CA        XCH     A,R2
0x087C    F0        MOVX    @DPTR,A
0x087D    A3        INC     DPTR
0x087E    C8        XCH     A,R0
0x087F    C582      XCH     A,DPL(0x82)
0x0881    C8        XCH     A,R0
0x0882    CA        XCH     A,R2
0x0883    C583      XCH     A,DPH(0x83)
0x0885    CA        XCH     A,R2
0x0886    DFE9      DJNZ    R7,C:0871
0x0888    DEE7      DJNZ    R6,C:0871
0x088A    80BE      SJMP    C:084A
```

```
0x088C     1209BF    LCALL    initialise_sfr(C:09BF)
0x088F     1209C6    LCALL    init_timer(C:09C6)
0x0892     758811    MOV      TCON(0x88),#a(0x11)
0x0895     12098A    LCALL    initialise(C:098A)

C:0x0898   E512      MOV      A,s(0x12)
C:0x089A   70FC      JNZ      C:0898
C:0x089C   E513      MOV      A,0x13
C:0x089E   24FE      ADD      A,#0xFE
C:0x08A0   604E      JZ       C:08F0
C:0x08A2   04        INC      A
C:0x08A3   70F3      JNZ      C:0898

C:0x08A5   E509      MOV      A,0x09
C:0x08A7   4508      ORL      A,tcount(0x08)
C:0x08A9   7017      JNZ      C:08C2

C:0x08AB   750803    MOV      tcount(0x08),#0x03
C:0x08AE   750994    MOV      0x09,#0x94

C:0x08B1   C294      CLR      chs3(0x90.4)
C:0x08B3   C293      CLR      chs2(0x90.3)
C:0x08B5   C292      CLR      chs1(0x90.2)

C:0x08B7   850B82    MOV      DPL(0x82),0x0B
C:0x08BA   850A83    MOV      DPH(0x83),adc(0x0A)
C:0x08BD   F0        MOVX     @DPTR,A

C:0x08BE   C2A7      CLR      a15(0xA0.7)

C:0x08C0   D2B2      SETB     aa(0xB0.2)

C:0x08C2   E511      MOV      A,a(0x11)
C:0x08C4   601F      JZ       C:08E5

C:0x08C6   C2A7      CLR      a15(0xA0.7)

C:0x08C8   E50E      MOV      A,0x0E
C:0x08CA   2510      ADD      A,0x10
C:0x08CC   F582      MOV      DPL(0x82),A
C:0x08CE   E50D      MOV      A,ram(0x0D)
C:0x08D0   350F      ADDC     A,ct(0x0F)
C:0x08D2   F583      MOV      DPH(0x83),A
C:0x08D4   E50C      MOV      A,dat(0x0C)
C:0x08D6   F0        MOVX     @DPTR,A

C:0x08D7   1209B0    LCALL    wr_time(C:09B0)

C:0x08DA   0510      INC      0x10
C:0x08DC   E510      MOV      A,0x10
C:0x08DE   7002      JNZ      C:08E2
C:0x08E0   050F      INC      ct(0x0F)

C:0x08E2   E4        CLR      A
C:0x08E3   F511      MOV      a(0x11),A
```

```
C:0x08E5    3000B0    JNB     b(0x20.0),C:0898
C:0x08E8    751200    MOV     s(0x12),#0x00
C:0x08EB    751302    MOV     0x13,#0x02

C:0x08EE    80A8      SJMP    C:0898

C:0x08F0    3000A5    JNB     b(0x20.0),C:0898

C:0x08F3    C2A7      CLR     a15(0xA0.7)

C:0x08F5    050E      INC     0x0E
C:0x08F7    E50E      MOV     A,0x0E
C:0x08F9    AE0D      MOV     R6,ram(0x0D)
C:0x08FB    7002      JNZ     C:08FF
C:0x08FD    050D      INC     ram(0x0D)
C:0x08FF    14        DEC     A
C:0x0900    F582      MOV     DPL(0x82),A
C:0x0902    8E83      MOV     DPH(0x83),R6
C:0x0904    E0        MOVX    A,@DPTR
C:0x0905    F50C      MOV     dat(0x0C),A

C:0x0907    F599      MOV     SBUF(0x99),A

C:0x0909    12093C    LCALL   delay(C:093C)

C:0x090C    808A      SJMP    C:0898

C:0x090E    C0E0      PUSH    ACC(0xE0)
C:0x0910    C0D0      PUSH    PSW(0xD0)

C:0x0912    309918    JNB     TI(0x98.1),C:092D

C:0x0915    E510      MOV     A,0x10
C:0x0917    450F      ORL     A,ct(0x0F)
C:0x0919    600A      JZ      C:0925
C:0x091B    E510      MOV     A,0x10
C:0x091D    1510      DEC     0x10
C:0x091F    700C      JNZ     C:092D
C:0x0921    150F      DEC     ct(0x0F)
C:0x0923    8008      SJMP    C:092D

C:0x0925    C200      CLR     b(0x20.0)
C:0x0927    751200    MOV     s(0x12),#0x00
C:0x092A    751301    MOV     0x13,#0x01

C:0x092D    309807    JNB     RI(0x98.0),C:0937
C:0x0930    E599      MOV     A,SBUF(0x99)
C:0x0932    B40102    CJNE    A,#0x01,C:0937
C:0x0935    D200      SETB    b(0x20.0)

C:0x0937    D0D0      POP     PSW(0xD0)
C:0x0939    D0E0      POP     ACC(0xE0)
C:0x093B    32        RETI
```

```
C:0x093C    E4        CLR     A
C:0x093D    FF        MOV     R7,A
C:0x093E    FE        MOV     R6,A

C:0x093F    E4        CLR     A
C:0x0940    FD        MOV     R5,A
C:0x0941    FC        MOV     R4,A
C:0x0942    0D        INC     R5
C:0x0943    BD0001    CJNE    R5,#0x00,C:0947
C:0x0946    0C        INC     R4
C:0x0947    ED        MOV     A,R5
C:0x0948    640A      XRL     A,#adc(0x0A)
C:0x094A    4C        ORL     A,R4
C:0x094B    70F5      JNZ     C:0942
C:0x094D    0F        INC     R7
C:0x094E    BF0001    CJNE    R7,#0x00,C:0952
C:0x0951    0E        INC     R6
C:0x0952    BE13EA    CJNE    R6,#0x13,C:093F
C:0x0955    BF88E7    CJNE    R7,#TCON(0x88),C:093F

C:0x0958    22        RET

C:0x0959    C0E0      PUSH    ACC(0xE0)
C:0x095B    C083      PUSH    DPH(0x83)
C:0x095D    C082      PUSH    DPL(0x82)

C:0x095F    751101    MOV     a(0x11),#0x01

C:0x0962    850B82    MOV     DPL(0x82),0x0B
C:0x0965    850A83    MOV     DPH(0x83),adc(0x0A)
C:0x0968    E0        MOVX    A,@DPTR
C:0x0969    F50C      MOV     dat(0x0C),A

C:0x096B    D082      POP     DPL(0x82)
C:0x096D    D083      POP     DPH(0x83)
C:0x096F    D0E0      POP     ACC(0xE0)
C:0x0971    32        RETI
C:0x0972    020A80    LJMP    C:0A80
C:0x0975    00        NOP
C:0x0976    020D00    LJMP    C:0D00
C:0x0979    0102      AJMP    C:0802
C:0x097B    08        INC     R0
C:0x097C    03        RR      A
C:0x097D    9401      SUBB    A,#0x01
C:0x097F    1100      ACALL   C:0800
C:0x0981    020F00    LJMP    C:0F00
C:0x0984    00        NOP
C:0x0985    021200    LJMP    C:1200
C:0x0988    0100      AJMP    C:0800


C:0x098A    758780    MOV     PCON(0x87),#P0(0x80)

C:0x098D    759850    MOV     SCON(0x98),#0x50




C:0x09C5    22        RET

C:0x09C6    758A22    MOV     TL0(0x8A),#0x22
```

5.3 C PROGRAM – TO RETRIEVE DATA

```
#include <dos.h>
#include <stdio.h>
#include <conio.h>
#define PORT1 0x3F8
 /* Defines Serial Ports Base Address */
 /* COM1 0x3F8  */
 /* COM2 0x2F8  */
 /* COM3 0x3E8  */
 /* COM4 0x2E8  */
void main(void)
      {     int c;
            int ch;
            outportb(PORT1 + 1 , 0);  /* Turn off interrupts - Port1 */
            /*      PORT 1 - Communication Settings       */
             outportb(PORT1 + 3 , 0x80);  /* SET DLAB ON */
             outportb(PORT1 + 0 , 0x03);  /* Set Baud rate - Divisor Latch
                                              Low Byte */
                                        /* Default 0x03 =  38,400 BPS */
                                        /*  0x01 = 115,200 BPS */
                                        /*  0x02 =  57,600 BPS */
                                        /*  0x06 =  19,200 BPS */
                                        /*  0x0C =   9,600 BPS */
                                        /*  0x18 =   4,800 BPS */
                                        /*   0x30 =   2,400 BPS */
```

```
outportb(PORT1 + 1 , 0x00);  /* Set Baud rate - Divisor Latch High Byte */
outportb(PORT1 + 3 , 0x03);  /* 8 Bits, No Parity, 1 Stop Bit */
outportb(PORT1 + 2 , 0xC7);  /* FIFO Control Register */
outportb(PORT1 + 4 , 0x0B);  /* Turn on DTR, RTS, and OUT2 */

printf("\nSerial Comm's Program. Press ESC to quit \n");

do { c = inportb(PORT1 + 5);            /* Check to see if char has been */
                                        /* received.                     */
    if (c & 1) {ch = inportb(PORT1);    /* If so, then get Char          */
            printf("%c",ch);}           /* Print Char to Screen          */

    if (kbhit()){ch = getch();          /* If key pressed, get Char */
            outportb(PORT1, ch);}       /* Send Char to Serial Port */

   } while (ch !=27);               /* Quit when ESC (ASC 27) is pressed */
}
```

6. APPLICATIONS

From the project title, it can be inferred that this data logging device can be used for many applications. Any type of input can be given to it. The major areas where it can be used are:

- Environmental monitoring
- Automotive testing
- Process control
- Structural monitoring
- Weather and Meteorology
- Industrial instruments duration and efficiency finder and many more

Some of the specific applications among the above generalized applications are:

- As horn duration finder
- Duration between two calls in telephone exchange
- Duration of a phone call can be measured
- Stability of UPS can be found out
- Frequency finder of any digital signal

CONCLUSION

Data logging and analysis calls in for a great deal of attention in the world today. The right solution to the complex problem is the biggest need of the hour. The culmination of our efforts has resulted in the birth of this data logging system.

The objective of this system to monitor at places where a computer cannot be accommodated and to store any type of input depending upon the application is effectively done in the most economical way.

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  By John B Peatman
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  By Intel Corporation

WEBSITES

www.8051.com

www.keil.com

www.microchip.com

:atures

- :ompatible with MCS-51™ Products
- ·K Bytes of In-System Reprogrammable Flash Memory
  - – Endurance: 1,000 Write/Erase Cycles
- :ully Static Operation: 0 Hz to 24 MHz
- 'hree-Level Program Memory Lock
- ı28 x 8-Bit Internal RAM
- ꞉2 Programmable I/O Lines
- ſwo 16-Bit Timer/Counters
- ꞉ix Interrupt Sources
- ᵖrogrammable Serial Channel
- ـow Power Idle and Power Down Modes

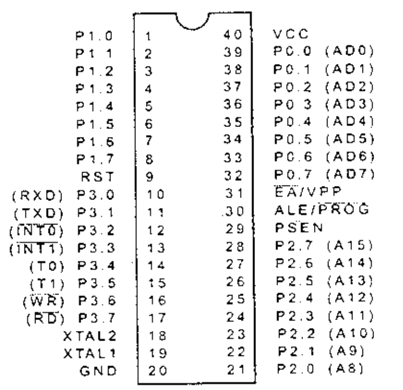
escription

ıe AT89C51 is a low-power, high-performance CMOS 8-bit microcomputer with 4K 'tes of Flash Programmable and Erasable Read Only Memory (PEROM). The ːvice is manufactured using Atmel's high density nonvolatile memory technology ıd is compatible with the industry standard MCS-51™ instruction set and pinout. The ı-chip Flash allows the program memory to be reprogrammed in-system or by a con- :ntional nonvolatile memory programmer. By combining a versatile 8-bit CPU with ash on a monolithic chip, the Atmel AT89C51 is a powerful microcomputer which ovides a highly flexible and cost effective solution to many embedded control appli- ıtions.

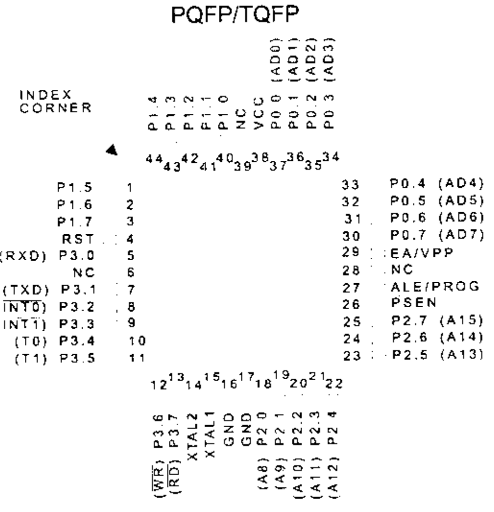
(continued)

'in Configurations

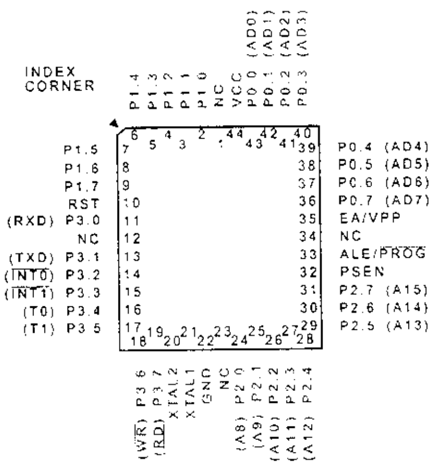
PDIP



PQFP/TQFP



PLCC

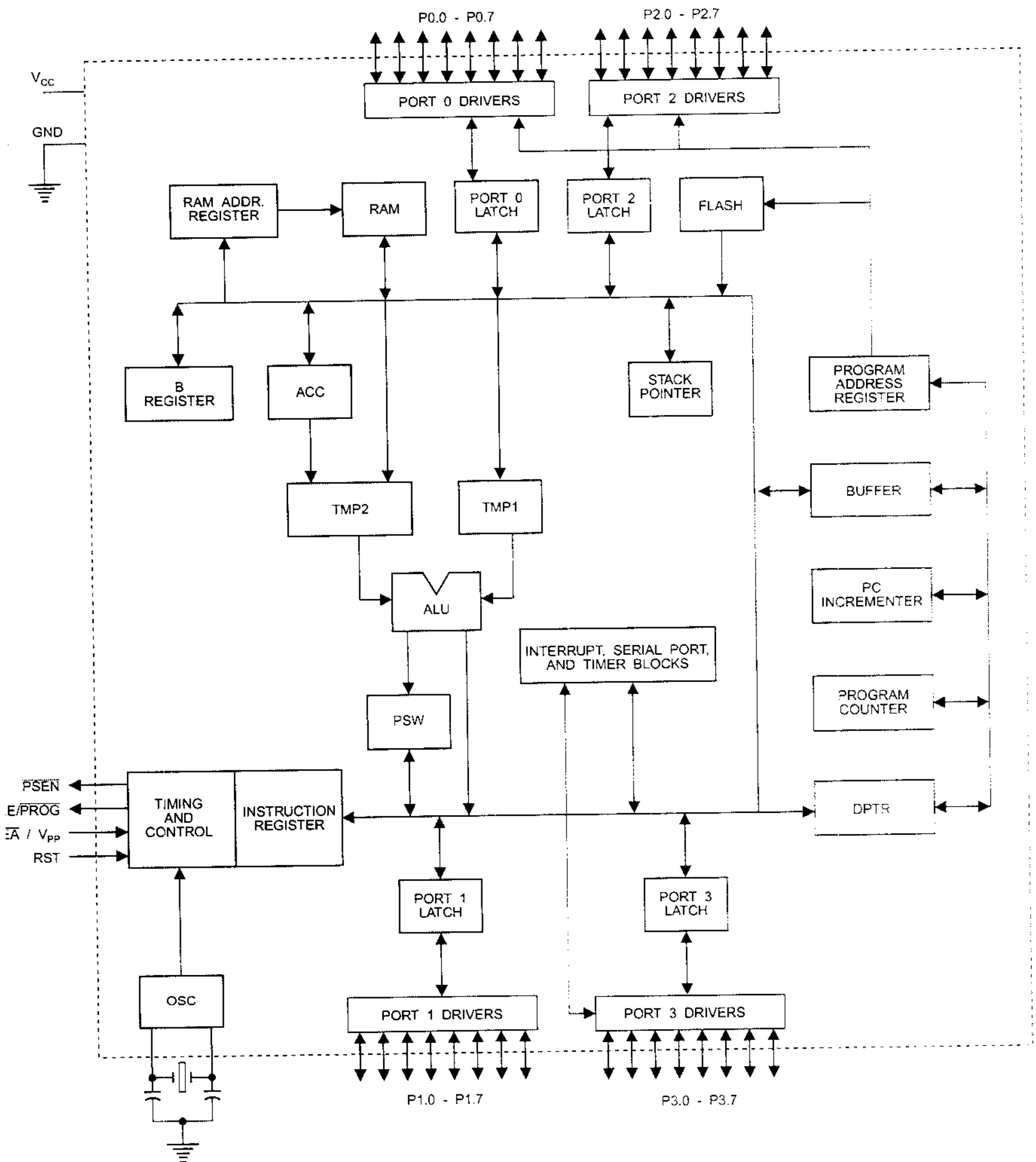


8-Bit Microcontroller with 4K Bytes Flash

AT89C51

0265F-A-12/97

k Diagram


P0.0 - P0.7
P2.0 - P2.7
VCC
GND
PORT 0 DRIVERS
PORT 2 DRIVERS
RAM ADDR. REGISTER
RAM
PORT 0 LATCH
PORT 2 LATCH
FLASH
B REGISTER
ACC
STACK POINTER
PROGRAM ADDRESS REGISTER
BUFFER
TMP2
TMP1
ALU
PC INCREMENTER
INTERRUPT, SERIAL PORT, AND TIMER BLOCKS
PSW
PROGRAM COUNTER
PSEN
E/PROG
EA / VPP
RST
TIMING AND CONTROL
INSTRUCTION REGISTER
DPTR
PORT 1 LATCH
PORT 3 LATCH
OSC
PORT 1 DRIVERS
PORT 3 DRIVERS
P1.0 - P1.7
P3.0 - P3.7

e AT89C51 provides the following standard features: 4K es of Flash, 128 bytes of RAM, 32 I/O lines, two 16-bit er/counters, a five vector two-level interrupt architecture, ull duplex serial port, on-chip oscillator and clock cirtry. In addition, the AT89C51 is designed with static logic operation down to zero frequency and supports two tware selectable power saving modes. The Idle Mode ps the CPU while allowing the RAM, timer/counters, ial port and interrupt system to continue functioning. The wer Down Mode saves the RAM contents but freezes oscillator disabling all other chip functions until the next rdware reset.

in Description

:C
ipply voltage.

ND
ound.

rt 0
rt 0 is an 8-bit open drain bidirectional I/O port. As an itput port each pin can sink eight TTL inputs. When 1s e written to port 0 pins, the pins can be used as highipedance inputs.

ort 0 may also be configured to be the multiplexed lowder address/data bus during accesses to external proam and data memory. In this mode P0 has internal pulps.

ort 0 also receives the code bytes during Flash programing, and outputs the code bytes during program verificaon. External pullups are required during program verificaon.

ort 1
ort 1 is an 8-bit bidirectional I/O port with internal pullups. he Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins they are pulled high by ie internal pullups and can be used as inputs. As inputs, ort 1 pins that are externally being pulled low will source urrent (I_{IL}) because of the internal pullups.

ort 1 also receives the low-order address bytes during lash programming and verification.

ort 2
ort 2 is an 8-bit bidirectional I/O port with internal pullups. he Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins they are pulled high by he internal pullups and can be used as inputs. As inputs, ort 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pullups.

ort 2 emits the high-order address byte during fetches rom external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application it uses strong internal pullups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

Port 3
Port 3 is an 8-bit bidirectional I/O port with internal pullups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pullups.

Port 3 also serves the functions of various special features of the AT89C51 as listed below:

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

Port 3 also receives some control signals for Flash programming and verification.

RST
Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

ALE/$\overline{PROG}$
Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during Flash programming.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

$\overline{PSEN}$
Program Store Enable is the read strobe to external program memory.

ıen the AT89C51 is executing code from external pro-
m memory, $\overline{PSEN}$ is activated twice each machine
:le, except that two $\overline{PSEN}$ activations are skipped during
:h access to external data memory.

/V_{PP}

ternal Access Enable. $\overline{EA}$ must be strapped to GND in
ler to enable the device to fetch code from external pro-
ım memory locations starting at 0000H up to FFFFH.
ıte, however, that if lock bit 1 is programmed, $\overline{EA}$ will be
ernally latched on reset.

ı should be strapped to V_{CC} for internal program execu-
ns.

is pin also receives the 12-volt programming enable volt-
e (V_{PP}) during Flash programming, for parts that require
-volt V_{PP}.

:AL1

put to the inverting oscillator amplifier and input to the
:ernal clock operating circuit.

TAL2

ıtput from the inverting oscillator amplifier.

ıscillator Characteristics

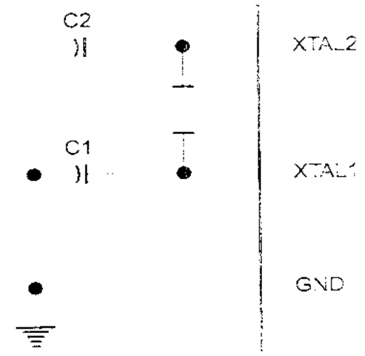
TAL1 and XTAL2 are the input and output, respectively,
an inverting amplifier which can be configured for use as
ı on-chip oscillator, as shown in Figure 1. Either a quartz
ystal or ceramic resonator may be used. To drive the
evice from an external clock source, XTAL2 should be left
ıconnected while XTAL1 is driven as shown in Figure 2.
here are no requirements on the duty cycle of the external
ock signal, since the input to the internal clocking circuitry
: through a divide-by-two flip-flop, but minimum and maxi-
ıum voltage high and low time specifications must be
bserved.

dle Mode

ı idle mode, the CPU puts itself to sleep while all the on-
hip peripherals remain active. The mode is invoked by
oftware. The content of the on-chip RAM and all the spe-
:ial functions registers remain unchanged during this
node. The idle mode can be terminated by any enabled
ıterrupt or by a hardware reset.

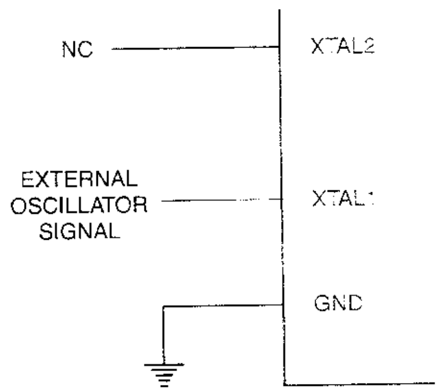
It should be noted that when idle is terminated by a hard ware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

Figure 1. Oscillator Connections



Note: C1, C2 = 30 pF ± 10 pF for Crystals
= 40 pF ± 10 pF for Ceramic Resonators

Figure 2. External Clock Drive Configuration



Status of External Pins During Idle and Power Down Modes

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power Down	Internal	0	0	Data	Data	Data	Data
Power Down	External	0	0	Float	Data	Data	Data

ɔwer Down Mode

:he power down mode the oscillator is stopped, and the truction that invokes power down is the last instruction ɜcuted. The on-chip RAM and Special Function Regis- s retain their values until the power down mode is termi- ted. The only exit from power down is a hardware reset. set redefines the SFRs but does not change the on-chip ‹M. The reset should not be activated before V_{CC} is ;tored to its normal operating level and must be held tive long enough to allow the oscillator to restart and sta- ze.

ɔck Bit Protection Modes

	Program Lock Bits			Protection Type
	LB1	LB2	LB3	
1	U	U	U	No program lock features.
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset, and further programming of the Flash is disabled.
3	P	P	U	Same as mode 2, also verify is disabled.
4	P	P	P	Same as mode 3, also external execution is disabled.

Program Memory Lock Bits

On the chip are three lock bits which can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the table below:

When lock bit 1 is programmed, the logic level at the $\overline{EA}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value, and holds that value until reset is activated. It is necessary that the latched value of $\overline{EA}$ be in agreement with the current logic level at that pin in order for the device to function properly.

'rogramming the Flash

ıe AT89C51 is normally shipped with the on-chip Flash ıemory array in the erased state (that is, contents = FFH) ıd ready to be programmed. The programming interface ɔcepts either a high-voltage (12-volt) or a low-voltage $/_{CC}$) program enable signal. The low voltage program- ıing mode provides a convenient way to program the .T89C51 inside the user's system, while the high-voltage rogramming mode is compatible with conventional third arty Flash or EPROM programmers.

he AT89C51 is shipped with either the high-voltage or ɔw-voltage programming mode enabled. The respective ɔp-side marking and device signature codes are listed in ıe following table.

	V_{PP} = 12V	V_{PP} = 5V
Top-Side Mark	AT89C51 xxxx yyww	AT89C51 xxxx-5 yyww
Signature	(030H)=1EH (031H)=51H (032H)=FFH	(030H)=1EH (031H)=51H (032H)=05H

ʳhe AT89C51 code memory array is programmed byte-by- ɔyte in either programming mode. *To program any non- blank byte in the on-chip Flash Memory, the entire memory must be erased using the Chip Erase Mode.*

Programming Algorithm: Before programming the AT89C51, the address, data and control signals should be set up according to the Flash programming mode table and Figures 3 and 4. To program the AT89C51, take the following steps.

1. Input the desired memory location on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise $\overline{EA}/V_{PP}$ to 12V for the high-voltage programming mode.
5. Pulse ALE/$\overline{PROG}$ once to program a byte in the Flash array or the lock bits. The byte-write cycle is self-timed and typically takes no more than 1.5 ms. Repeat steps 1 through 5, changing the address and data for the entire array or until the end of the object file is reached.

$\overline{\text{Data}}$ Polling: The AT89C51 features $\overline{\text{Data}}$ Polling to indicate the end of a write cycle. During a write cycle, an attempted read of the last byte written will result in the complement of the written datum on PO.7. Once the write cycle has been completed, true data are valid on all outputs, and the next cycle may begin. $\overline{\text{Data}}$ Polling may begin any time after a write cycle has been initiated.

Ready/$\overline{\text{Busy}}$: The progress of byte programming can also be monitored by the RDY/$\overline{BSY}$ output signal. P3.4 is pulled low after ALE goes high during programming to indicate BUSY. P3.4 is pulled high again when programming is done to indicate READY.

›gram Verify: If lock bits LB1 and LB2 have not been ·grammed, the programmed code data can be read back the address and data lines for verification. The lock bits ınot be verified directly. Verification of the lock bits is ıieved by observing that their features are enabled.

ip Erase: The entire Flash array is erased electrically using the proper combination of control signals and by lding ALE/$\overline{PROG}$ low for 10 ms. The code array is written h all "1"s. The chip erase operation must be executed fore the code memory can be re-programmed.

›ading the Signature Bytes: The signature bytes are ad by the same procedure as a normal verification of :ations 030H,

1H, and 032H, except that P3.6 and P3.7 must be pulled a logic low. The values returned are as follows.

(030H) = 1EH indicates manufactured by Atmel
(031H) = 51H indicates 89C51
(032H) = FFH indicates 12V programming
(032H) = 05H indicates 5V programming

Programming Interface

Every code byte in the Flash array can be written and the entire array can be erased by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

All major programming vendors offer worldwide support for the Atmel microcontroller series. Please contact your local programming vendor for the appropriate software revision.

Flash Programming Modes

ıode		RST	$\overline{PSEN}$	ALE/$\overline{PROG}$	$\overline{EA}/V_{PP}$	P2.6	P2.7	P3.6	P3.7
Vrite Code Data		H	L	‾_/‾	H/12V	L	H	H	H
Read Code Data		H	L	H	H	L	L	H	H
Write Lock	Bit - 1	H	L	‾_/‾	H/12V	H	H	H	H
	Bit - 2	H	L	‾_/‾	H/12V	H	H	L	L
	Bit - 3	H	L	‾_/‾	H/12V	H	L	H	L
Chip Erase		H	L	‾_/‾ (1)	H/12V	H	L	L	L
Read Signature Byte		H	L	H	H	L	L	L	L

ote: 1. Chip Erase requires a 10-ms $\overline{PROG}$ pulse.

ure 3. Programming the Flash

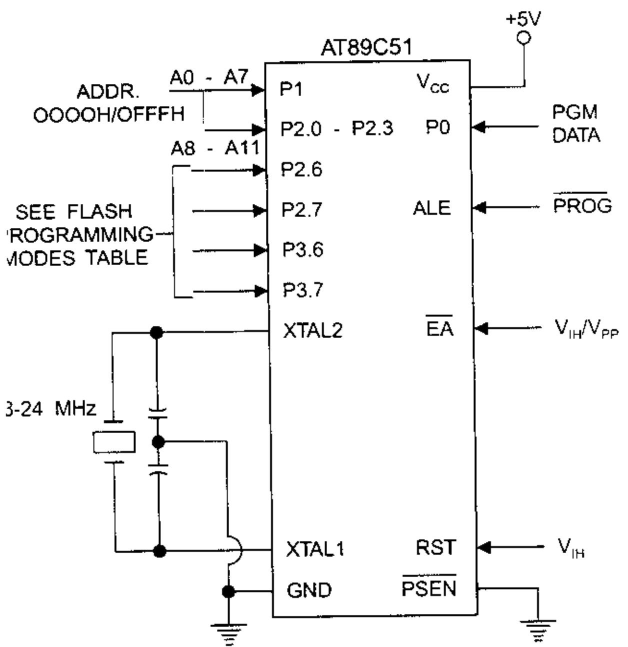
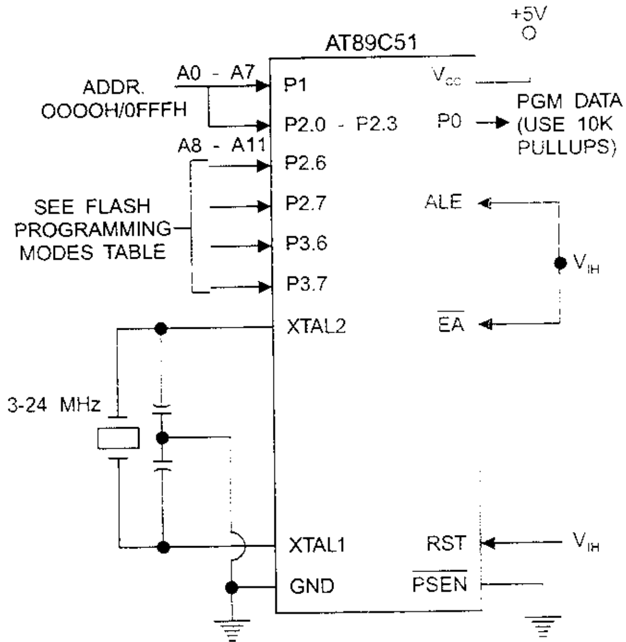


Figure 4. Verifying the Flash



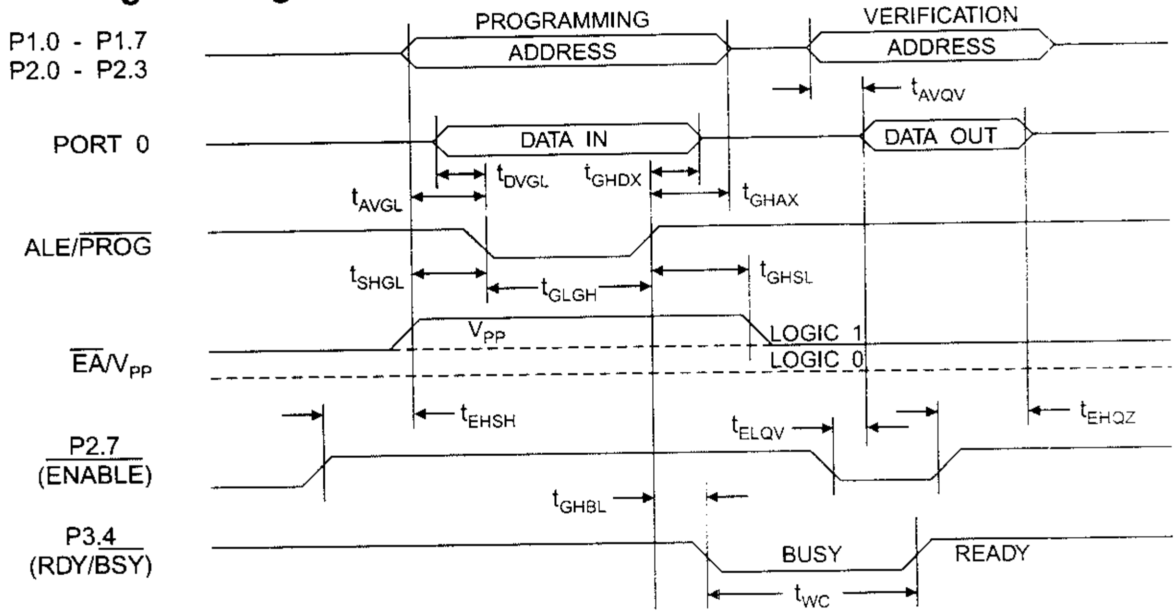
lash Programming and Verification Characteristics

$_A$ = 0°C to 70°C, V_{CC} = 5.0 ± 10%

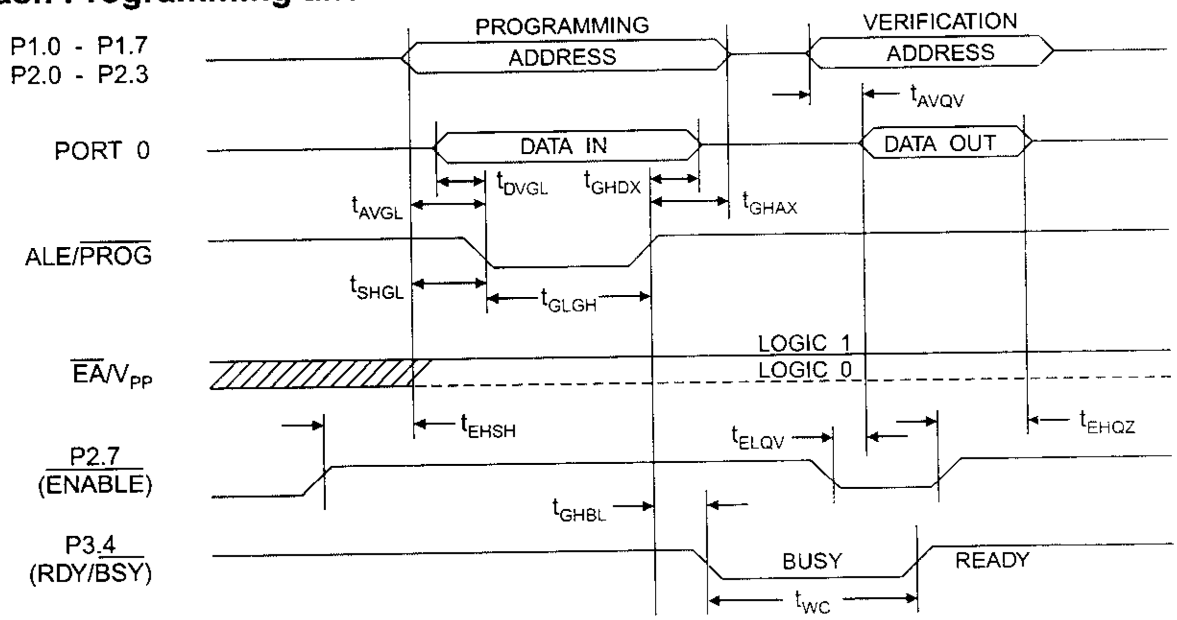
Symbol	Parameter	Min	Max	Units
V_{PP}(1)	Programming Enable Voltage	11.5	12.5	V
I_{PP}(1)	Programming Enable Current		1.0	mA
$1/t_{CLCL}$	Oscillator Frequency	3	24	MHz
t_{AVGL}	Address Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
t_{GHAX}	Address Hold After $\overline{PROG}$	$48t_{CLCL}$		
t_{DVGL}	Data Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
t_{GHDX}	Data Hold After $\overline{PROG}$	$48t_{CLCL}$		
t_{EHSH}	P2.7 ($\overline{ENABLE}$) High to V_{PP}	$48t_{CLCL}$		
t_{SHGL}	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
t_{GHSL}(1)	V_{PP} Hold After $\overline{PROG}$	10		µs
t_{GLGH}	$\overline{PROG}$ Width	1	110	µs
t_{AVQV}	Address to Data Valid		$48t_{CLCL}$	
t_{ELQV}	$\overline{ENABLE}$ Low to Data Valid		$48t_{CLCL}$	
t_{EHQZ}	Data Float After $\overline{ENABLE}$	0	$48t_{CLCL}$	
t_{GHBL}	$\overline{PROG}$ High to $\overline{BUSY}$ Low		1.0	µs
t_{WC}	Byte Write Cycle Time		2.0	ms

\ote: 1. Only used in 12-volt programming mode.

ash Programming and Verification Waveforms - High Voltage Mode (V_{PP} = 12V)



lash Programming and Verification Waveforms - Low Voltage Mode (V_{PP} = 5V)



ɔsolute Maximum Ratings*

perating Temperature	-55°C to +125°C
torage Temperature	-65°C to +150°C
ɔltage on Any Pin ith Respect to Ground	-1.0V to +7.0V
laximum Operating Voltage	6.6V
·C Output Current	15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

C Characteristics

= -40°C to 85°C, V_{CC} = 5.0V ± 20% (unless otherwise noted)

;ymbol	Parameter	Condition	Min	Max	Units
$'_{IL}$	Input Low Voltage	(Except $\overline{EA}$)	-0.5	0.2 V_{CC} - 0.1	V
$'_{IL1}$	Input Low Voltage ($\overline{EA}$)		-0.5	0.2 V_{CC} - 0.3	V
$'_{IH}$	Input High Voltage	(Except XTAL1, RST)	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V
$'_{IH1}$	Input High Voltage	(XTAL1, RST)	0.7 V_{CC}	V_{CC} + 0.5	V
$/_{OL}$	Output Low Voltage(1) (Ports 1,2,3)	I_{OL} = 1.6 mA		0.45	V
$/_{OL1}$	Output Low Voltage(1) (Port 0, ALE, $\overline{PSEN}$)	I_{OL} = 3.2 mA		0.45	V
$'_{OH}$	Output High Voltage (Ports 1,2,3, ALE, $\overline{PSEN}$)	I_{OH} = -60 μA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -25 μA	0.75 V_{CC}		V
		I_{OH} = -10 μA	0.9 V_{CC}		V
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)	I_{OH} = -800 μA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -300 μA	0.75 V_{CC}		V
		I_{OH} = -80 μA	0.9 V_{CC}		V
I_{IL}	Logical 0 Input Current (Ports 1,2,3)	V_{IN} = 0.45V		-50	μA
I_{TL}	Logical 1 to 0 Transition Current (Ports 1,2,3)	V_{IN} = 2V, VCC = 5V ± 10%		-650	μA
I_{LI}	Input Leakage Current (Port 0, $\overline{EA}$)	0.45 < V_{IN} < V_{CC}		±10	μA
RRST	Reset Pulldown Resistor		50	300	KΩ
C_{IO}	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
I_{CC}	Power Supply Current	Active Mode, 12 MHz		20	mA
		Idle Mode, 12 MHz		5	mA
	Power Down Mode(2)	V_{CC} = 6V		100	μA
		V_{CC} = 3V		40	μA

Notes: 1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
Maximum I_{OL} per port pin: 10 mA
Maximum I_{OL} per 8-bit port: Port 0: 26 mA
Ports 1, 2, 3: 15 mA
Maximum total I_{OL} for all output pins: 71 mA
If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Minimum V_{CC} for Power Down is 2V.

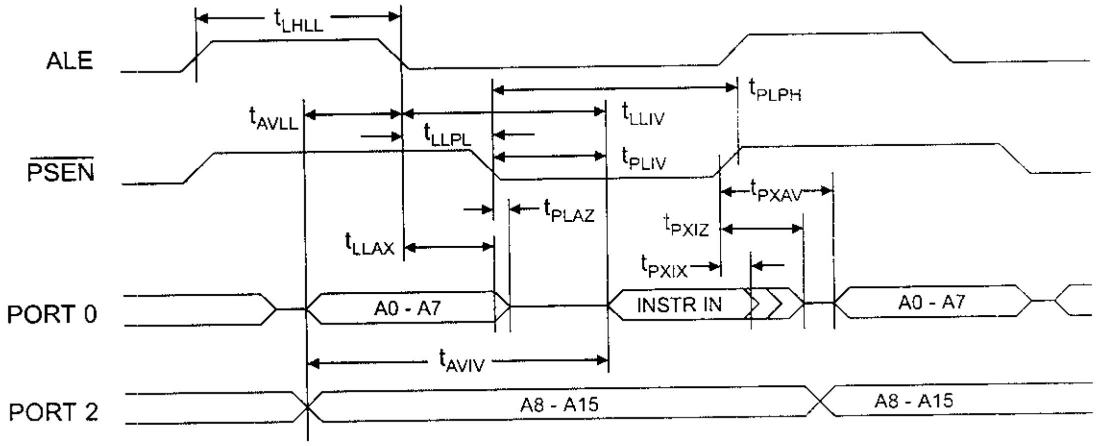
C Characteristics

nder Operating Conditions; Load Capacitance for Port 0, ALE/$\overline{\text{PROG}}$, and $\overline{\text{PSEN}}$ = 100 pF; Load Capacitance for all other puts = 80 pF)

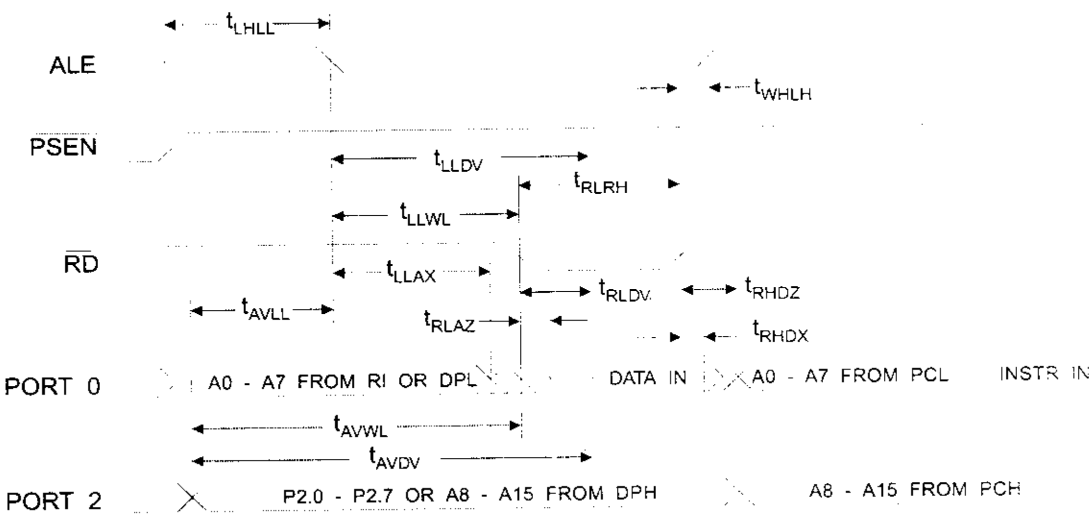
xternal Program and Data Memory Characteristics

ymbol	Parameter	12 MHz Oscillator		16 to 24 MHz Oscillator		Units
		Min	Max	Min	Max	
/t_{CLCL}	Oscillator Frequency			0	24	MHz
$_{HLL}$	ALE Pulse Width	127		$2t_{CLCL}$-40		ns
$_{VLL}$	Address Valid to ALE Low	43		t_{CLCL}-13		ns
$_{LAX}$	Address Hold After ALE Low	48		t_{CLCL}-20		ns
$_{LLIV}$	ALE Low to Valid Instruction In		233		$4t_{CLCL}$-65	ns
$_{LLPL}$	ALE Low to $\overline{\text{PSEN}}$ Low	43		t_{CLCL}-13		ns
$_{PLPH}$	$\overline{\text{PSEN}}$ Pulse Width	205		$3t_{CLCL}$-20		ns
$_{PLIV}$	$\overline{\text{PSEN}}$ Low to Valid Instruction In		145		$3t_{CLCL}$-45	ns
$_{PXIX}$	Input Instruction Hold After $\overline{\text{PSEN}}$	0		0		ns
$_{PXIZ}$	Input Instruction Float After $\overline{\text{PSEN}}$		59		t_{CLCL}-10	ns
$_{PXAV}$	$\overline{\text{PSEN}}$ to Address Valid	75		t_{CLCL}-8		ns
$_{AVIV}$	Address to Valid Instruction In		312		$5t_{CLCL}$-55	ns
$_{PLAZ}$	$\overline{\text{PSEN}}$ Low to Address Float		10		10	ns
t_{RLRH}	$\overline{\text{RD}}$ Pulse Width	400		$6t_{CLCL}$-100		ns
t_{WLWH}	$\overline{\text{WR}}$ Pulse Width	400		$6t_{CLCL}$-100		ns
t_{RLDV}	$\overline{\text{RD}}$ Low to Valid Data In		252		$5t_{CLCL}$-90	ns
t_{RHDX}	Data Hold After $\overline{\text{RD}}$	0		0		ns
t_{RHDZ}	Data Float After $\overline{\text{RD}}$		97		$2t_{CLCL}$-28	ns
t_{LLDV}	ALE Low to Valid Data In		517		$8t_{CLCL}$-150	ns
t_{AVDV}	Address to Valid Data In		585		$9t_{CLCL}$-165	ns
t_{LLWL}	ALE Low to $\overline{\text{RD}}$ or $\overline{\text{WR}}$ Low	200	300	$3t_{CLCL}$-50	$3t_{CLCL}$+50	ns
t_{AVWL}	Address to $\overline{\text{RD}}$ or $\overline{\text{WR}}$ Low	203		$4t_{CLCL}$-75		ns
t_{QVWX}	Data Valid to $\overline{\text{WR}}$ Transition	23		t_{CLCL}-20		ns
t_{QVWH}	Data Valid to $\overline{\text{WR}}$ High	433		$7t_{CLCL}$-120		ns
t_{WHQX}	Data Hold After $\overline{\text{WR}}$	33		t_{CLCL}-20		ns
t_{RLAZ}	$\overline{\text{RD}}$ Low to Address Float		0		0	ns
t_{WHLH}	$\overline{\text{RD}}$ or $\overline{\text{WR}}$ High to ALE High	43	123	t_{CLCL}-20	t_{CLCL}+25	ns

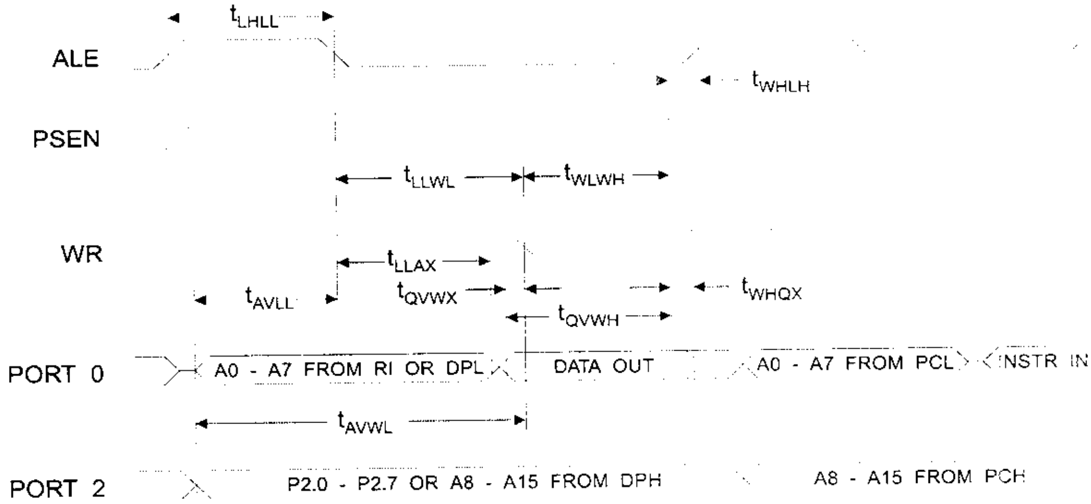
‹ternal Program Memory Read Cycle



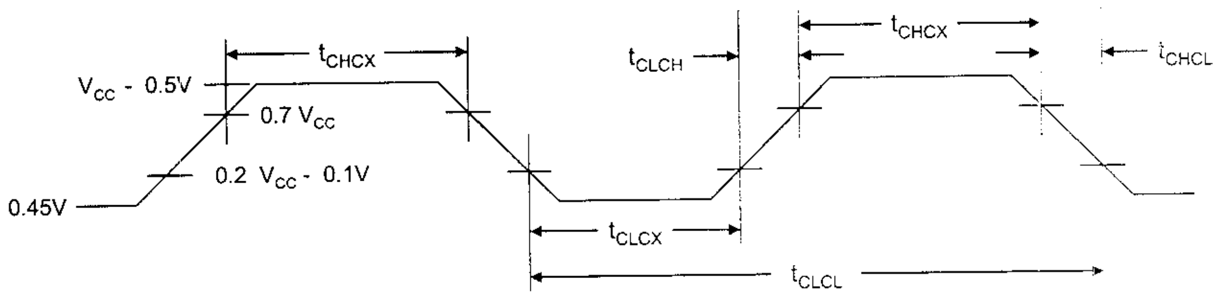
xternal Data Memory Read Cycle



‹ternal Data Memory Write Cycle



xternal Clock Drive Waveforms



:xternal Clock Drive

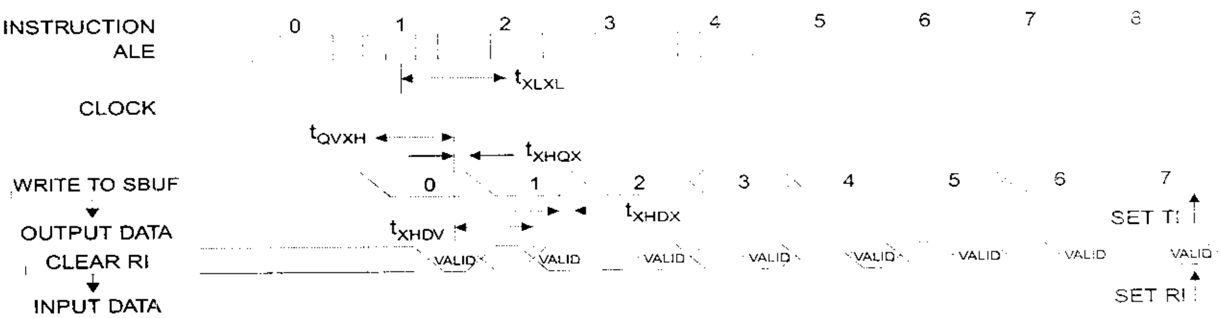
Symbol	Parameter	Min	Max	Units
$1/t_{CLCL}$	Oscillator Frequency	0	24	MHz
t_{CLCL}	Clock Period	41.6		ns
t_{CHCX}	High Time	15		ns
t_{CLCX}	Low Time	15		ns
t_{CLCH}	Rise Time		20	ns
t_{CHCL}	Fall Time		20	ns

ɜrial Port Timing: Shift Register Mode Test Conditions

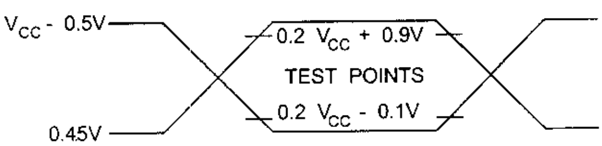
:C = 5.0 V ± 20%; Load Capacitance = 80 pF)

ymbol	Parameter	12 MHz Osc		Variable Oscillator		Units
		Min	Max	Min	Max	
:LXL	Serial Port Clock Cycle Time	1.0		$12t_{CLCL}$		µs
ʇVXH	Output Data Setup to Clock Rising Edge	700		$10t_{CLCL}$-133		ns
‹HQX	Output Data Hold After Clock Rising Edge	50		$2t_{CLCL}$-117		ns
‹HDX	Input Data Hold After Clock Rising Edge	0		0		ns
‹HDV	Clock Rising Edge to Input Data Valid		700		$10t_{CLCL}$-133	ns

hift Register Mode Timing Waveforms

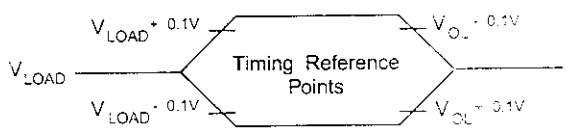


ιC Testing Input/Output Waveforms(1)



lote: 1. AC Inputs during testing are driven at V_{CC} - 0.5V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

Float Waveforms(1)



Note: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

rdering Information

Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
12	5V ± 20%	AT89C51-12AC	44A	Commercial (0°C to 70°C)
		AT89C51-12JC	44J	
		AT89C51-12PC	40P6	
		AT89C51-12QC	44Q	
		AT89C51-12AI	44A	Industrial (-40°C to 85°C)
		AT89C51-12JI	44J	
		AT89C51-12PI	40P6	
		AT89C51-12QI	44Q	
		AT89C51-12AA	44A	Automotive (-40°C to 105°C)
		AT89C51-12JA	44J	
		AT89C51-12PA	40P6	
		AT89C51-12QA	44Q	
16	5V ± 20%	AT89C51-16AC	44A	Commercial (0°C to 70°C)
		AT89C51-16JC	44J	
		AT89C51-16PC	40P6	
		AT89C51-16QC	44Q	
		AT89C51-16AI	44A	Industrial (-40°C to 85°C)
		AT89C51-16JI	44J	
		AT89C51-16PI	40P6	
		AT89C51-16QI	44Q	
		AT89C51-16AA	44A	Automotive (-40°C to 105°C)
		AT89C51-16JA	44J	
		AT89C51-16PA	40P6	
		AT89C51-16QA	44Q	
20	5V ± 20%	AT89C51-20AC	44A	Commercial (0°C to 70°C)
		AT89C51-20JC	44J	
		AT89C51-20PC	40P6	
		AT89C51-20QC	44Q	
		AT89C51-20AI	44A	Industrial (-40°C to 85°C)
		AT89C51-20JI	44J	
		AT89C51-20PI	40P6	
		AT89C51-20QI	44Q	

rdering Information

Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
24	5V ± 20%	AT89C51-24AC	44A	Commercial (0°C to 70°C)
		AT89C51-24JC	44J	
		AT89C51-24PC	44P6	
		AT89C51-24QC	44Q	
		AT89C51-24AI	44A	Industrial (-40°C to 85°C)
		AT89C51-24JI	44J	
		AT89C51-24PI	44P6	
		AT89C51-24QI	44Q	

Package Type	
44A	44 Lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
44J	44 Lead, Plastic J-Leaded Chip Carrier (PLCC)
40P6	40 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
44Q	44 Lead, Plastic Gull Wing Quad Flatpack (PQFP)

October 1999

National Semiconductor

ADC0808/ADC0809 8-Bit µP Compatible A/D Converters with 8-Channel Multiplexer

General Description

The ADC0808, ADC0809 data acquisition component is a monolithic CMOS device with an 8-bit analog-to-digital converter, 8-channel multiplexer and microprocessor compatible control logic. The 8-bit A/D converter uses successive approximation as the conversion technique. The converter features a high impedance chopper stabilized comparator, a 256R voltage divider with analog switch tree and a successive approximation register. The 8-channel multiplexer can directly access any of 8-single-ended analog signals.

The device eliminates the need for external zero and full-scale adjustments. Easy interfacing to microprocessors is provided by the latched and decoded multiplexer address inputs and latched TTL TRI-STATE® outputs.

The design of the ADC0808, ADC0809 has been optimized by incorporating the most desirable aspects of several A/D conversion techniques. The ADC0808, ADC0809 offers high speed, high accuracy, minimal temperature dependence, excellent long-term accuracy and repeatability, and consumes minimal power. These features make this device ideally suited to applications from process and machine control to consumer and automotive applications. For 16-channel multiplexer with common output (sample/hold port) see ADC0816 data sheet. (See AN-247 for more information.)

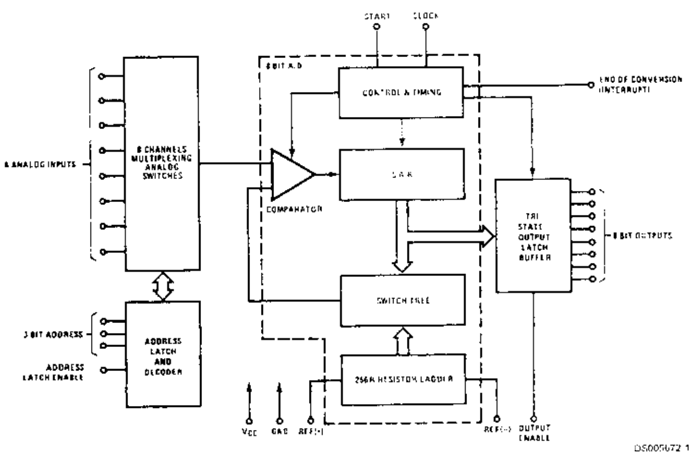
Features

- Easy interface to all microprocessors
- Operates ratiometrically or with 5 V_{DC} or analog span adjusted voltage reference
- No zero or full-scale adjust required
- 8-channel multiplexer with address logic
- 0V to 5V input range with single 5V power supply
- Outputs meet TTL voltage level specifications
- Standard hermetic or molded 28-pin DIP package
- 28-pin molded chip carrier package
- ADC0808 equivalent to MM74C949
- ADC0809 equivalent to MM74C949-1

Key Specifications

■ Resolution	8 Bits
■ Total Unadjusted Error	±½ LSB and ±1 LSB
■ Single Supply	5 V_{DC}
■ Low Power	15 mW
■ Conversion Time	100 µs

Block Diagram



DS005672-1

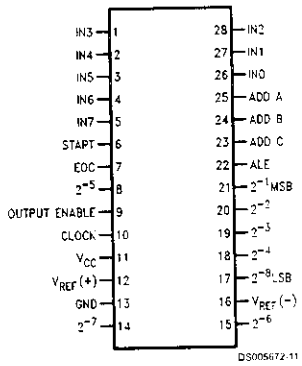
See Ordering Information

TRI-STATE® is a registered trademark of National Semiconductor Corp.

 DS005672

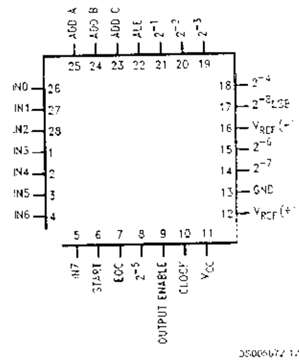
Connection Diagrams

Dual-In-Line Package



Order Number ADC0808CCN or ADC0809CCN
See NS Package J28A or N28A

Molded Chip Carrier Package



Order Number ADC0808CCV or ADC0809CCV
See NS Package V28A

Ordering Information

TEMPERATURE RANGE		−40˚C to +85˚C			−55˚C to +125˚C
Error	±½ LSB Unadjusted	ADC0808CCN	ADC0808CCV	ADC0808CCJ	ADC0808CJ
	±1 LSB Unadjusted	ADC0809CCN	ADC0809CCV		
Package Outline		N28A Molded DIP	V28A Molded Chip Carrier	J28A Ceramic DIP	J28A Ceramic DIP

Absolute Maximum Ratings (Notes 2, 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC}) (Note 3)	6.5V
Voltage at Any Pin	−0.3V to (V_{CC}+0.3V)
Except Control Inputs	
Voltage at Control Inputs	−0.3V to +15V
(START, OE, CLOCK, ALE, ADD A, ADD B, ADD C)	
Storage Temperature Range	−65°C to +150°C
Package Dissipation at T_A=25°C	875 mW
Lead Temp. (Soldering, 10 seconds)	
Dual-In-Line Package (plastic)	260°C
Dual-In-Line Package (ceramic)	300°C
Molded Chip Carrier Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
ESD Susceptibility (Note 8)	400V

Operating Conditions (Notes 1, 2)

Temperature Range (Note 1)	$T_{MIN} \le T_A \le T_{MAX}$
ADC0808CCN,ADC0809CCN	−40°C≤T_A≤+85°C
ADC0808CCV, ADC0809CCV	−40°C ≤ T_A ≤ +85°C
Range of V_{CC} (Note 1)	4.5 V_{DC} to 6.0 V_{DC}

Electrical Characteristics

Converter Specifications: V_{CC}=5 V_{DC}=V_{REF+}, $V_{REF(-)}$=GND, $T_{MIN} \le T_A \le T_{MAX}$ and f_{CLK}=640 kHz unless otherwise stated.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	ADC0808					
	Total Unadjusted Error	25°C			±½	LSB
	(Note 5)	T_{MIN} to T_{MAX}			±¾	LSB
	ADC0809					
	Total Unadjusted Error	0°C to 70°C			±1	LSB
	(Note 5)	T_{MIN} to T_{MAX}			±1¼	LSB
	Input Resistance	From Ref(+) to Ref(−)	1.0	2.5		kΩ
	Analog Input Voltage Range	(Note 4) V(+) or V(−)	GND−0.10		V_{CC}+0.10	V_{DC}
$V_{REF(+)}$	Voltage, Top of Ladder	Measured at Ref(+)		V_{CC}	V_{CC}+0.1	V
$\frac{V_{REF(+)}+V_{REF(-)}}{2}$	Voltage, Center of Ladder		V_{CC}/2-0.1	V_{CC}/2	V_{CC}/2+0.1	V
$V_{REF(-)}$	Voltage, Bottom of Ladder	Measured at Ref(−)	−0.1	0		V
I_{IN}	Comparator Input Current	f_c=640 kHz, (Note 6)	−2	±0.5	2	μA

Electrical Characteristics

Digital Levels and DC Specifications: ADC0808CCN, ADC0808CCV, ADC0809CCN and ADC0809CCV, 4.75≤V_{CC}≤5.25V, −40°C≤T_A≤+85°C unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
ANALOG MULTIPLEXER						
$I_{OFF(+)}$	OFF Channel Leakage Current	V_{CC}=5V, V_{IN}=5V,				
		T_A=25°C		10	200	nA
		T_{MIN} to T_{MAX}			1.0	μA
$I_{OFF(-)}$	OFF Channel Leakage Current	V_{CC}=5V, V_{IN}=0,				
		T_A=25°C	−200	−10		nA
		T_{MIN} to T_{MAX}	−1.0			μA
CONTROL INPUTS						
$V_{IN(1)}$	Logical "1" Input Voltage		V_{CC}−1.5			V
$V_{IN(0)}$	Logical "0" Input Voltage				1.5	V
$I_{IN(1)}$	Logical "1" Input Current (The Control Inputs)	V_{IN}=15V			1.0	μA
$I_{IN(0)}$	Logical "0" Input Current (The Control Inputs)	V_{IN}=0	−1.0			μA
I_{CC}	Supply Current	f_{CLK}=640 kHz		0.3	3.0	mA

Electrical Characteristics (Continued)

Digital Levels and DC Specifications: ADC0808CCN, ADC0808CCV, ADC0809CCN and ADC0809CCV, $4.75 \le V_{CC} \le 5.25V$, $-40^{\circ}C \le T_A \le +85^{\circ}C$ unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DATA OUTPUTS AND EOC (INTERRUPT)						
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 4.75V I_{OUT} = −360µA I_{OUT} = −10µA		 **2.4** **4.5**		 V(min) V(min)
$V_{OUT(0)}$	Logical "0" Output Voltage	I_O=1.6 mA			0.45	V
$V_{OUT(0)}$	Logical "0" Output Voltage EOC	I_O=1.2 mA			0.45	V
I_{OUT}	TRI-STATE Output Current	V_O=5V V_O=0	 −3		3	µA µA

Electrical Characteristics

Timing Specifications $V_{CC}=V_{REF(+)}=5V$, $V_{REF(-)}=GND$, $t_r=t_f=20$ ns and $T_A=25^{\circ}C$ unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{WS}	Minimum Start Pulse Width	(*Figure 5*)		100	200	ns
t_{WALE}	Minimum ALE Pulse Width	(*Figure 5*)		100	200	ns
t_s	Minimum Address Set-Up Time	(*Figure 5*)		25	50	ns
t_H	Minimum Address Hold Time	(*Figure 5*)		25	50	ns
t_D	Analog MUX Delay Time From ALE	R_S=0Ω (*Figure 5*)		1	2.5	µs
t_{H1}, t_{H0}	OE Control to Q Logic State	C_L=50 pF, R_L=10k (*Figure 8*)		125	250	ns
t_{1H}, t_{0H}	OE Control to Hi-Z	C_L=10 pF, R_L=10k (*Figure 8*)		125	250	ns
t_c	Conversion Time	f_c=640 kHz, (*Figure 5*) (Note 7)	90	100	116	µs
f_c	Clock Frequency		10	640	1280	kHz
t_{EOC}	EOC Delay Time	(*Figure 5*)	0		8+2 µS	Clock Periods
C_{IN}	Input Capacitance	At Control Inputs		10	15	pF
C_{OUT}	TRI-STATE Output Capacitance	At TRI-STATE Outputs		10	15	pF

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to GND, unless othewise specified.

Note 3: A zener diode exists, internally, from V_{CC} to GND and has a typical breakdown voltage of 7 V_{DC}.

Note 4: Two on-chip diodes are tied to each analog input which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC}n supply. The spec allows 100 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 100 mV, the output code will be correct. To achieve an absolute $0V_{DC}$ to $5V_{DC}$ input voltage range will therefore require a minimum supply voltage of 4.900 V_{DC} over temperature variations, initial tolerance and loading.

Note 5: Total unadjusted error includes offset, full-scale, linearity, and multiplexer errors. See *Figure 3*. None of these A/Ds requires a zero or full-scale adjust. However, if an all zero code is desired for an analog input other than 0.0V, or if a narrow full-scale span exists (for example: 0.5V to 4.5V full-scale) the reference voltages can be adjusted to achieve this. See *Figure 13*.

Note 6: Comparator input current is a bias current into or out of the chopper stabilized comparator. The bias current varies directly with clock frequency and has little temperature dependence (*Figure 6*). See paragraph 4.0.

Note 7: The outputs of the data register are updated one clock cycle before the rising edge of EOC.

Note 8: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Functional Description

Multiplexer. The device contains an 8-channel single-ended analog signal multiplexer. A particular input channel is selected by using the address decoder. *Table 1* shows the input states for the address lines to select any channel. The address is latched into the decoder on the low-to-high transition of the address latch enable signal.

TABLE 1.

SELECTED ANALOG CHANNEL	ADDRESS LINE		
	C	B	A
IN0	L	L	L
IN1	L	L	H
IN2	L	H	L
IN3	L	H	H
IN4	H	L	L
IN5	H	L	H
IN6	H	H	L
IN7	H	H	H

CONVERTER CHARACTERISTICS

The Converter

The heart of this single chip data acquisition system is its 8-bit analog-to-digital converter. The converter is designed to give fast, accurate, and repeatable conversions over a wide range of temperatures. The converter is partitioned into 3 major sections: the 256R ladder network, the successive approximation register, and the comparator. The converter's digital outputs are positive true.

The 256R ladder network approach (*Figure 1*) was chosen over the conventional R/2R ladder because of its inherent monotonicity, which guarantees no missing digital codes. Monotonicity is particularly important in closed loop feedback control systems. A non-monotonic relationship can cause oscillations that will be catastrophic for the system. Additionally, the 256R network does not cause load variations on the reference voltage.

The bottom resistor and the top resistor of the ladder network in *Figure 1* are not the same value as the remainder of the network. The difference in these resistors causes the output characteristic to be symmetrical with the zero and full-scale points of the transfer curve. The first output transition occurs when the analog signal has reached +½ LSB and succeeding output transitions occur every 1 LSB later up to full-scale.

The successive approximation register (SAR) performs 8 iterations to approximate the input voltage. For any SAR type converter, n-iterations are required for an n-bit converter. *Figure 2* shows a typical example of a 3-bit converter. In the ADC0808, ADC0809, the approximation technique is extended to 8 bits using the 256R network.

The A/D converter's successive approximation register (SAR) is reset on the positive edge of the start conversion (SC) pulse. The conversion is begun on the falling edge of the start conversion pulse. A conversion in process will be interrupted by receipt of a new start conversion pulse. Continuous conversion may be accomplished by tying the end-of-conversion (EOC) output to the SC input. If used in this mode, an external start conversion pulse should be applied after power up. End-of-conversion will go low between 0 and 8 clock pulses after the rising edge of start conversion.

The most important section of the A/D converter is the comparator. It is this section which is responsible for the ultimate accuracy of the entire converter. It is also the comparator drift which has the greatest influence on the repeatability of the device. A chopper-stabilized comparator provides the most effective method of satisfying all the converter requirements.

The chopper-stabilized comparator converts the DC input signal into an AC signal. This signal is then fed through a high gain AC amplifier and has the DC level restored. This technique limits the drift component of the amplifier since the drift is a DC component which is not passed by the AC amplifier. This makes the entire A/D converter extremely insensitive to temperature, long term drift and input offset errors.

Figure 4 shows a typical error curve for the ADC0808 as measured using the procedures outlined in AN-179.

Functional Description (Continued)

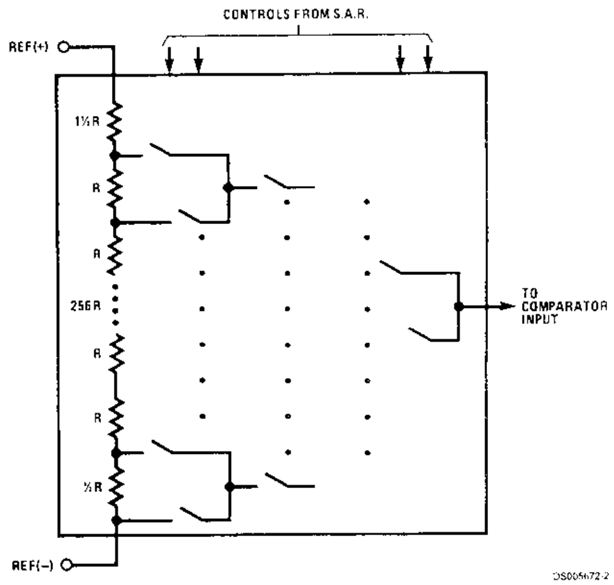


FIGURE 1. Resistor Ladder and Switch Tree

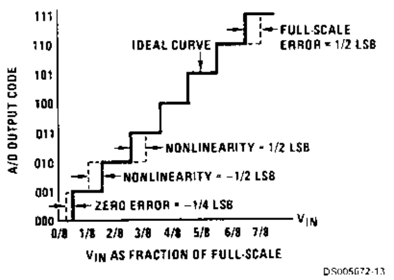


FIGURE 2. 3-Bit A/D Transfer Curve

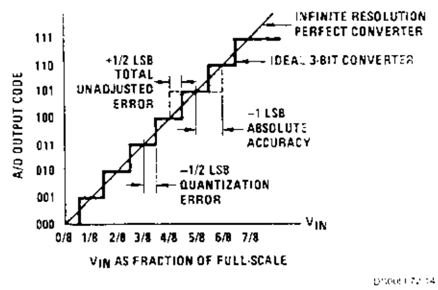


FIGURE 3. 3-Bit A/D Absolute Accuracy Curve

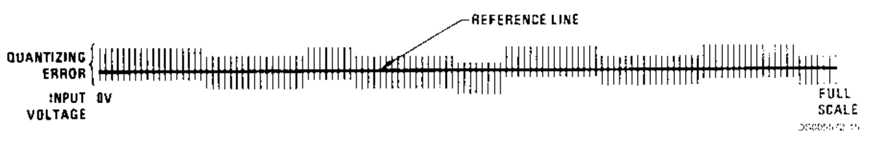


FIGURE 4. Typical Error Curve

Timing Diagram

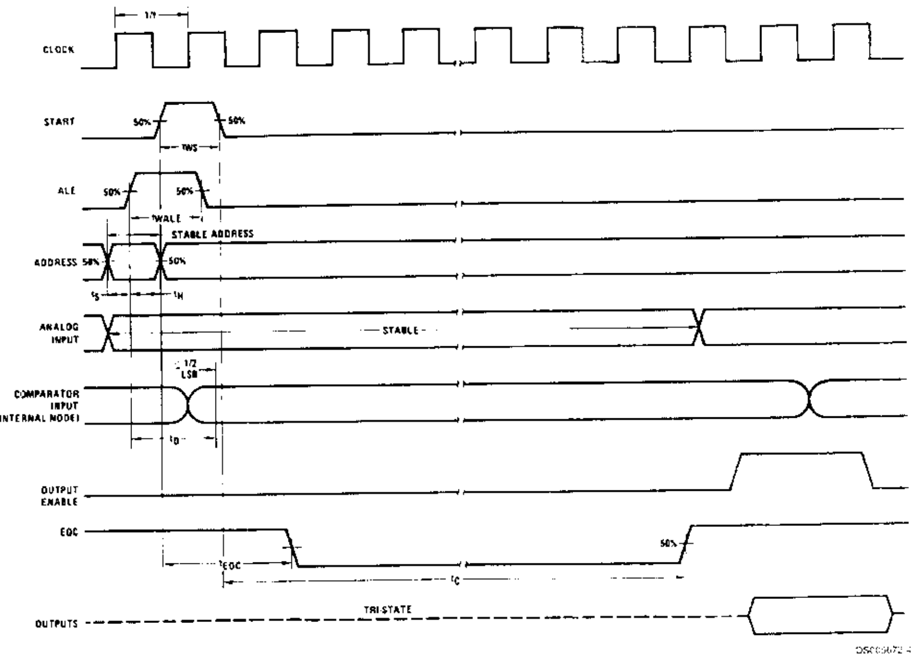


FIGURE 5.

Typical Performance Characteristics

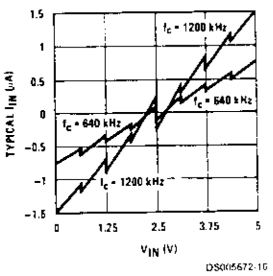


FIGURE 6. Comparator I_{IN} vs V_{IN} (V_{CC}=V_{REF}=5V)

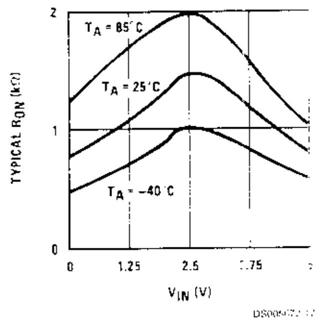


FIGURE 7. Multiplexer R_{ON} vs V_{IN} (V_{CC}=V_{REF}=5V)

TRI-STATE Test Circuits and Timing Diagrams

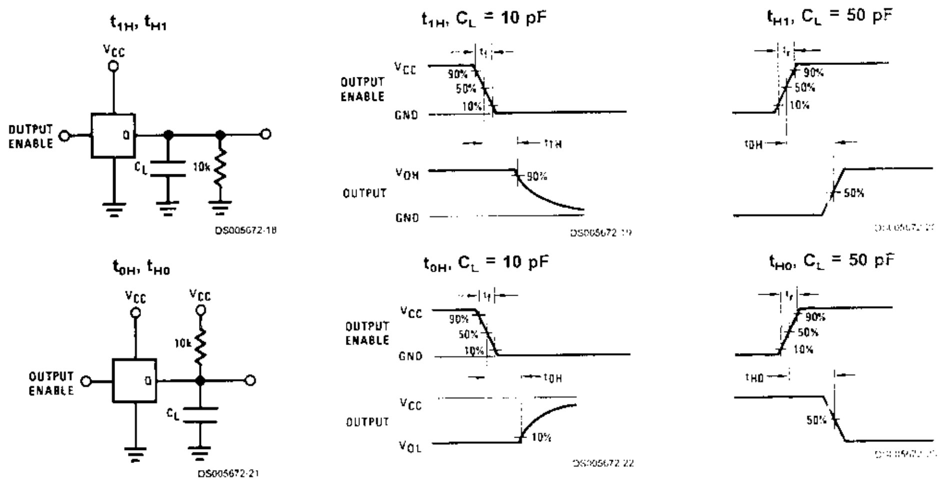


FIGURE 8.

Applications Information

OPERATION

1.0 RATIOMETRIC CONVERSION

The ADC0808, ADC0809 is designed as a complete Data Acquisition System (DAS) for ratiometric conversion systems. In ratiometric systems, the physical variable being measured is expressed as a percentage of full-scale which is not necessarily related to an absolute standard. The voltage input to the ADC0808 is expressed by the equation

$$\frac{V_{IN}}{V_{fs}-V_Z}=\frac{D_X}{D_{MAX}-D_{MIN}} \qquad (1)$$

V_{IN}=Input voltage into the ADC0808

V_{fs}=Full-scale voltage

V_Z=Zero voltage

D_X=Data point being measured

D_{MAX}=Maximum data limit

D_{MIN}=Minimum data limit

A good example of a ratiometric transducer is a potentiometer used as a position sensor. The position of the wiper is directly proportional to the output voltage which is a ratio of the full-scale voltage across it. Since the data is represented as a proportion of full-scale, reference requirements are greatly reduced, eliminating a large source of error and cost for many applications. A major advantage of the ADC0808, ADC0809 is that the input voltage range is equal to the supply range so the transducers can be connected directly across the supply and their outputs connected directly into the multiplexer inputs, (*Figure 9*).

Ratiometric transducers such as potentiometers, strain gauges, thermistor bridges, pressure transducers, etc., are suitable for measuring proportional relationships; however, many types of measurements must be referred to an absolute standard such as voltage or current. This means a sys-

Applications Information (Continued)

tem reference must be used which relates the full-scale voltage to the standard volt. For example, if $V_{CC}=V_{REF}=5.12V$, then the full-scale range is divided into 256 standard steps. The smallest standard step is 1 LSB which is then 20 mV.

2.0 RESISTOR LADDER LIMITATIONS

The voltages from the resistor ladder are compared to the selected into 8 times in a conversion. These voltages are coupled to the comparator via an analog switch tree which is referenced to the supply. The voltages at the top, center and bottom of the ladder must be controlled to maintain proper operation.

The top of the ladder, Ref(+), should not be more positive than the supply, and the bottom of the ladder, Ref(−), should not be more negative than ground. The center of the ladder voltage must also be near the center of the supply because the analog switch tree changes from N-channel switches to P-channel switches. These limitations are automatically satisfied in ratiometric systems and can be easily met in ground referenced systems.

Figure 10 shows a ground referenced system with a separate supply and reference. In this system, the supply must be trimmed to match the reference voltage. For instance, if a 5.12V is used, the supply should be adjusted to the same voltage within 0.1V.

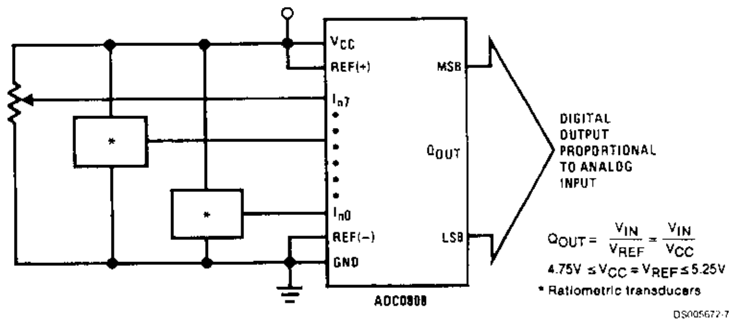
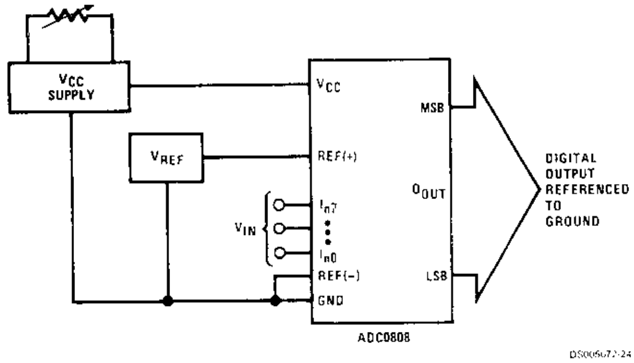


FIGURE 9. Ratiometric Conversion System

The ADC0808 needs less than a milliamp of supply current so developing the supply from the reference is readily accomplished. In *Figure 11* a ground referenced system is shown which generates the supply from the reference. The buffer shown can be an op amp of sufficient drive to supply the milliamp of supply current and the desired bus drive, or if a capacitive bus is driven by the outputs a large capacitor will supply the transient supply current as seen in *Figure 12*. The LM301 is overcompensated to insure stability when loaded by the 10 µF output capacitor.

The top and bottom ladder voltages cannot exceed V_{CC} and ground, respectively, but they can be symmetrically less than V_{CC} and greater than ground. The center of the ladder voltage should always be near the center of the supply. The sensitivity of the converter can be increased, (i.e., size of the LSB steps decreased) by using a symmetrical reference system. In *Figure 13*, a 2.5V reference is symmetrically centered about $V_{CC}/2$ since the same current flows in identical resistors. This system with a 2.5V reference allows the LSB bit to be half the size of a 5V reference system.

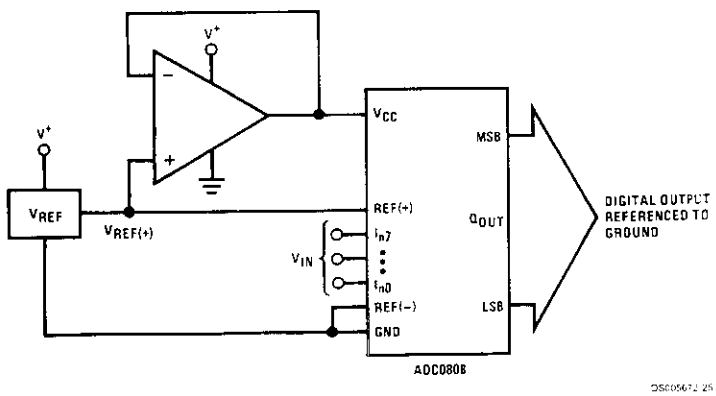
Applications Information (Continued)



$D_{OUT} = \frac{V_{IN}}{V_{REF}}$

$4.75V \leq V_{CC} = V_{REF} \leq 5.25V$

FIGURE 10. Ground Referenced Conversion System Using Trimmed Supply



$D_{OUT} = \frac{V_{IN}}{V_{REF}}$

$4.75V \leq V_{CC} = V_{REF} \leq 5.25V$

FIGURE 11. Ground Referenced Conversion System with Reference Generating V_{CC} Supply

Applications Information (Continued)

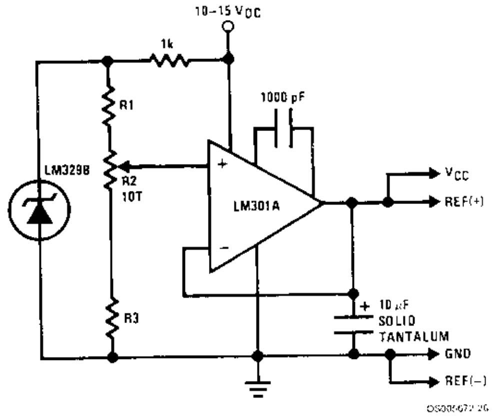
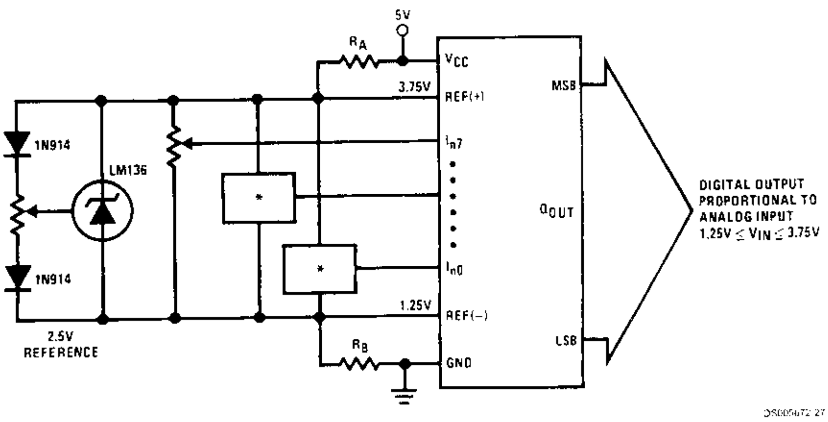


FIGURE 12. Typical Reference and Supply Circuit



$R_A = R_B$

*Ratiometric transducers

FIGURE 13. Symmetrically Centered Reference

3.0 CONVERTER EQUATIONS

The transition between adjacent codes N and N+1 is given by:

$$V_{IN} = \left\{ (V_{REF(+)} - V_{REF(-)}) \left[\frac{N}{256} + \frac{1}{512} \right] \pm V_{TUE} \right\} + V_{REF(-)} \quad (2)$$

The center of an output code N is given by:

$$V_{IN} = \left\{ (V_{REF(+)} - V_{REF(-)}) \left[\frac{N}{256} \right] \pm V_{TUE} \right\} + V_{REF(-)} \quad (3)$$

The output code N for an arbitrary input are the integers within the range:

$$N = \frac{V_{IN} - V_{REF(-)}}{V_{REF(+)} - V_{REF(-)}} \times 256 \pm \text{Absolute Accuracy} \quad (4)$$

Where: V_{IN}=Voltage at comparator input

$V_{REF(+)}$=Voltage at Ref(+)

$V_{REF(-)}$=Voltage at Ref(−)

V_{TUE}=Total unadjusted error voltage (typically $V_{REF(+)} \div 512$)

Applications Information (Continued)

4.0 ANALOG COMPARATOR INPUTS

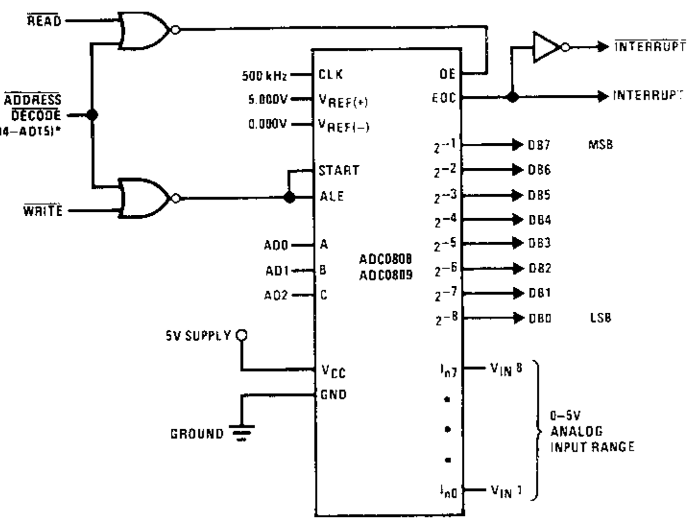
The dynamic comparator input current is caused by the periodic switching of on-chip stray capacitances. These are connected alternately to the output of the resistor ladder/switch tree network and to the comparator input as part of the operation of the chopper stabilized comparator.

The average value of the comparator input current varies directly with clock frequency and with V_{IN} as shown in *Figure 6*.

If no filter capacitors are used at the analog inputs and the signal source impedances are low, the comparator input current should not introduce converter errors, as the transient created by the capacitance discharge will die out before the comparator output is strobed.

If input filter capacitors are desired for noise reduction and signal conditioning they will tend to average out the dynamic comparator input current. It will then take on the characteristics of a DC bias current whose effect can be predicted conventionally.

Typical Application

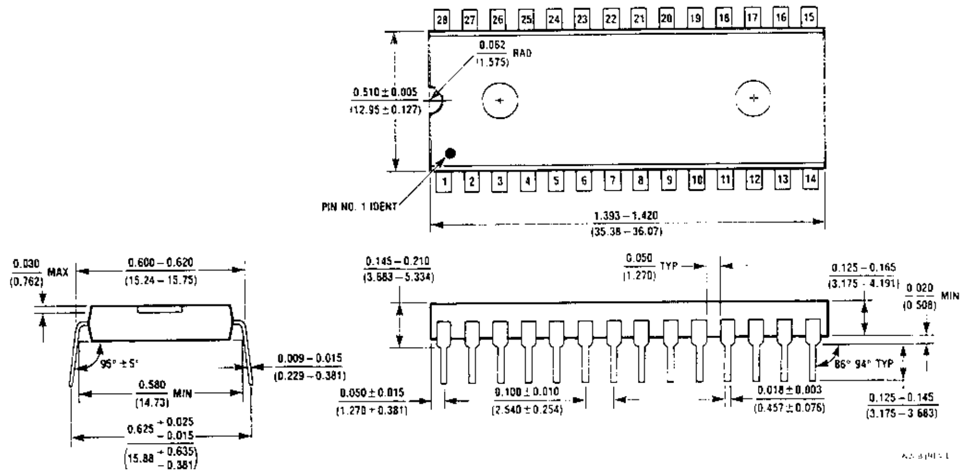


*Address latches needed for 8085 and SC/MP interfacing the ADC0808 to a microprocessor

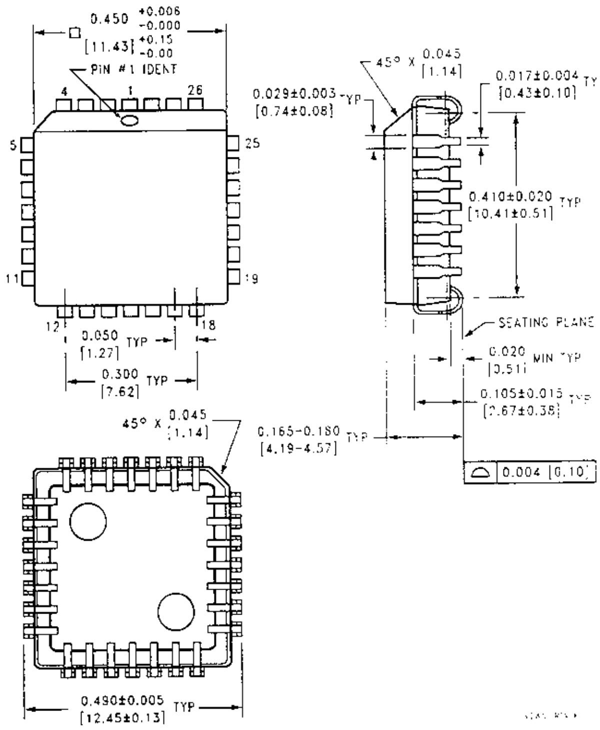
TABLE 2. Microprocessor Interface Table

PROCESSOR	$\overline{\text{READ}}$	$\overline{\text{WRITE}}$	INTERRUPT (COMMENT)
8080	$\overline{\text{MEMR}}$	$\overline{\text{MEMW}}$	INTR (Thru RST Circuit)
8085	$\overline{\text{RD}}$	$\overline{\text{WR}}$	INTR (Thru RST Circuit)
Z-80	$\overline{\text{RD}}$	$\overline{\text{WR}}$	$\overline{\text{INT}}$ (Thru RST Circuit, Mode 0)
SC/MP	NRDS	NWDS	SA (Thru Sense A)
6800	VMA•φ2•R/W	VMA•φ•$\overline{\text{R/W}}$	$\overline{\text{IRQA}}$ or $\overline{\text{IRQB}}$ (Thru PIA)

Physical Dimensions inches (millimeters) unless otherwise noted



Molded Dual-In-Line Package (N)
Order Number ADC0808CCN or ADC0809CCN
NS Package Number N28B



Molded Chip Carrier (V)
Order Number ADC0808CCV or ADC0809CCV
NS Package Number V28A

UT62256

32K X 8 BIT LOW POWER CMOS SRAM

FEATURES

- Access time : 35/70ns (max.)
- Low power consumption:
  Operating : 60/40 mA (typical.)
  Standby : 3mA (typical) normal
  2uA (typical) L-version
  1uA (typical) LL-version
- Single 5V power supply
- All inputs and outputs are TTL compatible
- Fully static operation
- Three state outputs
- Data retention voltage : 2V (min.)
- Package : 28-pin 600 mil PDIP
  28-pin 330 mil SOP
  28-pin 8x13.4mm STSOP

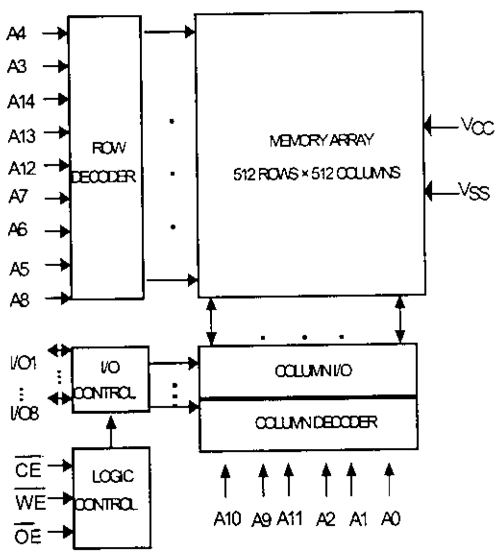
GENERAL DESCRIPTION

The UT62256 is a 262,144-bit low power CMOS static random access memory organized as 32,768 words by 8 bits. It is fabricated using high performance, high reliability CMOS technology.

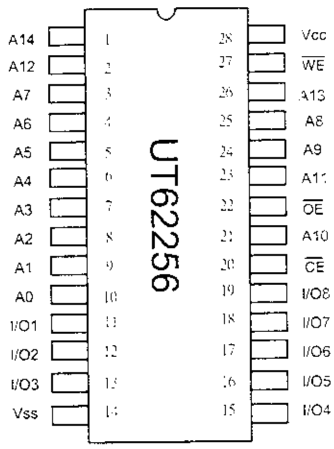
The UT62256 is designed for high-speed and low power application. It is particularly well suited for battery back-up nonvolatile memory application.

The UT62256 operates from a single 5V power supply and all inputs and outputs are fully TTL compatible

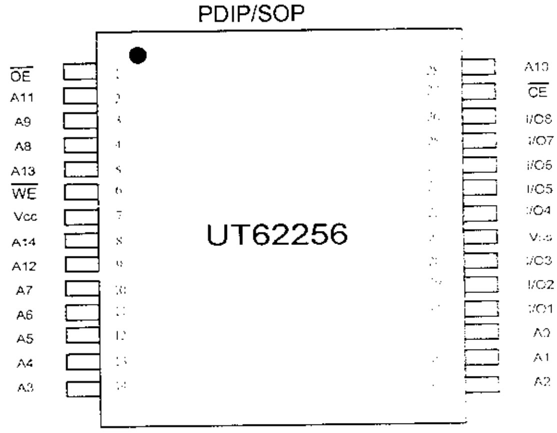
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



PDIP/SOP



STSOP

PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A14	Address Inputs
I/O1 - I/O8	Data Inputs/Outputs
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
V_{CC}	Power Supply
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Terminal Voltage with Respect to V_{SS}	V_{TERM}	-0.5 to +7.0	V
Operating Temperature	T_A	0 to +70	℃
Storage Temperature	T_{STG}	-65 to +150	℃
Power Dissipation	P_D	1	W
DC Output Current	I_{OUT}	50	mA
Soldering Temperature (under 10 sec0	Tsolder	260	℃

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those incicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O OPERATION	SUPPLY CURRENT
Standby	H	X	X	High - Z	ISB, ISB1
Output Disable	L	H	H	High - Z	I_{CC}
Read	L	L	H	D_{OUT}	I_{CC}
Write	L	X	L	D_{IN}	I_{CC}

Note: H = V_{IH}, L=V_{IL}, X = Don't care.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V±10%, TA = 0℃ to 70℃)

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Input High Voltage	V_{IH}			2.2	-	V_{CC}+0.5	V
Input Low Voltage	V_{IL}			- 0.5	-	0.8	V
Input Leakage Current	I_{LI}	$V_{SS} \leq V_{IN} \leq V_{CC}$		- 1	-	1	μA
Output Leakage Current	I_{LO}	$V_{SS} \leq V_{I/O} \leq V_{CC}$ $\overline{CE}=V_{IH}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$		- 1	-	1	μA
Output High Voltage	V_{OH}	I_{OH}= - 1mA		2.4	-	-	V
Output Low Voltage	V_{OL}	I_{OL}= 4mA		-	-	0.4	V
Operating Power Supply Current	I_{CC}	Cycle time=Min, $I_{I/O}$ = 0mA , $\overline{CE}=V_{IL}$	- 35	-	60	100	mA
			- 70	-	40	70	mA
Standby Power Supply Current	I_{SB}	$\overline{CE}=V_{IH}$	normal	-	1	10	mA
	I_{SB1}	$\overline{CE} \geq V_{CC}$-0.2V		-	0.3	5	mA
	I_{SB}	$\overline{CE}=V_{IH}$	-L/-LL	-	-	3	mA
	I_{SB1}	$\overline{CE} \geq V_{CC}$-0.2V	-L	-	2	100	μA
			-LL	-	1	50	μA

CAPACITANCE (TA=25℃, f=1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C_{IN}	-	8	pF
Input/Output Capacitance	$C_{I/O}$	-	10	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	C_L = 100pF, I_{OH}/I_{OL} = -1mA/4mA

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V±10% , TA = 0℃ to 70℃)

(1) READ CYCLE

PARAMETER	SYMBOL	UT62256-35		UT62256-70		UNIT
		MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t_{RC}	35	-	70	-	ns
Address Access Time	t_{AA}	-	35	-	70	ns
Chip Enable Access Time	t_{ACE}	-	35	-	70	ns
Output Enable Access Time	t_{OE}	-	25	-	35	ns
Chip Enable to Output in Low Z	t_{CLZ}*	10	-	10	-	ns
Output Enable to Output in Low Z	t_{OLZ}*	5	-	5	-	ns
Chip Disable to Output in High Z	t_{CHZ}*	-	25	-	35	ns
Output Disable to Output in High Z	t_{OHZ}*	-	25	-	35	ns
Output Hold from Address Change	t_{OH}	5	-	5	-	ns

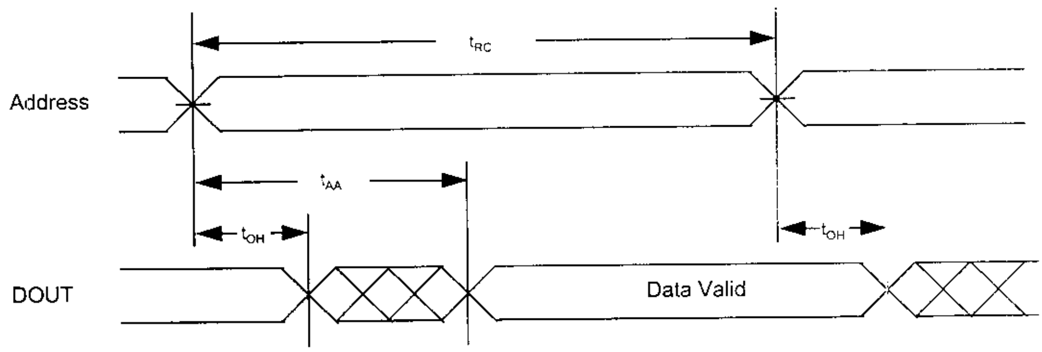
(2) WRITE CYCLE

PARAMETER	SYMBOL	UT62256-35		UT62256-70		UNIT
		MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t_{WC}	35	-	70	-	ns
Address Valid to End of Write	t_{AW}	30	-	60	-	ns
Chip Enable to End of Write	t_{CW}	30	-	60	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	ns
Write Pulse Width	t_{WP}	25	-	50	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	ns
Data to Write Time Overlap	t_{DW}	20	-	30	-	ns
Data Hold from End of Write Time	t_{DH}	0	-	0	-	ns
Output Active from End of Write	t_{OW}*	5	-	5	-	ns
Write to Output in High Z	t_{WHZ}*	-	15	-	25	ns

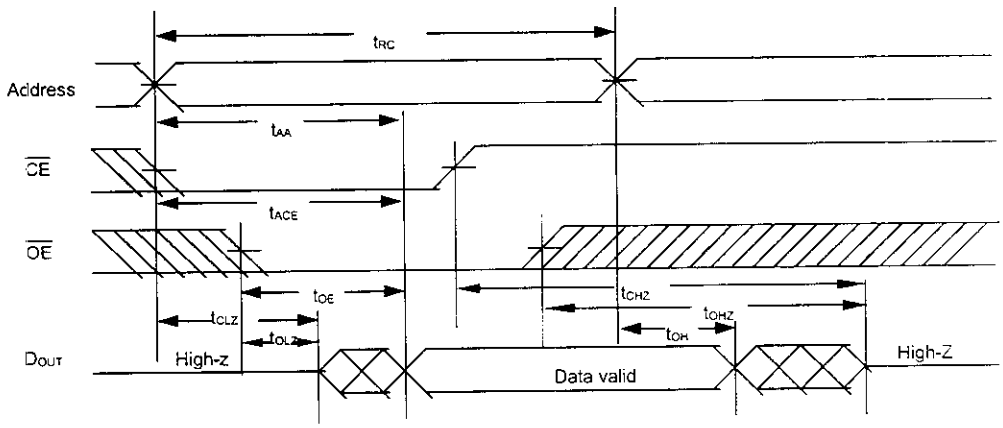
*These parameters are guaranteed by device characterization, but not production tested.

TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2,4)



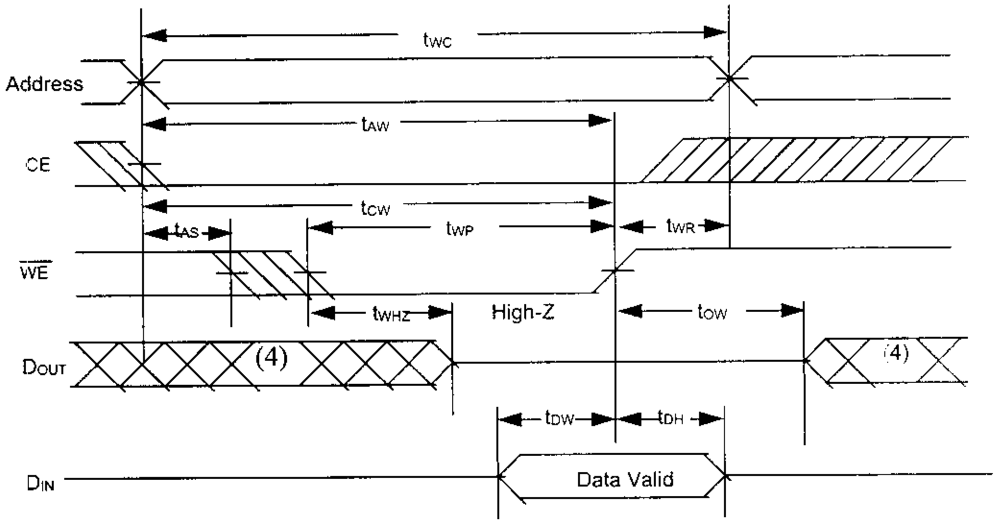
READ CYCLE 2 ($\overline{CE}$ and $\overline{OE}$ Controlled) (1,3,5,6)



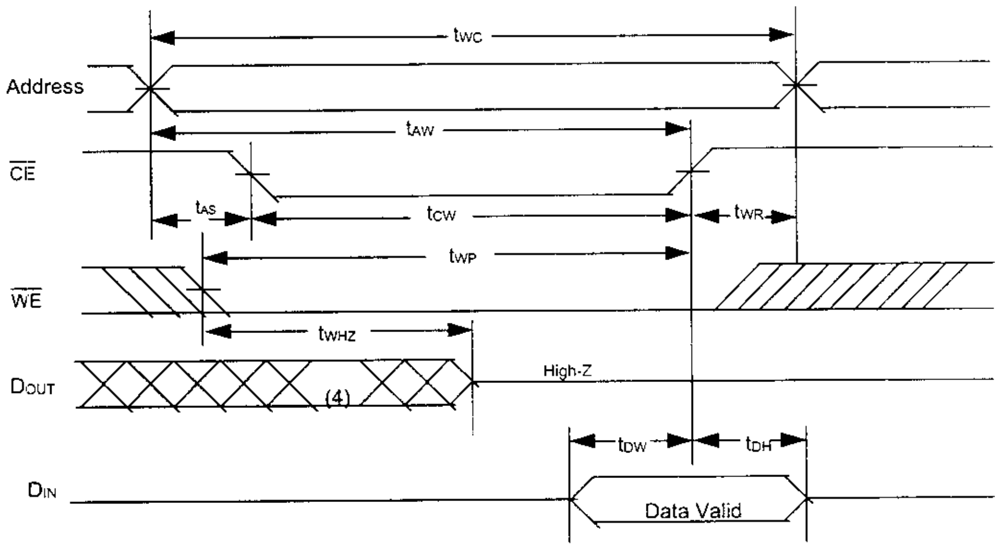
Notes :

1. $\overline{WE}$ is HIGH for read cycle.
2. Device is continuously selected $\overline{CE}$ = V_{IL}.
3. Address must be valid prior to or coincident with $\overline{CE}$ transition; otherwise t_{AA} is the limiting parameter.
4. $\overline{OE}$ is LOW.
5. t_{CLZ}, t_{OLZ}, t_{CHZ} and t_{OHZ} are specified with C_L = 5pF. Transition is measured ±500mV from steady state.
6. At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ}, t_{OHZ} is less than t_{OLZ}.

WRITE CYCLE 1 ($\overline{WE}$ Controlled) (1,2,3,5)



WRITE CYCLE 2 ($\overline{CE}$ Controlled) (1,2,5)



Notes :

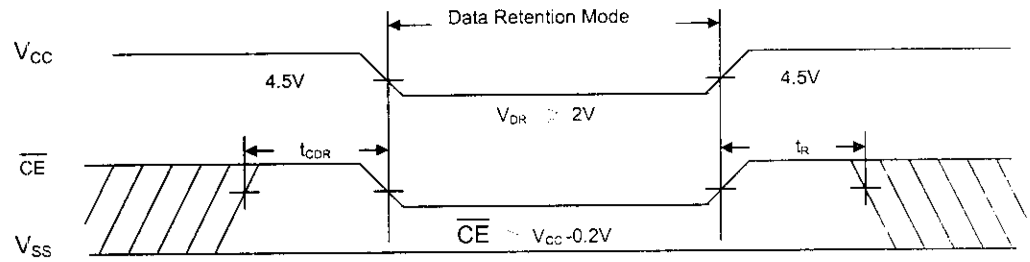
1. $\overline{WE}$ or $\overline{CE}$ must be HIGH during all address transitions.
2. A write occurs during the overlap of a low $\overline{CE}$ and a low $\overline{WE}$.
3. During a $\overline{WE}$ controlled with write cycle with $\overline{OE}$ LOW, t_{WP} must be greater than $t_{WHZ}+t_{OW}$ to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CE}$ LOW transition occurs simultaneously with or after $\overline{WE}$ LOW transition, the outputs remain in a high impedance state.
6. t_{OW} and t_{WHZ} are specified with C_L = 5pF. Transition is measured ±500mV from steady state.

DATA RETENTION CHARACTERISTICS (TA = 0℃ to 70℃)

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Vcc for Data Retention	V_{DR}	$\overline{CE} \geq V_{CC}$-0.2V		2.0	-	5.5	V
Data Retention Current	I_{DR}	Vcc=3V $\overline{CE} \geq V_{CC}$-0.2V	- L	-	1	50	μA
						20*	μA
			- LL	-	0.5	20	μA
						5*	μA
Chip Disable to Data Retention Time	t_{CDR}	See Data Retention Waveforms (below)		0	-	-	ns
Recovery Time	t_R			t_{RC^*}	-	-	ns

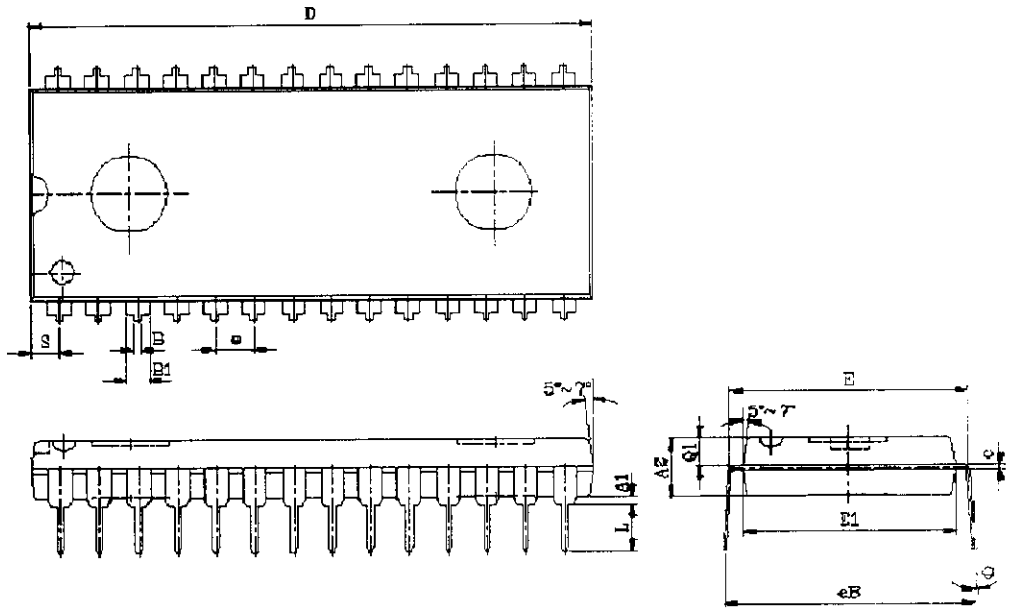
t_{RC^*} = Read Cycle Time
* Those parameters are limited for temperature below 40 ℃

DATA RETENTION WAVEFORM



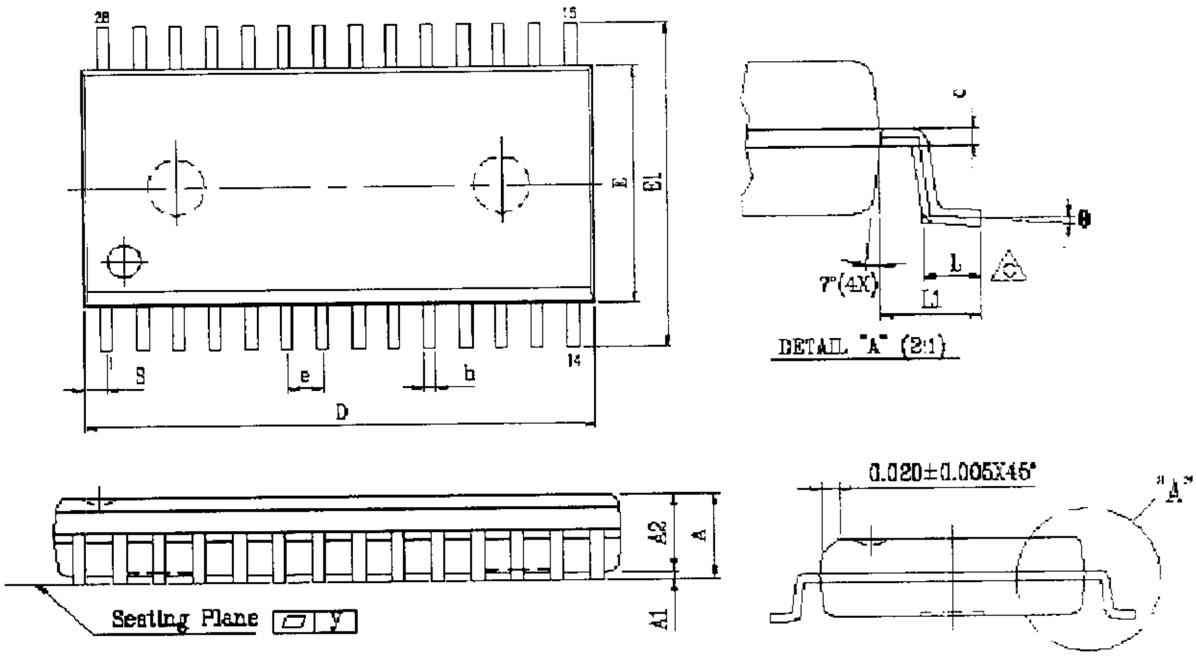
PACKAGE OUTLINE DIMENSION

28 pin 600 mil PDIP Package Outline Dimension



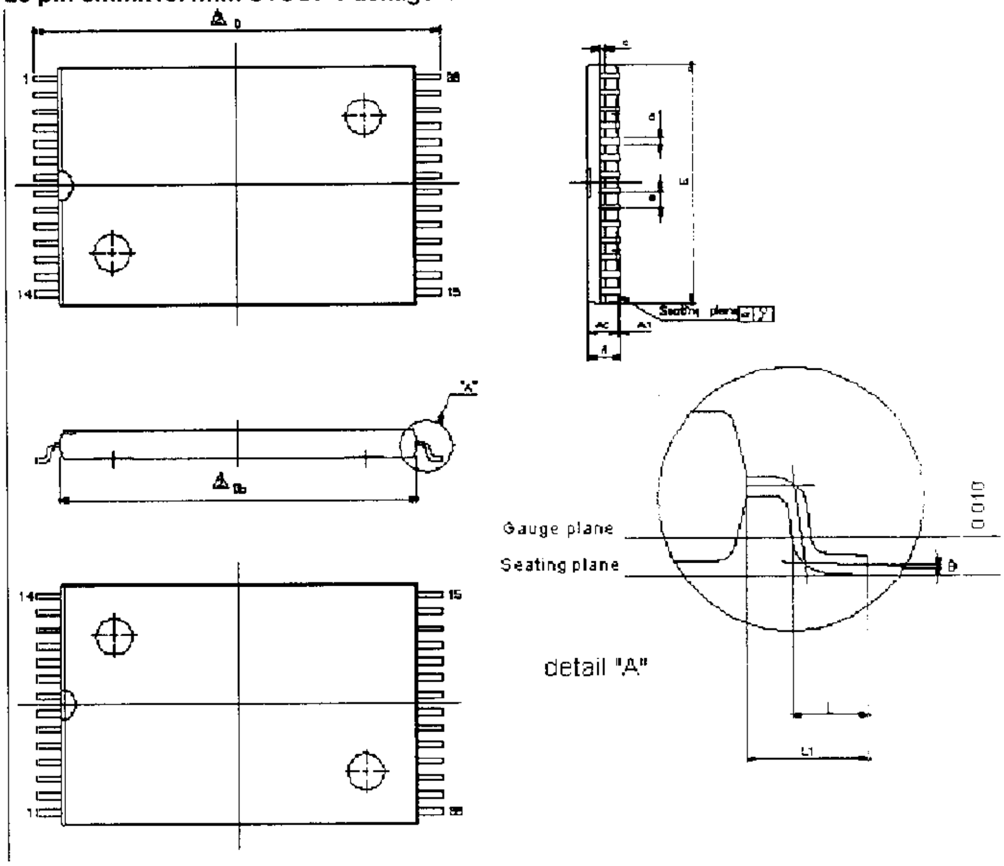
SYMBOL \ UNIT	INCH(BASE)	MM(REF)
A1	0.010 (MIN)	0.254 (MIN)
A2	0.150±0.005	3.810±0.127
B	0.020 (MAX)	0.508(MAX)
B1	0.055 (MAX)	1.397(MAX)
c	0.012 (MAX)	0.304 (MAX)
D	1.430 (MAX)	36.322 (MAX)
E	0.6 (TYP)	15.24 (TYP)
E1	0.52 (MAX)	13.208 (MAX)
e	0.100 (TYP)	2.540(TYP)
eB	0.625 (MAX)	15.87 (MAX)
L	0.180(MAX)	4.572(MAX)
S	0.06 (MAX)	1.524 (MAX)
Q1	0.08(MAX)	2.032(MAX)
Θ	15°(MAX)	15°(MAX)

28 pin 330 mil SOP Package Outline Dimension



	SYMBOL \ UNIT	INCH(BASE)	MM(REF)
	A	0.120 (MAX)	3.048 (MAX)
	A1	0.002(MIN)	0.05(MIN)
	A2	0.098±0.005	2.489±0.127
	b	0.0016 (TYP)	0.406(TYP)
	c	0.010 (TYP)	0.254(TYP)
	D	0.728 (MAX)	18.491 (MAX)
	E	0.340 (MAX)	8.636 (MAX)
△B	E1	0.465±0.012	11.811±0.305
	e	0.050 (TYP)	1.270(TYP)
△C	L	0.05 (MAX)	1.270 (MAX)
	L1	0.067±0.008	1.702 ±0.203
	S	0.047 (MAX)	1.194 (MAX)
△E	y	0.003(MAX)	0.076(MAX)
	θ	0°～10°	0°～10°

28 pin 8mmx13.4mm STSOP Package Outline Dimension



	SYMBOL \ UNIT	INCH(BASE)	MM(REF)
	A	0.047 (MAX)	1.20 (MAX)
	A1	0.004±0.002	0.10±0.05
	A2	0.039±0.002	1.00±0.05
	b	0.006 (TYP)	0.15(TYP)
	c	0.010 (TYP)	0.254(TYP)
△2	Db	0.465±0.004	11.80±0.10
	E	0.315±0.004	8.00±0.10
	e	0.022 (TYP)	0.55(TYP)
△2	D	0.528±0.008	13.40±0.20
△2	L	0.020±0.004	0.50±0.10
△2	L1	0.0315±0.004	0.80±0.10
△5	y	0.08(MAX)	0.003(MAX)
	Θ	0°~5°	0°~5°

Note :
E dimension is not including end flash the total of both sides' end flash is not above 0.3mm.

ORDERING INFORMATION

PART NO.	ACCESS TIME (ns)	STANDBY CURRENT (μA)	PACKAGE
UT62256PC-70	70	5 mA	28PIN PDIP
UT62256PC-70L	70	100 μA	28PIN PDIP
UT62256PC-70LL	70	50 μA	28PIN PDIP
UT62256SC-35	35	5 mA	28PIN SOP
UT62256SC-35L	35	100 μA	28PIN SOP
UT62256SC-35LL	35	50 μA	28PIN SOP
UT62256SC-70	70	5 mA	28PIN SOP
UT62256SC-70L	70	100 μA	28PIN SOP
UT62256SC-70LL	70	50 μA	28PIN SOP
UT62256LS-35L	35	100 μA	28PIN STSOP
UT62256LS-35LL	35	50 μA	28PIN STSOP
UT62256LS-70L	70	100 μA	28PIN STSOP
UT62256LS-70LL	70	50 μA	28PIN STSOP

REVISION HISTORY

REVISION	DESCRIPTION	DATE
REV. 1.0	Original.	
REV 1.1	The value of symbol "E" is revised as 0.35 inch.	AUG. 24,1999
REV. 1.2	Combine version_UT62256(normal) and version_UT62256SC-35 into version_UT62256	DEC. 8,1999
REV. 1.4	1. The pin configurations' name of TSOP-1 is revised as STSOP. 2. The data retention waveform, $\overline{CE} \geqq V_{CC}$-0.2V. (page 6)	MAY. 10,2001
REV. 1.5	Add data retention current for temperature below 40℃.	JUL.11 ,2001

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT573
Octal D-type transparent latch; 3-state

Product specification
File under Integrated Circuits, IC06

December 1990

Philips
Semiconductors

PHILIPS

FEATURES

- Inputs and outputs on opposite sides of package allowing easy interface with microprocessors
- Useful as input or output port for microprocessors/microcomputers
- 3-state non-inverting outputs for bus oriented applications
- Common 3-state output enable input
- Functionally identical to the "563" and "373"
- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT573 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT573 are octal D-type transparent latches featuring separate D-type inputs for each latch and 3-state outputs for bus oriented applications.
A latch enable (LE) input and an output enable ($\overline{OE}$) input are common to all latches.

The "573" consists of eight D-type transparent latches with 3-state true outputs. When LE is HIGH, data at the D_n inputs enter the latches. In this condition the latches are transparent, i.e. a latch output will change state each time its corresponding D-input changes.

When LE is LOW the latches store the information that was present at the D-inputs a set-up time preceding the HIGH-to-LOW transition of LE.
When $\overline{OE}$ is LOW, the contents of the 8 latches are available at the outputs.
When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state.
Operation of the $\overline{OE}$ input does not affect the state of the latches.

The "573" is functionally identical to the "563" and "373", but the "563" has inverted outputs and the "373" has a different pin arrangement.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay	C_L = 15 pF; V_{CC} = 5 V			
	D_n to Q_n		14	17	ns
	LE to Q_n		15	15	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per latch	notes 1 and 2	26	26	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

   f_i = input frequency in MHz; f_o = output frequency in MHz

   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

   C_L = output load capacitance in pF; V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}; for HCT the condition is V_I = GND to V_{CC} − 1.5 V

ORDERING INFORMATION

See *"74HC/HCT/HCU/HCMOS Logic Package Information"*.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
2, 3, 4, 5, 6, 7, 8, 9	D_0 to D_7	data inputs
11	LE	latch enable input (active HIGH)
1	$\overline{OE}$	3-state output enable input (active LOW)
10	GND	ground (0 V)
19, 18, 17, 16, 15, 14, 13, 12	Q_0 to Q_7	3-state latch outputs
20	V_{CC}	positive supply voltage

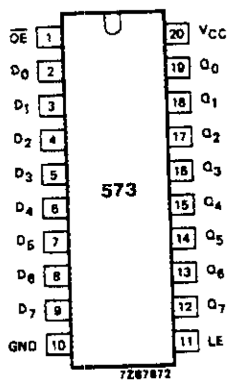


Fig.1 Pin configuration.

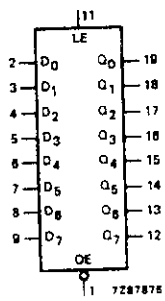


Fig.2 Logic symbol.

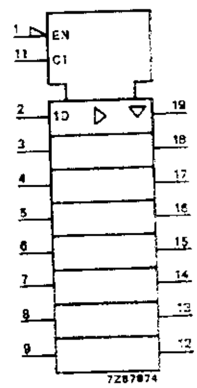


Fig.3 IEC logic symbol.

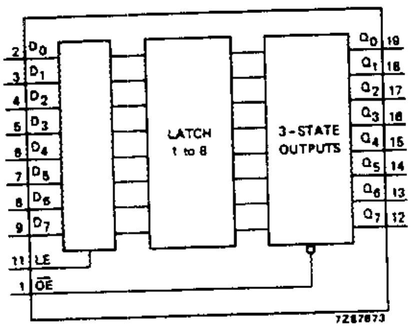


Fig.4 Functional diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL LATCHES	OUTPUTS
	$\overline{OE}$	LE	D_N		Q_0 to Q_7
enable and read register (transparent mode)	L L	H H	L H	L H	L H
latch and read register	L L	L L	l h	L H	L H
latch register and disable outputs	H H	L L	l h	L H	Z Z

Notes

1. H = HIGH voltage level
   h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition
   L = LOW voltage level
   l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition
   Z = high impedance OFF-state

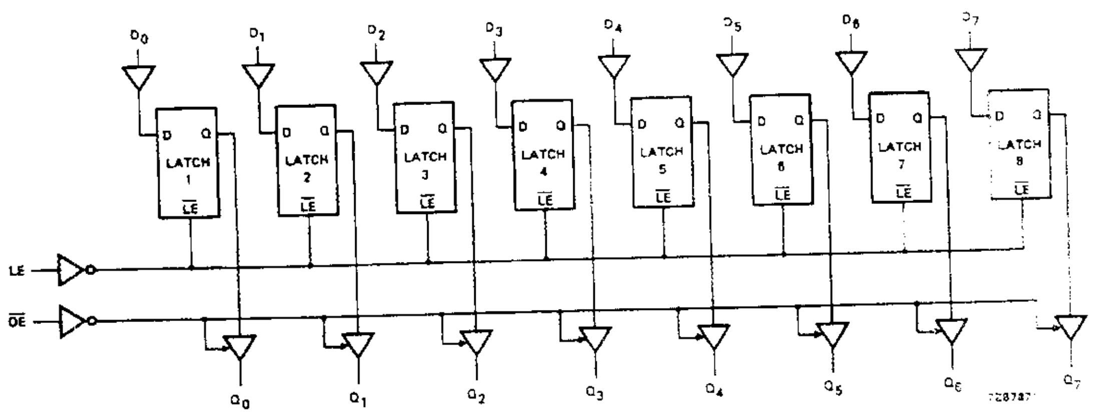


Fig.5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	Tamb (°C) 74HC +25 min.	typ.	max.	−40 to +85 min.	max.	−40 to +125 min.	max.	UNIT	TEST CONDITIONS V_{CC} (V)	WAVEFORMS
t_{PHL}/t_{PLH}	propagation delay D_n to Q_n		47 17 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.6
t_{PHL}/t_{PLH}	propagation delay LE to Q_n		50 18 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.7
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to Q_n		44 16 13	140 28 24		175 35 30		210 42 36	ns	2.0 4.5 6.0	Fig.8
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to Q_n		55 20 16	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.8
t_{THL}/t_{TLH}	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig.6
t_W	enable pulse width HIGH	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.7
t_{su}	set-up time D_n to LE	50 10 9	11 4 3		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig.9
t_h	hold time D_n to LE	5 5 5	3 1 1		5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig.9

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

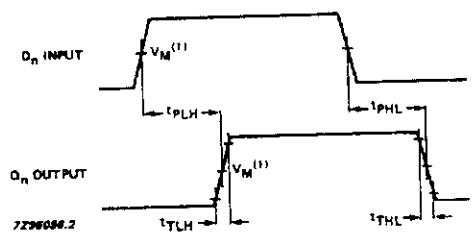
INPUT	UNIT LOAD COEFFICIENT
D_n	0.35
LE	0.65
$\overline{OE}$	1.25

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

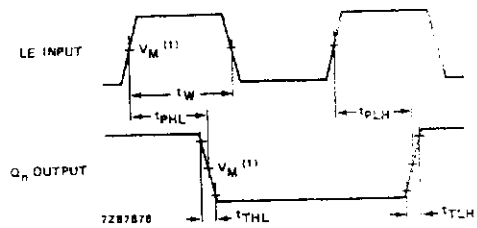
SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay D_n to Q_n		20	35		44		53	ns	4.5	Fig.6
t_{PHL}/t_{PLH}	propagation delay LE to Q_n		18	35		44		53	ns	4.5	Fig.7
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to Q_n		17	30		38		45	ns	4.5	Fig.8
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to Q_n		18	30		38		45	ns	4.5	Fig.8
t_{THL}/t_{TLH}	output transition time		5	12		15		18	ns	4.5	Fig.6
t_W	enable pulse width HIGH	16	5		20		24		ns	4.5	Fig.7
t_{su}	set-up time D_n to LE	13	7		16		20		ns	4.5	Fig.9
t_h	hold time D_n to LE	9	4		11		14		ns	4.5	Fig.9

AC WAVEFORMS



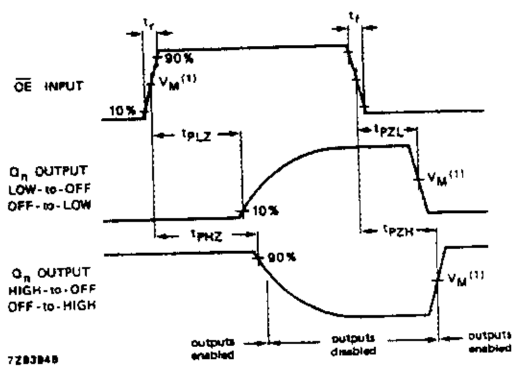
(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.6 Waveforms showing the data input (D_n) to output (Q_n) propagation delays and the output transition times.



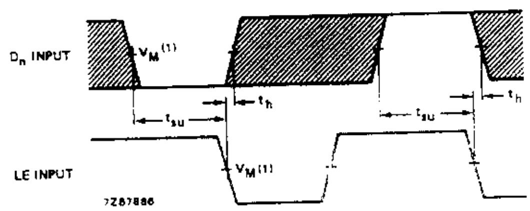
(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.7 Waveforms showing the latch enable input (LE) pulse width, the latch enable input to output (Q_n) propagation delays and the output transition times.



(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.8 Waveforms showing the 3-state enable and disable times.



The shaded areas indicate when the input is permitted to change for predictable output performance.

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.9 Waveforms showing the data set-up and hold times for D_n input to LE input.

PACKAGE OUTLINES

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.

19-4323; Rev 9; 4/00

MAXIM

+5V-Powered, Multichannel RS-232 Drivers/Receivers

MAX220–MAX249

General Description

The MAX220–MAX249 family of line drivers/receivers is intended for all EIA/TIA-232E and V.28/V.24 communications interfaces, particularly applications where ±12V is not available.

These parts are especially useful in battery-powered systems, since their low-power shutdown mode reduces power dissipation to less than 5μW. The MAX225, MAX233, MAX235, and MAX245/MAX246/MAX247 use no external components and are recommended for applications where printed circuit board space is critical.

Applications

Portable Computers

Low-Power Modems

Interface Translation

Battery-Powered RS-232 Systems

Multidrop RS-232 Networks

Features

Superior to Bipolar

- ♦ **Operate from Single +5V Power Supply (+5V and +12V—MAX231/MAX239)**
- ♦ **Low-Power Receive Mode in Shutdown (MAX223/MAX242)**
- ♦ **Meet All EIA/TIA-232E and V.28 Specifications**
- ♦ **Multiple Drivers and Receivers**
- ♦ **3-State Driver and Receiver Outputs**
- ♦ **Open-Line Detection (MAX243)**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX220CPE	0°C to +70°C	16 Plastic DIP
MAX220CSE	0°C to +70°C	16 Narrow SO
MAX220CWE	0°C to +70°C	16 Wide SO
MAX220C/D	0°C to +70°C	Dice*
MAX220EPE	-40°C to +85°C	16 Plastic DIP
MAX220ESE	-40°C to +85°C	16 Narrow SO
MAX220EWE	-40°C to +85°C	16 Wide SO
MAX220EJE	-40°C to +85°C	16 CERDIP
MAX220MJE	-55°C to +125°C	16 CERDIP

Ordering Information continued at end of data sheet.

**Contact factory for dice specifications.*

Selection Table

Part Number	Power Supply (V)	No. of RS-232 Drivers/Rx	No. of Ext. Caps	Nominal Cap. Value (μF)	SHDN & Three-State	Rx Active in SHDN	Data Rate (kbps)	Features
MAX220	+5	2/2	4	4.7/10	No	—	120	Ultra-low-power, industry-standard pinout
MAX222	+5	2/2	4	0.1	Yes	—	200	Low-power shutdown
MAX223 (MAX213)	+5	4/5	4	1.0 (0.1)	Yes	✓	120	MAX241 and receivers active in shutdown
MAX225	+5	5/5	0	—	Yes	✓	120	Available in SO
MAX230 (MAX200)	+5	5/0	4	1.0 (0.1)	Yes	—	120	5 drivers with shutdown
MAX231 (MAX201)	+5 and +7.5 to +13.2	2/2	2	1.0 (0.1)	No	—	120	Standard +5/+12V or battery supplies; same functions as MAX232
MAX232 (MAX202)	+5	2/2	4	1.0 (0.1)	No	—	120 (64)	Industry standard
MAX232A	+5	2/2	4	0.1	No	—	200	Higher slew rate, small caps
MAX233 (MAX203)	+5	2/2	0	—	No	—	120	No external caps
MAX233A	+5	2/2	0	—	No	—	200	No external caps, high slew rate
MAX234 (MAX204)	+5	4/0	4	1.0 (0.1)	No	—	120	Replaces 1488
MAX235 (MAX205)	+5	5/5	0	—	Yes	—	120	No external caps
MAX236 (MAX206)	+5	4/3	4	1.0 (0.1)	Yes	—	120	Shutdown, three state
MAX237 (MAX207)	+5	5/3	4	1.0 (0.1)	No	—	120	Complements IBM PC serial port
MAX238 (MAX208)	+5	4/4	4	1.0 (0.1)	No	—	120	Replaces 1488 and 1489
MAX239 (MAX209)	+5 and +7.5 to +13.2	3/5	2	1.0 (0.1)	No	—	120	Standard +5/+12V or battery supplies; single-package solution for IBM PC serial port
MAX240	+5	5/5	4	1.0	Yes	—	120	DIP or flatpack package
MAX241 (MAX211)	+5	4/5	4	1.0 (0.1)	Yes	—	120	Complete IBM PC serial port
MAX242	+5	2/2	4	0.1	Yes	✓	200	Separate shutdown and enable
MAX243	+5	2/2	4	0.1	No	—	200	Open-line detection simplifies cabling
MAX244	+5	8/10	4	1.0	No	—	120	High slew rate
MAX245	+5	8/10	0	—	Yes	✓	120	High slew rate, int. caps, two shutdown modes
MAX246	+5	8/10	0	—	Yes	✓	120	High slew rate, int. caps, three shutdown modes
MAX247	+5	8/9	0	—	Yes	✓	120	High slew rate, int. caps, nine operating modes
MAX248	+5	8/8	4	1.0	Yes	✓	120	High slew rate, selective half-chip enables
MAX249	+5	6/10	4	1.0	Yes	✓	120	Available in quad flatpack package

+5V-Powered, Multichannel RS-232 Drivers/Receivers

ABSOLUTE MAXIMUM RATINGS—MAX220/222/232A/233A/242/243

Supply Voltage (V_{CC}) ....-0.3V to +6V
Input Voltages
T_{IN} ....-0.3V to (V_{CC} - 0.3V)
R_{IN} (Except MAX220) ....±30V
R_{IN} (MAX220) ....±25V
T_{OUT} (Except MAX220) (Note 1) ....±15V
T_{OUT} (MAX220) ....±13.2V
Output Voltages
T_{OUT} ....±15V
R_{OUT} ....-0.3V to (V_{CC} + 0.3V)
Driver/Receiver Output Short Circuited to GND..........Continuous
Continuous Power Dissipation (T_A = +70°C)
16-Pin Plastic DIP (derate 10.53mW/°C above +70°C)....842mW
18-Pin Plastic DIP (derate 11.11mW/°C above +70°C)....889mW
20-Pin Plastic DIP (derate 8.00mW/°C above +70°C) ..440mW
16-Pin Narrow SO (derate 8.70mW/°C above +70°C) ...696mW
16-Pin Wide SO (derate 9.52mW/°C above +70°C)......762mW
18-Pin Wide SO (derate 9.52mW/°C above +70°C)...... 762mW
20-Pin Wide SO (derate 10.00mW/°C above +70°C).....800mW
20-Pin SSOP (derate 8.00mW/°C above +70°C) 640mW
16-Pin CERDIP (derate 10.00mW/°C above +70°C).....800mW
18-Pin CERDIP (derate 10.53mW/°C above +70°C).....842mW
Operating Temperature Ranges
MAX2_ _AC_ _, MAX2_ _C_ _ ....0°C to +70°C
MAX2_ _AE_ _, MAX2_ _E_ _ ....-40°C to +85°C
MAX2_ _AM_ _, MAX2_ _M_ _ ....-55°C to +125°C
Storage Temperature Range ....-65°C to +160°C
Lead Temperature (soldering, 10sec) ....+300°C

Note 1: Input voltage measured with T_{OUT} in high-impedance state, $\overline{SHDN}$ or V_{CC} = 0V.
Note 2: For the MAX220, V+ and V- can have a maximum magnitude of 7V, but their absolute difference cannot exceed 13V.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—MAX220/222/232A/233A/242/243

(V_{CC} = +5V ±10%, C1–C4 = 0.1µF, MAX220, C1 = 0.047µF, C2–C4 = 0.33µF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
RS-232 TRANSMITTERS						
Output Voltage Swing	All transmitter outputs loaded with 3kΩ to GND		±5	±8		V
Input Logic Threshold Low				1.4	0.8	V
Input Logic Threshold High	All except MAX220		2	1.4		V
	MAX220: V_{CC} = 5.0V		2.4			
Logic Pull-Up/Input Current	All except MAX220, normal operation			5	40	µA
	$\overline{SHDN}$ = 0V, MAX222/242, shutdown, MAX220			±0.01	±1	
Output Leakage Current	V_{CC} = 5.5V, $\overline{SHDN}$ = 0V, V_{OUT} = ±15V, MAX222/242			±0.01	±10	µA
	V_{CC} = $\overline{SHDN}$ = 0V, V_{OUT} = ±15V			±0.01	±10	
Data Rate	All except MAX220, normal operation			200	116	kb/s
Transmitter Output Resistance	V_{CC} = V+ = V- = 0V, V_{OUT} = ±2V		300	10M		Ω
Output Short-Circuit Current	V_{OUT} = 0V		±7	±22		mA
RS-232 RECEIVERS						
RS-232 Input Voltage Operating Range					±30	V
RS-232 Input Threshold Low	V_{CC} = 5V	All except MAX243 $R2_{IN}$	0.8	1.3		V
		MAX243 $R2_{IN}$ (Note 2)	-3			
RS-232 Input Threshold High	V_{CC} = 5V	All except MAX243 $R2_{IN}$		1.8	2.4	V
		MAX243 $R2_{IN}$ (Note 2)		-0.5	-0.1	
RS-232 Input Hysteresis	All except MAX243, V_{CC} = 5V, no hysteresis in shdn.		0.2	0.5	1	V
	MAX243			-		
RS-232 Input Resistance			3	5	7	kΩ
TTL/CMOS Output Voltage Low	I_{OUT} = 3.2mA			0.2	0.4	V
TTL/CMOS Output Voltage High	I_{OUT} = -1.0mA		3.5	V_{CC} - 0.2		V
TTL/CMOS Output Short-Circuit Current	Sourcing V_{OUT} = GND		-2	-10		mA
	Shrinking V_{OUT} = V_{CC}		10	30		

MAXIM

Detailed Description

he MAX220–MAX249 contain four sections: dual harge-pump DC-DC voltage converters, RS-232 dri-ers, RS-232 receivers, and receiver and transmitter nable control inputs.

Dual Charge-Pump Voltage Converter

'he MAX220–MAX249 have two internal charge-pumps hat convert +5V to ±10V (unloaded) for RS-232 driver peration. The first converter uses capacitor C1 to dou-le the +5V input to +10V on C3 at the V+ output. The econd converter uses capacitor C2 to invert +10V to -10V on C4 at the V- output.

A small amount of power may be drawn from the +10V (V+) and -10V (V-) outputs to power external circuitry (see the *Typical Operating Characteristics* section), except on the MAX225 and MAX245–MAX247, where these pins are not available. V+ and V- are not regulated, so the output voltage drops with increasing load current. Do not load V+ and V- to a point that violates the minimum ±5V EIA/TIA-232E driver output voltage when sourcing current from V+ and V- to external circuitry.

When using the shutdown feature in the MAX222, MAX225, MAX230, MAX235, MAX236, MAX240, MAX241, and MAX245–MAX249, avoid using V+ and V- to power external circuitry. When these parts are shut down, V- falls to 0V, and V+ falls to +5V. For applications where a +10V external supply is applied to the V+ pin (instead of using the internal charge pump to generate +10V), the C1 capacitor must not be installed and the $\overline{SHDN}$ pin must be tied to V_{CC}. This is because V+ is internally connected to V_{CC} in shutdown mode.

RS-232 Drivers

The typical driver output voltage swing is ±8V when loaded with a nominal 5kΩ RS-232 receiver and V_{CC} = +5V. Output swing is guaranteed to meet the EIA/TIA-232E and V.28 specification, which calls for ±5V minimum driver output levels under worst-case conditions. These include a minimum 3kΩ load, V_{CC} = +4.5V, and maximum operating temperature. Unloaded driver output voltage ranges from (V+ -1.3V) to (V- +0.5V).

Input thresholds are both TTL and CMOS compatible. The inputs of unused drivers can be left unconnected since 400kΩ input pull-up resistors to V_{CC} are built in (except for the MAX220). The pull-up resistors force the outputs of unused drivers low because all drivers invert. The internal input pull-up resistors typically source 12μA, except in shutdown mode where the pull-ups are disabled. Driver outputs turn off and enter a high-impedance state—where leakage current is typically microamperes (maximum 25μA)—when in shutdown mode, in three-state mode, or when device power is removed. Outputs can be driven to ±15V. The power-supply current typically drops to 8μA in shutdown mode. The MAX220 does not have pull-up resistors to force the ouputs of the unused drivers low. Connect unused inputs to GND or V_{CC}.

The MAX239 has a receiver three-state control line, and the MAX223, MAX225, MAX235, MAX236, MAX240, and MAX241 have both a receiver three-state control line and a low-power shutdown control. Table 2 shows the effects of the shutdown control and receiver three-state control on the receiver outputs.

The receiver TTL/CMOS outputs are in a high-impedance, three-state mode whenever the three-state enable line is high (for the MAX225/MAX235/MAX236/MAX239–MAX241), and are also high-impedance whenever the shutdown control line is high.

When in low-power shutdown mode, the driver outputs are turned off and their leakage current is less than 1μA with the driver output pulled to ground. The driver output leakage remains less than 1μA, even if the transmitter output is backdriven between 0V and (V_{CC} + 6V). Below -0.5V, the transmitter is diode clamped to ground with 1kΩ series impedance. The transmitter is also zener clamped to approximately V_{CC} + 6V, with a series impedance of 1kΩ.

The driver output slew rate is limited to less than 30V/μs as required by the EIA/TIA-232E and V.28 specifications. Typical slew rates are 24V/μs unloaded and 10V/μs loaded with 3Ω and 2500pF.

RS-232 Receivers

EIA/TIA-232E and V.28 specifications define a voltage level greater than 3V as a logic 0, so all receivers invert. Input thresholds are set at 0.8V and 2.4V, so receivers respond to TTL level inputs as well as EIA/TIA-232E and V.28 levels.

The receiver inputs withstand an input overvoltage up to ±25V and provide input terminating resistors with

Table 2. Three-State Control of Receivers

PART	SHDN	$\overline{SHDN}$	EN	$\overline{EN(R)}$	RECEIVERS
MAX223	—	Low High High	X Low High	—	High Impedance Active High Impedance
MAX225	—	—	—	Low High	High Impedance Active
MAX235 MAX236 MAX240	Low Low High	—	—	Low High X	High Impedance Active High Impedance

nominal 5kΩ values. The receivers implement Type 1 interpretation of the fault conditions of V.28 and EIA/TIA-232E.

The receiver input hysteresis is typically 0.5V with a guaranteed minimum of 0.2V. This produces clear output transitions with slow-moving input signals, even with moderate amounts of noise and ringing. The receiver propagation delay is typically 600ns and is independent of input swing direction.

Low-Power Receive Mode

The low-power receive-mode feature of the MAX223, MAX242, and MAX245–MAX249 puts the IC into shutdown mode but still allows it to receive information. This is important for applications where systems are periodically awakened to look for activity. Using low-power receive mode, the system can still receive a signal that will activate it on command and prepare it for communication at faster data rates. This operation conserves system power.

Negative Threshold—MAX243

The MAX243 is pin compatible with the MAX232A, differing only in that RS-232 cable fault protection is removed on one of the two receiver inputs. This means that control lines such as CTS and RTS can either be driven or left floating without interrupting communication. Different cables are not needed to interface with different pieces of equipment.

The input threshold of the receiver without cable fault protection is -0.8V rather than +1.4V. Its output goes positive only if the input is connected to a control line that is actively driven negative. If not driven, it defaults to the 0 or "OK to send" state. Normally, the MAX243's other receiver (+1.4V threshold) is used for the data line (TD or RD), while the negative threshold receiver is connected to the control line (DTR, DTS, CTS, RTS, etc.).

Other members of the RS-232 family implement the optional cable fault protection as specified by EIA/TIA-232E specifications. This means a receiver output goes high whenever its input is driven negative, left floating, or shorted to ground. The high output tells the serial communications IC to stop sending data. To avoid this, the control lines must either be driven or connected with jumpers to an appropriate positive voltage level.

Shutdown—MAX222–MAX242

On the MAX222, MAX235, MAX236, MAX240, and MAX241, all receivers are disabled during shutdown. On the MAX223 and MAX242, two receivers continue to operate in a reduced power mode when the chip is in shutdown. Under these conditions, the propagation delay increases to about 2.5µs for a high-to-low input transition. When in shutdown, the receiver acts as a CMOS inverter with no hysteresis. The MAX223 and MAX242 also have a receiver output enable input ($\overline{EN}$ for the MAX242 and EN for the MAX223) that allows receiver output control independent of $\overline{SHDN}$ (SHDN for MAX241). With all other devices, $\overline{SHDN}$ (SHDN for MAX241) also disables the receiver outputs.

The MAX225 provides five transmitters and five receivers, while the MAX245 provides ten receivers and eight transmitters. Both devices have separate receiver and transmitter-enable controls. The charge pumps turn off and the devices shut down when a logic high is applied to the ENT input. In this state, the supply current drops to less than 25µA and the receivers continue to operate in a low-power receive mode. Driver outputs enter a high-impedance state (three-state mode). On the MAX225, all five receivers are controlled by the $\overline{ENR}$ input. On the MAX245, eight of the receiver outputs are controlled by the $\overline{ENR}$ input, while the remaining two receivers (RA5 and RB5) are always active. RA1–RA4 and RB1–RB4 are put in a three-state mode when $\overline{ENR}$ is a logic high.

Receiver and Transmitter Enable Control Inputs

The MAX225 and MAX245–MAX249 feature transmitter and receiver enable controls.

The receivers have three modes of operation: full-speed receive (normal active), three-state (disabled), and low-power receive (enabled receivers continue to function at lower data rates). The receiver enable inputs control the full-speed receive and three-state modes. The transmitters have two modes of operation: full-speed transmit (normal active) and three-state (disabled). The transmitter enable inputs also control the shutdown mode. The device enters shutdown mode when all transmitters are disabled. Enabled receivers function in the low-power receive mode when in shutdown.

+5V-Powered, Multichannel RS-232 Drivers/Receivers

Tables 1a–1d define the control states. The MAX244 has no control pins and is not included in these tables.

The MAX246 has ten receivers and eight drivers with two control pins, each controlling one side of the device. A logic high at the A-side control input ($\overline{ENA}$) causes the four A-side receivers and drivers to go into a three-state mode. Similarly, the B-side control input ($\overline{ENB}$) causes the four B-side drivers and receivers to go into a three-state mode. As in the MAX245, one A-side and one B-side receiver (RA5 and RB5) remain active at all times. The entire device is put into shutdown mode when both the A and B sides are disabled ($\overline{ENA}$ = $\overline{ENB}$ = +5V).

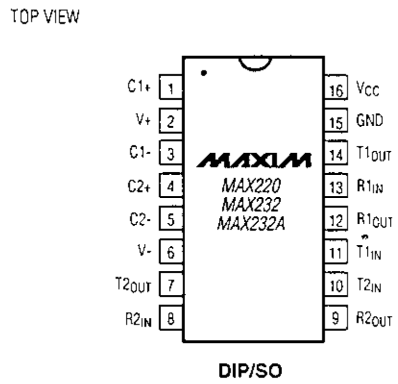
The MAX247 provides nine receivers and eight drivers with four control pins. The $\overline{ENRA}$ and $\overline{ENRB}$ receiver enable inputs each control four receiver outputs. The $\overline{ENTA}$ and $\overline{ENTB}$ transmitter enable inputs each control four drivers. The ninth receiver (RB5) is always active. The device enters shutdown mode with a logic high on both $\overline{ENTA}$ and $\overline{ENTB}$.

The MAX248 provides eight receivers and eight drivers with four control pins. The $\overline{ENRA}$ and $\overline{ENRB}$ receiver enable inputs each control four receiver outputs. The $\overline{ENTA}$ and $\overline{ENTB}$ transmitter enable inputs control four drivers each. This part does not have an always-active receiver. The device enters shutdown mode and transmitters go into a three-state mode with a logic high on both $\overline{ENTA}$ and $\overline{ENTB}$.

The MAX249 provides ten receivers and six drivers with four control pins. The $\overline{ENRA}$ and $\overline{ENRB}$ receiver enable inputs each control five receiver outputs. The $\overline{ENTA}$ and $\overline{ENTB}$ transmitter enable inputs control three drivers each. There is no always-active receiver. The device enters shutdown mode and transmitters go into a three-state mode with a logic high on both $\overline{ENTA}$ and $\overline{ENTB}$. In shutdown mode, active receivers operate in a low-power receive mode at data rates up to 20kbits/sec.

Applications Information

Figures 5 through 25 show pin configurations and typical operating circuits. In applications that are sensitive to power-supply noise, V_{CC} should be decoupled to ground with a capacitor of the same value as C1 and C2 connected as close as possible to the device.



CAPACITANCE (μF)					
DEVICE	C1	C2	C3	C4	C5
MAX220	4.7	4.7	10	10	4.7
MAX232	1.0	1.0	1.0	1.0	1.0
MAX232A	0.1	0.1	0.1	0.1	0.1

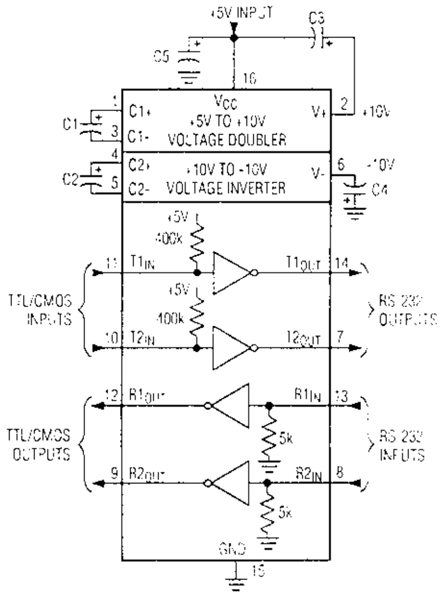
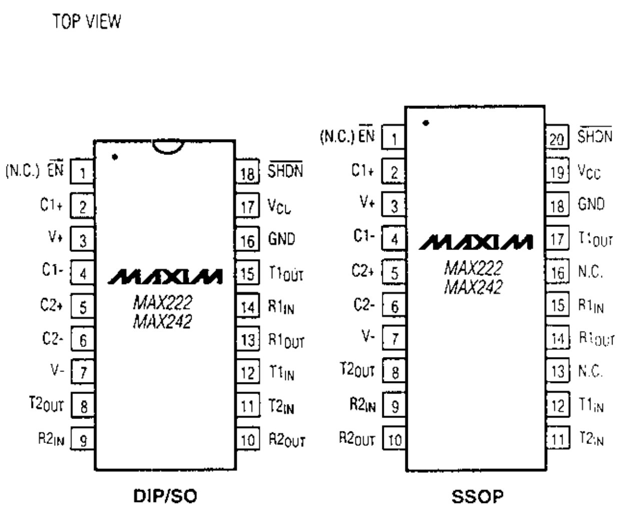


Figure 5. MAX220/MAX232/MAX232A Pin Configuration and Typical Operating Circuit



( ) ARE FOR MAX222 ONLY.
PIN NUMBERS IN TYPICAL OPERATING CIRCUIT ARE FOR DIP/SO PACKAGES ONLY.

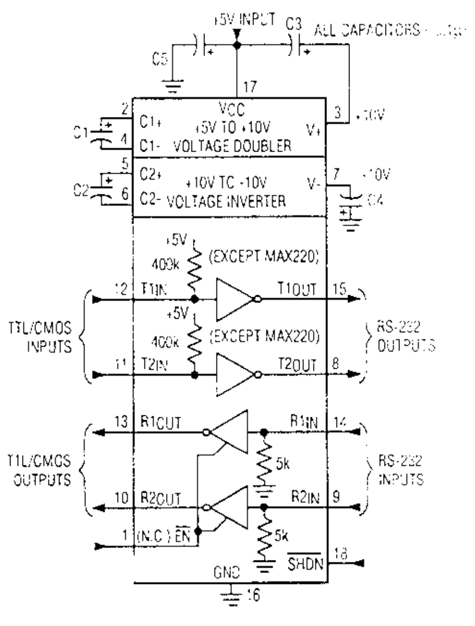


Figure 6. MAX222/MAX242 Pin Configurations and Typical Operating Circuit

National Semiconductor

November 2000

LM35
Precision Centigrade Temperature Sensors

General Description

The LM35 series are precision integrated-circuit temperature sensors, whose output voltage is linearly proportional to the Celsius (Centigrade) temperature. The LM35 thus has an advantage over linear temperature sensors calibrated in ˚ Kelvin, as the user is not required to subtract a large constant voltage from its output to obtain convenient Centigrade scaling. The LM35 does not require any external calibration or trimming to provide typical accuracies of ±¼˚C at room temperature and ±¾˚C over a full −55 to +150˚C temperature range. Low cost is assured by trimming and calibration at the wafer level. The LM35's low output impedance, linear output, and precise inherent calibration make interfacing to readout or control circuitry especially easy. It can be used with single power supplies, or with plus and minus supplies. As it draws only 60 µA from its supply, it has very low self-heating, less than 0.1˚C in still air. The LM35 is rated to operate over a −55˚ to +150˚C temperature range, while the LM35C is rated for a −40˚ to +110˚C range (−10˚ with improved accuracy). The LM35 series is available packaged in hermetic TO-46 transistor packages, while the LM35C, LM35CA, and LM35D are also available in the plastic TO-92 transistor package. The LM35D is also available in an 8-lead surface mount small outline package and a plastic TO-220 package.

Features

- Calibrated directly in ˚ Celsius (Centigrade)
- Linear + 10.0 mV/˚C scale factor
- 0.5˚C accuracy guaranteeable (at +25˚C)
- Rated for full −55˚ to +150˚C range
- Suitable for remote applications
- Low cost due to wafer-level trimming
- Operates from 4 to 30 volts
- Less than 60 µA current drain
- Low self-heating, 0.08˚C in still air
- Nonlinearity only ±¼˚C typical
- Low impedance output, 0.1 Ω for 1 mA load

Typical Applications

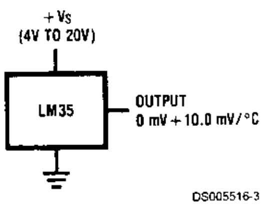
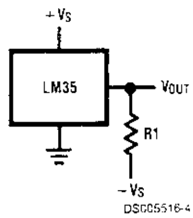


FIGURE 1. Basic Centigrade Temperature Sensor (+2˚C to +150˚C)



Choose $R_1 = -V_S/50\ \mu A$

V_{OUT} = +1,500 mV at +150˚C

= +250 mV at +25˚C

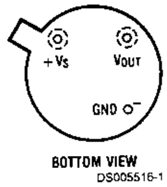
= −550 mV at −55˚C

FIGURE 2. Full-Range Centigrade Temperature Sensor

 DS005516

Connection Diagrams

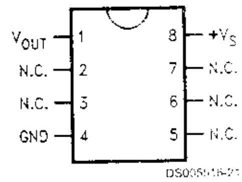
TO-46
Metal Can Package*



*Case is connected to negative pin (GND)

Order Number LM35H, LM35AH, LM35CH, LM35CAH or LM35DH
See NS Package Number H03H

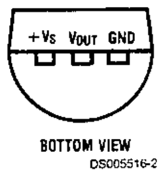
SO-8
Small Outline Molded Package



N.C. = No Connection

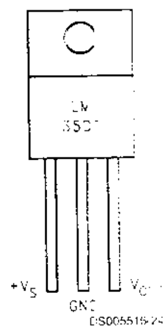
Top View
Order Number LM35DM
See NS Package Number M08A

TO-92
Plastic Package



Order Number LM35CZ, LM35CAZ or LM35DZ
See NS Package Number Z03A

TO-220
Plastic Package*



*Tab is connected to the negative pin (GND).
Note: The LM35DT pinout is different than the discontinued LM35DP.

Order Number LM35DT
See NS Package Number TA03F

Absolute Maximum Ratings (Note 10)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	+35V to −0.2V
Output Voltage	+6V to −1.0V
Output Current	10 mA
Storage Temp.;	
TO-46 Package,	−60°C to +180°C
TO-92 Package,	−60°C to +150°C
SO-8 Package,	−65°C to +150°C
TO-220 Package,	−65°C to +150°C
Lead Temp.:	
TO-46 Package, (Soldering, 10 seconds)	300°C
TO-92 and TO-220 Package, (Soldering, 10 seconds)	260°C
SO Package (Note 12)	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
ESD Susceptibility (Note 11)	2500V
Specified Operating Temperature Range: T_{MIN} to T_{MAX} (Note 2)	
LM35, LM35A	−55°C to +150°C
LM35C, LM35CA	−40°C to +110°C
LM35D	0°C to +100°C

Electrical Characteristics

(Notes 1, 6)

Parameter	Conditions	LM35A			LM35CA			Units
		Typical	Tested Limit (Note 4)	Design Limit (Note 5)	Typical	Tested Limit (Note 4)	Design Limit (Note 5)	(Max.)
Accuracy (Note 7)	T_A=+25°C	±0.2	±0.5		±0.2	±0.5		°C
	T_A=−10°C	±0.3			±0.3		±1.0	°C
	T_A=T_{MAX}	±0.4	±1.0		±0.4	±1.0		°C
	T_A=T_{MIN}	±0.4	±1.0		±0.4		±1.5	°C
Nonlinearity (Note 8)	T_{MIN}≤T_A≤T_{MAX}	**±0.18**		**±0.35**	**±0.15**		**±0.3**	°C
Sensor Gain (Average Slope)	T_{MIN}≤T_A≤T_{MAX}	**+10.0**	**+9.9, +10.1**		**+10.0**		**+9.9, +10.1**	mV/°C
Load Regulation (Note 3) 0≤I_L≤1 mA	T_A=+25°C	±0.4	±1.0		±0.4	±1.0		mV/mA
	T_{MIN}≤T_A≤T_{MAX}	**±0.5**		**±3.0**	**±0.5**		**±3.0**	mV/mA
Line Regulation (Note 3)	T_A=+25°C	±0.01	±0.05		±0.01	±0.05		mV/V
	4V≤V_S≤30V	**±0.02**		**±0.1**	**±0.02**		**±0.1**	mV/V
Quiescent Current (Note 9)	V_S=+5V, +25°C	56	67		56	67		µA
	V_S=+5V	**105**		**131**	**91**		**114**	µA
	V_S=+30V, +25°C	56.2	68		56.2	68		µA
	V_S=+30V	**105.5**		**133**	**91.5**		**116**	µA
Change of Quiescent Current (Note 3)	4V≤V_S≤30V, +25°C	0.2	1.0		0.2	1.0		µA
	4V≤V_S≤30V	**0.5**		**2.0**	**0.5**		**2.0**	µA
Temperature Coefficient of Quiescent Current		**+0.39**		**+0.5**	**+0.39**		**+0.5**	µA/°C
Minimum Temperature for Rated Accuracy	In circuit of *Figure 1*, I_L=0	+1.5		+2.0	+1.5		+2.0	°C
Long Term Stability	T_J=T_{MAX}, for 1000 hours	±0.08			±0.08			°C

Electrical Characteristics

(Notes 1, 6)

Parameter	Conditions	LM35 Typical	LM35 Tested Limit (Note 4)	LM35 Design Limit (Note 5)	LM35C, LM35D Typical	LM35C, LM35D Tested Limit (Note 4)	LM35C, LM35D Design Limit (Note 5)	Units (Max.)
Accuracy, LM35, LM35C (Note 7)	T_A=+25°C	±0.4	±1.0		±0.4	±1.0		°C
	T_A=−10°C	±0.5			±0.5		±1.5	°C
	$T_A=T_{MAX}$	±0.8	±1.5		±0.8		±1.5	°C
	$T_A=T_{MIN}$	±0.8		±1.5	±0.8		±2.0	°C
Accuracy, LM35D (Note 7)	T_A=+25°C				±0.6	±1.5		°C
	$T_A=T_{MAX}$				±0.9		±2.0	°C
	$T_A=T_{MIN}$				±0.9		±2.0	°C
Nonlinearity (Note 8)	$T_{MIN}\le T_A\le T_{MAX}$	**±0.3**		**±0.5**	**±0.2**		**±0.5**	°C
Sensor Gain (Average Slope)	$T_{MIN}\le T_A\le T_{MAX}$	**+10.0**	**+9.8, +10.2**		**+10.0**		**+9.8, +10.2**	mV/°C
Load Regulation (Note 3) $0\le I_L\le 1$ mA	T_A=+25°C	±0.4	±2.0		±0.4	±2.0		mV/mA
	$T_{MIN}\le T_A\le T_{MAX}$	**±0.5**		**±5.0**	**±0.5**		**±5.0**	mV/mA
Line Regulation (Note 3)	T_A=+25°C	±0.01	±0.1		±0.01	±0.1		mV/V
	$4V\le V_S\le 30V$	**±0.02**		**±0.2**	**±0.02**		**±0.2**	mV/V
Quiescent Current (Note 9)	V_S=+5V, +25°C	56	80		56	80		μA
	V_S=+5V	**105**		**158**	**91**		**138**	μA
	V_S=+30V, +25°C	56.2	82		56.2	82		μA
	V_S=+30V	**105.5**		**161**	**91.5**		**141**	μA
Change of Quiescent Current (Note 3)	$4V\le V_S\le 30V$, +25°C	0.2	2.0		0.2	2.0		μA
	$4V\le V_S\le 30V$	**0.5**		**3.0**	**0.5**		**3.0**	μA
Temperature Coefficient of Quiescent Current		**+0.39**		**+0.7**	**+0.39**		**+0.7**	μA/°C
Minimum Temperature for Rated Accuracy	In circuit of *Figure 1*, I_L=0	+1.5		+2.0	+1.5		+2.0	°C
Long Term Stability	$T_J=T_{MAX}$, for 1000 hours	±0.08			±0.08			°C

Note 1: Unless otherwise noted, these specifications apply: $-55°C\le T_J\le +150°C$ for the LM35 and LM35A; $-40°C\le T_J\le +110°C$ for the LM35C and LM35CA; and $0°C\le T_J\le +100°C$ for the LM35D. V_S=+5Vdc and I_{LOAD}=50 μA, in the circuit of *Figure 2*. These specifications also apply from +2°C to T_{MAX} in the circuit of *Figure 1*. Specifications in **boldface** apply over the full rated temperature range.

Note 2: Thermal resistance of the TO-46 package is 400°C/W, junction to ambient, and 24°C/W junction to case. Thermal resistance of the TO-92 package is 180°C/W junction to ambient. Thermal resistance of the small outline molded package is 220°C/W junction to ambient. Thermal resistance of the TO-220 package is 90°C/W junction to ambient. For additional thermal resistance information see table in the Applications section.

Note 3: Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output due to heating effects can be computed by multiplying the internal dissipation by the thermal resistance.

Note 4: Tested Limits are guaranteed and 100% tested in production.

Note 5: Design Limits are guaranteed (but not 100% production tested) over the indicated temperature and supply voltage ranges. These limits are not used to calculate outgoing quality levels.

Note 6: Specifications in **boldface** apply over the full rated temperature range.

Note 7: Accuracy is defined as the error between the output voltage and 10mv/°C times the device's case temperature, at specified conditions of voltage, current, and temperature (expressed in °C).

Note 8: Nonlinearity is defined as the deviation of the output-voltage-versus-temperature curve from the best-fit straight line over the device's rated temperature range.

Note 9: Quiescent current is defined in the circuit of *Figure 1*.

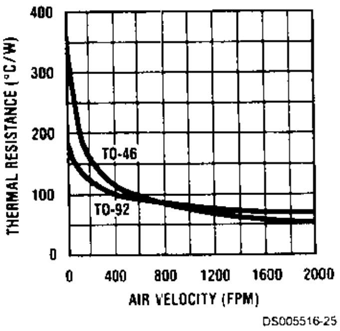
Note 10: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions. See Note 1.

Note 11: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

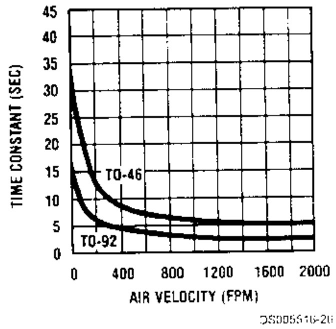
Note 12: See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" or the section titled "Surface Mount" found in a current National Semiconductor Linear Data Book for other methods of soldering surface mount devices.

Typical Performance Characteristics

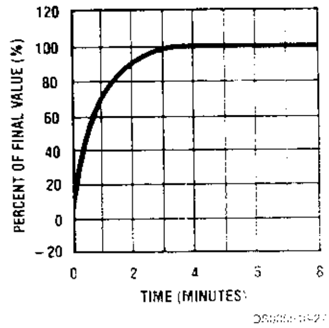
Thermal Resistance Junction to Air



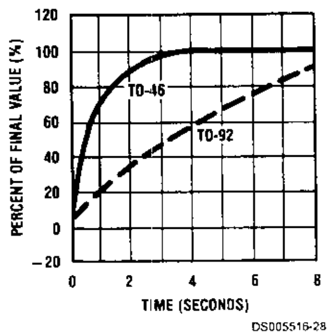
Thermal Time Constant



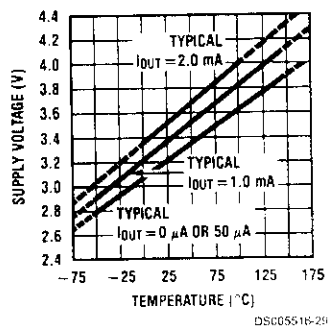
Thermal Response in Still Air



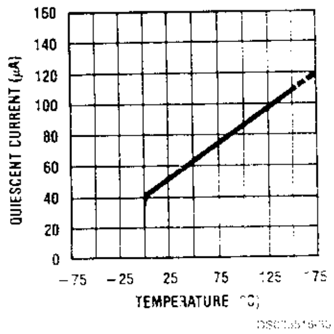
Thermal Response in Stirred Oil Bath



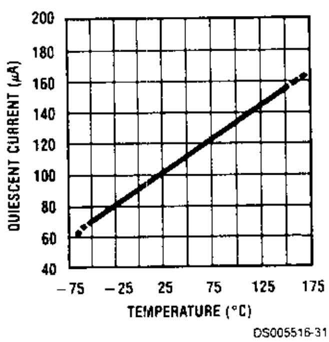
Minimum Supply Voltage vs. Temperature



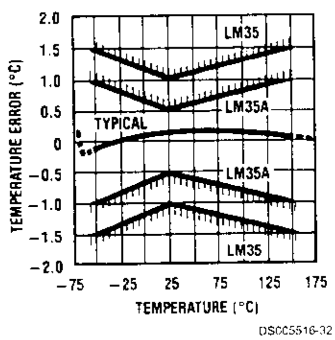
Quiescent Current vs. Temperature (In Circuit of *Figure 1*.)



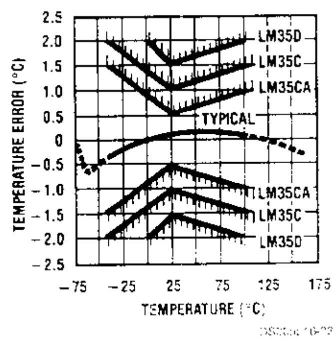
Quiescent Current vs. Temperature (In Circuit of *Figure 2*.)



Accuracy vs. Temperature (Guaranteed)

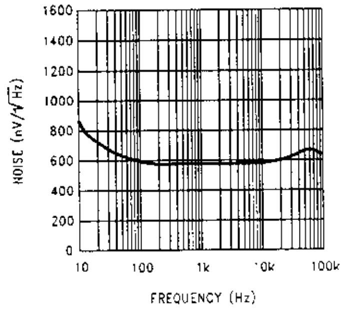


Accuracy vs. Temperature (Guaranteed)

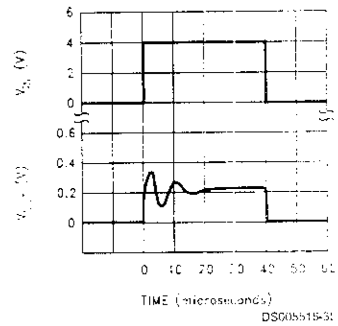


Typical Performance Characteristics (Continued)

Noise Voltage



Start-Up Response



Applications

The LM35 can be applied easily in the same way as other integrated-circuit temperature sensors. It can be glued or cemented to a surface and its temperature will be within about 0.01˚C of the surface temperature.

This presumes that the ambient air temperature is almost the same as the surface temperature; if the air temperature were much higher or lower than the surface temperature, the actual temperature of the LM35 die would be at an intermediate temperature between the surface temperature and the air temperature. This is expecially true for the TO-92 plastic package, where the copper leads are the principal thermal path to carry heat into the device, so its temperature might be closer to the air temperature than to the surface temperature.

To minimize this problem, be sure that the wiring to the LM35, as it leaves the device, is held at the same temperature as the surface of interest. The easiest way to do this is to cover up these wires with a bead of epoxy which will insure that the leads and wires are all at the same temperature as the surface, and that the LM35 die's temperature will not be affected by the air temperature.

The TO-46 metal package can also be soldered to a metal surface or pipe without damage. Of course, in that case the V− terminal of the circuit will be grounded to that metal. Alternatively, the LM35 can be mounted inside a sealed-end metal tube, and can then be dipped into a bath or screwed into a threaded hole in a tank. As with any IC, the LM35 and accompanying wiring and circuits must be kept insulated and dry, to avoid leakage and corrosion. This is especially true if the circuit may operate at cold temperatures where condensation can occur. Printed-circuit coatings and varnishes such as Humiseal and epoxy paints or dips are often used to insure that moisture cannot corrode the LM35 or its connections.

These devices are sometimes soldered to a small light-weight heat fin, to decrease the thermal time constant and speed up the response in slowly-moving air. On the other hand, a small thermal mass may be added to the sensor, to give the steadiest reading despite small deviations in the air temperature.

Temperature Rise of LM35 Due To Self-heating (Thermal Resistance, θ_{JA})

	TO-46, no heat sink	TO-46*, small heat fin	TO-92, no heat sink	TO-92**, small heat fin	SO-8 no heat sink	SO-8** small heat fin	TO-220 no heat sink
Still air	400˚C/W	100˚C/W	180˚C/W	140˚C/W	220˚C/W	110˚C/W	90˚C/W
Moving air	100˚C/W	40˚C/W	90˚C/W	70˚C/W	105˚C/W	90˚C/W	26˚C/W
Still oil	100˚C/W	40˚C/W	90˚C/W	70˚C/W			
Stirred oil	50˚C/W	30˚C/W	45˚C/W	40˚C/W			
(Clamped to metal, Infinite heat sink)	(24˚C/W)				(55˚C/W)		

*Wakefield type 201, or 1" disc of 0.020" sheet brass, soldered to case, or similar.
**TO-92 and SO-8 packages glued and leads soldered to 1" square of 1/16" printed circuit board with 2 oz. foil or similar.

Typical Applications

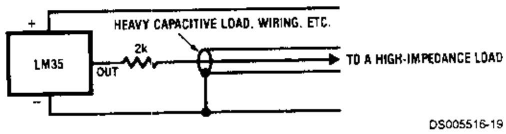


FIGURE 3. LM35 with Decoupling from Capacitive Load

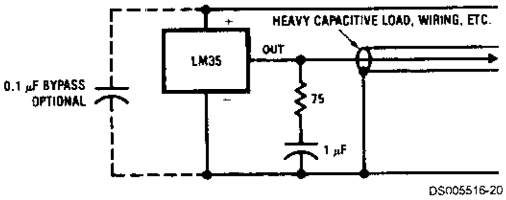


FIGURE 4. LM35 with R-C Damper

CAPACITIVE LOADS

Like most micropower circuits, the LM35 has a limited ability to drive heavy capacitive loads. The LM35 by itself is able to drive 50 pf without special precautions. If heavier loads are anticipated, it is easy to isolate or decouple the load with a resistor; see *Figure 3*. Or you can improve the tolerance of capacitance with a series R-C damper from output to ground; see *Figure 4*.

When the LM35 is applied with a 200Ω load resistor as shown in *Figure 5*, *Figure 6* or *Figure 8* it is relatively immune to wiring capacitance because the capacitance forms a bypass from ground to input, not on the output. However, as with any linear circuit connected to wires in a hostile environment, its performance can be affected adversely by intense electromagnetic sources such as relays, radio transmitters, motors with arcing brushes, SCR transients, etc, as its wiring can act as a receiving antenna and its internal junctions can act as rectifiers. For best results in such cases, a bypass capacitor from V_{IN} to ground and a series R-C damper such as 75Ω in series with 0.2 or 1 μF from output to ground are often useful. These are shown in *Figure 13*, *Figure 14*, and *Figure 16*.

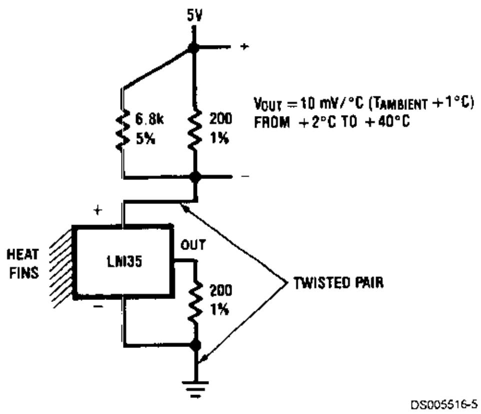


FIGURE 5. Two-Wire Remote Temperature Sensor (Grounded Sensor)

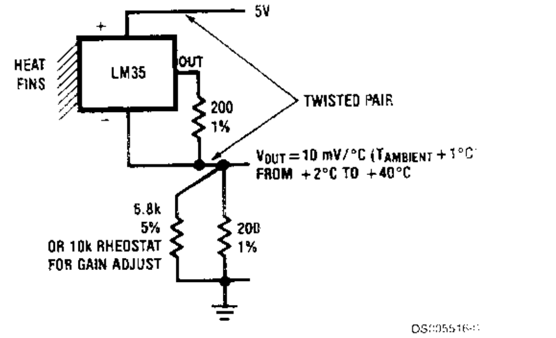


FIGURE 6. Two-Wire Remote Temperature Sensor (Output Referred to Ground)

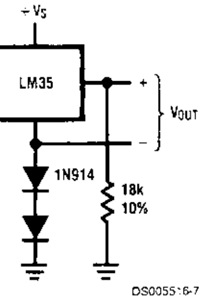


FIGURE 7. Temperature Sensor, Single Supply, −55° to +150°C

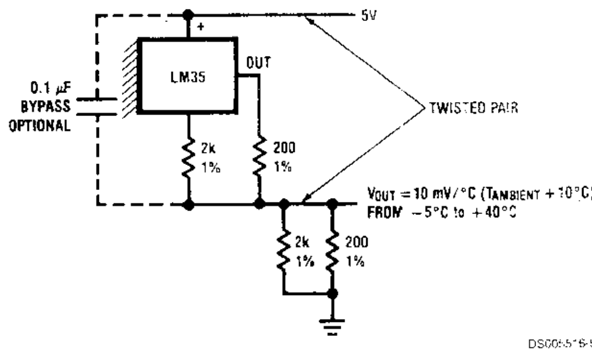


FIGURE 8. Two-Wire Remote Temperature Sensor (Output Referred to Ground)

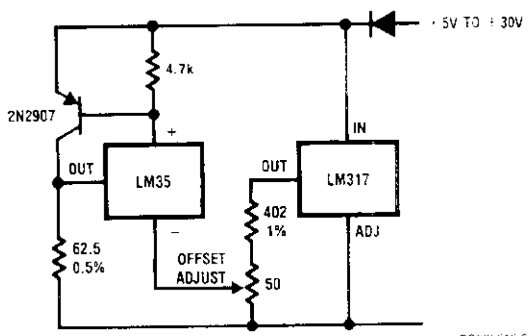


FIGURE 9. 4-To-20 mA Current Source (0°C to +100°C)

Typical Applications (Continued)

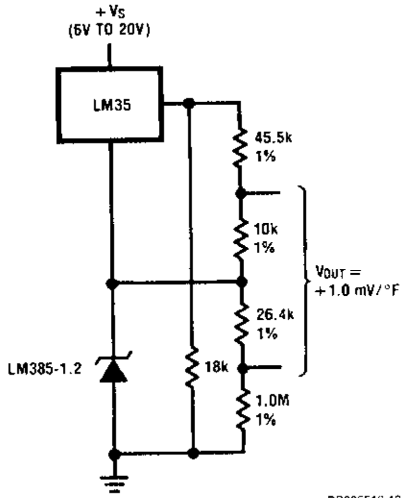


FIGURE 10. Fahrenheit Thermometer

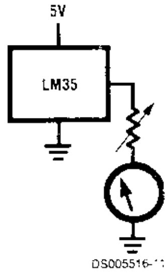


FIGURE 11. Centigrade Thermometer (Analog Meter)

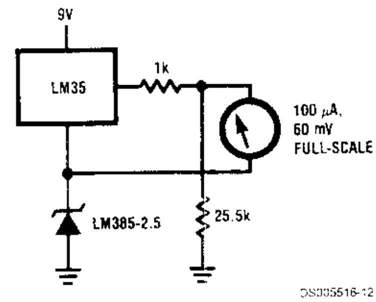


FIGURE 12. Fahrenheit ThermometerExpanded Scale Thermometer (50° to 80° Fahrenheit, for Example Shown)

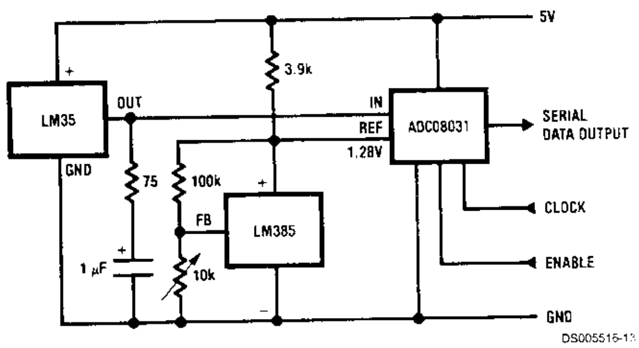


FIGURE 13. Temperature To Digital Converter (Serial Output) (+128°C Full Scale)

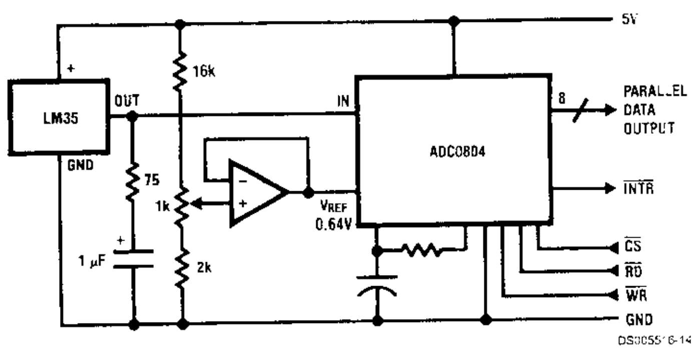
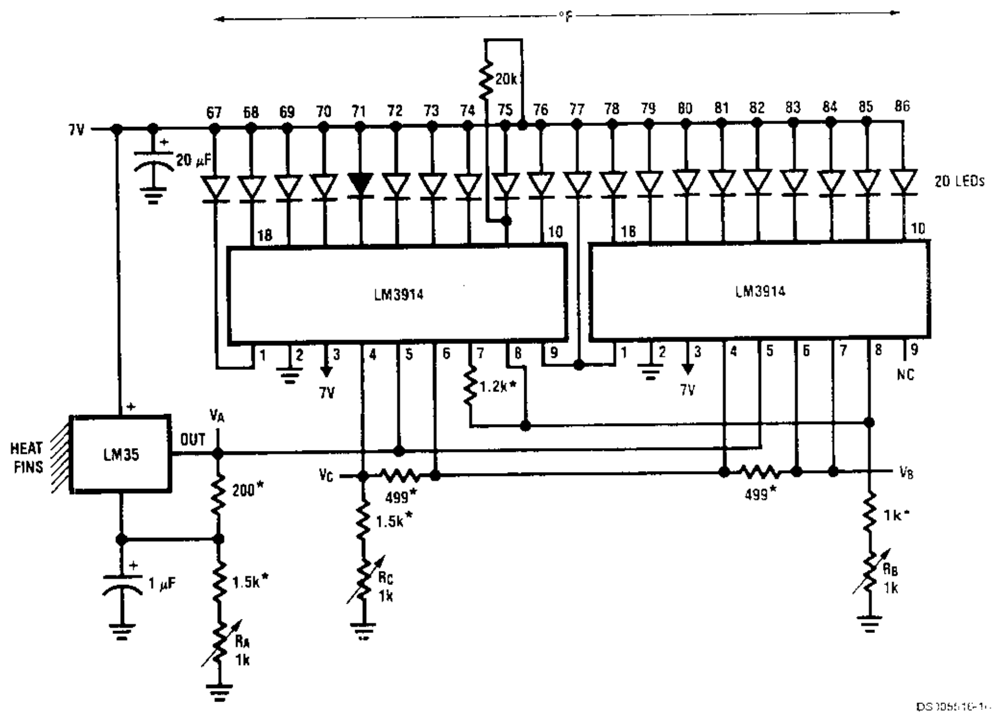


FIGURE 14. Temperature To Digital Converter (Parallel TRI-STATE™ Outputs for Standard Data Bus to µP Interface) (128°C Full Scale)

Typical Applications (Continued)



* =1% or 2% film resistor
Trim R_B for V_B=3.075V
Trim R_C for V_C=1.955V
Trim R_A for V_A=0.075V + 100mV/°C x $T_{ambient}$
Example, V_A=2.275V at 22°C

FIGURE 15. Bar-Graph Temperature Display (Dot Mode)

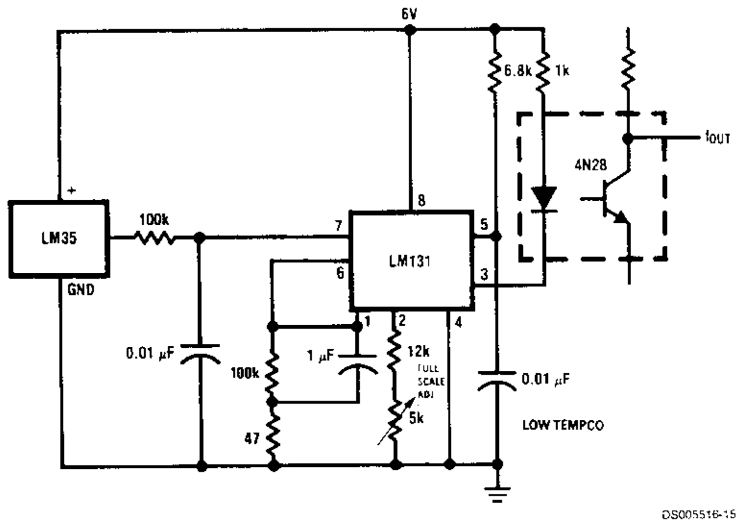
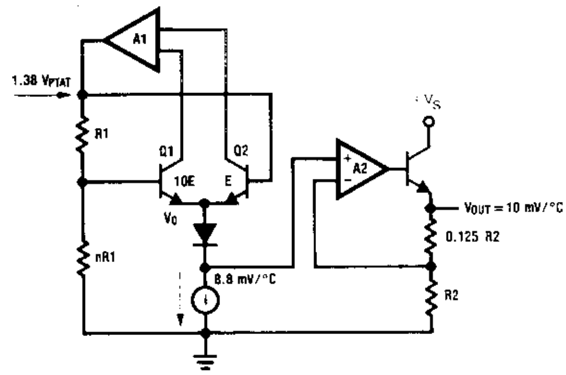


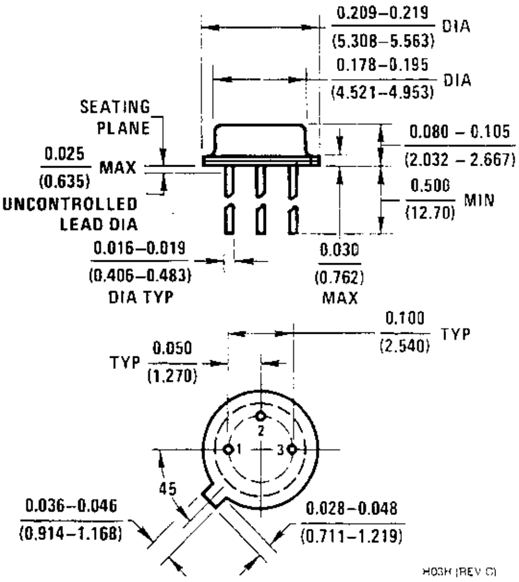
FIGURE 16. LM35 With Voltage-To-Frequency Converter And Isolated Output (2°C to +150°C; 20 Hz to 1500 Hz)

Block Diagram

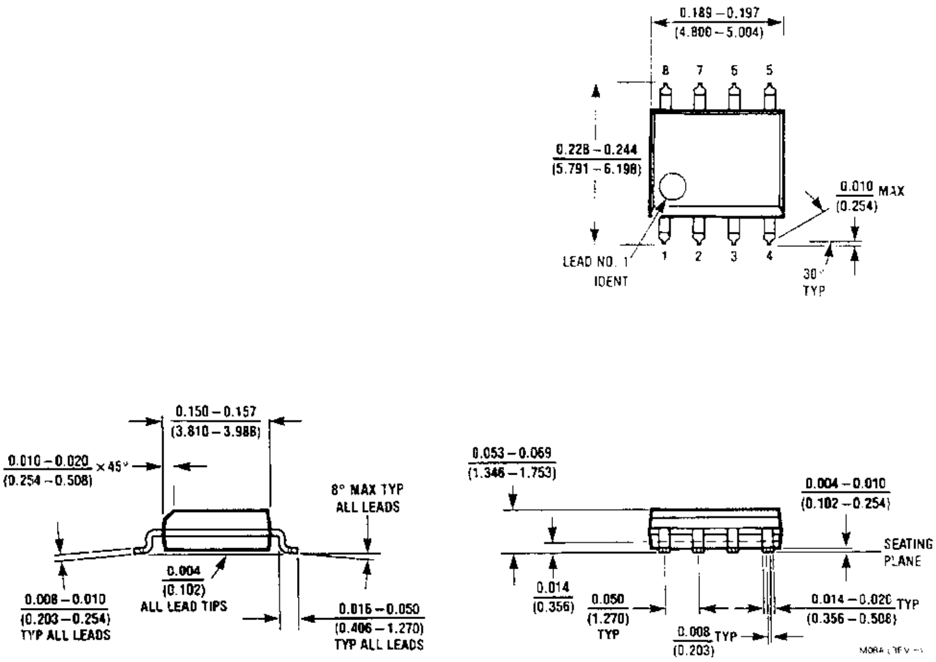


DS005516-23

Physical Dimensions inches (millimeters) unless otherwise noted

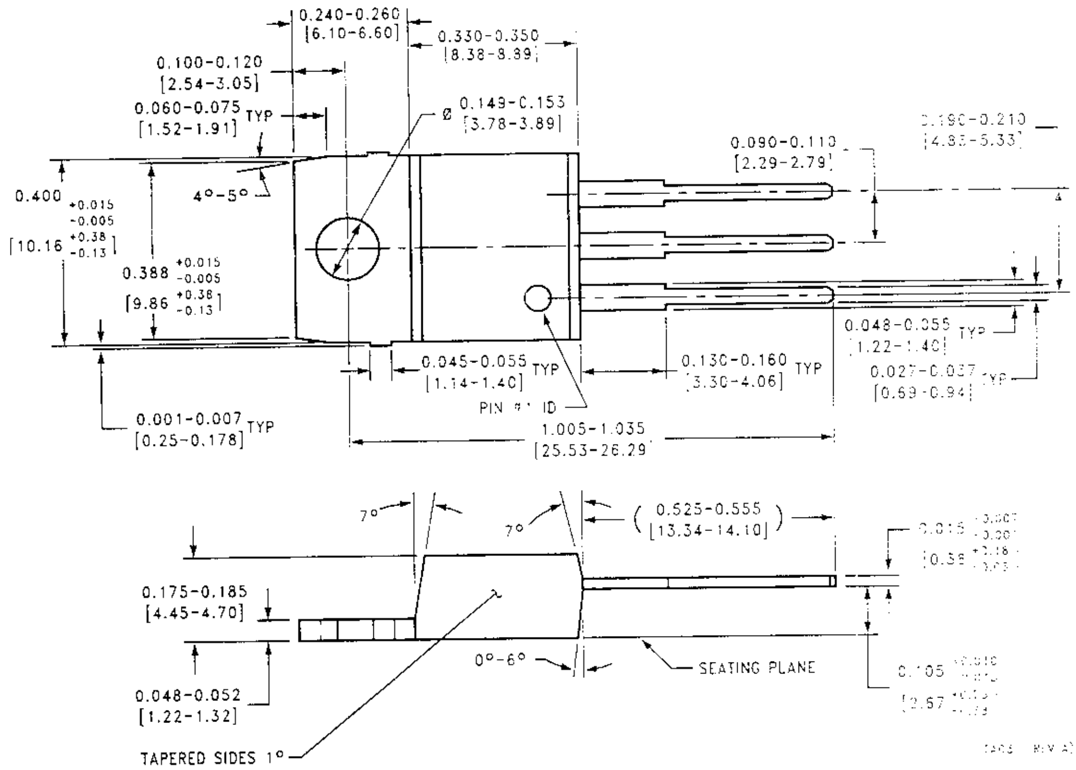


TO-46 Metal Can Package (H)
Order Number LM35H, LM35AH, LM35CH, LM35CAH, or LM35DH
NS Package Number H03H



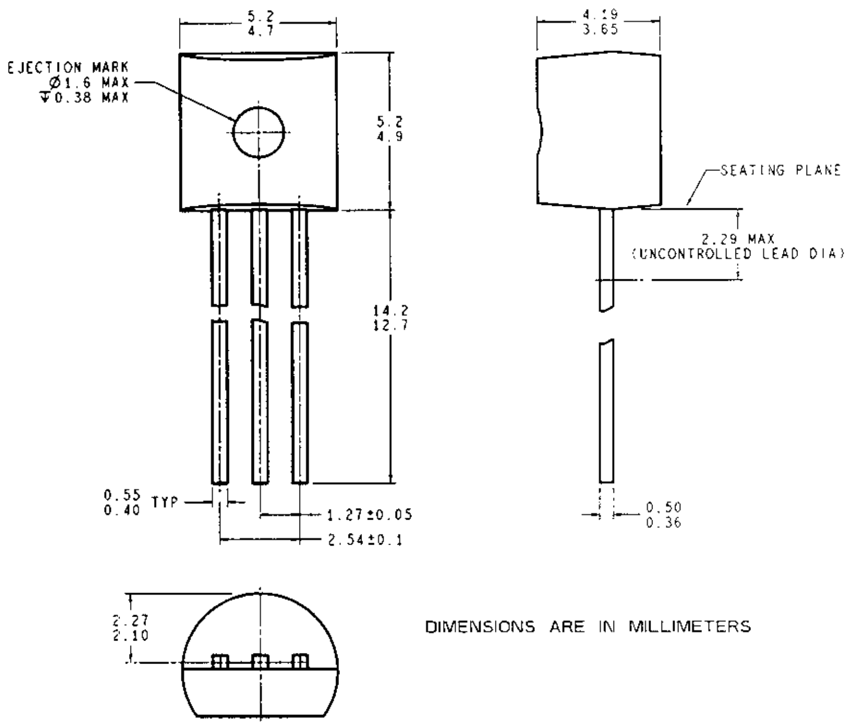
SO-8 Molded Small Outline Package (M)
Order Number LM35DM
NS Package Number M08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Power Package TO-220 (T)
Order Number LM35DT
NS Package Number TA03F

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



TO-92 Plastic Package (Z)
Order Number LM35CZ, LM35CAZ or LM35DZ
NS Package Number Z03A

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National Semiconductor

December 1994

LM108/LM208/LM308 Operational Amplifiers

General Description

The LM108 series are precision operational amplifiers having specifications a factor of ten better than FET amplifiers over a −55°C to +125°C temperature range.

The devices operate with supply voltages from ±2V to ±20V and have sufficient supply rejection to use unregulated supplies. Although the circuit is interchangeable with and uses the same compensation as the LM101A, an alternate compensation scheme can be used to make it particularly insensitive to power supply noise and to make supply bypass capacitors unnecessary.

The low current error of the LM108 series makes possible many designs that are not practical with conventional amplifiers. In fact, it operates from 10 MΩ source resistances, introducing less error than devices like the 709 with 10 kΩ sources. Integrators with drifts less than 500 μV/sec and analog time delays in excess of one hour can be made using capacitors no larger than 1 μF.

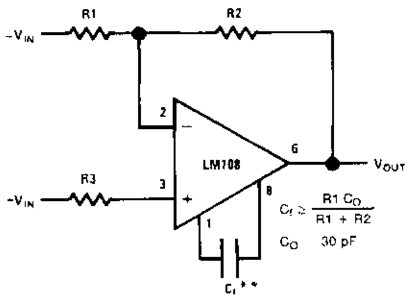
The LM108 is guaranteed from −55°C to +125°C, the LM208 from −25°C to +85°C, and the LM308 from 0°C to +70°C.

Features

- Maximum input bias current of 3.0 nA over temperature
- Offset current less than 400 pA over temperature
- Supply current of only 300 μA, even in saturation
- Guaranteed drift characteristics

Compensation Circuits

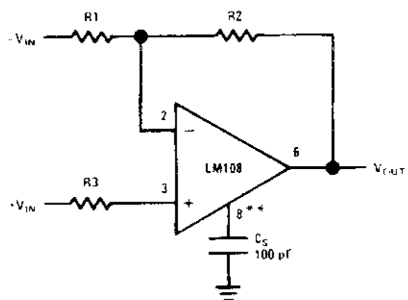
Standard Compensation Circuit



TL/H/7758-1

**Bandwidth and slew rate are proportional to $1/C_f$

Alternate* Frequency Compensation

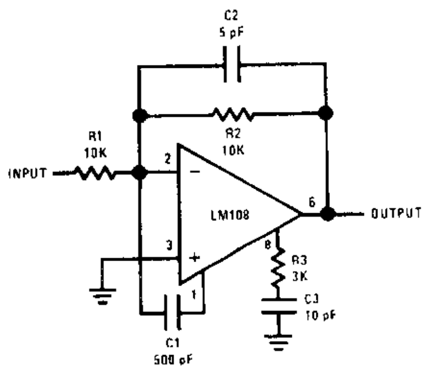


TL/H/7758-2

*Improves rejection of power supply noise by a factor of ten

**Bandwidth and slew rate are proportional to $1/C_S$

Feedforward Compensation



TL/H/7758-3

 RRD-B30M115/Printed in U.S.A.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

(Note 5)

	LM108/LM208	LM308
Supply Voltage	±20V	±18V
Power Dissipation (Note 1)	500 mW	500 mW
Differential Input Current (Note 2)	±10 mA	±10 mA
Input Voltage (Note 3)	±15V	±15V
Output Short-Circuit Duration	Continuous	Continuous
Operating Temperature Range (LM108)	−55°C to +125°C	0°C to +70°C
(LM208)	−25°C to +85°C	
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)		
DIP	260°C	260°C
H Package Lead Temp		
(Soldering 10 seconds)	300°C	300°C
Soldering Information		
Dual-In-Line Package		
Soldering (10 seconds)	260°C	
Small Outline Package		
Vapor Phase (60 seconds)	215°C	
Infrared (15 seconds)	220°C	

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD Tolerance (Note 6)	2000V	

Electrical Characteristics (Note 4)

Parameter	Condition	LM108/LM208			LM308			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$T_A = 25°C$		0.7	2.0		2.0	7.5	mV
Input Offset Current	$T_A = 25°C$		0.05	0.2		0.2	1	nA
Input Bias Current	$T_A = 25°C$		0.8	2.0		1.5	7	nA
Input Resistance	$T_A = 25°C$	30	70		10	40		MΩ
Supply Current	$T_A = 25°C$		0.3	0.6		0.3	0.8	mA
Large Signal Voltage Gain	$T_A = 25°C, V_S = \pm 15V$ $V_{OUT} = \pm 10V, R_L \geq 10\ k\Omega$	50	300		25	300		V/mV
Input Offset Voltage				3.0			10	mV
Average Temperature Coefficient of Input Offset Voltage			3.0	15		6.0	30	μV/°C
Input Offset Current				0.4			1.5	nA
Average Temperature Coefficient of Input Offset Current			0.5	2.5		2.0	10	pA/°C
Input Bias Current				3.0			10	nA
Supply Current	$T_A = +125°C$		0.15	0.4				mA
Large Signal Voltage Gain	$V_S = \pm 15V, V_{OUT} = \pm 10V$ $R_L \geq 10\ k\Omega$	25			15			V/mV
Output Voltage Swing	$V_S = \pm 15V, R_L = 10\ k\Omega$	±13	±14		±13	±14		V

Electrical Characteristics (Note 4) (Continued)

Parameter	Condition	LM108/LM208			LM308			Units
		Min	Typ	Max	Min	Typ	Max	
Input Voltage Range	$V_S = \pm 15V$	±13.5			±14			V
Common Mode Rejection Ratio		85	100		80	100		dB
Supply Voltage Rejection Ratio		80	96		80	96		dB

Note 1: The maximum junction temperature of the LM108 is 150°C, for the LM208, 100°C and for the LM308, 85°C. For operating at elevated temperatures, devices in the H08 package must be derated based on a thermal resistance of 160°C/W, junction to ambient, or 20°C/W, junction to case. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

Note 2: The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used.

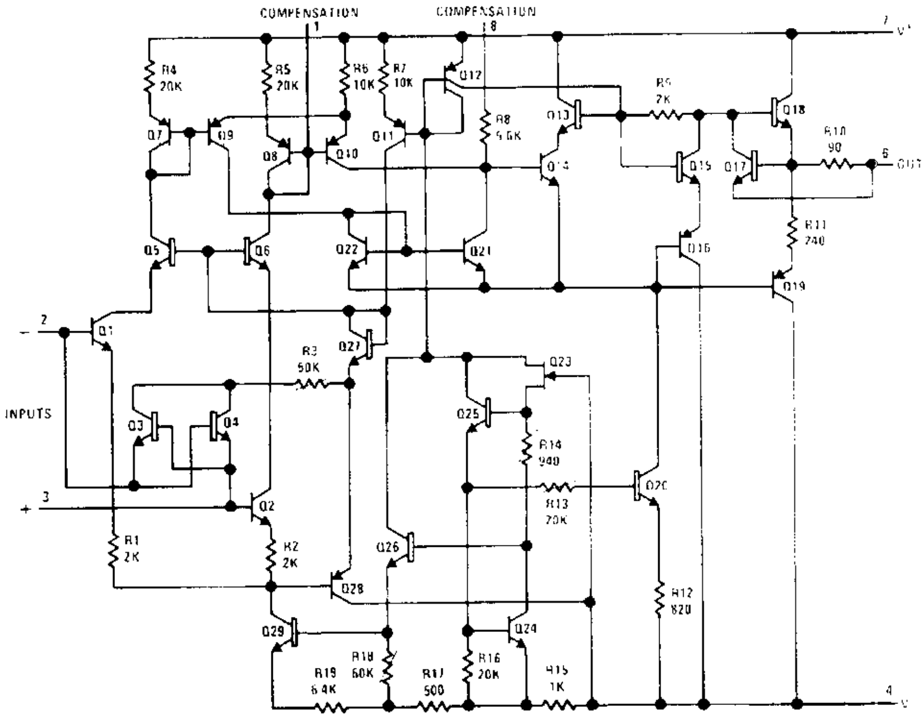
Note 3: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 4: These specifications apply for $\pm 5V \le V_S \le \pm 20V$ and $-55°C \le T_A \le +125°C$, unless otherwise specified. With the LM208, however, all temperature specifications are limited to $-25°C \le T_A \le 85°C$, and for the LM308 they are limited to $0°C \le T_A \le 70°C$.

Note 5: Refer to RETS108X for LM108 military specifications and RETs 108AX for LM108A military specifications.

Note 6: Human body model, 1.5 kΩ in series with 100 pF.

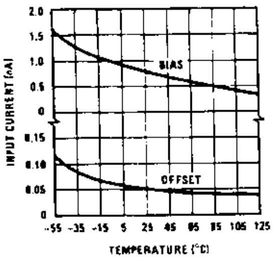
Schematic Diagram



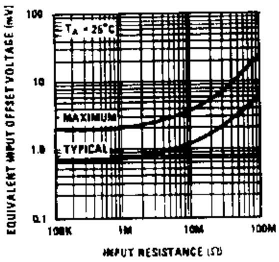
TL/H/7758-4

Typical Performance Characteristics LM108/LM208

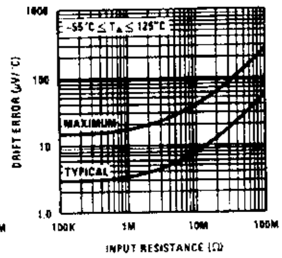
Input Currents



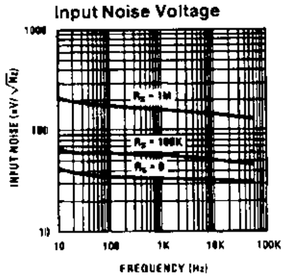
Offset Error



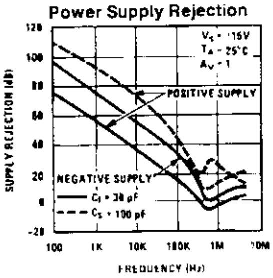
Drift Error



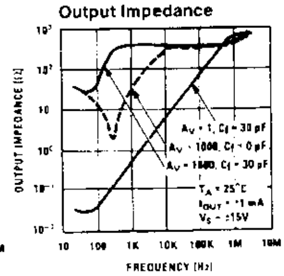
Input Noise Voltage



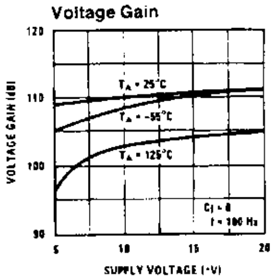
Power Supply Rejection



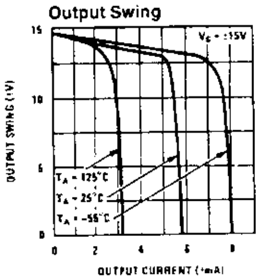
Closed Loop
Output Impedance



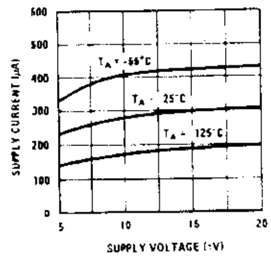
Voltage Gain



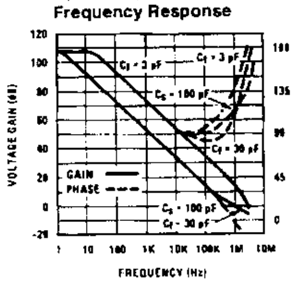
Output Swing



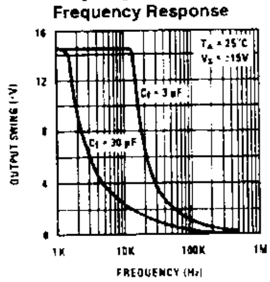
Supply Current



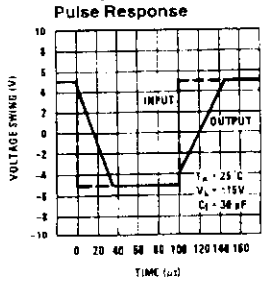
Open Loop
Frequency Response



Large Signal
Frequency Response



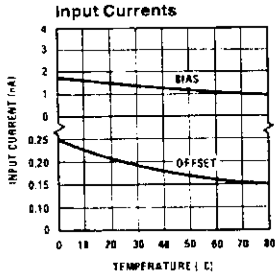
Voltage Follower
Pulse Response



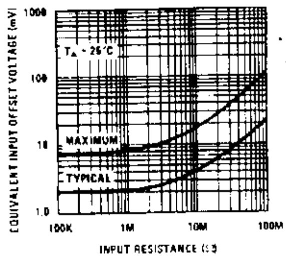
TL/H/7758-6

Typical Performance Characteristics LM308

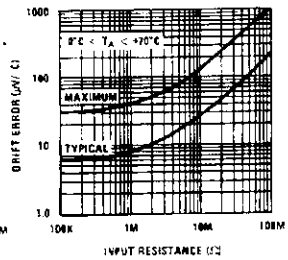
Input Currents



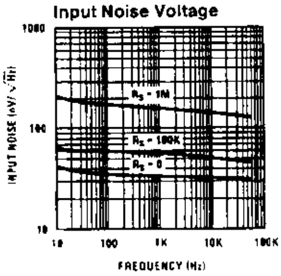
Offset Error



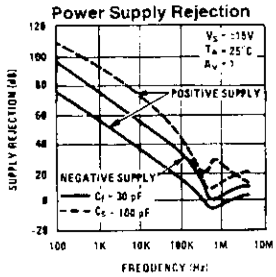
Drift Error



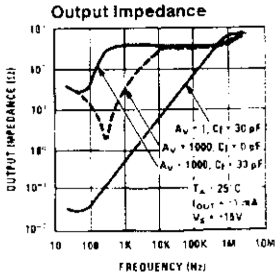
Input Noise Voltage



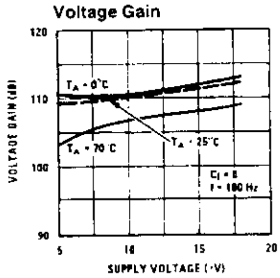
Power Supply Rejection



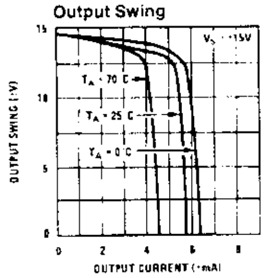
Closed Loop Output Impedance



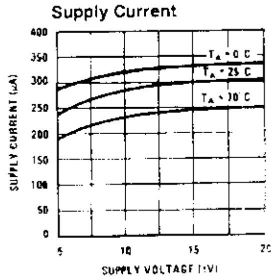
Voltage Gain



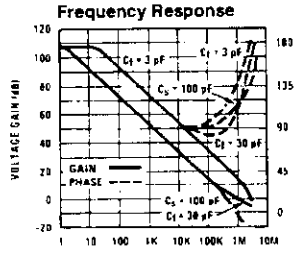
Output Swing



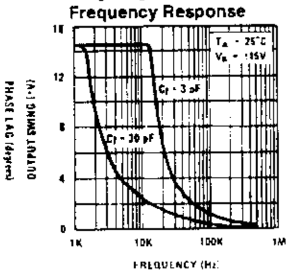
Supply Current



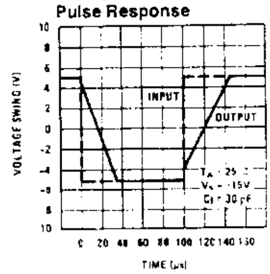
Open Loop Frequency Response



Large Signal Frequency Response



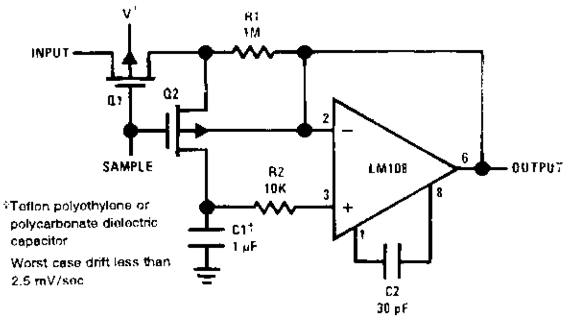
Voltage Follower Pulse Response



TL/H/7753-7

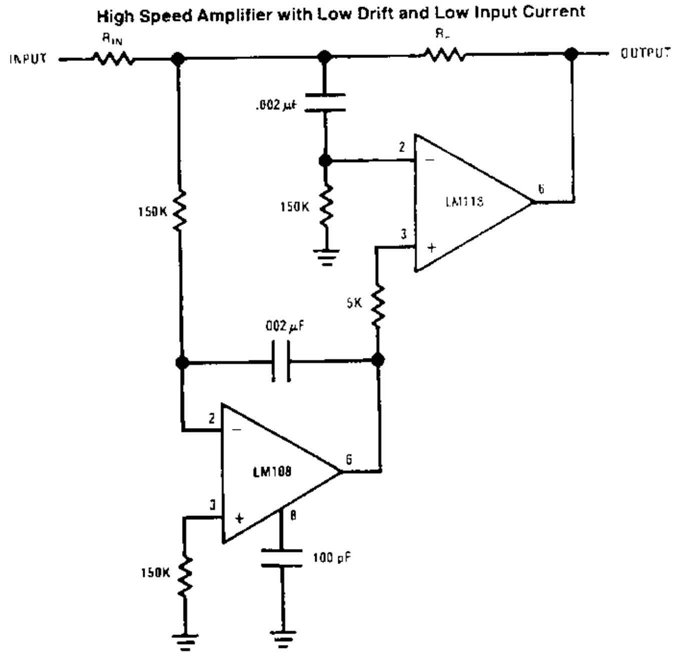
Typical Applications

Sample and Hold



TL/H/7758-4

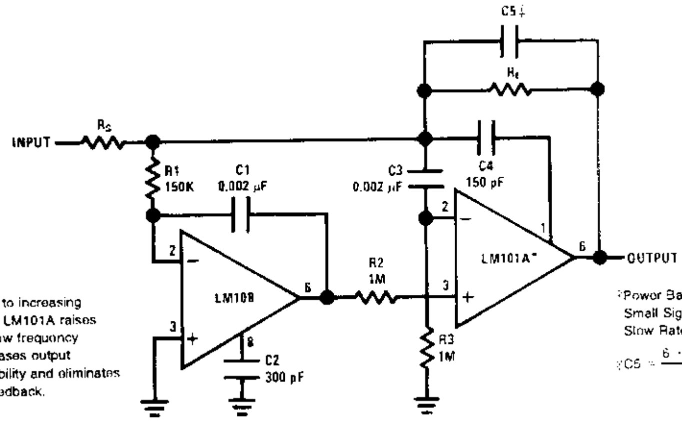
High Speed Amplifier with Low Drift and Low Input Current



TL/H/7758-5

Typical Applications (Continued)

Fast† Summing Amplifier



*In addition to increasing speed, the LM101A raises high and low frequency gain, increases output drive capability and eliminates thermal feedback.

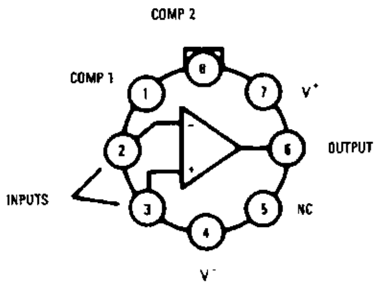
†Power Bandwidth: 250 KHz
Small Signal Bandwidth: 3.5 MHz
Slew Rate: 10V/µS

$$‡C5 = \frac{6 \cdot 10^{-8}}{R_f}$$

TL/H/7758-12

Connection Diagrams

Metal Can Package



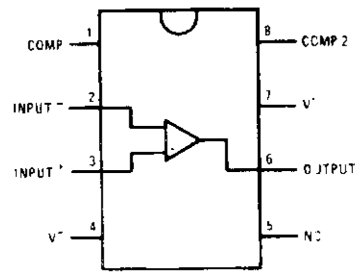
TL/H/7758-13

*Package is connected to Pin 4 (V−)

**Unused pin (no internal connection) to allow for input anti-leakage guard ring on printed circuit board layout.

Order Number LM108H, LM108H/883, LM308AH or LM308H
See NS Package Number H08C

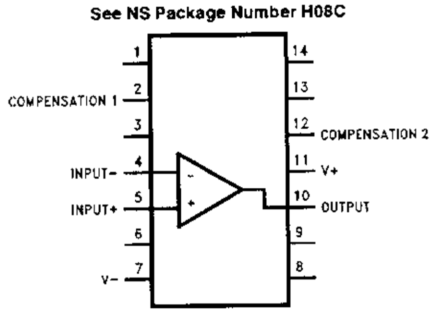
Dual-In-Line Package



TL/H/7758-13

Top View

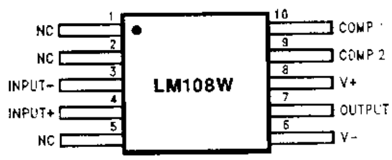
Order Number LM108J-8/883, LM308M or LM308N
See NS Package Number J08A, M08A or N08E



TL/H/7758-16

Top View

Order Number LM108J/883
See NS Package Number J14A

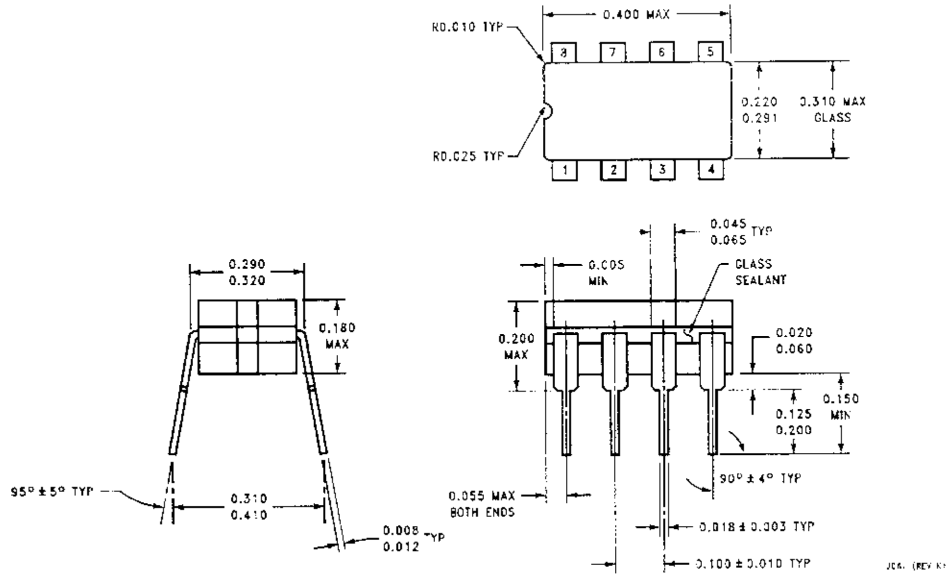


TL/H/7758-17

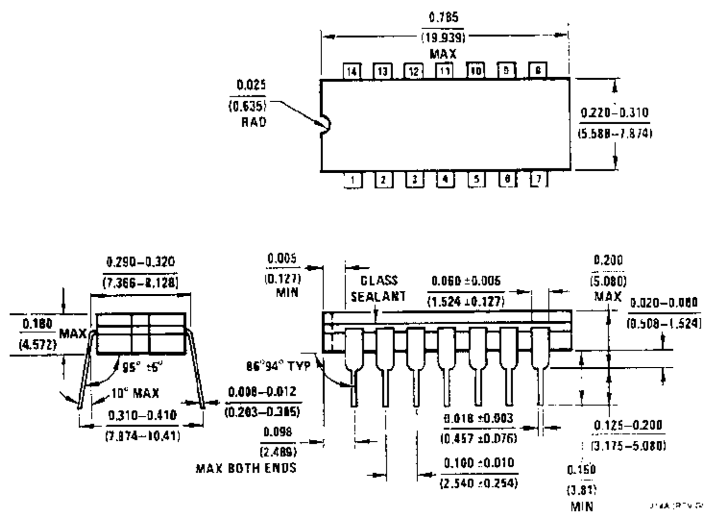
Order Number LM108W/883
See NS Package Number W10A

†Also available per JM38510/10104

Physical Dimensions inches (millimeters)

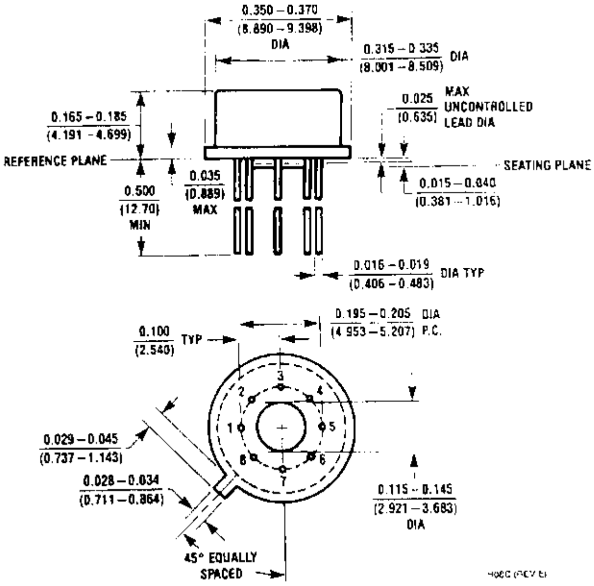


Ceramic Dual-In-Line Package (J)
Order Number LM108J/883
NS Package Number J08A

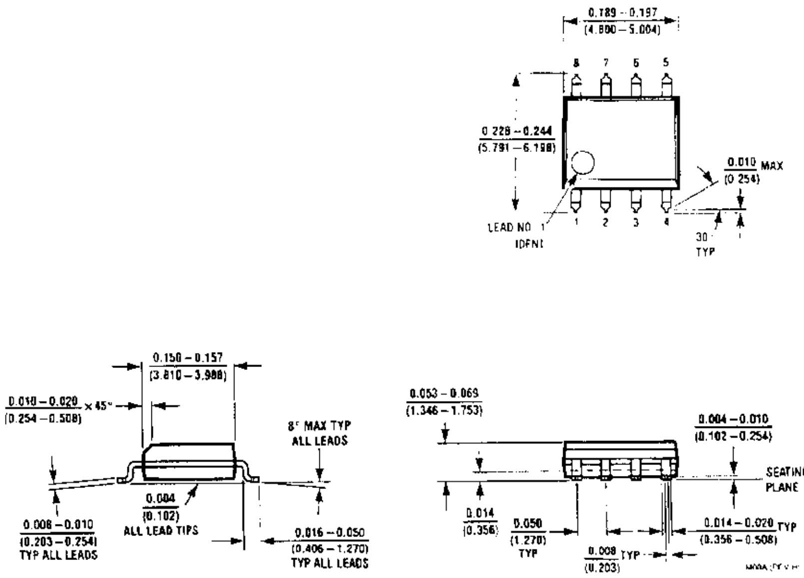


Ceramic Dual-In-Line Package (J)
Order Number LM108/883
NS Package Number J14A

Physical Dimensions inches (millimeters) (Continued)



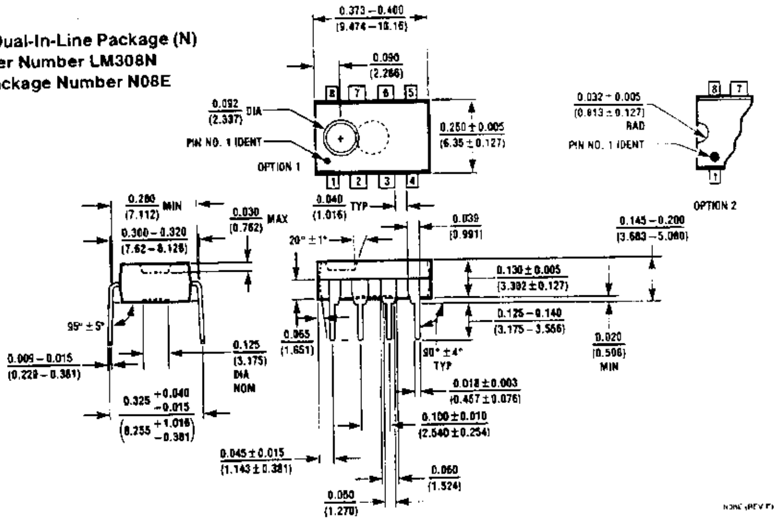
Metal Can Package (H)
Order Number LM108H, LM108H/883 or LM308H
NS Package Number H08C



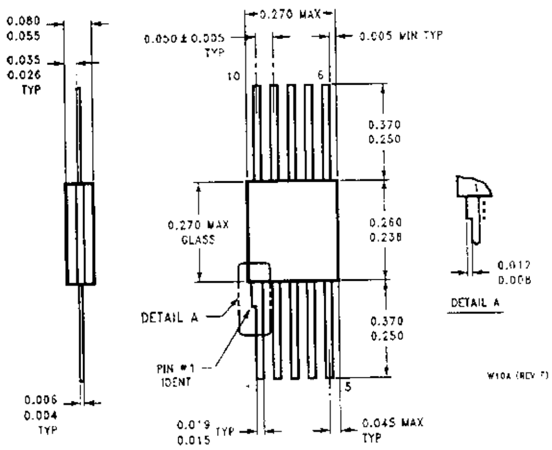
S.O. Package (M)
Order Number LM308M
NS Package Number M08A

Physical Dimensions inches (millimeters) (Continued)

Molded Dual-In-Line Package (N)
Order Number LM308N
NS Package Number N08E



Ceramic Flatpack Package (W)
Order Number LM108AW/883 or LM108W/883
NS Package Number W10A



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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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