HANDHELD TRANSDUCER CALIBRATOR USING MSP430F149A

Estd-1984

Submitted By

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Under the Guidance of

Mr.G.C.THYAGARAJAN,M.E.,

IN PARTIAL FULFILMENT OF THE REQUIRMENTS FOR THE AWARD OF THE DEGREE OF BACHELOR OF ENGINEERING IN ELECTRONICS AND COMMUNICATION ENGINEERING OF BHARATHIYAR UNIVERSITY, COIMBATORE

Department Of Electronics and Communication Engineering

Kumaraguru College of Technology
Coimbatore-641006

Kumaraguru College of Technology
Coimbatore – 641 006

Department of Electronics and Communication Engineering

CERTIFICATE

This is to certify that this project entitled

HAND HELD TRANSDUCER CALIBRATOR

has been submitted by

Mr.D.Ashwin
Mr.M.Karthik
Mr.C.M.Nanda kumar

in partial fulfillment of the requirements for the award of degree of

Bachelor of Engineering in Electronics and Communication Engineering

Branch of BHARATHIAR UNIVERSITY , Coimbatore

during the academic year 2002-2003.

G. J... 12/3/03

(Internal Guide) **(Head of the Department)**

Certified that the candidates were examined by us in the project work Viva-Voce Examination held on 18.03.2003

University Register Number ____________________

(Internal Examiner) **(External Examiner)**

CERTIFICATE

This is to certify that the following B.E. [Branch : Electronics & Communication Engineering] students of KUMARAGURU COLLEGE OF **TECHNOLOGY,** Coimbatore, had undertaken their project "Handheld **Transducer Calibrator** using MSP430F149A", from May 2002 to March 2003 at our Industry and have successfully completed it.

Mr.C.M. Nanda Kumar

Mr.D. Ashwin

Mr.M. Karthik

Their performance during that period was found to be good. We wish them all success.

Place : Coimbatore

Date : March 15, 2003

Industry Seal

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K K VENKATARAMAN
Vice President - R&D

CONTENTS

SYNOPSIS

The project is based on testing a measuring head which has a capacitive transducer . The measuring head is a commonly used testing device in textile industry to measure the width of the thread. It gives analog output depending upon the width of the thread in the capacitors dielectric medium. The other end of the measuring head is connected to the electronic unit .The measuring head has some error and this has to be rectified by tapping the signal to the electronic unit without affecting the normal process of electronic unit. For this purpose we design a measuring head tester which has to be hand held and consume less power .

The MSP430F149A is a ultralow power microcontroller consuming less than 400 micro ampere of current in active mode at 1Mhz .The current consumption can be further lowered by using low power modes . It has a in-built analog to digital converter which reduces the peripherals . A typical 3.3 Volts system is very compatible for the working of MSP430F149 and this makes it a very optimum choice for the system which should not sink any current going to the electronic unit .

The no thread value of the measuring head can assume a wide range of values depending upon the practical conditions. Initially the system as to be adjusted to the no thread value so that only the signal variation due to thread insertion is displayed. After this the signal is averaged to avoid the fluctuation in the thread . Since each thread as a standard signal variation value , depending on the displayed value the error in the measuring head is rectified .

ACKNOWLEDGEMENT

Any teamwork requires the wholehearted contribution of not only the team members, but also of the people who guide and support the work . In this regard, on the successful completion of our project, we would like to express our heartfelt gratitude to a few people .

To begin with we express our deep sense of our gratitude to our principal, **Dr. K.K.Padmanadhan, B.Sc(Engg), M.Tech, Ph.D**, for having provided necessary facilities to carry out this project successfully .

We would like to convey our sincere thanks to our Head Of the Department of Electronics and Communication Engineering., **Prof. Muthuraman Ramasamy, M.E, MISTE, C.Eng.(I), MBMESI., MIEEE(USA),FIETE,FIE** for his excellent motivation and guidance .

We are indebted to our guide **Mr. G.C. Thiagarajan, M.E** for his effort in taking valuable time out to help whenever we needed . We also express our heartfelt thanks to our project coordinator **Prof. S. Govindaraju, M.E,** ECE Department for their valuable assistance .

We would like to take this opportunity to thank **Mr.K.K.Venkatraman,M.B.A Vice President, Premier Polytronics** , for having given us the opportunity to undertake a project in Premier Polytronics . We would like to thank **Mr.Balraj ,HR** for giving us this opportunity to take up project at Premier Polytronics

Its our duty to thank our guide **Mrs.Tahnisha Jammal, Deputy** Enginneer **Research & Development** for having guided us right from the inception of our project .

We would be failing in our duty if we do not thank **Mr.S.Pradeep kumar Asst Engineer ,Research & Development** , who helped us complete to our project .

Last but not the least, we thank the teaching and non teaching staff members of Department of Electronics and Communication Engineering of our college .

Introduction

INTRODUCTION:

(1) MEASURING HEAD:

Measuring head uses capacitive transducer which is used in textile industry for measuring the width of the thread . This will be connected to the EU board where required manipulation is done . The EU will check the count of the thread and also indicate if any damages in the thread . This will ensure the quality of the thread at winding unit .

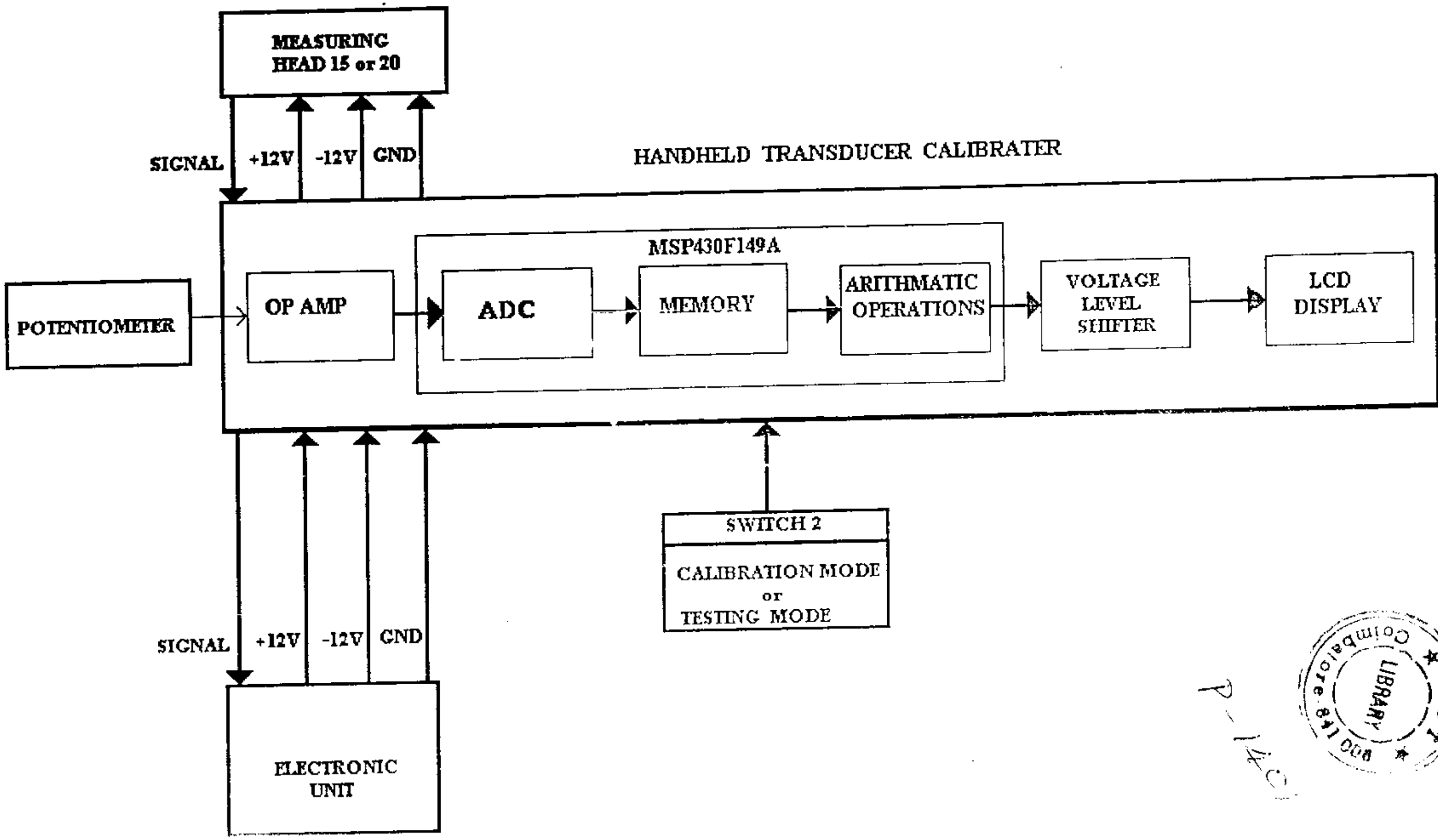
(2) NEED FOR MEASURING HEAD TESTER:

Measuring head tester is an device which detects the fault in measuring head . Capacitive transducer which present in measuring head degrades its performance in course of time . So we need to test proper working of the capacitive transducer . At present there is no device to test the head at the working stations .It has to be taken to production station and test with standard table present here . Measuring head tester is an hand held device which can be taken to the working place and can test the device .

This tester uses an ultra low power micro-controller , an amplifier and LCD module . This equipment will tap the signals between the EU and the measuring head . This will check the signals from the measuring head and check it with standard value and will display the change in the value .

Block Diagram

CALIBRATION OF CAPACITIVE TRANSDUCER USING MSP430F149A



FUNCTIONAL BLOCK DIAGRAM

1)MEASURING HEAD

This unit is used to measure the width of the thread using capacitive transducer . The signal is produced due to variation of dielectric medium wher the thread is inserted and it is sent to the eletronic unit which supplies the required power for the measuring head.

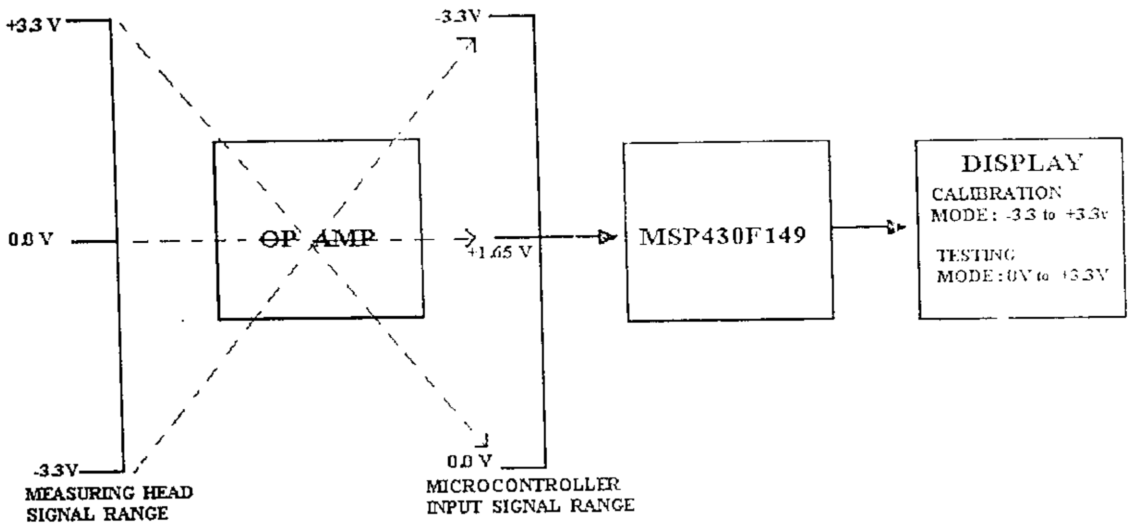
2) ELECTRONIC UNIT

This unit process the signal received from the measuring head about the quality of the thread and issues required feedback to improve the quality of the thread.

3)HANDHELD TRANSDUCER CALIBRATER

➢ OPERATIONAL AMPLIFIER

Since the input signal range of microcontroller is 0 to +3.3Volts, any signal out of this range has to be brought into this range . During calibration mode the difference amplifier has 0.5 gain so that signal is brought into the required range. Similarly during testing mode difference amplifier has gain of 15 so that a higher resolution is obtained . The **potentiometer** is used to set offset voltage at non-inverting terminal equal to no thread value.



Here op-amp 0P07 is used .

➤ MICROCONTROLLER UNIT:

Here the Analog to digital converter is inbuilt within the micro controller & uses slope conversion method. Here the minimum to maximum range is given as 0 to 3.3Volts. After each sampling the digital value of each sample is stored in a 12bit memory. Since thread has little fluctuation the sampled values cannot displayed directly .They have to be averaged before displaying .Also the display unit is slower than the micro controller unit and required delay routines are also provided.

➤ LEVEL SHIFTER :

The display unit requires active signal range 5 volts. But microcontroller outputs only 3.3 v as active signal . Similarly handshake signal from display unit has to be sent back to microcontroller unit. For this bi-directional low voltage converter is used.

➢ LCD DISPLAY:

Here the display is 4 x 20 matrix . Here the two modes, measuring head output value and initial no thread value are displayed. It drives required current from the low voltage converter.

HARDWARE DESCRIPTION:

(1) THE MICROCONTROLLER – MSP430F149A:

The MSP430 employs a von-Neumann architecture, therefore , all memory and peripherals are in one address space . The MSP430 devices constitute a family of ultra low-power ,16-bit RISC microcontrollers with an advanced architecture and rich peripheral set. The architecture uses advanced timing and design features, as well as a highly orthogonal structure to deliver a processor that is both powerful and flexible.

The MSP430 consumes less than 400 µA in active mode operating at 1 MHz in a typical 3-V system and can wake up from a <2-µA standby mode to fully synchronized operation in less than 6 µ s. These exceptionally low current requirements, combined with the fast wake-up time, enable a user to build a system with minimum current consumption and maximum battery life. Additionally, the MSP430F149A family has an abundant mix of peripherals and memory sizes enabling true system-on-a-chip designs. The peripherals include a 12-bit A/D, slope A/D, multiple timers (some with capture/ compare registers and PWM output capability), on-chip clock generation, H/W multiplier , USART(s), watchdog Timer , 6 eight bit I/O ports, and others.

➢ LOW POWER CONSUMPTION CAPABILITIES

Ultra low-power architecture:

0.1– 400 µA nominal operating current @1 MHz

1.8 – 3.6 V operation

6µs wake-up from standby mode

Extensive interrupt capability relieves need for polling

The ultra-low power system design which uses complementary metal-oxide Semiconductor (CMOS) technology, takes into account three different needs:

- The desire for speed and data throughput despite conflicting needs for ultra-low power
- Minimization of individual current consumption
- Limitation of the activity state to the minimum required by the use of low power modes

	SCG1	SCG0	OscOff	CPUOff
LPM0	0	0	0	1
LPM1	0	1	0	1
LPM2	1	0	0	1
LPM3	1	1	0	1
LPM4	1	1	1	1

➢ FLEXIBLE AND POWERFUL PROCESSING CAPABILITIES:

- ❖ Seven source-address modes
- ❖ Four destination-address modes

- Only 27 core instructions
- Prioritized, nested interrupts
- No interrupt or subroutine level limits
- Large register file
- Ram execution capability
- Efficient table processing
- Fast hex-to-decimal conversion

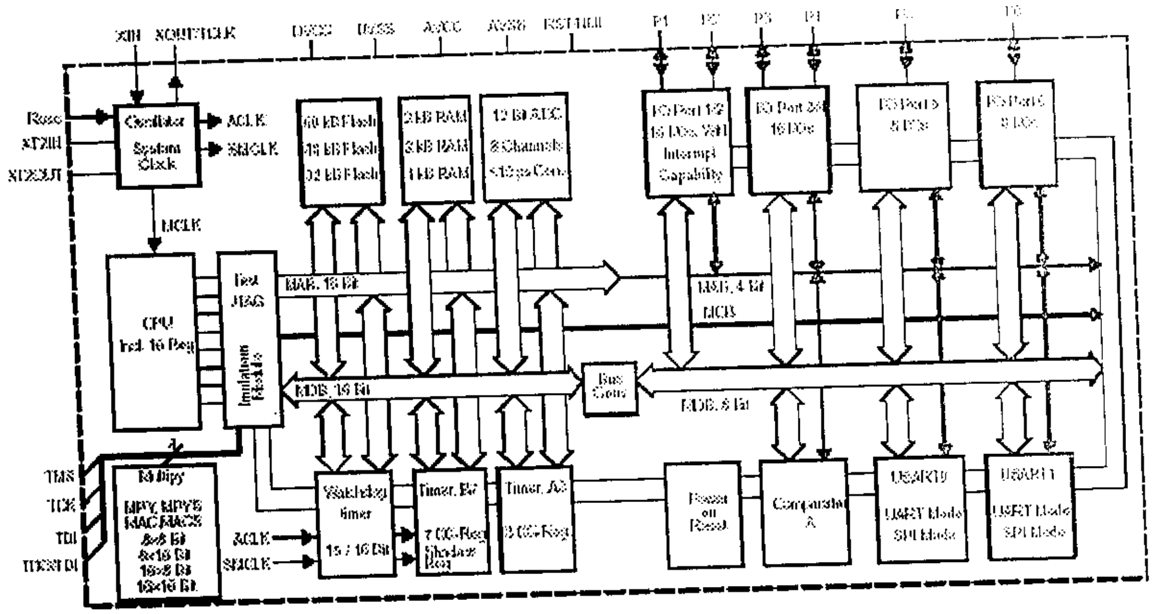
➢ PERIPHERAL SET:

- Integrated 12-bit A/D converter
- Integrated precision comparator
- Multiple timers and PWM capability
- Slope A/D conversion (all devices)
- Integrated USART(s)
- Watchdog Timer
- Multiple I/O with extensive interrupt capability
- Integrated programmable oscillator
- 32-kHz crystal oscillator (all devices)
- 450-kHz – 8-MHz crystal oscillator (selected devices)

➢ ARCHITECTURE:

This section describes the basic functions of an MSP430-based system.

The architecture of the MSP430 family is based on a memory-to-memory architecture, a common address space for all functional blocks, and a reduced instruction set applicable to all functional blocks as illustrated in figure



The MSP430 devices contain the following main elements:

- ❖ Central processing unit
- ❖ Program memory
- ❖ Data memory
- ❖ Operation control
- ❖ Peripheral modules

➢ CENTRAL PROCESSING UNIT:

The CPU incorporates a reduced and highly transparent instruction set and a highly orthogonal design. It consists of a 16-bit arithmetic logic unit (ALU), 16 registers, and instruction control logic. Four of these registers are used for Special purposes. These are the program counter (PC), stack pointer (SP), status register (SR), and constant generator (CGx). All registers, except the constant-generator registers R3/CG2 and part of R2/CG1, can be accessed using the complete instruction set. The constant generator supplies instruction constants, and is not used for data storage. The addressing mode used on CG1 separates the data from the constants.

The CPU control over the program counter, the status register, and the stack pointer (with the reduced instruction set) allows the development of applications with sophisticated addressing modes and software algorithms.

➢ PROGRAM MEMORY:

Instruction fetches from program memory are always 16-bit accesses, Whereas data memory can be accessed using word (16-bit) or byte (8-bit) instructions. Any access uses the 16-bit memory data bus (MDB)and as many of the least-significant address lines of the memory address bus (MAB) as required to access the memory locations. Blocks of memory are automatically selected through module-enable signals. This technique reduces overall current consumption. Program memory is integrated as programmable or mask-programmed memory.

In addition to program code, data may also be placed in the ROM section of the memory map and may be accessed using word or byte instructions; this is useful for data tables, for example. This unique feature gives the MSP430 an advantage over other microcontrollers, because the data tables do not have to be copied to RAM for usage. Sixteen words of memory are reserved for reset and interrupt vectors at the top of the 64-kilobytes address space from 0FFFFh down to 0FFE0h.

Register by Functions:

Program counter (PC)	R0
Stack pointer (SP)	R1
Status register (SR)	R2
Constant generator (CG1)	
Constant generator (CG2)	R3
Working register R4	R4
Working register R5	R5
:	:
Working register R13	R13
Working register R14	R14
Working register R15	R15

➤ DATA MEMORY:

The data memory is connected to the CPU through the same two buses as the program memory (ROM) : the memory address bus (MAB) and the memory data bus (MDB). The data memory can be accessed with full(word) data width or with reduced (byte) data width. Additionally, because the RAM and ROM are connected to the CPU via the same busses, program code can be loaded into and executed from RAM. This is another unique feature of the MSP430 devices, and provides valuable, easy-to-use debugging capability.

➤ OPERATION CONTROL:

The operation of the different MSP430 members is controlled mainly by the information stored in the special–function registers (SFRs) . The different bits in the SFRs enable interrupts, provide information about the status of interrupt flags, and define the operating modes of the peripherals . By disabling peripherals that are not needed during an operation, total current consumption can be reduced.

➤ PERIPHERALS:

Peripherals are connected to the CPU through data, address, and control busses, and can be easily handled using all memory-manipulation instructions.

➤ OSCILLATOR AND SYSTEM CLOCK

Three clocks are used in the system the main system (master) clock (MCLK) used by the CPU and the system, the subsystem (master) clock (SMCLK) used by the peripheral modules, and the auxiliary clock (ACLK) originated by LFXT1CLK (crystal frequency) and used by the peripheral modules . Following a POR the DCOCLK is used by default, the DCOR bit is reset, and the DCO is set to the nominal initial frequency . Additionally, if either LFXT1CLK or XT2CLK fails as the source for MCLK, DCOCLK is automatically selected to ensure fail-safe operation . SMCLK can be generated from XT2CLK or DCOCLK . ACLK is always generated from LFXT1CLK . Crystal oscillator LFXT1 can be defined to operate with watch crystals (32,768 Hz) or with higher-frequency ceramic resonators or crystals . If the high-frequency XT1 mode is selected, external capacitors from XIN to VSS and XOUT to VSS are required, as specified by the crystal manufacturer. The LFXT1 oscillator starts after application of VCC . If the OscOff bit is set to 1, the oscillator stops when it is not used for MCLK.

Crystal oscillator XT2 is identical to oscillator LFXT1, but only operates with higher-frequency ceramic resonators or crystals. Clock signals ACLK , MCLK, and SMCLK may be used externally via port pins .

Different application requirements and system conditions dictate different system-clock requirements, including :

- ❖ High frequency for quick reaction to system hardware requests or events
- ❖ Low frequency to minimize current consumption, EMI, etc .
- ❖ Stable peripheral clock for timer applications, such as real-time clock
- ❖ Start-stop operation that can be enabled with minimum delay

➢ DIGITAL I/O :

There are six 8-bit I/O ports implemented— ports P1 through P6 . Ports P1 and P2 use seven control registers, while ports P3, P4, P5, and P6 use only four of the control registers to provide maximum digital input /output flexibility to the application:

- ❖ All individual I/O bits are independently programmable .
- ❖ Any combination of input, output, and interrupt conditions is possible.
- ❖ Interrupt processing of external events is fully implemented for all eight bits of ports P1 and P2.
- ❖ Read/write access to all registers using all instructions is possible.

The seven control registers are:

- Input register 8 bits at ports P1 through P6
- Output register 8 bits at ports P1 through P6
- Direction register 8 bits at ports P1 through P6
- Interrupt edge select 8 bits at ports P1 and P2
- Interrupt flags 8 bits at ports P1 and P2
- Interrupt enable 8 bits at ports P1 and P2
- Selection (port or module) 8 bits at ports P1 through P6

Each one of these registers contains eight bits. Two interrupt vectors are implemented: one commonly used for any interrupt event on ports P1.0 to P1.7, and another commonly used for any interrupt event on ports P2.0 to P2.7. Ports P3, P4, P5, and P6 have no interrupt capability.

➢ WATCHDOG TIMER

The primary function of the Watchdog Timer (WDT) module is to perform a controlled system restart after a software upset has occurred. A system reset is generated if the selected time interval expires. If an application does not require this watchdog function, the module can work as an interval timer, which generates an interrupt after a selected time interval. The Watchdog Timer counter (WDTCNT) is a 15/16 - bit up-counter not directly accessible by software. The WDTCNT is controlled using the

Watchdog Timer control register (WDTCTL), which is an 8 -bit read/write Register . Writing to WDTCTL in either operating mode (watchdog or timer) is only possible when using the correct password (05Ah) in the high-byte . If any value other than 05Ah is written to the high-byte of the WDTCTL, a system reset PUC is generated . The password is read as 069h to minimize accidental write operations to the WDTCTL register. The low-byte stores data written to the WDTCTL . In addition to the Watchdog Timer control bits, there are two bits included in the WDTCTL that configure the NMI pin.

➤ USART0 and USART1

There are two USART peripherals implemented in the MSP430F149A : USART0 and USART1 . They use different pins to communicate, and different registers for module control . Registers with identical functions have different addresses .

The universal synchronous / asynchronous interface is a dedicated peripheral module used in serial communications . The USART supports synchronous SPI (3- or 4-pin), and asynchronous UART communication protocols, using double-buffered transmit and receive channels . Data streams of 7 or 8 bits in length can be transferred at a rate determined by the program, or by an external clock . Low-power applications are optimized by UART mode options which allow for the reception of only the first byte of a complete frame . The application software should then decide if the succeeding data is to be processed . This option reduces power consumption .

Two dedicated interrupt vectors are assigned to each USART module —one for the receive and one for the transmit channels .

➢ TIMER A :

Timer_A is an extremely versatile timer made up of :

- ❖ 16-bit counter with 4 operating modes
- ❖ Selectable and configurable clock source
- ❖ Three or five independently configurable capture / compare registers with configurable inputs
- ❖ Three or five individually configurable output modules with 8 output modes

Timer_A can support multiple, simultaneous, timings ; multiple capture compares ; multiple output waveforms such as PWM signals ; and any combination of these . Also, each capture/compare register has hardware support for implementing serial communications such as UART protocol .

➢ TIMER B :

In its default condition, Timer_B operates identically to Timer_A, except the SCCI bit is not implemented on Timer_B .

- ❖ 16-bit counter with 4 operating modes and four selectable lengths (8-bit, 10-bit, 12-bit, or 16-bit)
- ❖ Up to seven independently - configurable capture/compare registers with configurable inputs and double-buffered compare registers .
- ❖ Up to seven individually-configurable output modules with eight output modes

➢ A/D CONVERTER

The 12- bit analog –to -digital converter (ADC) uses a 10- bit weighted capacitor array plus a 2-bit resistor string . The CMOS threshold detector in the successive - approximation conversion technique determines each bit by examining the charge on a series of binary-weighted capacitors . The features of the ADC are :

- ❖ 12-bit converter with ±1 LSB differential (DNL) and ±1 LSB integral non linearity (INL)
- ❖ Built- in sample -and – hold
- ❖ Eight external and four internal analog channels. The external ADC input terminals are shared with digital port I/O pins.

- ❖ Internal reference voltage VREF+ of 1.5 V or 2.5 V, software - selectable by
- ❖ control bit 2-5 V
- ❖ Internal – temperature diode for temperature measurement
- ❖ Battery – voltage measurement: N = 0.5 × (AVCC - AVSS) × 4096/1.5V;

  VREF+ is selected for 1.5 V.
- ❖ Source of positive reference voltage level VR+ can be selected as internal (1.5 V or 2.5 V), external, or AVCC.
- ❖ The source is selected individually for each channel.
- ❖ Source of negative reference voltage level VR- can be selected as external

Table 4. Reference Voltage Configurations

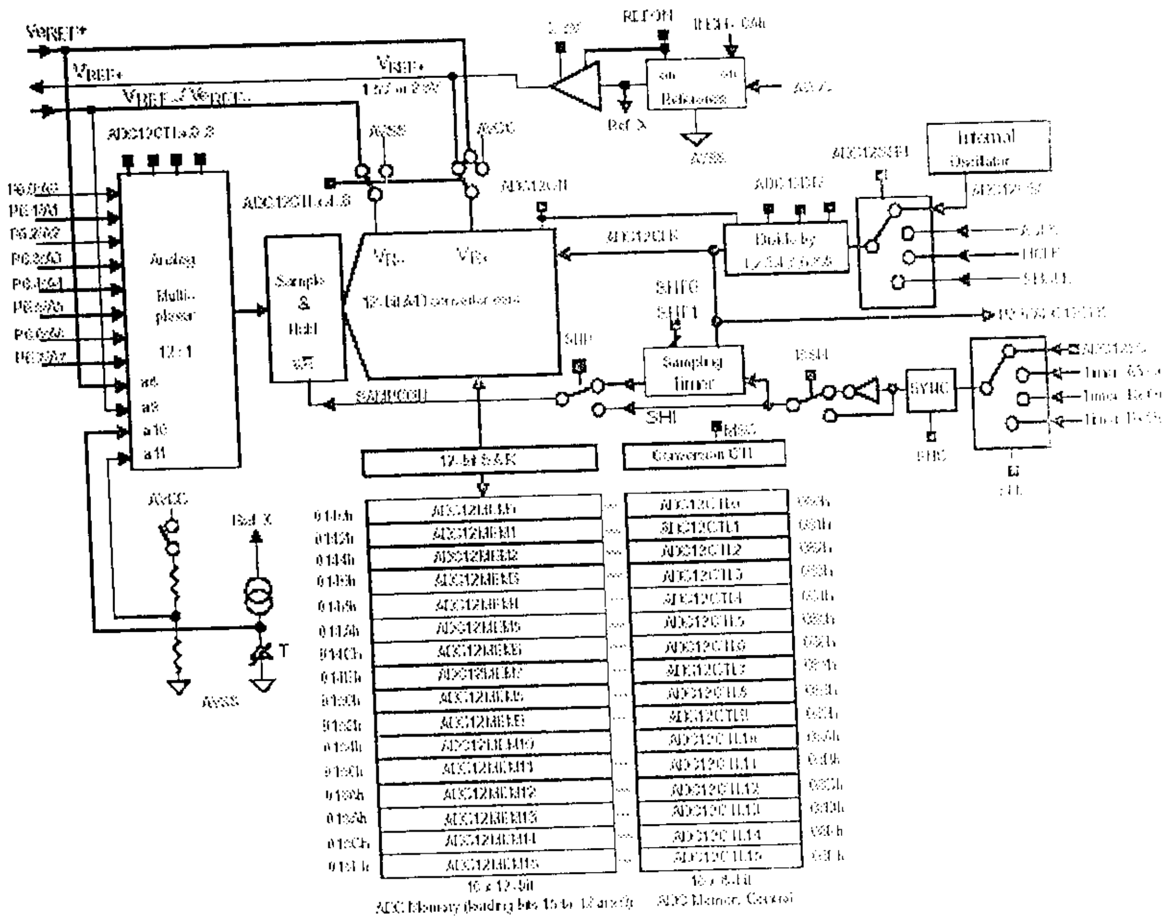
SREF	VOLTAGE AT VR+	VOLTAGE AT VR–
0	AV_{CC}	AV_{SS}
1	V_{REF+} (internal)	AV_{SS}
2, 3	V_{eREF+} (external)	AV_{SS}
4	AV_{CC}	V_{REF-}/V_{eREF-} (internal or external)
5	V_{REF+} (internal)	V_{REF-}/V_{eREF-} (internal or external)
6, 7	V_{eREF+} (external)	V_{REF-}/V_{eREF-} (internal or external)

or AVSS. The source is selected individually for each channel

- ❖ Conversion time can be selected from various clock sources: ACLK, MCLK, SMCLK, or the internal ADC12CLK oscillator. The clock source is divided by an integer from 1 to 8, as selected by software.
- ❖ Channel conversion : individual channels, a group o f channels, or repeated conversion of a group of channels. If conversion of a group of channels is

selected , the sequence, the channels, and the number of channels in the group can be defined by software . For example, a1-a2-a5-a2-a2-....

- The conversion is enabled by the ENC bit, and can be triggered by software via sample and conversion control bit ADC12SC, Timer_A3, or Timer_Bx. Most of the control bits can be modified only if ENC control Bit is low. This prevents unpredictable results caused by unintended modification.
- Sampling time can be 4 × n0 × ADC12CLK or 4 × n1 × ADC12CLK. It can be selected to sample as long as the sample signal is high (ISSH=0) or low (ISSH=1). SHT0 defines n0 and SHT1 defines n1.
- The conversion result is stored in one of sixteen registers. The sixteen registers have individual addresses and can be accessed via software. Each of the sixteen registers is linked to an 8-bit register that defines the positive and negative reference source and the channel assigned.



➢ Flash Memory:

The flash memory module is electrically erasable and programmable. Devices with a flash memory module are multiple-time programmable devices (MTP). They can be erased and programmed off-board, or in a system via the MSP430's JTAG peripheral module or via the processor's resources. Software running on an MSP430 device can erase and program the flash memory module . This active software may run in RAM, in ROM, or in the flash memory . The flash memory may be a different memory module or the same memory module . The active software may not be in a memory location which is actively erased .

(2) AMPLIFIER (OP07C):

This device offer low offset and long-term stability by means of a low-noise, chopperless, bipolar-input-transistor amplifier circuit . For most applications, external components are not required for offset nulling and frequency compensation . The true differential input, with a wide input-voltage range and outstanding common-mode rejection, provides maximum flexibility and performance in high-noise environments and in noninverting applications. Low bias currents and extremely high input impedances are maintained over the entire temperature range . The OP07 is unsurpassed for low-noise, high-accuracy amplification of very-low-level signals .

- Low Noise
- Wide input voltage range 0 to +/- 14 typ
- Wide supply voltage range +/-3 to +/- 18 typ

(3) OCTAL BUS TRANSCEIVER AND 3.3-V TO 5-V SHIFTER(SN74LVC4245A):

This 8-bit (octal) non-inverting bus transceiver contains two separate Supply rails ; B port has VCCB, which is set at 3.3 V, and A port has VCCA, which is set at 5 V . This allows for translation from a 3.3-V to a 5-V environment, and vice versa .

The SN74LVC4245A is designed for asynchronous communication between data buses . The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction – control (DIR) input . The output - enable (OE) input can be used to disable the device so the buses are effectively isolated .

The SN74LVC4245A pin out allows the designer to switch to a normal all - 3.3 - V or all –5 - V 20 - pin '245 device without board re-layout.

(4) VOLTAGE REGULATORS:

➢ 7805 (12 V to 5 V) REGULATOR:

This type of voltage regulators are monolithic integrated circuits designed as fixed voltage regulators for a wide variety of applications including local, on card regulation . These regulators employ internal current limiting, thermal shutdown, and safe area compensation . With adequate heat sinking they can deliver output currents in excess of 1.0 A . Although designed primarily as a fixed voltage regulator , these devices can be used with external components to obtain adjustable voltages and currents .

- Output Current in Excess of 1.0 A
- No External Components Required
- Internal Thermal Overload Protection
- Internal Short Circuit Current Limiting
- Output Voltage Offered in 2% and 4% Tolerance

➢ REG1117 Positive Regulator:

The REG1117 is a family of easy-to-use three – terminal voltage regulators . The family includes a variety of fixed and adjustable - voltage versions, two currents (800mA and1A) and two package types (SOT-223 and DDPAK) .

Output voltage of the adjustable versions is set with two external resistors. The REG1117's low dropout voltage allows its use with as little as 1V input – output voltage differential.

Laser trimming assures excellent output voltage accuracy without adjustment. An NPN output stage allows output stage drive to contribute to the load current for maximum efficiency.

(4) SWITCHES:

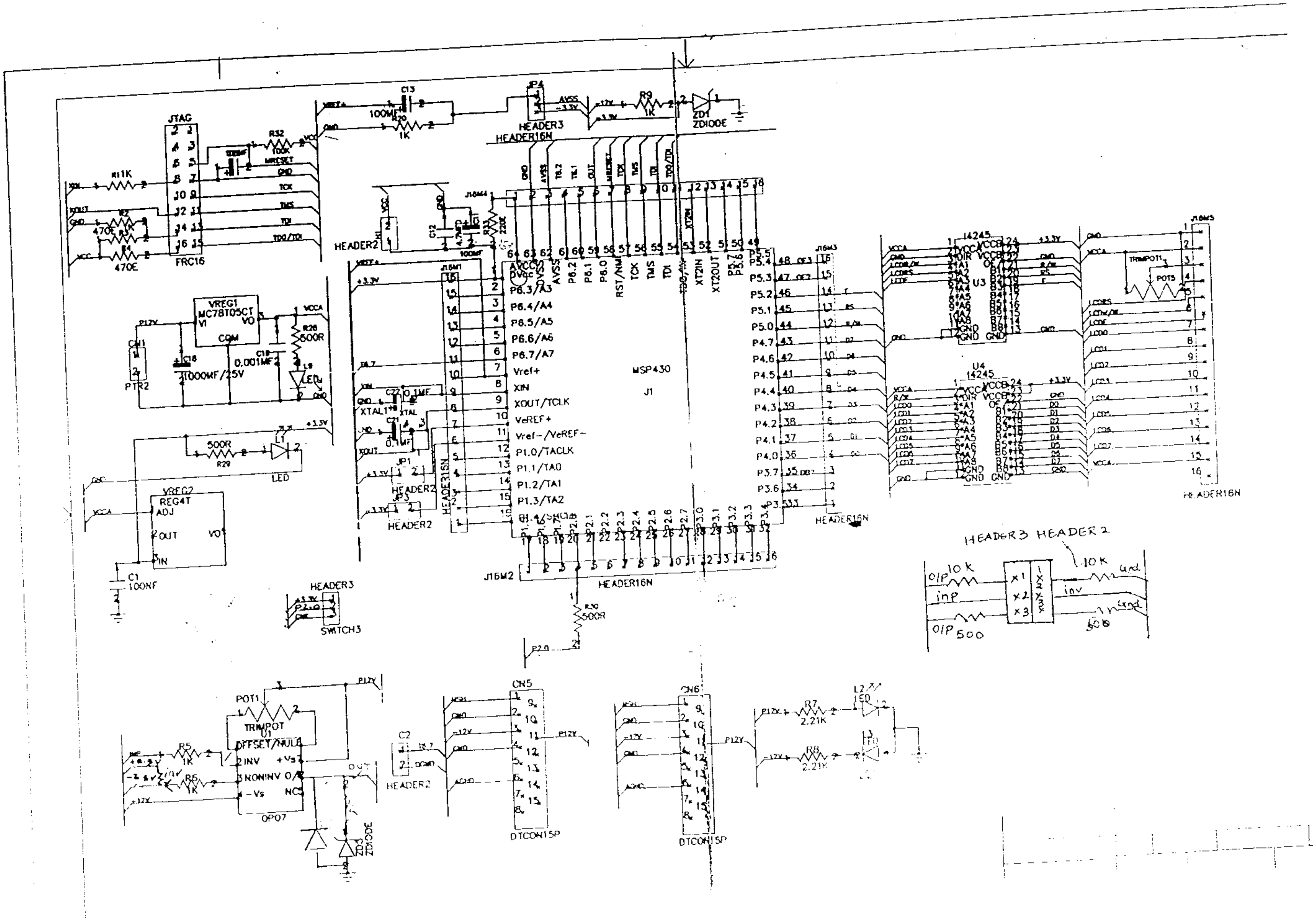
➢ DPDT SWITCH AND SPST:

Double pole double throw switch is used here for selection of input signal and mode of operation. The single pole single throw switch used here for head selection. These switches are ordinary movable switch. These are placed on top of the cabin.

(5) ODM-SERIES LCD DOT MATRIX MODULE:

The Oriole's Display Module is a dot matrix liquid crystal display that displays alphanumeric, Japanese characters and symbols. The built in controller and driver LSIs provide convenient connectivity between a dot matrix LCD and most 4 or 8 bit microprocessors or microcontrollers. All the functions required for dot matrix liquid crystal display drive are internally provided . The CMOS technology makes the device ideal for applications in hand held, portable and other battery powered instruments with low power consumption . Some of the features in ODM module are

- ❖ Built-in Dot Matrix LCD controller with font 5x7 or 5x10 dots .
- ❖ Display Data Ram for 80 characters (80x8 bits) .
- ❖ Character generator ROM ,with 160 characters in font 5x7 and 32 characters in 5x10 dots .
- ❖ Internal automatic reset circuit on power ON .
- ❖ Built in Oscillator circuit .
- ❖ Wide range of instruction functions .


JTAG
FRC16
R11K
470E
R32
100K
MRESET
GND
TCK
TMS
TDI
TDO/TDI
C13
100MF
R20
1K
JP4
AVSS
HEADER3
R9
1K
ZD1
ZD100E
HEADER16N
J16M4
HEADER2
C12
R33
220E
VREG1
MC78T05CT
VI
VO
COM
C18
1000MF/25V
C19
0.001MF
R26
500R
LED
PTR2
R29
500R
L1
VREG2
REG4T
ADJ
OUT
IN
C1
100NF
J16M1
XTAL1
XTAL
C22
0.1MF
C21
JP1
JP3
HEADER2
HEADER16N
MSP430
J1
AVCC
DVCC
AVSS
P6.3/A3
P6.4/A4
P6.5/A5
P6.6/A6
P6.7/A7
Vref+
XIN
XOUT/TCLK
VeREF+
Vref-/VeREF-
P1.0/TACLK
P1.1/TA0
P1.2/TA1
P1.3/TA2
P6.2
P6.1
P6.0
RST/NMI
TCK
TMS
TDI
XT2IN
XT2OUT
P5.7
P5.6
P5.5
P5.4
P5.3
P5.2
P5.1
P5.0
P4.7
P4.6
P4.5
P4.4
P4.3
P4.2
P4.1
P4.0
P3.7
P3.6
P3.5
P3.4
P3.3
P3.2
P3.1
P3.0
P2.7
P2.6
P2.5
P2.4
P2.3
P2.2
P2.1
J16M3
J16M2
R30
500R
HEADER3
SWITCH3
14245
U3
U4
VCCA
VCCB
DIR
OE
GND
J16M5
TRIMPOT1
POT5
HEADER3 HEADER2
O/P 10K
inp
O/P 500
10K
Gnd
inv
500
POT1
TRIMPOT
U1
OFFSET/NULL
INV
NONINV
+Vs
-Vs
O/P
NC
OP07
R5
1K
OUT
ZD3
ZD100E
CN5
CN6
C2
HEADER2
DTCON15P
P12V
R7
2.21K
R8
2.21K
L2
L3
LED

CONNECTION DESCRIPTION AND PROCEDURE:

The components that are used in this project are as follows:

a) MSP430F149A controller

b) JTAG connector

c) Op-amp OP07C

d) SN74LVC4245

e) DPDT switches

f) Potentiometer

g) Regulators - REG7805, REG1117

h) ORIOLE LCD Module

PIN ALLOTMENTS AND COMPONENT WORKING:

The components that are connected to the micro-controller are as follows .

a) OPERATIONAL AMPLIFIER:

The OPAMP gets input from MH15/MH20 capacitive transducer and the amplified output is given to the port pin p6.0 of the MSP430 .This pin function acts as an ADC converter . The opamp is designed for differential amplifier . The amplification of the differential amplifier is designed different for different modes . For the calibration mode and for dc value calculation the gain is as that output is half the input . For the testing mode the gain is kept at 15 times the input .

The inputs to the op-amp is given as follows . The input to the opamp from measuring head is given to the inverting terminal . The non-inverting terminal input is as reference which is given from potentiometer which can be varied between -3 t0 +3 v . Certain initial conditions are set for the opamp to ensure the safety of the device . The non-inverting input POT is adjusted for +3 v initially.

The calibration here is done by making the dc voltage of measuring head at inverting equal to same voltage at the non-inverting input . Thus the output of amplifier is zero . This procedure is done in calibration mode. In the testing mode the variation from the dc value after thread is inserted into the measuring head .

b) SWITCHES (DPDT) :

In the circuit two DPDT switches are used . Each for different purpose . One of the DPDT switch is used for the mode selection and input selection . The one output of it is given to the port pin p2.0 and other to the inverting terminal of the op-amp . This is in synchronous with the other DPDT switch in such a way that in mode selection of other switch here switches will give the feedback resistance of the amplifier . This implies that in calibration mode the feedback will be different that of testing mode . Thus other switch will be connected with required feedback resistance .

c) REGULATORS:

The regulators that are used are I) REG7805 II) REG1117 . These are used for converting from available voltage to required voltage and also for

regulated power supply . Here the REG7805 is used for converting voltage from +12 to 5v . The regulated supply is given to REG1117 , level shifter and oriole module . The voltage from this given to the REG1117 will convert it to 3.3 v . This will supply power for MSP430 . This also goes to the level shifter. The MSP pins AVCC and DVCC gets an regulated voltage from this regulator .

d) BI-DIRECTIONAL LEVEL SHIFTER:

This level shifter is connected to the MSP430 port pins p5 and p4 . The data lines and control lines for the LCD is given through this port pins . This level shifter acts as an function of converting an 3.3v data signal from MSP to an LCD module which logic operating at 5 v . Thus also the data and control from LCD can be got by MSP as level shifter is bi-directional i.e. from 5v to 3.3v . Thus an flexible approach is got in using the LCD module . This level shifter is supplied power from the two regulators used in the circuit . The 3.3v side is connected to the MSP ports and the 5 v side is connected to the LCD module port .

e) **ORIOLE LCD MODULE:**

The ORIOLE display used here is 20x4 line display . This gets control signals from the MSP through an level shifter . The supply to this is given from the REG7805 output as it operates on 5 v. The contrast for the lcd can be adjusted using the trimpot used here . The display is initialized by series of simple routine and then characters for display is send . This display is used for viewing the ADC output and the present calibration .

f) **JTAG CIRCUIT :**

This circuit here is to load the program from cpu to the flash memory in the MSP . This pins are connected to various pins of the controller as shown in the circuit diagram .

SOFTWARE IMPLEMENTATION:

The following algorithm and flow chart give an overview of the flow of operation of the measuring head testing device.

GENERAL ALGORITHM:

The measuring head testing device has two modes of operations,

a) Calibration mode

b) Testing mode

CALIBRATION MODE:

1) Here before calibrating , the DC voltage of the measuring head without any filament in its chamber is noted down . It is for noting the output voltage change with respect to its surrounding and atmospheric conditions.

2) The ADC is activated for the particular sampling time . The start of conversion and end of conversion are given after the sampling time. Then the DC voltage is converted to digital and stored in its allotted memory locations.

3) The DC converted voltage will be in hexadecimal value. This value is converted to decimal values. This is done by repeated addition of the single bit resolution for that operating voltage(0v-3.3v).This gives the

single bit resolution of $8.0495658113 \times 10^{-5}$ .The hexadecimal value is compared with the middle i,e $7FF_{16}$ of the total range of 12 bits of ADC. If the value is more than $7FF_{16}$, then the number is recognized as 'negative' number. If otherwise , the number is recognized as 'positive' number . The corresponding symbol is displayed on the output.

4) The resolution for DC calibration is kept as 0.0016111328125 . This reading is stored in memory permanently and is given to the display routine. To calibrate its output the resolution per bit is given as $8.0495658113 \times 10^{-4}$.

5) This voltage is then clamped to zero using the opamp as an clamper . This is done using an potentiometer.

6) The output values are continuously checked for zero . If it is found , then the display will display that the output is calibrated.

7) The switch position of the DPDT switch is checked again to get the users decision on which routine to go next, depending on the choice the next routine is called.

TESTING MODE:

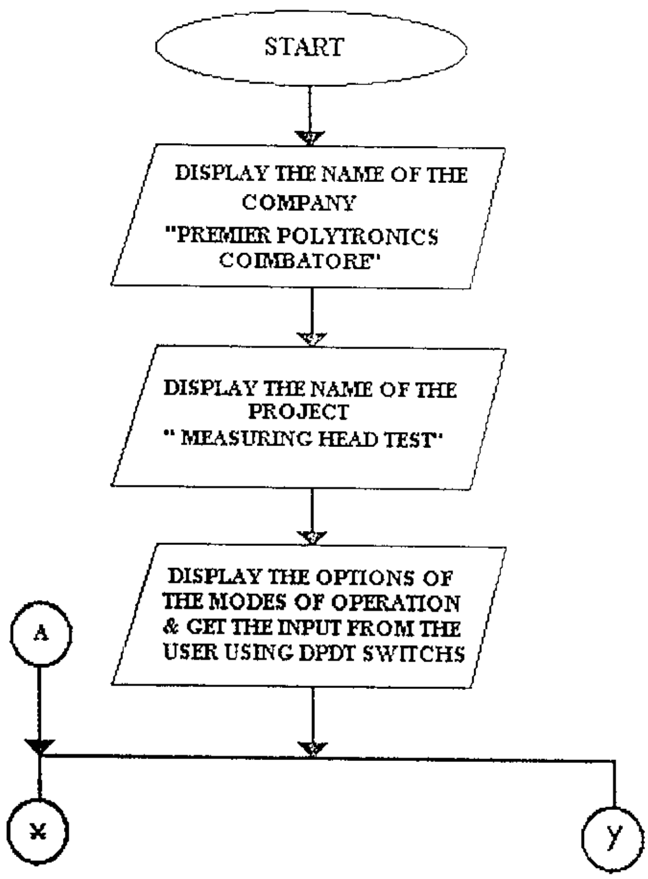
1) In this mode too the Dc voltage is displayed from the memory location. This is for user identification.

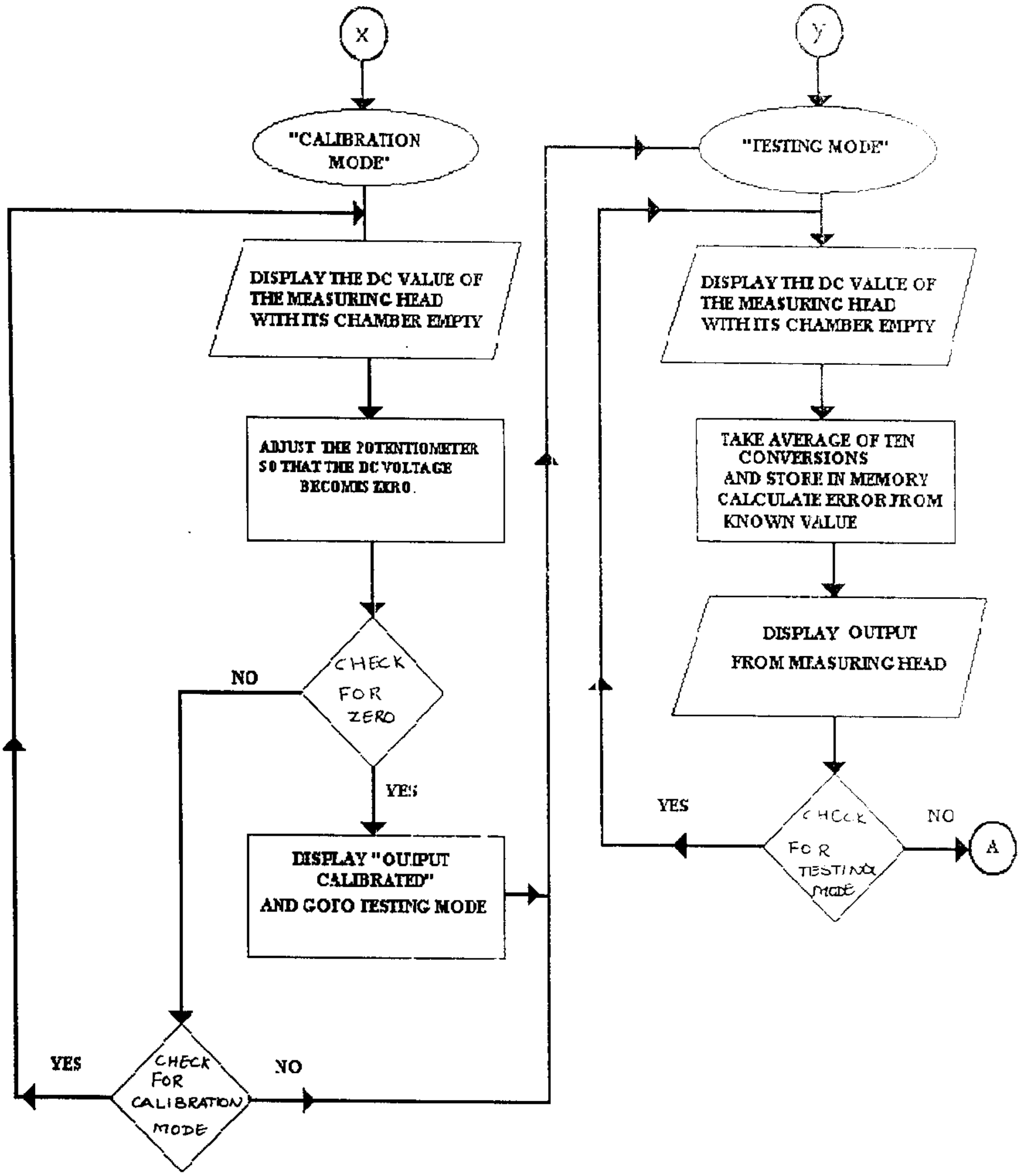
2) The purpose for this mode is that, to see the voltage shift in the measuring head when inserting the filament.

3) The output voltage is again converted to digital using ADC. This is again converted to decimal with the resolution of $8.0495658113 \times 10^{-5}$ per bit.

4) The switch position of the DPDT switch is checked again to get the users decision on which routine to go next, depending on the choice the next routine is called.

FLOWCHART


START
DISPLAY THE NAME OF THE COMPANY "PREMIER POLYTRONICS COIMBATORE"
DISPLAY THE NAME OF THE PROJECT " MEASURING HEAD TEST"
DISPLAY THE OPTIONS OF THE MODES OF OPERATION & GET THE INPUT FROM THE USER USING DPDT SWITCHS
A
X
Y


X
"CALIBRATION MODE"
DISPLAY THE DC VALUE OF THE MEASURING HEAD WITH ITS CHAMBER EMPTY
ADJUST THE POTENTIOMETER SO THAT THE DC VOLTAGE BECOMES ZERO.
CHECK FOR ZERO
NO
YES
DISPLAY "OUTPUT CALIBRATED" AND GOTO TESTING MODE
CHECK FOR CALIBRATION MODE
YES
NO
Y
"TESTING MODE"
DISPLAY THE DC VALUE OF THE MEASURING HEAD WITH ITS CHAMBER EMPTY
TAKE AVERAGE OF TEN CONVERSIONS AND STORE IN MEMORY CALCULATE ERROR FROM KNOWN VALUE
DISPLAY OUTPUT FROM MEASURING HEAD
CHECK FOR TESTING MODE
YES
NO
A

```
;*****************************************************************************
;
;
;        CALIBRATION OF CAPACITIVE TRANSDUCER USING MSP430F149A
;                ----------------------------------------------
;
;
;*****************************************************************************
#include      "msp430x14x.h"
;_____________________________________________________________________________
;
;                      LABLES INTALIZATION
;                          ------------------
;_____________________________________________________________________________
RW          equu       0x001
RS          equ        0x002
E           equ        0x004
#define     ANSD3      0x0206
#define     ANSD2      0x0204
#define     ANSD1      0x0202
#define     ANSA       0x0200
#define     count1     0x0600
#define     count2     0x0610
#define     temp1      0x0620
#define     first      0x0210
#define     second     0x0211
#define     third      0x0212
#define     fourth     0x0213
#define     fifth      0x0214
#define     sixth      0x0215
#define     seventh    0x0216
#define     dc_sign    0x0310
#define     dc_first   0x0211
#define     dc_second  0x0312
#define     dc_third   0x0313
#define     dc_fourth  0x0315
#define     dc_fifth   0x0316
;_____________________________________________________________________________

            RSEG       CSTACK
            DS         0

;_____________________________________________________________________________

            RSEG       CODE
;_____________________________________________________________________________
;
```

```
;          LCD INITIALISATION ROUTINE (FUNCTION SET)
;              ---------------------------- ----------
;
;____________________________________________________________
lcd_init1    mov.b    #0x38,&P4OUT     ;function set
             bis.b    #E,&P5OUT        ;enable enable
             call     #lcd_stable      ;to stabilize enable
;____________________________________________________________
lcd_init2    mov.b    #0x38,&P4OUT     ;function set
             bis.b    #E,&P5OUT        ;enable enable
             call     #lcd_stable      ;to stabilize enable
;____________________________________________________________
lcd_init3    mov.b    #0x38,&P4OUT     ;function set
             bis.b    #E,&P5OUT        ;enable enable
             call     #lcd_stable      ;to stabilize enable
             jmp      lcd_init4
;____________________________________________________________
;
;                   DELAY ROUTINES
;                   ---------------
;
;____________________________________________________________
lcd_rise     mov      #0x0006,r4
repeat_1     mov.w    #WDT_MDLY_32,&WDTCTL     ; WDT ~32ms interval timer
             bis.b    #WDTIE,&IE1              ; Enable WDT interrupt
             eint                              ; Enable interrupts
             bis.w    #CPUOFF,SR               ; CPU off
             nop
             dec      r4
             jnz      repeat_1
             clr      r4
             mov.w    #WDTPW+WDTHOLD,&WDTCTL   ; Stop WDT
             bic.b    #E,&P5OUT                ;clear enable
             bic.b    #RS,&P5OUT
             ret
;============================================================
lcd_stable   mov      #0x000A,r4
repeat_2     mov.w    #0x5A1A,&WDTCTL          ; WDT ~0.5ms interval timer
             bis. b   #WDTIE,&IE1              ; Enable WDT interrupt
             eint                              ; Enable interrupts
             bis.w    #CPUOFF,SR               ; CPU off
             nop
             dec      r4
             jnz      repeat_2
             clr      r4
             mov.w    #WDTPW+WDTHOLD,&WDTCTL   ; Stop WDT
             bic.b    #E,&P5OUT                ;clear enable
             bic.b    #RS,&P5OUT
```

```
            ret
;==================================================================
lcd_busy    mov     #0x0003,r4
repeat_3    mov.w   #0x5A1A,&WDTCTL          ; WDT ~0.5ms interval timer
            bis.b   #WDTIE,&IE1              ; Enable WDT interrupt
            eint                             ; Enable interrupts
            bis.w   #CPUOFF,SR               ; CPU off
            nop
            dec     r4
            jnz     repeat_3
            clr     r4
            mov.w   #WDTPW+WDTHOLD,&WDTCTL   ; Stop WDT
            bic.b   #E,&P5OUT                ;clear enable
            bic.b   #RS,&P5OUT
            ret
;==================================================================
lcd_1_second
            mov     #0x001f,r4
repeat_4    mov.w   #0x5A18,&WDTCTL          ; WDT ~0.5ms interval timer
            bis.b   #WDTIE,&IE1              ; Enable WDT interrupt
            eint                             ; Enable interrupts
            bis.w   #CPUOFF,SR               ; CPU off
            nop
            dec     r4
            jnz     repeat_4
            clr     r4
            mov.w   #WDTPW+WDTHOLD,&WDTCTL   ; Stop WDT
            bic.b   #E,&P5OUT                ;clear enable
            bic.b   #RS,&P5OUT
            ret
;__________________________________________________________________
;
;                 ROUTINE TO CLEAR DISPLAY
;                 -----------------------
;__________________________________________________________________

clr_disp  call    #lcd_busy         ;"CLEAR DISPLAY ROUTINE"
          mov.b   #0x01,&P4OUT      ;clear display
          bis.b   #E,&P5OUT         ;Enable enable
          call    #lcd_stable       ;check LCD busy flag
          ret
;__________________________________________________________________
;
;      TO GIVE THE ON/OFF CONTROL,CLEAR DISPLAY,ENTRY MODE
;                      FORTHE LCD
;      ----------------------------------------------------------
```

```
;_______________________________________________________________________________
lcd_init4     mov.b     #0x0e,&P4OUT          ;display ON/OFF control word
              bis.b     #E,&P5OUT             ;Enable enable
              call      #lcd_busy             ;delay
;_______________________________________________________________________________
next          mov.b     #0x06,&P4OUT          ;display ON/OFF control word
              bis.b     #E,&P5OUT             ;Enable enable
              call      #lcd_busy             ;check LCD busy flag
              mov.b     #0x01,&P4OUT          ;Entry mode set
              bis.b     #E,&P5OUT             ;Enable enable
              call      #lcd_busy             ;check LCD busy flag
              jmp       next_1                ;jump to display routine
;_______________________________________________________________________________
;===============================================================================
;                    MAIN MODULE PROGRAM.
;                    --------------------
;===============================================================================
;_______________________________________________________________________________
start         mov       #SFE(CSTACK),SP                 ; stack intalization
              mov       #WDTHOLD+WDTPW,&WDTCTL          ; stoping watch dog timer
              mov.b     #0xff,&P4DIR                    ; ports 2,3,4,5 intalization
              mov.b     #0xff,&P5DIR
              mov.b     #0x00,&P3DIR
              mov.b     #0x00,&P2DIR
              clr.b     &P5OUT                          ;clearing output registers
              clr.b     &P4OUT                          ; of ports 4&5
              call      #lcd_rise
              jmp       lcd_init1                       ;jump to LCD intalization routine
;_______________________________________________________________________________
;
;             A ROUTINE TO DISPLAY IN LCD AS
;             :-----------------------------------:
;             | PREMIER POLYTRONICS |
;             |                                   |
;             '-----------------------------------'
;
;_______________________________________________________________________________
next_1        call      #lcd_stable
              mov.b     #0xc0,&P4OUT          ;select II line of 20x4 LCD
              bis.b     #E,&P5OUT             ;Enable enable
              call      #lcd_busy             ;check if LCD busy?
              mov       #0x00000,r14          ;clr PC count value
disp_1        cmp       #0x000a0,r14          ;is char disp over?
              jz        nxt_rout_1            ;'yes',clear display
              call      #lookup_1             ;call 'lookup_1'
              bis.b     #RS,&P5OUT            ;Enable RS
              bis.b     #E,&P5OUT             ;enable enable
```

```
            call     #lcd_busy             ;check LCD busy flag
            add      #0x00008,r14          ;inc PC count value to next char
            jmp      disp_1                ;jump to disp next char
nxt_rout_1  call     #lcd_stable
            jmp      next_2
;___________________________________________________________________________
;
;      THE LOOK UP TABLE FOR DISPLAYING 'PREMIER POLYTRONICS'.
;            ------------------------------------------------
;
;___________________________________________________________________________
lookup_1    add      r14,pc                ;add with PC to goto next char
            mov.b    #0x50,&P4OUT          ;display 'P'
            ret
            mov.b    #0x52,&P4OUT          ;display 'R'
            ret
            mov.b    #0x45,&P4OUT          ;display 'E'
            ret
            mov.b    #0x4d,&P4OUT          ;display 'M'
            ret
            mov.b    #0x49,&P4OUT          ;display 'I'
            ret
            mov.b    #0x45,&P4OUT          ;display 'E'
            ret
            mov.b    #0x52,&P4OUT          ;display 'R'
            ret
            mov.b    #0x20,&P4OUT          ;display ' '
            ret
            mov.b    #0x50,&P4OUT          ;display 'P'
            ret
            mov.b    #0x4f,&P4OUT          ;display 'O'
            ret
            mov.b    #0x3c,&P4OUT          ;display 'L'
            ret
            mov.b    #0x59,&P4OUT          ;display 'Y'
            ret
            mov.b    #0x54,&P4OUT          ;display 'T'
            ret
            mov.b    #0x52,&P4OUT          ;display 'R'
            ret
            mov.b    #0x4f,&P4OUT          ;display 'O'
            ret
            mov.b    #0x4e,&P4OUT          ;display 'N'
            ret
            mov.b    #0x49,&P4OUT          ;display 'I'
            ret
            mov.b    #0x43,&P4OUT          ;display 'C'
```

```
          ret
          mov.b    #0x53,&P4OUT              ;display 'S'
          ret
;___________________________________________________________________________
;
;         A ROUTINE TO DISPLAY IN LCD AS
;         :-------------------------:
;         |                         |
;         |  COIMBATORE
;         '-------------------------'
;___________________________________________________________________________
next_2    call     #lcd_stable
          mov.b    #0x94,&P4OUT              ;select III line of 20x4 LCD
          bis.b    #E,&P5OUT                 ;Enable enable
          call     #lcd_busy                 ;check if LCD busy?
          mov      #0x00000,r14              ;clr PC count value
disp_2    cmp      #0x00080,r14              ;is char disp over?
          jz       nxt_rout_2                ; 'yes',clear display
          call     #lookup_2                 ;call 'lookup_1'
          bis.b    #RS,&P5OUT                ;Enable RS
          bis.b    #E,&P5OUT                 ;enable enable
          call     #lcd_busy                 ;check LCD busy flag
          add      #0x00008,r14              ;inc PC count value to next char
          jmp      disp_2                    ;jump to disp next char
nxt_rout_2 call    #lcd_1_second             ;delay
          jmp      next_3
;___________________________________________________________________________
;
;      THE LOOK UP TABLE FOR DISPLAYING 'COIMBATORE'.
;         -------------------------------------------
;___________________________________________________________________________
lookup_2  add      r14,pc                    ;add with PC to goto next char
          mov.b    #0x20,&P4OUT              ;display ' '
          ret
          mov.b    #0x20,&P4OUT              ;display ' '
          ret
          mov.b    #0x20,&P4OUT              ;display ' '
          ret
          mov.b    #0x20,&P4OUT              ;display ' '
          ret
          mov.b    #0x20,&P4OUT              ;display ' '
          ret
          mov.b    #0x43,&P4OUT              ;display 'C'
          ret
          mov.b    #0x4f,&P4OUT              ;display 'O'
          ret
```

```
        mov.b   #0x49,&P4OUT            ;display 'I'
        ret
        mov.b   #0x4d,&P4OUT            ;display 'M'
        ret
        mov.b   #0x42,&P4OUT            ;display 'B'
        ret
        mov.b   #0x41,&P4OUT            ;display 'A'
        ret
        mov.b   #0x54,&P4OUT            ;display 'T'
        ret
        mov.b   #0x4f,&P4OUT            ;display 'O'
        ret
        mov.b   #0x52,&P4OUT            ;display 'R'
        ret
        mov.b   #0x45,&P4OUT            ;display 'E'
        ret
;______________________________________________________________________
;
;       A ROUTINE TO DISPLAY IN LCD AS
;       :------------------------------:
;       | MEASURING HEAD               |
;       |                              |
;       '------------------------------'
;______________________________________________________________________
next_3  call    #lcd_1_second
        call    #clr_disp
        call    #lcd_stable
        mov.b   #0xc0,&P4OUT            ;select II line of 20x4 LCD
        bis.b   #E,&P5OUT               ;Enable enable
        call    #lcd_busy               ;check if LCD busy?
        mov     #0x00000,r14            ;clr PC count value
disp_3  cmp     #0x00088,r14            ;is char disp over?
        jz      nxt_rout_3              ;'yes',clear display
        call    #lookup_3               ;call 'lookup_1'
        bis.b   #RS,&P5OUT              ;Enable RS
        bis.b   #E,&P5OUT               ;enable enable
        call    #lcd_busy               ;check LCD busy flag
        add     #0x00008,r14            ;inc PC count value to next char
        jmp     disp_3                  ;jump to disp next char

nxt_rout_3
        call    #lcd_stable
        jmp     next_4
;______________________________________________________________________
;
;       THE LOOK UP TABLE FOR DISPLAYING 'MEASURING HEAD'.
```

```
;                 ---------------------------------------------
;_______________________________________________________________________
lookup_3   add     r14,pc              ;add with PC to goto next char
           mov.b   #0x20,&P4OUT           ;display ' '
           ret
           mov.b   #0x20,&P4OUT              ;display ' '
           ret
           mov.b   #0x20,&P4OUT              ;display ' '
           ret
           mov.b   #0x4d,&P4OUT              ;display 'M'
           ret
           mov.b   #0x45,&P4OUT              ;display 'E'
           ret
           mov.b   #0x41,&P4OUT              ;display 'A'
           ret
           mov.b   #0x53,&P4OUT              ;display 'S'
           ret
           mov.b #0x55,&P4OUT                ;display 'U'
           ret
           mov.b #0x52,&P4OUT                ;display 'R'
           ret
           mov.b   #0x49,&P4OUT              ;display 'I'
           ret
           mov.b   #0x4e,&P4OUT              ;display 'N'
           ret
           mov.b   #0x47,&P4OUT              ;display 'G'
           ret
           mov.b   #0x20,&P4OUT              ;display ' '
           ret
           mov.b   #0x48,&P4OUT              ;display 'H'
           ret
           mov.b   #0x45,&P4OUT              ;display 'E'
           ret
           mov.b #0x41,&P4OUT                ;display 'A'
           ret
           mov.b   #0x44,&P4OUT              ;display 'D'
           ret
;_______________________________________________________________________
;
;          A ROUTINE TO DISPLAY IN LCD AS
;          :-------------------:
;          |                   |
;          |   TEST            |
;          '-------------------'
;_______________________________________________________________________
next_4    call      #lcd_stable
```

```
         mov.b     #0x94,&P4OUT         ;select III line of 20x4 LCD
         bis.b     #E,&P5OUT            ;Enable enable
         call      #lcd_busy            ;check if LCD busy?
         mov       #0x00000,r14         ;clr PC count value
disp_4   cmp       #0x00060,r14         ;is char disp over?
         jz        nxt_rout_4           ;'yes',clear display
         call      #lookup_4            ;call 'lookup_1'
         bis.b     #RS,&P5OUT           ;Enable RS
         bis.b     #E,&P5OUT            ;enable enable
         call      #lcd_busy            ;check LCD busy flag
         add       #0x00008,r14         ;inc PC count value to next char
         jmp       disp_4               ;jump to disp next char
nxt_rout_4
         call   #lcd_stable
         jmp    next_5
;______________________________________________________________________
;
;        THE LOOK UP TABLE FOR DISPLAYING 'TEST'.
;             --------------------------------------
;______________________________________________________________________
lookup_4     add     r14,pc              ;add with PC to goto next char
             mov.b   #0x20,&P4OUT        ;display ' '
             ret
             mov.b   #0x20,&P4OUT        ;display ' '
             ret
             mov.b   #0x20,&P4OUT        ;display ' '
             ret
             mov.b   #0x20,&P4OUT        ;display ' '
             ret
             mov.b   #0x20,&P4OUT        ;display ' '
             ret
             mov.b   #0x54,&P4OUT        ;display 'T'
             ret
             mov.b   #0x45,&P4OUT        ;display 'E'
             ret
             mov.b   #0x53,&P4OUT        ;display 'S'
             ret
             mov.b   #0x54,&P4OUT        ;display 'T'
             ret
             mov.b   #0x20,&P4OUT        ;display ' '
             ret
             mov.b   #0x20,&P4OUT        ; display ' '
             ret
             mov.b   #0x20,&P4OUT        ;display ' '
             ret
             mov.b   #0x20,&P4OUT        ;display ' '
```

```
            ret
            mov.b   #0x20,&P4OUT              ;display ' '
            ret


;-----------------------------------------------------------------------------------
;
;       A ROUTINE TO DISPLAY IN LCD AS
;
;
;           :-------------------:
;           |SELECT MODE:_      | TO DISPLAY THE CHARACTERS IN I LINE.
;           '-------------------'
;
;-----------------------------------------------------------------------------------
next_5      call    #lcd_1_second
            call    #clr_disp          ;call clear display routine
            call    #lcd_stable
            mov.b   #0x80,&P4OUT           ;select I line of 20x4 LCD
            bis.b   #E,&P5OUT          ;Enable enable
            call    #lcd_busy          ;check if LCD busy?
            mov     #0x00000,r14       ;clr PC count value
disp_5      cmp     #0x00060,r14       ;is char disp over?
            jz      next_6             ;'yes',goto 'next_line'
            call    #lookup_5          ;call 'lookup_2'
            bis.b   #RS,&P5OUT         ;Enable RS
            bis.b   #E,&P5OUT          ;enable enable
            call    #lcd_busy          ;check LCD busy flag
            add     #0x00008,r14       ;inc PC count value to next char
            jmp     disp_5             ;jump to disp next char
;-----------------------------------------------------------------------------------
;
;       THE LOOK UP TABLE FOR DISPLAYING 'SELECT MODE:'.
;           ------------------------------------------
;-----------------------------------------------------------------------------------
lookup_5    add     r14,pc                   ;add with PC to goto next char
            mov.b #0x53,&P4OUT               ;display 'S'
            ret
            mov.b #0x45,&P4OUT               ;display 'E'
            ret
            mov.b #0x4c,&P4OUT               ;display 'L'
            ret
            mov.b #0x45,&P4OUT               ;display 'E'
            ret
            mov.b #0x43,&P4OUT               ;display 'C'
            ret
            mov.b #0x54,&P4OUT               ;display 'T'
            ret
```

```
                mov.b  #0x20,&P4OUT              ;display ' '
                ret
                mov.b  #0x4d,&P4OUT              ;display 'M'
                ret
                mov.b  #0x4f,&P4OUT              ;display 'O'
                ret
                mov.b  #0x44,&P4OUT              ;display 'D'
                ret
                mov.b  #0x45,&P4OUT              ;display 'E'
                ret
                mov.b  #0x3a,&P4OUT              ;display ':'
                ret
;------------------------------------------------------------
;
;           A ROUTINE TO DISPLAY IN LCD AS
;
;               :------------------- -        :
;               |SELECT MODE          :       |
;               |CALIBERATION MODE_   | TO DISPLAY THE CHARACTERS IN II LINE.
;               '-------------------          '
;___________________________________________________________________________
next_6          call    #lcd_stable
                mov.b   #0xc0,&P4OUT          ;select II line of 20x4 LCD
                bis.b   #E,&P5OUT             ;Enable enable
                call    #lcd_busy             ;check if LCD busy?
                mov     #0x00000,r14          ;clr PC count value
disp_6          cmp     #0x00088,r14          ;is char disp over?
                jz      next_7                ;'yes',goto 'next_line_2'
                call    #lookup_6             ;call 'lookup_3'
                bis.b   #RS,&P5OUT            ;Enable RS
                bis.b   #E,&P5OUT             ;enable enable
                call    #lcd_busy             ;check LCD busy flag
                add     #0x00008,r14          ;inc PC count value to next char
                jmp     disp_6                ;jump to disp next char
;___________________________________________________________________________
;
;       THE LOOK UP TABLE FOR DISPLAYING 'CALIBRATION MODE'.
;               -----------------------------------------------
;___________________________________________________________________________
lookup_6        add     r14,pc                ;add with PC to goto next char
                mov.b #0x43,&P4OUT               ;display 'C'
                ret
                mov.b #0x41,&P4OUT               ;display 'A'
                ret
                mov.b   #0x4c,&P4OUT             ;display 'L'
                ret
```

```
        mov.b  #0x49,&P4OUT              ;display 'I'
        ret
        mov.b  #0x42,&P4OUT              ;display 'B'
        ret
        mov.b  #0x52,&P4OUT              ;display 'R'
        ret
        mov.b  #0x41,&P4OUT              ;display 'A'
        ret
        mov.b  #0x54,&P4OUT              ;display 'T'
        ret
        mov.b  #0x49,&P4OUT              ;display 'I'
        ret
        mov.b  #0x4f,&P4OUT              ;display 'O'
        ret
        mov.b  #0x4e,&P4OUT              ;display 'N'
        ret
        mov.b  #0x20,&P4OUT              ;display ' '
        ret
        mov.b  #0x4d,&P4OUT              ;display 'M'
        ret
        mov.b  #0x4f,&P4OUT              ;display 'O'
        ret
        mov.b  #0x44,&P4OUT              ;display 'D'
        ret
        mov.b  #0x45,&P4OUT              ;display 'E'
        ret
;____________________________________________________________________________
;
;       A ROUTINE TO DISPLAY IN LCD AS
;         ;-------------------      :
;         |SELECT MODE:             |
;         |CALIBERATION MODE        | TO DISPLAY THE CHARACTERS IN III LINE.
;         |TESTING MODE_            |
;         '-------------------      '
;____________________________________________________________________________
next_7  call   #lcd_stable
        mov.b  #0x94,&P4OUT          ;select III line of 20x4 LCD
        bis.b  #E,&P5OUT             ;Enable enable
        call   #lcd_busy             ;check if LCD busy?
        nop
        mov    #0x00000,r14          ;clr PC count value
disp_7  cmp    #0x00060,r14          ;is char disp over?
        jz     time                  ;'yes',clear display
        call   #lookup_4             ;call 'lookup_4'
        bis.b  #RS,&P5OUT            ;Enable RS
        bis.b  #E,&P5OUT             ;enable enable
```

```
            call    #lcd_busy           ;check LCD busy flag
            add     #0x00008,r14        ;inc PC count value to next char
            jmp     disp_7              ;jump to disp next char
;____________________________________________________________________________
;
;           THE LOOK UP TABLE FOR DISPLAYING 'TESTING MODE'
;           --------------------------------------------
;____________________________________________________________________________
lookup_7    add     r14,pc              ;add with PC to goto next char
            mov.b   #0x54,&P4OUT            ;display 'T'
            ret
            mov.b   #0x45,&P4OUT            ;display 'E'
            ret
            mov.b   #0x53,&P4OUT            ;display 'S'
            ret
            mov.b   #0x54,&P4OUT            ;display 'T'
            ret
            mov.b   #0x49,&P4OUT            ;display 'I'
            ret
            mov.b   #0x4e,&P4OUT            ;display 'N'
            ret
            mov.b   #0x47,&P4OUT            ;display 'G'
            ret
            mov.b   #0x20,&P4OUT            ;display ' '
            ret
            mov.b   #0x4d,&P4OUT            ;display 'M'
            ret
            mov.b   #0x4f,&P4OUT            ;display 'O'
            ret
            mov.b   #0x44,&P4OUT            ;display 'D'
            ret
            mov.b   #0x45,&P4OUT            ;display 'E'
            ret
;____________________________________________________________________________
;
;               ARROW HEAD DISPLAY(I)
;                   -----------------
;____________________________________________________________________________
ARROW       bit.b   #BIT0,P2IN
            jc      ARROW_II
            mov.b   #0xA6,&P4OUT        ;line II arrow
            bis.b   #E,&P5OUT           ;Enable enable
            call    #lcd_busy           ;check if LCD busy?
            mov.b   #0x020,&P4OUT
            bis.b   #RS,&P5OUT          ;Enable RS
            bis.b   #E,&P5OUT           ;enable enable
```

```
                call        #lcd_busy
;-------------------------------------------------------------------
                mov.b       #0xD2,&P4OUT        ;select III line of 20x4 LCD
                bis.b       #E,&P5OUT           ;Enable enable
                call        #lcd_busy           ;check if LCD busy?
                mov.b       #0x07f,&P4OUT
                bis.b       #RS,&P5OUT          ;Enable RS
                bis.b       #E,&P5OUT           ;enable
                call        #lcd_busy           ;check LCD busy flag
                jmp         GOBACK
;-------------------------------------------------------------------
ARROW_II        mov.b       #0xD2,&P4OUT        ;select III line of 20x4 LCD
                bis.b       #E,&P5OUT           ;Enable enable
                call        #lcd_busy           ;check if LCD busy?
                mov.b       #0x020,&P4OUT
                bis.b       #RS,&P5OUT          ;Enable RS
                bis.b       #E,&P5OUT           ;enable enable
                call        #lcd_busy           ;check LCD busy flag
;-------------------------------------------------------------------
                mov.b       #0xA6,&P4OUT        ;select III line of 20x4 LCD
                bis.b       #E,&P5OUT           ;Enable enable
                call        #lcd_busy           ;check if LCD busy?
                mov.b       #0x07F,&P4OUT
                bis.b       #RS,&P5OUT          ;Enable RS
                bis.b       #E,&P5OUT           ;enable enable
                call        #lcd_busy           ;check LCD busy flag
GOBACK          ret
;___________________________________________________________________
;
;               TIMER COUNT
;               -----------
;___________________________________________________________________
time            mov     #0x0006,r12
REPEAT          mov     #0x001f,r11
TIMER
                bis.b   #WDTIE,&IE1             ; Enable WDT interrupt
                eint                            ; Enable interrupts
SetupWDT        mov.w   #0x5A18,&WDTCTL         ; WDT ~32ms interval timer
                bis.w   #CPUOFF,SR              ; CPU off
                nop
                dec     r11
                jnz     TIMER
                clr     r13
                mov     r12,r13
                dec     r13
                add     #0x030,r13
```

```
            call    #lcd_stable
            mov.b   #0xE5,&P4OUT            ;select III line of 20x4 LCD
            bis.b   #E,&P5OUT               ;Enable enable
            call    #lcd_busy               ;check if LCD busy?
            mov.b   r13,&P4OUT
            bis.b   #RS,&P5OUT              ;Enable RS
            bis.b   #E,&P5OUT               ;enable enable
            call    #lcd_busy               ;check LCD busy flag
            call    #ARROW
            dec     r12
            jnz     REPEAT
StopWDT1    mov.w   #WDTPW+WDTHOLD,&WDTCTL  ; Stop WDT
            clr     r11
            clr     r12
            clr     r13

;-------------------------------------------------------------------------------
;
;           DC VOLTAGE CALCULATION
;           ----------------------
;-------------------------------------------------------------------------------
DC_ADC      call    #lcd_stable
            clr     &count1
            clr     &count2
            clr     &temp1
            clrc
SetupADC12_dc
            mov     #ADC12ON+#SHT0_15,&ADC12CTL0    ; ADC12ON
            bis.b   #01h,&P6SEL                     ; P6.0 ADC option select
Mainloop1_dc
            bis     #ENC+ADC12SC,&ADC12CTL0         ; Sampling open
            bic     #ADC12SC,&ADC12CTL0             ; Sampling closed, start
                                                    ; conversion
L1_dc       bit     #ADC12BUSY,&ADC12CTL1           ; ADC12BUSY?
            jnz     L1_dc
testIFG_dc  bit     #BIT0,&ADC12IFG                 ; Conversion done?
            jz      testIFG_dc                      ; No, test again
            addc    &ADC12MEM0,&temp1               ; Move result
            inc     &count1
            bic     #ENC,&ADC12CTL0
            bic     #BIT0,&ADC12IFG
            cmp     #0000ah,&count1
            jnz     Mainloop1_dc
            mov     &temp1,R4
            clrc
;-------------------------------------------------------------------------------
```

```
            clr    r5
loop_dc     sub    &count1,r4
            jnc    out_dc
            inc    r5
            jmp    loop_dc
out_dc      nop
            mov    r5,r4
mainloop_dc
            nop
            clr    r10
            clr    r8
            clr.b  &dc_first
            clr.b  &dc_second
            clr.b  &dc_third
            clr.b  &dc_fourth
            clr.b  &dc_fifth
            clr    &ANSA
            clr    &ANSD1
            clr    &ANSD2
            clr    &ANSD3
            cmp    #007ffh,r4
            jeq    ansequ
            cmp    #007ffh,r4
            jn     anssub
            mov.b  #02dh,&dc_sign
            sub    #007ffh,r4
loop1_dc    clrc
            dadd   #08125h,&ANSD3
            dadc   &ANSD2
            dadd   #01132h,&ANSD2
            dadc   &ANSD1
            dadd   #00016h,&ANSD1
            dadc   &ANSA
            dec    r4
            jnz    loop1_dc
            jmp    adju_dc

ansequ      mov.b  #020h,&dc_sign
            clr    &ANSA
            clr    &ANSD1
            clr    &ANSD2
            clr    &ANSD3
            jmp    adju_dc
anssub      mov.b  #02bh,&dc_sign
            mov    #007ffh,r8
            sub    r4,r8
```

```
loop2_dc clrc
        dadd   #08125h,&ANSD3
        dadc   &ANSD2
        dadd   #01132h,&ANSD2
        dadc   &ANSD1
        dadd   #00016h,&ANSD1
        dadc   &ANSA
        dec    r8
        jnz    loop2_dc
;________________________________________________________________________________
;
;             BCD TO ASCII CONVERSION
;             ----------------------
;________________________________________________________________________________
adju_dc     clr    r5
            clr    r4
;______________________________________________
            mov    &ANSA,r5
            and.b  #000fh,r5
            add.b  #0030h,r5
            mov.b  r5,&dc_first          ; first  data  after sign
            clr    r5
            clr    r4

;______________________________________________
            mov    &ANSD1,r5
            and    #0f000h,r5
            mov    #0000ch,r4
first1_dc   rra    r5
            dec    r4
            jnz    first1_dc
            and.b  #000fh,r5
            add.b  #0030h,r5
            mov.b  r5,&dc_second         ; second  data  after sign
            clr    r5
            clr    r4
;______________________________________________
            mov    &ANSD1,r5
            and    #00f00h,r5
            mov    #00008h,r4
second1_dc
            rra    r5
            dec    r4
            jnz    second1_dc
            and.b  #000fh,r5
            add.b  #0030h,r5
```

```
        mov.b  r5,&dc_third        ; third  data after sign
        clr    r5
        clr    r4
;____________________________________________________
        mov    &ANSD1,r5
        and    #000f0h,r5
        mov    #0004h,r4
third1_dc
        rra    r5
        dec    r4
        jnz    third1_dc
        and.b  #000fh,r5
        add.b  #0030h,r5
        mov.b  r5,&dc_fourth       ; fourth  data  after  decimal
        clr    r5
        clr    r4
;____________________________________________________
        mov    &ANSD1,r5
        and.b  #000fh,r5
        add.b  #0030h,r5
        mov.b  r5,&dc_fifth
        clr      r5
        clr      r4

;__________________________________________________________________________
;
;           CHECK FOR MODE
;           --------------
;__________________________________________________________________________
        bit.b   #BIT0,&P2IN        ;check input of the port2 {1AND(p2in)}
        jz      next_8             ;jump to calibration mode
        jmp     next12             ;jump to testing mode
;__________________________________________________________________________
;
;          ROUTINE TO DISPLAY (C)
;          ----------------------
;__________________________________________________________________________
next_8  call      #clr_disp            ;clear display
        mov.b    #0x90,&P4OUT          ;select I line of LCD display for d.splay of (C)
        bis.b    #E,&P5OUT
        call     #lcd_busy
        mov      #0x00000,r14            ;clr PC count value
disp_8  cmp      #0x00018,r14            ;is char disp over?
        jz       next_9
        call     #lookup_8             ;call 'lookup_8'
        bis.b    #RS,&P5OUT              ;Enable RS
```

```
         bis.b   #E,&P5OUT              ;enable enable
         call    #lcd_busy              ;check LCD busy flag
         add     #0x00008,r14           ;inc PC count value to next char
         jmp     disp_8                 ;jump to disp next char
;------------------------------------------------------------------------
;
;        THE LOOK UP TABLE FOR DISPLAYING '(c)'.
;        ------------------------------------
;
;------------------------------------------------------------------------
lookup_8     add     r14,pc             ;add with PC to goto next char
             mov.b   #0x28,&P4OUT           ;display '('
             ret
             mov.b   #0x43,&P4OUT           ;display 'C'
             ret
             mov.b   #0x29,&P4OUT           ;display ')'
             ret
;------------------------------------------------------------------------
;
;        DISPLAY dc value
;        --------------
;
;------------------------------------------------------------------------
next_9       call    #lcd_stable
             mov.b   #0xC0,&P4OUT       ;select II line of the 20x4 LCD display
             bis.b   #E,&P5OUT
             call    #lcd_busy
             clr     r14
disp_9       cmp     #0x00098,r14       ;is char disp over?
             jz      next_10            ;'yes',goto 'next_line'
             call    #lookup_9          ;call 'lookup_9'
             bis.b   #RS,&P5OUT         ;Enable RS
             bis.b   #E,&P5OUT          ;enable enable
             call    #lcd_busy          ;check LCD busy flag
             add     #0x00008,r14       ;inc PC count value to next char
             jmp     disp_9             ;jump to disp next char
;------------------------------------------------------------------------
;
;        THE LOOK UP TABLE FOR DISPLAYING 'DC VALUE:'
;        --------------------------------------------
;
;------------------------------------------------------------------------
lookup_9     add     r14,pc                 ;add with PC to goto next char
             mov.b   #0x44,&P4OUT           ;display 'D'
             ret
             mov.b   #0x43,&P4OUT           ;display 'C'
             ret
             mov.b   #0x20,&P4OUT           ;display ' '
             ret
```

```
        mov.b  #0x56,&P4OUT              ;display 'V'
        ret
        mov.b  #0x41,&P4OUT              ;display 'A'
        ret
        mov.b  #0x4c,&P4OUT              ;display 'L'
        ret
        mov.b  #0x55,&P4OUT              ;display 'U'
        ret
        mov.b  #0x45,&P4OUT              ;display 'E'
        ret
        mov.b  #0x3a,&P4OUT              ;display ' : '
        ret
        mov.b  &dc_sign,&P4OUT           ;sign
        ret
        mov.b  &dc_first,&P4OUT          ; first digit
        ret
        mov.b  &dc_second,&P4OUT         ; second digit
        ret
        mov.b  &dc_third,&P4OUT          ;third  digit
        ret
        mov.b  &dc_fourth,&P4OUT         ;fourth digit
        ret
        mov.b  #0x2e,&P4OUT              ;display '.'
        ret
        mov.b  &dc_fifth,&P4OUT          ;fifth  digit
        ret
        mov.b  #0x20,&P4OUT              ; display ' '
        ret
        mov.b  #0x6d,&P4OUT              ;display 'm'
        ret
        mov.b  #0x76,&P4OUT              ;display 'v'
        ret

;______________________________________________________________________
;
;          DISPLAY " TUNE UNTIL ZERO"
;          ------------------------
;______________________________________________________________________

next_10   call    #lcd_stable
          mov.b   #0x094,&P4OUT         ;select III line of 20x4 LCD
          bis.b   #E,&P5OUT             ;Enable enable
          call    #lcd_busy             ;check if LCD busy?
          clr     r14                   ;clr PC count value
disp_10   cmp     #0x00080,r14          ;is char disp over?
          jz      calib_adc             ;'yes',goto'next_line_3'
```

```
          call    #lookup_10         ;call 'lookup_5'
          bis.b   #RS,&P5OUT         ;Enable RS
          bis.b   #E,&P5OUT          ;enable enable
          call    #lcd_busy          ;check LCD busy flag
          add     #0x00008,r14       ;inc PC count value to next char
          jmp     disp_10            ;jump to disp next char
;--------------------------------------------------------------------------
;
;         THE LOOK UP TABLE FOR DISPLAYING 'TUNE UNTIL ZERO'
;         -----------------------------------------------
;
;--------------------------------------------------------------------------

lookup_10 add     r14,pc             ;add with PC to goto next char
          mov.b   #0x54,&P4OUT       ;display 'T'
          ret
          mov.b   #0x55,&P4OUT       ;display 'U'
          ret
          mov.b   #0x4E,&P4OUT       ;display 'N'
          ret
          mov.b   #0x45,&P4OUT       ;display 'E'
          ret
          mov.b   #0x20,&P4OUT       ;display ' '
          ret
          mov.b   #0x55,&P4OUT       ;display 'U'
          ret
          mov.b   #0x4e,&P4OUT       ; display 'N'
          ret
          mov.b   #0x54,&P4OUT       ;display 'T'
          ret
          mov.b   #0x49,&P4OUT       ;display 'I'
          ret
          mov.b   #0x4c,&P4OUT       ;display 'L'
          ret
          mov.b   #0x20,&P4OUT       ;display ' '
          ret
          mov.b   #0x5A,&P4OUT       ; display 'Z'
          ret
          mov.b   #0x45,&P4OUT       ;display 'E'
          ret
          mov.b   #0x52,&P4OUT       ;display 'R'
          ret
          mov.b   #0x4f,&P4OUT       ;display 'O'
          ret
          mov.b   #0x3A,&P4OUT       ;display ':'
          ret
```

```
;________________________________________________________________________
;
;              ADC ROUTINE FOR CALIBRATION MODE
;              --------------------------------
;________________________________________________________________________
calib_adc     call  #lcd_stable
        clr   &count1
        clr   &count2
        clr   &temp1
        clrc
SetupADC12_c
        mov   #ADC12ON+SHT0_15,&ADC12CTL0    ; ADC12ON
        bis.b #01h,&P6SEL          ; P6.0 ADC option select
Mainloop1_c
        bis   #ENC+ADC12SC,&ADC12CTL0 ; Sampling open
        bic   #ADC12SC,&ADC12CTL0    ; Sampling closed, start conversion
L1_c    bit   #ADC12BUSY,&ADC12CTL1  ; ADC12BUSY?
        jnz   L1_c
testIFG_c
        bit   #BIT0,&ADC12IFG        ; Conversion done?
        jz    testIFG_c              ; No, test again
        addc  &ADC12MEM0,&temp1      ; Move result
        inc   &count1
        bic   #ENC,&ADC12CTL0
        bic   #BIT0,&ADC12IFG
        cmp   #0000ah,&count1
        jnz   Mainloop1_c
        mov   &temp1,R4
        clrc
;------------------------------------------------------------------------
        clr   r5
loop_c  sub   &count1,r4
        jnc   out_c
        inc   r5
        jmp   loop_c
out_c   nop
        mov   r5,r4
mainloop_c
        nop
        clr   r10
        clr   &ANSA
        clr   &ANSD1
        clr   &ANSD2
        clr   &ANSD3
loop2_c clrc
        dadd  #00625h,&ANSD3
```

```
        dadc   &ANSD2
        dadd   #05664h,&ANSD2
        dadc   &ANSD1
        dadd   #00080h,&ANSD1
        dadc   &ANSA
        dec    r4
        jnz    loop2_c
        jmp    adju_c
;______________________________________________________________
temp_1      jmp    next_8
;______________________________________________________________
;
;           BCD TO ASCII CONVERSION
;           -----------------------
;______________________________________________________________
adju_c  clr    second
        clr    third
        clr    fourth
        clr    fifth
        clr    sixth
        clr    r5
        clr    r4
        mov    &ANSA,r5
        and    #000f0h,r5
        mov    #00004h,r4
first0_c rra   r5
        dec    r4
        jnz    first0_c
        and.b  #0000fh,r5
        add.b  #030h,r5
        mov.b  r5,&second        ;data after sign
        clr    r5
        clr    r4
;______________________________________
        mov    &ANSA,r5
        and    #0000fh,r5
        and.b  #000fh,r5
        add.b  #0030h,r5
        mov.b  r5,&third         ; data after decimal
        clr    r5
        clr    r4

;______________________________________
        mov    &ANSD1,r5
        and    #0f000h,r5
        mov    #000ch,r4
```

```
firstl_c  rra     r5
          dec     r4
          jnz     firstl_c
          and.b   #000fh,r5
          add.    #0030h,r5
          mov.b   r5,&fourth        ; second data after decimal
          clr     r5
          clr     r4
;______________________________________________________
          mov     &ANSD1,r5
          and     #00f00h,r5
          mov     #00008h,r4
second1_c
          rra     r5
          dec     r4
          jnz     second1_c
          and.b   #000fh,r5
          add.b   #0030h,r5
          mov.b   r5,&fifth         ; third data after decimal
          clr     r5
          clr     r4
;______________________________________________________
          mov     &ANSD1,r5
          and     #000f0h,r5
          mov     #0004h,r4
third1_c
          rra     r5
          dec     r4
          jnz     third1_c
          and.b   #000fh,r5
          add.b   #0030h,r5
          mov.b   r5,&sixth         ; fourth data after decimal
          clr     r5
          clr     r4
;______________________________________________________
          mov     &ANSD1,r5
          and     #0000fh,r5
          and.b   #000fh,r5
          add.b   #0030h,r5
          mov.b   r5,&seventh
          clr     r5
          clr     r4
;______________________________________________________________________
;
;         DISPLAY 'OUTPUT'
;         ----------------
;
```

```
;________________________________________________________________________________
next_11      call    #lcd_stable
             mov.b   #0xd4,&P4OUT        ;select IV line of 20x4 LCD
             bis.b   #E,&P5OUT           ;Enable enable
             call    #lcd_busy           ;check if LCD busy?
             mov     #0x00000,r14        ;clr PC count value
disp_11      cmp     #0x00038,r14        ;is char disp over?
             jz      chk_mod_1           ;'yes',goto 'next_line_2'
             call    #lookup_11          ;call 'lookup_11'
             bis.b   #RS,&P5OUT          ;Enable RS
             bis.b   #E,&P5OUT           ;enable enable
             call    #lcd_busy           ;check LCD busy flag
             add     #0x00008,r14        ;inc PC count value to next char
             jmp     disp_11
;--------------------------------------------------------------------------------
lookup_11    add     r14,pc
             mov.b   &first,&P4OUT              ;display sign
             ret
             mov.b   &second,&P4OUT             ;display first digit
             ret
             mov.b   #0x2e,&P4OUT               ;display '.'
             ret
             mov.b   &third,&P4OUT              ;display second digit
             ret
             mov.b   &fourth,&P4OUT             ;display third digit
             ret
             mov.b   &fifth,&P4OUT              ;display fourth digit
             ret
             mov.b   &sixth,&P4OUT              ;display fifth digit
             ret
;________________________________________________________________________________
;
;            CHECK FOR MODE
;            --------------
;________________________________________________________________________________
chk_mod_1    bit.b   #BIT0,&P2IN         ;check input of the port2 {1AND(p2in)}
             jz      calib_adc           ;jump to calibration mode
             jmp     next12              ;jump to testing mode
;________________________________________________________________________________
;
;            DISPLAY (T)
;            -----------
;________________________________________________________________________________
next12       call    #clr_disp           ;clear display
             mov.b   #0x90,&P4OUT        ;select I line of LCD display
                                         ;for display of (T)
```

```
                bis.b   #E,&P5OUT
                call    #lcd_busy
                mov     #0x00000,r14            ;clr PC count value
disp_12         cmp     #0x00018,r14            ;is char disp over?
                jz      next_13
                call    #lookup_12              ;call 'lookup_8'
                bis.b   #RS,&P5OUT              ;Enable RS
                bis.b   #E,&P5OUT               ;enable enable
                call    #lcd_busy               ;check LCD busy flag
                add     #0x00008,r14            ;inc PC count value to next char
                jmp     disp_12                 ;jump to disp next char
;------------------------------------------------------------------------------
;
;               THE LOOK UP TABLE FOR DISPLAYING '(T)' .
;               ------------------------------------
;
;------------------------------------------------------------------------------
lookup_12       add     r14,pc                  ;add with PC to goto next char
                mov.b   #0x28,&P4OUT                    ;display '('
                ret
                mov.b   #0x54,&P4OUT                    ;display 'T'
                ret
                mov.b   #0x29,&P4OUT                    ;display ')'
                ret
;------------------------------------------------------------------------------
;
;          DISPLAY OUTPUT
;          -------------
;
;------------------------------------------------------------------------------
next_13    mov.b        #0xC0,&P4OUT            ;select I line of the 20x4 LCD display
           bis.b        #E,&P5OUT
           call         #lcd_busy
           mov          #0x00000,r14            ;clr PC count value
disp_13    cmp          #0x00098,r14            ;is char disp over?
           jz           next_14                 ;'yes',goto 'next_line'
           call         #lookup_13              ;call 'lookup_9'
           bis.b        #RS,&P5OUT              ;Enable RS
           bis.b        #E,&P5OUT               ;enable enable
           call         #lcd_busy               ;check LCD busy flag
           add          #0x00008,r14            ;inc PC count value to next char
           jmp          disp_13                 ;jump to disp next char
;------------------------------------------------------------------------------
;temp_1         jmp     next_8
;------------------------------------------------------------------------------
;
;               THE LOOK UP TABLE FOR DISPLAYING 'DC VALUE:
;               ---------------------------------------------
```

```
;________________________________________________________________________________
lookup_13   add     r14,pc                      ;add with PC to goto next char
            mov.b   #0x44,&P4OUT                ;display 'D'
            ret
            mov.b   #0x43,&P4OUT                ;display 'C'
            ret
            mov.b   #0x20,&P4OUT                ;display ' '
            ret
            mov.b   #0x56,&P4OUT                ;display 'V'
            ret
            mov.b   #0x41,&P4OUT                ;display 'A'
            ret
            mov.b   #0x4c,&P4OUT                ;display 'L'
            ret
            mov.b   #0x45,&P4OUT                ;display 'U'
            ret
            mov.b   #0x3a,&P4OUT                ;display ':'
            ret
            mov.b   #0x20,&P4OUT                ;display ' '
            ret
            mov.b   &dc_sign,&P4OUT             ;sign
            ret
            mov.b   &dc_first,&P4OUT    ;first digit
            ret
            mov.b   &dc_second,&P4OUT       ;second digit
            ret
            mov.b   &dc_third,&P4OUT      ;third  digit
            ret
            mov.b   &dc_fourth,&P4OUT      ;fourth digit
            ret
            mov.b   #0x2e,&P4OUT         ;display '.'
            ret
            mov.b   &dc_fifth,&P4OUT      ;fifth  digit
            ret
            mov.b   #0x20,&P4OUT         ;display ' '
            ret
            mov.b   #0x6d,&P4OUT         ;display 'm'
            ret
            mov.b   #0x76,&P4OUT         ;display 'v'
            ret

;________________________________________________________________________________
;
;           DISPLAY OUTPUT
;           --------------
;________________________________________________________________________________
```

```
next_14         call    #lcd_stable
                mov.b   #0x94,&P4OUT              ;select III line of 20x4 LCD
                bis.b   #E,&P5OUT              ;Enable enable
                call    #lcd_busy              ;check if LCD busy?
                mov     #0x00000,r14           ;clr PC count value
disp_14         cmp     #0x00038,r14           ;is char disp over?
                jz      cal_adcpresent         ;'yes',goto 'next_line'
                call    #lookup_14             ;call 'lookup_6'
                bis.b   #RS,&P5OUT             ;Enable RS
                bis.b   #E,&P5OUT              ;enable enable
                call    #lcd_busy              ;check LCD busy flag
                add     #0x00008,r14           ;inc PC count value to next char
                jmp     disp_14                   ;jump to disp next char
;------------------------------------------------------------------------------
;
;               THE LOOK UP TABLE FOR DISPLAYING OUTPUT:
;               ---------------------------------------
;
;------------------------------------------------------------------------------
lookup_14       add     r14,pc                    ;add with PC to goto next char
                mov.b   #0x4f,&P4OUT              ;display 'O'
                ret
                mov.b   #0x55,&P4OUT              ;display 'U'
                ret
                mov.b   #0x54,&P4OUT              ;display 'T'
                ret
                mov.b   #0x50,&P4OUT              ;display 'P'
                ret
                mov.b   #0x55,&P4OUT              ;display 'U'
                ret
                mov.b   #0x54,&P4OUT              ;display 'T'
                ret
                mov.b   #0x3a,&P4OUT              ;display ':'
                ret
;------------------------------------------------------------------------------
;
;           ADC CONVERSION(To calculate present value)
;           --------------
;
;------------------------------------------------------------------------------
cal_adcpresent call  #lcd_stable
          clr    &count1
          clr    &count2
          clr    &temp1
          clrc
SetupADC12_t
         mov    #ADC12ON+SHT0_15,&ADC12CTL0    ; ADC12ON
          bis.b  #01h,&P6SEL          ; P6.0 ADC option select
```

```
Mainloop1_t
        bis   #ENC+ADC12SC,&ADC12CTL0 ; Sampling open
        bic   #ADC12SC,&ADC12CTL0    ; Sampling closed, start conversion
L1_t    bit   #ADC12BUSY,&ADC12CTL1  ; ADC12BUSY?
        jnz   L1_t
testIFG_t
        bit   #BIT0,&ADC12IFG        ; Conversion done?
        jz    testIFG_t              ; No, test again
        addc  &ADC12MEM0,&temp1      ; Move result
        inc   &count1
        bic   #ENC,&ADC12CTL0
        bic   #BIT0,&ADC12IFG
        cmp   #0000ah,&count1
        jnz   Mainloop1_t
        mov   &temp1,R4
        clrc
;-------------------------------------------------------------------------------
        clr   r5
loop_t  sub   &count1,r4
        jnc   out_t
        inc   r5
        jmp   loop_t
out_t   nop
        mov   r5,r4
mainloop_t
        nop
        clr   r10
        clr   &ANSA
        clr   &ANSD1
        clr   &ANSD2
        clr   &ANSD3
loop2_t
        clrc
        dadd  #00625h,&ANSD3
        dadc  &ANSD2
        dadd  #05664h,&ANSD2
        dadc  &ANSD1
        dadd  #00080h,&ANSD1
        dadc  &ANSA
        dec   r4
        jnz   loop2_t
        jmp   adju_t
;_______________________________________________________________________________
temp_2      jmp    temp_1
;_______________________________________________________________________________
;
```

```
;               BCD TO ASCII CONVERSION
;               ---------------------
;_______________________________________________________________
adju_t      clr   second
            clr   third
            clr   fourth
            clr   fifth
            clr   sixth
            clr   r5
            clr   r4
            mov   &ANSA,r5
            and   #000f0h,r5
            mov   #00004h,r4
first0      rra   r5
            dec   r4
            jnz   first0
            and.b #0000fh,r5
            add.b #030h,r5
            mov.b r5,&second        ;data after sign
            clr   r5
            clr   r4
;_______________________________________________
            mov   &ANSA,r5
            and   #0000fh,r5
            and.b #000fh,r5
            add.b #0030h,r5
            mov.b r5,&third         ; data after decimal
            clr   r5
            clr   r4

;_______________________________________________
            mov   &ANSD1,r5
            and   #0f000h,r5
            mov   #000ch,r4
first1      rra   r5
            dec   r4
            jnz   first1
            and.b #000fh,r5
            add.b #0030h,r5
            mov.b r5,&fourth        ; second data after decimal
            clr   r5
            clr   r4
;_______________________________________________
            mov   &ANSD1,r5
            and   #00f00h,r5
            mov   #00008h,r4
```

```
second1  rra    r5
         dec    r4
         jnz    second1
         and.b  #000fh,r5
         add.b  #0030h,r5
         mov.b  r5,&fifth       ; third  data after decimal
         clr    r5
         clr    r4
;____________________________________________________
         mov    &ANSD1,r5
         and    #000f0h,r5
         mov    #0004h,r4
third1   rra    r5
         dec    r4
         jnz    third1
         and.b  #000fh,r5
         add.b  #0030h,r5
         mov.b  r5,&sixth       ; fourth  data after  decimal
         clr    r5
         clr    r4
;____________________________________________________
         mov    &ANSD1,r5
         and    #0000fh,r5
         and.b  #000fh,r5
         add.b  #0030h,r5
         mov.b  r5,&seventh
         clr    r5
         clr    r4
;____________________________________________________________________________
;
;        DISPLAY 'OUTPUT'
;        ----------------
;____________________________________________________________________________
next_15       mov.b #0xd4,&P4OUT              ;select IV line of 20x4 LCD
              bis.b  #E,&P5OUT          ;Enable enable
              call   #lcd_busy          ;check if LCD busy?
              mov    #0x00000,r14       ;clr PC count value
disp_15       cmp    #0x00048,r14       ;is char disp over?
              jz     chk_mod_2          ;'yes',goto 'next_line_2'
              call   #lookup_15         ;call 'lookup_11'
              bis.b  #RS,&P5OUT         ;Enable RS
              bis.b  #E,&P5OUT          ;enable enable
              call   #lcd_busy          ;check LCD busy flag
              add    #0x00008,r14       ;inc PC count value to next char
              jmp    disp_15
;---------------------------------------------------------------------------
```

```
lookup_15   add     r14,pc
            mov.b   &first,&P4OUT          ;display sign
            ret
            mov.b   &second,&P4OUT         ;display first digit
            ret
            mov.b   &third,&P4OUT          ;display second digit
            ret
            mov.b   &fourth,&P4OUT         ;display third digit
            ret
            mov.b   #0x2e,&P4OUT           ;display '.'
            ret
            mov.b   &fifth,&P4OUT          ;display fourth digit
            ret
            mov.b   &sixth,&P4OUT          ;display fifth digit
            ret
            mov.b   #0x6d,&P4OUT           ;display 'm'
            ret
            mov.b   #0x76,&P4OUT           ;display 'v'
            ret

;____________________________________________________________
;____________________________________________________________
;
;           CHECK FOR MODE
;           --------------
;____________________________________________________________

chk_mod_2   bit.b   #BIT0,&P2IN         ;check input of the port2 {1AND(p2in)}
            jz      temp_2              ;jump to calibration mode
            jmp     cal_adcpresent      ;jump to testing mode
;____________________________________________________________
;------------------------------------------------------------
WDT_ISR;
;------------------------------------------------------------
        bic     #10h,0(sp)          ;
        reti                        ;
;~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
        COMMON INTVEC
         ORG   WDT_VECTOR
        DW WDT_ISR
        ORG    RESET_VECTOR
         DW start

;~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
            END
;~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
```

PROJECT IMPLEMENTATION:

1) ***Component selection*** criteria were as follows:

➢ Aimed at being a hand held compact device , one important criterion for component selection is ***size***. The size should be ideal to fit a hand held device.

➢ Since the power to the testing device is actually tapped from the line to the measuring head . The power consumption of all the peripherals and devices should be made as minimum as possible.

2) The choice of the components are justified as follows :

➢ The micro controller , MSP430F149A is chosen for its ***ultra low power consumption***, its ability to operate over a wide range of voltages, and its internal flash memory.It has also inbuilt ADC converter which in turn reduces the size of the system.

➢ The SN74LVC4245A , is a ***voltage converter***, which converts +3.3v to +5v. This is used to interface the port output voltages of the controller to the display module . The power consumed by this module is very low.

➢ The ORIOLE LCD module is a display component that consumes ***minimum power*** while operating . It has a permanent back lit LED whose power can be reduced.

3) After the proper choice of the components , each of the modules is ***tested*** separately for desired behaviors and their characteristics are noted . Any changes to be made to alter the module behaviors on the basis of the derived information.

4) When each of the modules was successfully tested , the modules were interconnected and tested for the desired behavior.

CONCLUSION:

Hand held transducer calibrater eliminates the need to detach the measuring head from factory site and carry to lab for checking the error. Without sinking current from the electronic unit now it is possible to rectify the error. It can be also programmed in a such a manner , it can be used with different types of measuring heads like MH15 or MH20. If the standard thread value is already known it is possible now to program the microcontroller to display the error & percentage deviation .

BIBILOGRAPHY

1. www.ti.com
2. 'Linear Integrated circuits ' by Roy chowdury
3. IAR Embedded Workbench
4. MSP430F149A manual
5. CADSTAR pcb design software

- **Low Supply-Voltage Range, 1.8 V . . . 3.6 V**
- **Ultralow-Power Consumption:**
  - **Standby mode: 1.3 µA**
  - **RAM Retention Off Mode: 0.1 µA**
- **Low Operating Current:**
  - **7 µA at 32 kHz, 2.2 V**
  - **250 µA at 1 MHz, 2.2 V**
- **Five Power-Saving Modes**
- **Wake-Up From Standby Mode in 6 µs**
- **16-Bit RISC Architecture, 125-ns Instruction Cycle Time**
- **12-Bit A/D Converter With Internal Reference, Sample-And-Hold and Autoscan Feature**
- **16-Bit Timer With Seven Capture/Compare-With-Shadow Registers, Timer_B**
- **16-Bit Timer With Three Capture/Compare Registers, Timer_A**
- On-Chip Comparator
- Serial Onboard Programming, No External Programming Voltage Needed Programmable Code Protection by Security Fuse
- Family Members Include:
  - MSP430F133†: 8KB Flash Memory, 256B RAM
  - MSP430F135†: 16KB Flash Memory, 512B RAM
  - MSP430F147†: 32KB Flash Memory, 1KB RAM
  - MSP430F148†: 48KB Flash Memory, 2KB RAM
  - MSP430F149†: 60KB Flash Memory, 2KB RAM
- Available in 64-Pin Quad Flat Pack (QFP)

†Advanced Information

description

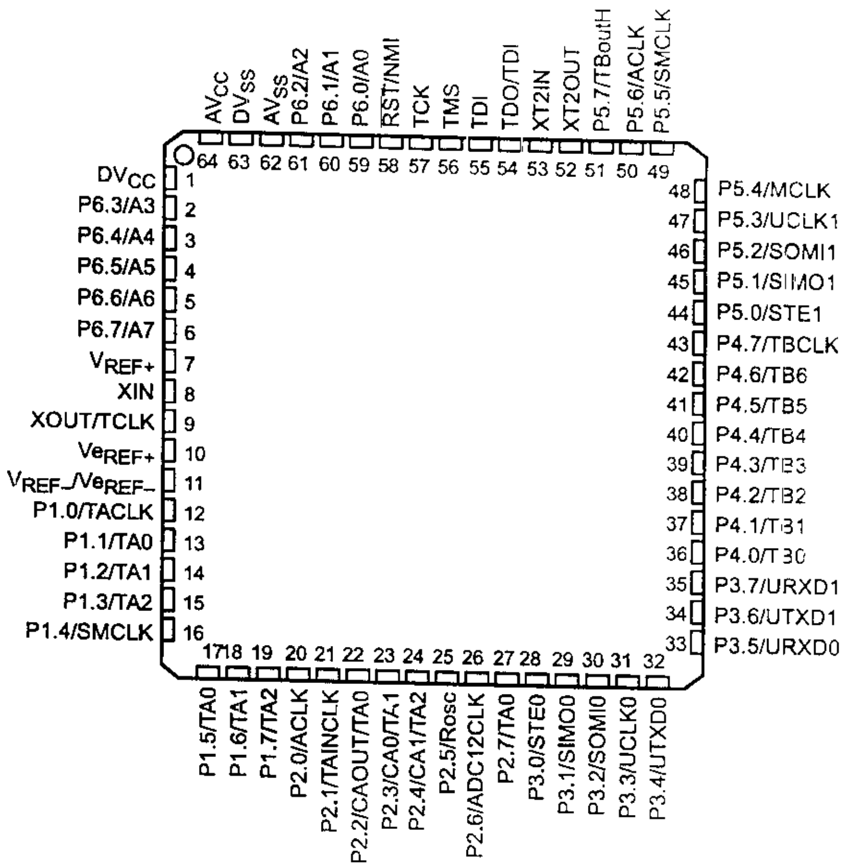
The Texas Instruments MSP430 series is an ultralow-power microcontroller family consisting of several devices featuring different sets of modules targeted to various applications. The microcontroller is designed to be battery operated for use in extended-time applications. The MSP430 achieves maximum code efficiency with its 16-bit RISC architecture, 16-bit CPU-integrated registers, and a constant generator. The digitally-controlled oscillator provides wake-up from low-power mode to active mode in less than 6 µs. The MSP430x13x and the MSP430x14x series are microcontroller configurations with two built-in 16-bit timers, a fast 12-bit A/D converter, one or two universal serial synchronous/asynchronous communication interfaces (USART), and 48 I/O pins.

Typical applications include sensor systems that capture analog signals, convert them to digital values, and process and transmit the data to a host system. The timers make the configurations ideal for industrial control applications such as ripple counters, digital motor control, EE-meters, hand-held meters, etc. The hardware multiplier enhances the performance and offers a broad code and hardware-compatible family solution.

PRODUCT PREVIEW

pin designation, MSP430F147, MSP430F148, MSP430F149

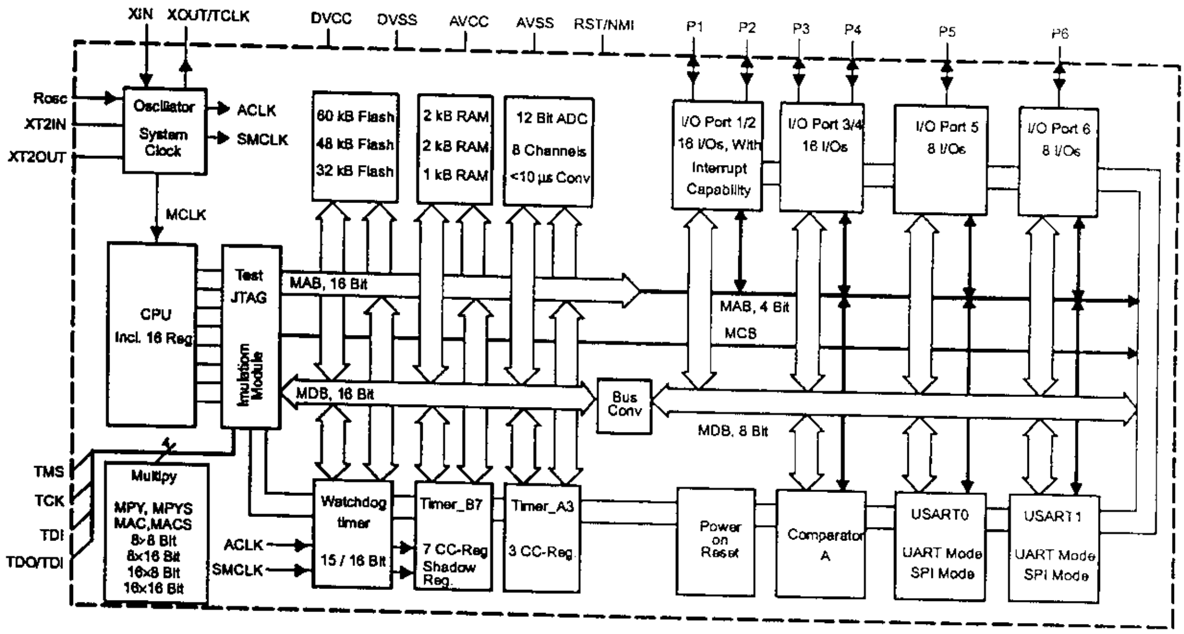
PM PACKAGE
(TOP VIEW)



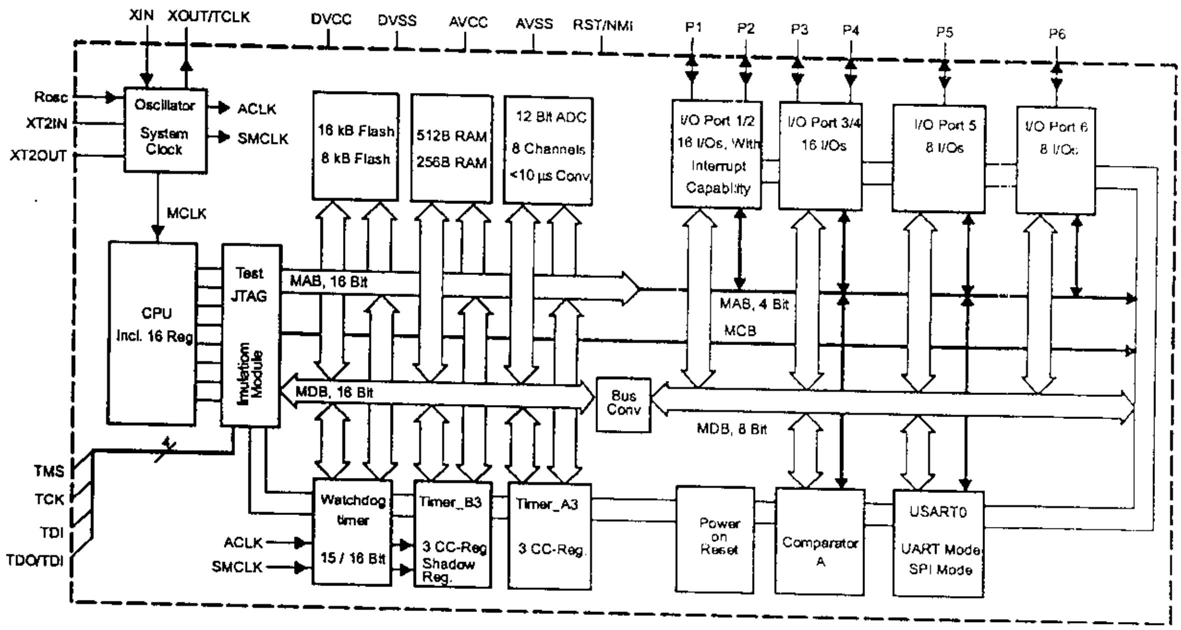
PRODUCT PREVIEW

functional block diagrams

MSP430x14x



MSP430x13x



Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
AV_{CC}	64		Analog supply voltage, positive terminal. Supplies only the analog portion of the analog-to-digital converter.
AV_{SS}	62		Analog supply voltage, negative terminal. Supplies only the analog portion of the analog-to-digital converter.
DV_{CC}	1		Digital supply voltage, positive terminal. Supplies all digital parts.
DV_{SS}	63		Digital supply voltage, negative terminal. Supplies all digital parts.
P1.0/TACLK	12	I/O	General digital I/O pin/Timer_A, clock signal TACLK input
P1.1/TA0	13	I/O	General digital I/O pin/Timer_A, capture: CCI0A input, compare: Out0 output
P1.2/TA1	14	I/O	General digital I/O pin/Timer_A, capture: CCI1A input, compare: Out1 output
P1.3/TA2	15	I/O	General digital I/O pin/Timer_A, capture: CCI2A input, compare: Out2 output
P1.4/SMCLK	16	I/O	General digital I/O pin/SMCLK signal output
P1.5/TA0	17	I/O	General digital I/O pin/Timer_A, compare: Out0 output
P1.6/TA1	18	I/O	General digital I/O pin/Timer_A, compare: Out1 output
P1.7/TA2	19	I/O	General digital I/O pin/Timer_A, compare: Out2 output/
P2.0/ACLK	20	I/O	General digital I/O pin/ACLK output
P2.1/TAINCLK	21	I/O	General digital I/O pin/Timer_A, clock signal at INCLK
P2.2/CAOUT/TA0	22	I/O	General digital I/O pin/Timer_A, capture: CCI0B input/Comparator_A output
P2.3/CA0/TA1	23	I/O	General digital I/O pin/Timer_A, compare: Out1 output/Comparator_A input
P2.4/CA1/TA2	24	I/O	General digital I/O pin/Timer_A, compare: Out2 output/Comparator_A input
P2.5/Rosc	25	I/O	General-purpose digital I/O pin, input for external resistor defining the DCO nominal frequency
P2.6/ADC12CLK	26	I/O	General digital I/O pin, conversion clock – 12-bit ADC
P2.7/TA0	27	I/O	General digital I/O pin/Timer_A, compare: Out0 output
P3.0/STE0	28	I/O	General digital I/O, slave transmit enable – USART0/SPI mode
P3.1/SIMO0	29	I/O	General digital I/O, slave in/master out of USART0/SPI mode
P3.2/SOMI0	30	I/O	General digital I/O, slave out/master in of USART0/SPI mode
P3.3/UCLK0	31	I/O	General digital I/O, external clock input – USART0/UART or SPI mode, clock output – USART0/SPI mode
P3.4/UTXD0	32	I/O	General digital I/O, transmit data out – USART0/UART mode
P3.5/URXD0	33	I/O	General digital I/O, receive data in – USART0/UART mode
P3.6/UTXD1†	34	I/O	General digital I/O, transmit data out – USART1/UART mode
P3.7/URXD1†	35	I/O	General digital I/O, receive data in – USART1/UART mode
P4.0/TB0	36	I/O	General-purpose digital I/O, capture I/P or PWM output port – Timer_B7 CCR0
P4.1/TB1	37	I/O	General-purpose digital I/O, capture I/P or PWM output port – Timer_B7 CCR1
P4.2/TB2	38	I/O	General-purpose digital I/O, capture I/P or PWM output port – Timer_B7 CCR2
P4.3/TB3†	39	I/O	General-purpose digital I/O, capture I/P or PWM output port – Timer_B7 CCR3
P4.4/TB4†	40	I/O	General-purpose digital I/O, capture I/P or PWM output port – Timer_B7 CCR4
P4.5/TB5†	41	I/O	General-purpose digital I/O, capture I/P or PWM output port – Timer_B7 CCR5
P4.6/TB6†	42	I/O	General-purpose digital I/O, capture I/P or PWM output port – Timer_B7 CCR6
P4.7/TBCLK	43	I/O	General-purpose digital I/O, input clock TBCLK – Timer_B7
P5.0/STE1†	44	I/O	General-purpose digital I/O, slave transmit enable – USART1/SPI mode
P5.1/SIMO1†	45	I/O	General-purpose digital I/O slave in/master out of USART1/SPI mode
P5.2/SOMI1†	46	I/O	General-purpose digital I/O, slave out/master in of USART1/SPI mode
P5.3/UCLK1†	47	I/O	General-purpose digital I/O, external clock input – USART1/UART or SPI mode, clock output – USART1/SPI mode
P5.4/MCLK	48	I/O	General-purpose digital I/O, main system clock MCLK output
P5.5/SMCLK	49	I/O	General-purpose digital I/O, submain system clock SMCLK output

† 14x devices only

PRODUCT PREVIEW

Terminal Functions (Continued)

TERMINAL NAME	NO.	I/O	DESCRIPTION
P5.6/ACLK	50	I/O	General-purpose digital I/O, auxiliary clock ACLK output
P5.7/TboutH	51	I/O	General-purpose digital I/O, switch all PWM digital output ports to high impedance – Timer_B7 TB0 to TB6
P6.0/A0	59	I/O	General digital I/O, analog input a0 – 12-bit ADC
P6.1/A1	60	I/O	General digital I/O, analog input a1 – 12-bit ADC
P6.2/A2	61	I/O	General digital I/O, analog input a2 – 12-bit ADC
P6.3/A3	2	I/O	General digital I/O, analog input a3 – 12-bit ADC
P6.4/A4	3	I/O	General digital I/O, analog input a4 – 12-bit ADC
P6.5/A5	4	I/O	General digital I/O, analog input a5 – 12-bit ADC
P6.6/A6	5	I/O	General digital I/O, analog input a6 – 12-bit ADC
P6.7/A7	6	I/O	General digital I/O, analog input a7 – 12-bit ADC
RST/NMI	58	I	Reset input, nonmaskable interrupt input port, or bootstrap loader start (in Flash devices).
TCK	57	I	Test clock. TCK is the clock input port for device programming test and bootstrap loader start (in Flash devices).
TDI	55	I	Test data input. TDI is used as a data input port. The device protection fuse is connected to TDI.
TDO/TDI	54	I/O	Test data output port. TDO/TDI data output or programming data input terminal
TMS	56	I	Test mode select. TMS is used as an input port for device programming and test.
Ve_{REF+}	10	I/P	Input for an external reference voltage to the ADC
V_{REF+}	7	O	Output of positive terminal of the reference voltage in the ADC
V_{REF-}/Ve_{REF-}	11	O	Negative Terminal for the ADC's reference voltage for both sources, the internal reference voltage, or an external applied reference voltage
XIN	8	I	Input port for crystal oscillator XT1. Standard or watch crystals can be connected.
XOUT/TCLK	9	I/O	Output terminal of crystal oscillator XT1 or test clock input
XT2IN	53	I	Input port for crystal oscillator XT2. Only standard crystals can be connected.
XT2OUT	52	O	Output terminal of crystal oscillator XT2

short-form description

processing unit

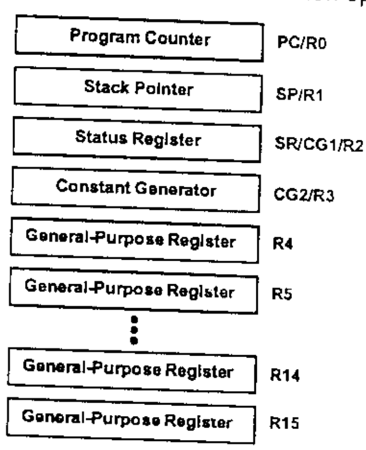
The processing unit is based on a consistent and orthogonal CPU and instruction set. This design structure results in a RISC-like architecture, highly transparent to the application development and notable for its ease of programming. All operations other than program-flow instructions are consequently performed as register operations in conjunction with seven addressing modes for source and four modes for destination operand.

CPU

The CPU has sixteen registers that provide reduced instruction execution time. This reduces the register-to-register operation execution time to one cycle of the processor frequency.

Four of the registers are reserved for special use as program counter, stack pointer, status register, and constant generator. The remaining registers are available as general-purpose registers.

Peripherals are connected to the CPU using a data address and control bus, and can be easily handled with all memory manipulation instructions.



TEXAS INSTRUMENTS
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ELECTRICAL CHARACTERISTICS (V_{in} = 10 V, I_O = 500 mA, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristic	Symbol	MC7805B			MC7805C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = 25°C)	V_O	4.8	5.0	5.2	4.8	5.0	5.2	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤15 W) 7.0 Vdc ≤ V_{in} ≤ 20 Vdc 8.0 Vdc ≤ V_{in} ≤ 20 Vdc	V_O	– 4.75	– 5.0	– 5.25	4.75 –	5.0 –	5.25 –	Vdc
Line Regulation, T_J = 25°C (Note 2) 7.0 Vdc ≤ V_{in} ≤ 25 Vdc 8.0 Vdc ≤ V_{in} ≤ 12 Vdc	Reg_{line}	– –	5.0 1.3	100 50	– –	5.0 1.3	100 50	mV
Load Regulation, T_J = 25°C (Note 2) 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	– –	1.3 0.15	100 50	– –	1.3 0.15	100 50	mV
Quiescent Current (T_J = 25°C)	I_B	–	3.2	8.0	–	3.2	8.0	mA
Quiescent Current Change 7.0 Vdc ≤ V_{in} ≤ 25 Vdc 8.0 Vdc ≤ V_{in} ≤ 25 Vdc 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	– – –	– – –	– 1.3 0.5	– – –	– – –	1.3 – 0.5	mA
Ripple Rejection 8.0 Vdc ≤ V_{in} ≤ 18 Vdc, f = 120 Hz	RR	–	68	–	–	68	–	dB
Dropout Voltage (I_O = 1.0 A, T_J = 25°C)	$V_I - V_O$	–	2.0	–	–	2.0	–	Vdc
Output Noise Voltage (T_A = 25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	–	10	–	–	10	–	µV/V_O
Output Resistance f = 1.0 kHz	r_O	–	0.9	–	–	0.9	–	mΩ
Short Circuit Current Limit (T_A = 25°C) V_{in} = 35 Vdc	I_{SC}	–	0.2	–	–	0.2	–	A
Peak Output Current (T_J = 25°C)	I_{max}	–	2.2	–	–	2.2	–	A
Average Temperature Coefficient of Output Voltage	TCV_O	–	−0.3	–	–	−0.3	–	mV/°C

ELECTRICAL CHARACTERISTICS (V_{in} = 10 V, I_O = 1.0 A, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristic	Symbol	MC7805AC			Unit
		Min	Typ	Max	
Output Voltage (T_J = 25°C)	V_O	4.9	5.0	5.1	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤15 W) 7.5 Vdc ≤ V_{in} ≤ 20 Vdc	V_O	4.8	5.0	5.2	Vdc
Line Regulation (Note 2) 7.5 Vdc ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA 8.0 Vdc ≤ V_{in} ≤ 12 Vdc 8.0 Vdc ≤ V_{in} ≤ 12 Vdc, T_J = 25°C 7.3 Vdc ≤ V_{in} ≤ 20 Vdc, T_J = 25°C	Reg_{line}	– – – –	5.0 1.3 1.3 4.5	50 50 25 50	mV
Load Regulation (Note 2) 5.0 mA ≤ I_O ≤ 1.5 A, T_J = 25°C 5.0 mA ≤ I_O ≤ 1.0 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	– – –	1.3 0.8 0.15	100 100 50	mV
Quiescent Current (T_J = 25°C)	I_B	– –	– 3.2	6.0 6.0	mA
Quiescent Current Change 8.0 Vdc ≤ V_{in} ≤ 25 Vdc, I_O = 500 mA 7.5 Vdc ≤ V_{in} ≤ 20 Vdc, T_J = 25°C 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	– – –	– – –	0.8 0.8 0.5	mA

NOTES: 1. T_{low} = 0°C for MC78XXAC, C = −40°C for MC78XXB; T_{high} = +125°C for MC78XXAC, C, B

2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS (continued) (V_{in} = 10 V, I_O = 1.0 A, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristic	Symbol	MC7805AC			Unit
		Min	Typ	Max	
Ripple Rejection 8.0 Vdc ≤ V_{in} ≤ 18 Vdc, f = 120 Hz, I_O = 500 mA	RR	–	68	–	dB
Dropout Voltage (I_O = 1.0 A, T_J = 25°C)	$V_I - V_O$	–	2.0	–	Vdc
Output Noise Voltage (T_A = 25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	–	10	–	µV/V_O
Output Resistance (f = 1.0 kHz)	r_O	–	0.9	–	mΩ
Short Circuit Current Limit (T_A = 25°C) V_{in} = 35 Vdc	I_{SC}	–	0.2	–	A
Peak Output Current (T_J = 25°C)	I_{max}	–	2.2	–	A
Average Temperature Coefficient of Output Voltage	TCV_O	–	–0.3	–	mV/°C

ELECTRICAL CHARACTERISTICS (V_{in} = 11 V, I_O = 500 mA, T_J = T_{low} to T_{high} [Note 1], unless otherwise noted.)

Characteristic	Symbol	MC7806B			MC7806C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = 25°C)	V_O	5.75	6.0	6.25	5.75	6.0	6.25	Vdc
Output Voltage (5.0 mA ≤ I_O ≤ 1.0 A, P_D ≤ 15 W) 8.0 Vdc ≤ V_{in} ≤ 21 Vdc 9.0 Vdc ≤ V_{in} ≤ 21 Vdc	V_O	– 5.7	– 6.0	– 6.3	5.7 –	6.0 –	6.3 –	Vdc
Line Regulation, T_J = 25°C (Note 2) 8.0 Vdc ≤ V_{in} ≤ 25 Vdc 9.0 Vdc ≤ V_{in} ≤ 13 Vdc	Reg_{line}	– –	5.5 1.4	120 60	– –	5.5 1.4	120 60	mV
Load Regulation, T_J = 25°C (Note 2) 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	– –	1.3 0.2	120 60	– –	1.3 0.2	120 60	mV
Quiescent Current (T_J = 25°C)	I_B	–	3.3	8.0	–	3.3	8.0	mA
Quiescent Current Change 8.0 Vdc ≤ V_{in} ≤ 25 Vdc 9.0 Vdc ≤ V_{in} ≤ 25 Vdc 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	– – –	– – –	– 1.3 0.5	– – –	– – –	1.3 – 0.5	mA
Ripple Rejection 9.0 Vdc ≤ V_{in} ≤ 19 Vdc, f = 120 Hz	RR	–	65	–	–	65	–	dB
Dropout Voltage (I_O = 1.0 A, T_J = 25°C)	$V_I - V_O$	–	2.0	–	–	2.0	–	Vdc
Output Noise Voltage (T_A = 25°C) 10 Hz ≤ f ≤ 100 kHz	V_n	–	10	–	–	10	–	µV/V_O
Output Resistance f = 1.0 kHz	r_O	–	0.9	–	–	0.9	–	mΩ
Short Circuit Current Limit (T_A = 25°C) V_{in} = 35 Vdc	I_{SC}	–	0.2	–	–	0.2	–	A
Peak Output Current (T_J = 25°C)	I_{max}	–	2.2	–	–	2.2	–	A
Average Temperature Coefficient of Output Voltage	TCV_O	–	–0.3	–	–	–0.3	–	mV/°C

NOTES: 1. T_{low} = 0°C for MC78XXAC, C T_{high} = +125°C for MC78XXAC, C, B
= –40°C for MC78XXB

2. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

comparator_A

The control bits are:

CAOUT,	05Ah, bit0	Comparator output
CAF,	05Ah, bit1	The comparator output is transparent or fed through a small filter
P2CA0,	05Ah, bit2	0: Pin P2.3/CA0/TA1 is not connected to Comparator_A. 1: Pin P2.3/CA0/TA1 is connected to Comparator_A.
P2CA1,	05Ah, bit3	0: Pin P2.4/CA1/TA2 is not connected to Comparator_A. 1: Pin P2.4/CA1/TA2 is connected to Comparator_A.
CACTL2.4 to CATCTL2.7	05Ah, bit4 05Ah, bit7	Bits are implemented but do not control any hardware in this device.
CAIFG,	059h, bit0	Comparator_A interrupt flag
CAIE,	059h, bit1	Comparator_A interrupt enable
CAIES,	059h, bit2	Comparator_A interrupt edge select bit 0: The rising edge sets the Comparator_A interrupt flag CAIFG 1: The falling edge set the Comparator_A interrupt flag CAIFG
CAON,	059h, bit3	The comparator is switched on.
CAREF,	059h, bit4,5	Comparator_A reference 0: Internal reference is switched off, an external reference can be applied. 1: 0.25 × VCC reference selected. 2: 0.50 × VCC reference selected. 3: A diode reference selected.
CARSEL,	059h, bit6	An internal reference V_{CAREF}, selected by CAREF bits, can be applied to signal path CA0 or CA1. The signal V_{CAREF} is only driven by a voltage source if the value of CAREF control bits is 1, 2, or 3.
CAEX,	059h, bit7	The comparator inputs are exchanged, used to measure and compensate the offset of the comparator.

Eight additional bits are implemented into the Comparator_A module. They enable the software to switch off the input buffer of Port P2. A CMOS input buffer can dissipate supply current when the input is not near V_{SS} or V_{CC}. Control bits CAPI0 to CAIP7 are initially reset and the port input buffer is active. The port input buffer is inactive if the corresponding control bit is set.

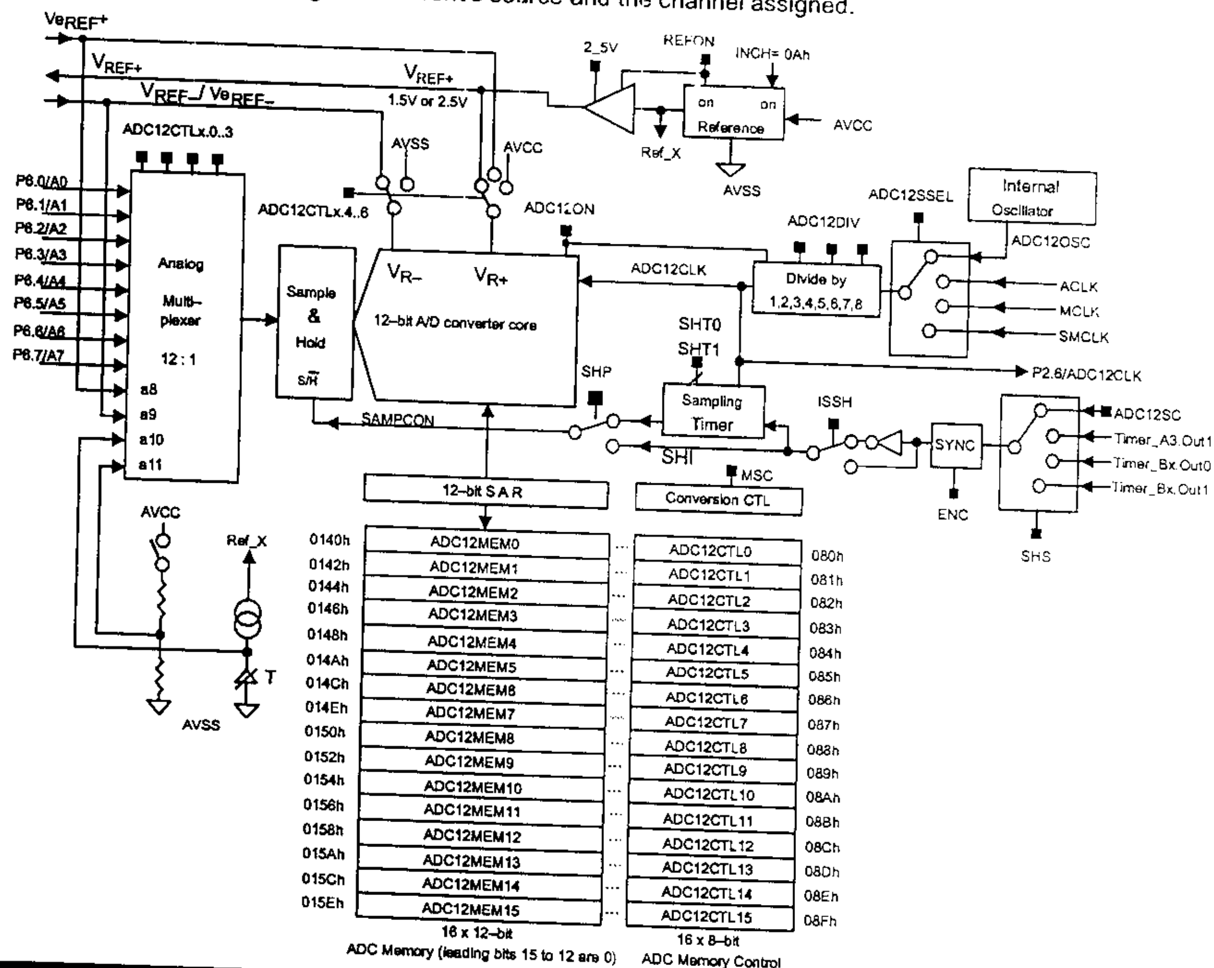
A/D converter

The 12-bit analog-to-digital converter (ADC) uses a 10-bit weighted capacitor array plus a 2-bit resistor string. The CMOS threshold detector in the successive-approximation conversion technique determines each bit by examining the charge on a series of binary-weighted capacitors. The features of the ADC are:

- 12-bit converter with ±1 LSB differential (DNL) and ±1 LSB integral nonlinearity (INL)
- Built-in sample-and-hold
- Eight external and four internal analog channels. The external ADC input terminals are shared with digital port I/O pins.
- Internal reference voltage V_{REF+} of 1.5 V or 2.5 V, software-selectable by control bit 2_5V
- Internal-temperature diode for temperature measurement
- Battery-voltage measurement: $N = 0.5 \times (AV_{CC} - AV_{SS}) \times 4096/1.5V$; V_{REF+} is selected for 1.5 V.

A/D converter (continued)

- Source of positive reference voltage level V_{R+} can be selected as internal (1.5 V or 2.5 V), external, or AV_{CC}. The source is selected individually for each channel.
- Source of negative reference voltage level V_{R-} can be selected as external or AV_{SS}. The source is selected individually for each channel.
- Conversion time can be selected from various clock sources: ACLK, MCLK, SMCLK, or the internal ADC12CLK oscillator. The clock source is divided by an integer from 1 to 8, as selected by software.
- Channel conversion: individual channels, a group of channels, or repeated conversion of a group of channels. If conversion of a group of channels is selected, the sequence, the channels, and the number of channels in the group can be defined by software. For example, a1-a2-a5-a2-a2-....
- The conversion is enabled by the ENC bit, and can be triggered by software via sample and conversion control bit ADC12SC, Timer_A3, or Timer_Bx. Most of the control bits can be modified only if ENC control bit is low. This prevents unpredictable results caused by unintended modification.
- Sampling time can be 4 × n0 × ADC12CLK or 4 × n1 × ADC12CLK. It can be selected to sample as long as the sample signal is high (ISSH=0) or low (ISSH=1). SHT0 defines n0 and SHT1 defines n1.
- The conversion result is stored in one of sixteen registers. The sixteen registers have individual addresses and can be accessed via software. Each of the sixteen registers is linked to an 8-bit register that defines the positive and negative reference source and the channel assigned.



A/D converter (continued)

Table 4. Reference Voltage Configurations

SREF	VOLTAGE AT VR+	VOLTAGE AT VR–
0	AV_{CC}	AV_{SS}
1	V_{REF+} (internal)	AV_{SS}
2, 3	Ve_{REF+} (external)	AV_{SS}
4	AV_{CC}	V_{REF-}/Ve_{REF-} (internal or external)
5	V_{REF+} (internal)	V_{REF-}/Ve_{REF-} (internal or external)
6, 7	Ve_{REF+} (external)	V_{REF-}/Ve_{REF-} (internal or external)

control registers ADC12CTL0 and ADC12CTL1

All control bits are reset during POR. POR is active after V_{CC} or a reset condition is applied to pin RST/NMI. A more detailed description of the control bit functions is found in the ADC12 module description (in the user's guide). Most of the control bits in registers ADC12CTL0, ADC12CTL1, and ADC12MCTLx can only be modified if ENC is low.

The following illustration highlights these bits. Six bits are excluded and can be unrestrictedly modified: ADC12SC, ENC, ADC12TOVIE, ADC12OVIE, and CONSEQ.

The control bits of control registers ADC12CTL0 and ADC12CTL1 are:

ADC12CTL0
01A0h

Bits	15–12	11–8	7	6	5	4	3	2	1	0
Field	SHT1	SHT0	MSC	2_5V	REF ON	ADC12 ON	ADC12 OVIE	ADC12 TOVIE	ENC	ADC12 SC
Access	rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)

ADC12SC
01A0h, bit0

Sample and convert. The ADC12SC bit is used to control the conversion by software. It is recommended that ISSH=0.

SHP=1: Changing the ADC12SC bit from 0 to 1 starts the sample and conversion operation. Bit ADC12SC is automatically reset when the conversion is complete (BUSY=0).

SHP=0: A high level of bit ADC12SC determines the sample time. Conversion starts once it is reset (by software). The conversion takes 13 ADC12CLK cycles.

ENC
01A0h, bit1

Enable conversion. A conversion can be started by software (via ADC12SC) or by external signals, only if the enable conversion bit ENC is high. Most of the control bits in ADC12CTL0 and ADC12CTL1, and all the bits in ADCMCTL.x can only be changed if ENC is low.

0 : No conversion can be started. This is the initial state.

1: The first sample and conversion starts with the first rising edge of the sampling signal. The operation selected proceeds as long as ENC is set.

control registers ADC12CTL0 and ADC12CTL1

ADC12TOVIE 01A0h, bit2
Conversion time overflow interrupt enable.
The timing overflow takes place and a timing overflow vector is generated if another start of sample and conversion is requested while the current conversion or sequence of conversions is still active. The timing overflow enable, if set, may request an interrupt.

ADC12OVIE 01A0h, bit3
Overflow interrupt enables the individual enable for the overflow-interrupt vector.
The overflow takes place if the next conversion result is written into ADC memory ADC12MEMx but the previous result was not read. If an overflow vector is generated, the overflow-interrupt enable flag ADC12OVIE and the general-interrupt enable GIE are set and an interrupt service is requested.

ADC12ON 01A0h, bit4
Switch on the 12-bit ADC core. Make sure that the settling timing constraints are met if ADC core is powered up.
0: Power consumption of the core is off. No conversion is started.
1: ADC core is supplied with power. If no A/D conversion is required, ADC12ON can be reset to conserve power.

REFON 01A0h, bit5
Reference voltage on
0: The internal reference voltage is switched off. No power is consumed by the reference voltage generator.
1: The internal reference voltage is switched on and consumes additional power. The settling time of the reference voltage should be over before the first sample and conversion is started.

2_5V 01A0h, bit6
Reference voltage level
0: The internal-reference voltage is 1.5 V if REFON = 1.
1: The internal-reference voltage is 2.5 V if REFON = 1.

MSC 01A0h, bit7
Multiple sample and conversion. Works only when the sample timer is selected to generate the sample signal and to repeat single channel, sequence of channel, or when repeat sequence of channel (CONSEQ≠0) is selected.
0 : Only one sample is taken.
1 : If SHP is set and CONSEQ = {1, 2, or 3}, then the rising edge of the sample timer's input signal starts the repeat and/or the sequence of channel mode. Then the second and all further conversions are immediately started after the current conversion is completed.

SHT0 01A0h, bit8–11
Sample-and-hold Time0

SHT1 01A0h, bit12–15
Sample-and-hold Time1
The sample time is a multiple of the ADC12CLK × 4:

$$t_{sample} = 4 \times ADC12CLK \times n$$

SHT0/1	0	1	2	3	4	5	6	7	8	9	10	11	12–15
n	1	2	4	8	16	24	32	48	64	96	128	192	256

The sampling time defined by SHT0 is used when ADC12MEM0 through ADC12MEM7 are used during conversion. The sampling time defined by SHT1 is used when ADC12MEM8 through ADC12MEM15 are used during conversion.

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control registers ADC12CTL0 and ADC12CTL1 (continued)

ADC12CTL1 01A2h	15							8	7							0
	CSStartAdd				SHS		SHP	ISSH	ADC12DIV			ADC12SSEL		CONSEQ		ADC12 BUSY
	rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)	r –(0)

ADC12BUSY 01A2h, bit0
The BUSY signal indicates an active sample and conversion operation.
0: No conversion is active. The enable conversion bit ENC can be reset normally.
1: A sample period. Conversion or conversion sequence is active.

CONSEQ 01A2h, bit1/2
Select the conversion mode. Repeat mode is on if CONSEQ.1 (bit 1) is set.
0: One single channel is converted
1: One single sequence of channels is converted
2: Repeating conversion of one single channel
3: Repeating conversion of a sequence of channels

ADC12SSEL 01A2h, bit3/4
Selects the clock source for the converter core
0: Internal oscillator embedded in the ADC12 module
1: ACLK
2: MCLK
3: SMCLK

ADC12DIV 01A2h, bit5,6,7
Selects the division rate for the clock source selected by ADC12SSEL. The clock-operation signal ADC12CLK is used in the converter core. The conversion, without sampling time, requires 13 ADC12CLK clocks.
0 to 7: Divide selected clock source by integer from 1 to 8

ISSH 01A2h, bit8
Invert source for the sample signal
0: The source for the sample signal is not inverted.
1: The source for the sample signal is inverted.

SHP 01A2h, bit9
Sample-and-hold pulse, programmable length of sample pulse
0: The sample operation lasts as long as the sample-and-hold signal is 1. The conversion operation starts if the sample-and-hold signal goes from 1 to 0.
1: The sample time (sample signal is high) is defined by nx4x(1/$f_{ADC12CLK}$). SHTx holds the data for n. The conversion starts when the sample signal goes from 1 to 0.

SHS 01A2h, bit10/11
Source for sample-and-hold
0: Control bit ADC12SC triggers sample-and-hold followed by the A/D conversion.
1: The trigger signal for sample-and-hold and conversion comes from Timer_A3.EQU1.
2: The trigger signal for sample-and-hold and conversion comes from Timer_B.EQU0.
3: The trigger signal for sample-and-hold and conversion comes from Timer_B.EQU1.

CStartAdd 01A2h, bit12 to bit15
Conversion start address CstartAdd is used to define which ADC12 control memory is used to start a (first) conversion. The value of CstartAdd ranges from 0 to 0Fh, corresponding to ADC12MEM0 to ADC12MEM15 and the associated control registers ADC12MCTL0 to ADC12MCTL15.

control register ADC12MCTLx and conversion memory ADC12MEMx

All control bits are reset during POR. POR is active after application of V_{CC}, or after a reset condition is applied to pin RST/NMI. Control registers ADC12MCTL.x can be modified only if enable conversion control bit ENC is reset. Any instruction that writes to an ADC12MCTLx register while the ENC bit is reset has no effect. A more detailed description of the control bit functions is found in the ADC12 module description (in the *MSP430x1xx User's Guide*).

There are sixteen ADC12MCTLx 8-bit memory control registers and sixteen ADC12MEMx 16-bit registers. Each of the memory control registers is associated with one ADC12MEMx register; for example, ADC12MEM0 is associated with ADC12MCTL0, ADC12MEM1, is associated with ADC12MCTL1, etc.

ADC12MCTLx 080h....08Fh	7		0
	EOS	Sref, Source of Reference	INCH, Input Channel a0 to a11
	rw–(0)	rw–(0)	rw–(0)

The control register bits are used to select the analog channel, the reference voltage sources for V_{R+} and V_{R-}, and a control signal which marks the last channel in a group of channels. The sixteen 16-bit registers ADC12MEMx are used to hold the conversion results.

The following illustration shows the conversion-result registers ADC12MEM0 to ADC12MEM15:

ADC12MEM 0140h...015Eh	15			12	11											0
	0	0	0	0	MSB											LSB
	r0	r0	r0	r0	rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)	rw–(0)

ADC12MEM0 to	0140h, bit0,	The 12 bits of the conversion result are stored in 16 control registers ADC12MEM0 to ADC12MEM15.
ADC12MEM15	015Eh, bit15	The 12 bits are right-justified and the upper four bits are always read as 0.

ADC12 interrupt flags ADC12IFG.x and enable registers ADC12IEN.x

There are 16 ADC12IFG.x interrupt flags, 16 ADC12IE.x interrupt-enable bits, and one interrupt-vector word. The 16 interrupt flags and enable bits are associated with the 16 ADC12MEMx registers. For example, register ADC12MEM0, interrupt flag ADC12IFG.0, and interrupt-enable bit ADC12IE.0 form one conversion-result block.

ADC12IFG.0 has the highest priority and ADC12IFG.15 has the lowest priority.

All interrupt flags and interrupt-enable bits are reset during POR. POR is active after application of V_{CC} or after a reset condition is applied to the RST/NMI pin.

ADC12 interrupt vector register

The 12-bit ADC has one interrupt vector for the overflow flag, the timing overflow flag, and sixteen interrupt flags. This vector indicates that a conversion result is stored into registers ADC12MEMx. Handling of the 18 flags is assisted by the interrupt-vector word. The 16-bit vector word ADC12IV indicates the highest pending interrupt. The interrupt-vector word is used to add an offset to the program counter so that the interrupt-handler software continues at the corresponding program location according to the interrupt event. This simplifies the interrupt-handler operation and assigns each interrupt event the same five-cycle overhead.

peripheral file map

PERIPHERALS WITH WORD ACCESS			
Watchdog	Watchdog Timer control	WDTCTL	0120h
Timer_B7 Timer_B3 (see Note 9)	Timer_B interrupt vector	TBIV	011Eh
	Timer_B control	TBCTL	0180h
	Capture/compare control 0	CCTL0	0182h
	Capture/compare control 1	CCTL1	0184h
	Capture/compare control 2	CCTL2	0186h
	Capture/compare control 3	CCTL3	0188h
	Capture/compare control 4	CCTL4	018Ah
	Capture/compare control 5	CCTL5	018Ch
	Capture/compare control 6	CCTL6	018Eh
	Timer_B register	TBR	0190h
	Capture/compare register 0	CCR0	0192h
	Capture/compare register 1	CCR1	0194h
	Capture/compare register 2	CCR2	0196h
	Capture/compare register 3	CCR3	0198h
	Capture/compare register 4	CCR4	019Ah
	Capture/compare register 5	CCR5	019Ch
	Capture/compare register 6	CCR6	019Eh
Timer_A3	Timer_A interrupt vector	TAIV	012Eh
	Timer_A control	TACTL	0160h
	Capture/compare control 0	CCTL0	0162h
	Capture/compare control 1	CCTL1	0164h
	Capture/compare control 2	CCTL2	0166h
	Reserved		0168h
	Reserved		016Ah
	Reserved		016Ch
	Reserved		016Eh
	Timer_A register	TAR	0170h
	Capture/compare register 0	CCR0	0172h
	Capture/compare register 1	CCR1	0174h
	Capture/compare register 2	CCR2	0176h
	Reserved		0178h
	Reserved		017Ah
	Reserved		017Ch
	Reserved		017Eh
Multiply In MSP430x14x only	Sum extend	SumExt	013Eh
	Result high word	ResHi	013Ch
	Result low word	ResLo	013Ah
	Second operand	OP_2	0138h
	Multiply signed +accumulate/operand1	MACS	0136h
	Multiply+accumulate/operand1	MAC	0134h
	Multiply signed/operand1	MPYS	0132h
	Multiply unsigned/operand1	MPY	0130h

NOTE 10: Timer_B7 in MSP430x14x family has 7 CCR, Timer_B3 in MSP430x13x family has 3 CCR.

peripheral file map (continued)

PERIPHERALS WITH WORD ACCESS (CONTINUED)			
Flash	Flash control 3	FCTL3	012Ch
	Flash control 2	FCTL2	012Ah
	Flash control 1	FCTL1	0128h
ADC12 See also *Peripherals with Byte Access*	Conversion memory 15	ADC12MEM15	015Eh
	Conversion memory 14	ADC12MEM14	015Ch
	Conversion memory 13	ADC12MEM13	015Ah
	Conversion memory 12	ADC12MEM12	0158h
	Conversion memory 11	ADC12MEM11	0156h
	Conversion memory 10	ADC12MEM10	0154h
	Conversion memory 9	ADC12MEM9	0152h
	Conversion memory 8	ADC12MEM8	0150h
	Conversion memory 7	ADC12MEM7	014Eh
	Conversion memory 6	ADC12MEM6	014Ch
	Conversion memory 5	ADC12MEM5	014Ah
	Conversion memory 4	ADC12MEM4	0148h
	Conversion memory 3	ADC12MEM3	0146h
	Conversion memory 2	ADC12MEM2	0144h
	Conversion memory 1	ADC12MEM1	0142h
	Conversion memory 0	ADC12MEM0	0140h
	Interrupt-vector-word register	ADC12IV	01A8h
	Inerrupt-enable register	ADC12IE	01A6h
	Inerrupt-flag register	ADC12IFG	01A4h
	Control register 1	ADC12CTL1	01A2h
	Control register 0	ADC12CTL0	01A0h
ADC12	ADC memory-control register15	ADC12MCTL15	08Fh
	ADC memory-control register14	ADC12MCTL14	08Eh
	ADC memory-control register13	ADC12MCTL13	08Dh
	ADC memory-control register12	ADC12MCTL12	08Ch
	ADC memory-control register11	ADC12MCTL11	08Bh
	ADC memory-control register10	ADC12MCTL10	08Ah
	ADC memory-control register9	ADC12MCTL9	089h
	ADC memory-control register8	ADC12MCTL8	088h
	ADC memory-control register7	ADC12MCTL7	087h
	ADC memory-control register6	ADC12MCTL6	086h
	ADC memory-control register5	ADC12MCTL5	085h
	ADC memory-control register4	ADC12MCTL4	084h
	ADC memory-control register3	ADC12MCTL3	083h
	ADC memory-control register2	ADC12MCTL2	082h
	ADC memory-control register1	ADC12MCTL1	081h
	ADC memory-control register0	ADC12MCTL0	080h

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peripheral file map (continued)

PERIPHERALS WITH BYTE ACCESS			
UART1 (Only in 'x14x)	Transmit buffer	UTXBUF.1	07Fh
	Receive buffer	URXBUF.1	07Eh
	Baud rate	UBR1.1	07Dh
	Baud rate	UBR0.1	07Ch
	Modulation control	UMCTL.1	07Bh
	Receive control	URCTL.1	07Ah
	Transmit control	UTCTL.1	079h
	UART control	UCTL.1	078h
UART0	Transmit buffer	UTXBUF.0	077h
	Receive buffer	URXBUF.0	076h
	Baud rate	UBR1.0	075h
	Baud rate	UBR0.0	074h
	Modulation control	UMCTL.0	073h
	Receive control	URCTL.0	072h
	Transmit control	UTCTL.0	071h
	UART control	UCTL.0	070h
Comparator_A	Comp._A port disable	CAPD	05Bh
	Comp._A control2	CACTL2	05Ah
	Comp._A control1	CACTL1	059h
System Clock	Basic clock system control2	BCSCTL2	058h
	Basic clock system control1	BCSCTL1	057h
	DCO clock frequency control	DCOCTL	056h
Port P6	Port P6 selection	P6SEL	037h
	Port P6 direction	P6DIR	036h
	Port P6 output	P6OUT	035h
	Port P6 input	P6IN	034h
Port P5	Port P5 selection	P5SEL	033h
	Port P5 direction	P5DIR	032h
	Port P5 output	P5OUT	031h
	Port P5 input	P5IN	030h
Port P4	Port P4 selection	P4SEL	01Fh
	Port P4 direction	P4DIR	01Eh
	Port P4 output	P4OUT	01Dh
	Port P4 input	P4IN	01Ch
Port P3	Port P3 selection	P3SEL	01Bh
	Port P3 direction	P3DIR	01Ah
	Port P3 output	P3OUT	019h
	Port P3 input	P3IN	018h
Port P2	Port P2 selection	P2SEL	02Eh
	Port P2 interrupt enable	P2IE	02Dh
	Port P2 interrupt-edge select	P2IES	02Ch
	Port P2 interrupt flag	P2IFG	02Bh
	Port P2 direction	P2DIR	02Ah
	Port P2 output	P2OUT	029h
	Port P2 input	P2IN	028h

peripheral file map (continued)

PERIPHERALS WITH BYTE ACCESS			
Port P1	Port P1 selection	P1SEL	026h
	Port P1 interrupt enable	P1IE	025h
	Port P1 interrupt-edge select	P1IES	024h
	Port P1 interrupt flag	P1IFG	023h
	Port P1 direction	P1DIR	022h
	Port P1 output	P1OUT	021h
	Port P1 input	P1IN	020h
Special Functions	SFR module enable 2	ME2	005h
	SFR module enable 1	ME1	004h
	SFR interrupt flag2	IFG2	003h
	SFR interrupt flag1	IFG1	002h
	SFR interrupt enable2	IE2	001h
	SFR interrupt enable1	IE1	000h

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Voltage applied at V_{CC} to V_{SS} .... –0.3 V to + 4.1 V
Voltage applied to any pin (referenced to V_{SS}) .... –0.3 V to V_{CC}+0.3 V
Diode current at any device terminal .... ±2 mA
Storage temperature (unprogrammed device) .... –55°C to 150°C
Storage Temperature (programmed device) .... –40°C to 85°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE: All voltages referenced to V_{SS}.

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recommended operating conditions

PARAMETER			MIN	NOM	MAX	UNITS
Supply voltage during program execution, V_{CC} ($AV_{CC} = DV_{CC} = V_{CC}$)		MSP430F13x, MSP430F14x	1.8		3.6	V
Supply voltage during flash memory programming, V_{CC} ($AV_{CC} = DV_{CC} = V_{CC}$)		MSP430F13x, MSP430F14x	2.7		3.6	V
Supply voltage, V_{SS}			0.0		0.0	V
Operating free-air temperature range, T_A		MSP430x13x MSP430x14x	–40		85	°C
LFXT1 crystal frequency, $f_{(LFXT1)}$ (see Notes 10, 11)	LF selected, XTS=0	Watch crystal		32768		Hz
	XT1 selected, XTS=1	Ceramic resonator	450		8000	kHz
	XT1 selected, XTS=1	Crystal	1000		8000	kHz
XT2 crystal frequency, $f_{(XT2)}$		Ceramic resonator	450		8000	kHz
		Crystal	1000		8000	kHz
Processor frequency (signal MCLK), $f_{(System)}$		V_{CC} = 2.2 V	DC		5	MHz
		V_{CC} = 3.6 V	DC		8	MHz
Flash-timing-generator frequency, $f_{(FTG)}$		MSP430F13x, MSP430F14x	257		476	kHz
Cumulative program time, $t_{(CPT)}$ (see Note 12)		V_{CC} = 2.7 V/3.6 V MSP430F13x MSP430F14x			3	ms
Low-level input voltage (TCK, TMS, TDI, RST/NMI), V_{IL} (excluding Xin, Xout)		V_{CC} = 2.2 V/3 V	V_{SS}		V_{SS} +0.6	V
High-level input voltage (TCK, TMS, TDI, RST/NMI), V_{IH} (excluding Xin, Xout)		V_{CC} = 2.2 V/3 V	$0.8V_{CC}$		V_{CC}	V
Input levels at Xin and Xout	$V_{IL(Xin, Xout)}$	V_{CC} = 2.2 V/3 V	V_{SS}		$0.2 \times V_{SS}$	V
	$V_{IH(Xin, Xout)}$		$0.8 \times V_{CC}$		V_{CC}	

NOTES: 11. In LF mode, the LFXT1 oscillator requires a watch crystal and the LFXT1 oscillator requires a 5.1-MΩ resistor from XOUT to VSS when VCC < 2.5 V. In XT1-mode, the LFXT1. and XT2 oscillators accept a ceramic resonator or a crystal frequency of 4 MHz at $V_{CC} \geq 2.2$ V. In XT1-mode, the LFXT1 and XT2 oscillators accept a ceramic resonator or an 8-MHz crystal frequency at $V_{CC} \geq 2.8$ V.

12. In LF mode, the LFXT1 oscillator requires a watch crystal. LFXT1 accepts a ceramic resonator or a crystal in XT1 mode.

13. The cumulative program time must not be exceeded during a segment-write operation.

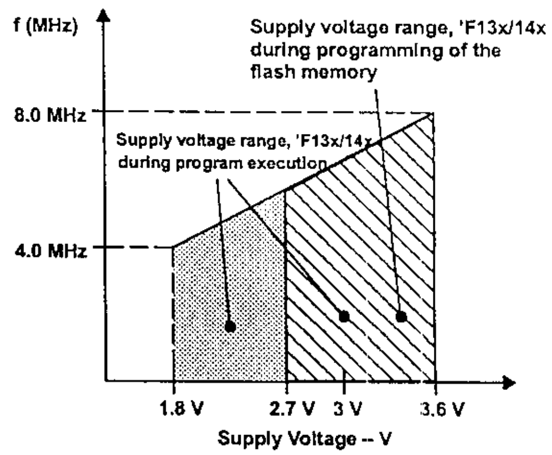

Figure 3. Frequency vs Supply Voltage, MSP430F13x or MSP430F14x

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

supply current into AV_{CC} + DV_{CC} excluding external current, $f_{(System)}$ = 1 MHz

PARAMETER			TEST CONDITIONS		MIN	NOM	MAX	UNIT
$I_{(AM)}$	Active mode, $f_{(MCLK)} = f_{(SMCLK)}$ = 1 MHz, $f_{(ACLK)}$ = 32,768 Hz XTS=0, SELM=(0,1)	F135, F149	T_A = –40°C to 85°C	V_{CC} = 2.2 V		225	TBD	μA
				V_{CC} = 3 V		340	TBD	
$I_{(AM)}$	Active mode, $f_{(MCLK)} = f_{(SMCLK)}$ = 4 096 Hz, $f_{(ACLK)}$ = 4,096 Hz XTS=0, SELM=(0,1) XTS=0, SELM=3	F135, F149	T_A = –40°C to 85°C	V_{CC} = 2.2 V		TBD	TBD	μA
				V_{CC} = 3 V		TBD	TBD	
$I_{(LPM0)}$	Low-power mode, (LPM0)	F135, F149	T_A = –40°C to 85°C	V_{CC} = 2.2 V		65	TBD	μA
				V_{CC} = 3 V		70	TBD	
$I_{(LPM2)}$	Low-power mode, (LPM2)		T_A = –40°C to 85°C	V_{CC} = 2.2 V		11	TBD	μA
				V_{CC} = 3 V		17	TBD	
$I_{(LPM3)}$	Low-power mode, (LPM3) $f_{(MCLK)} = f_{(SMCLK)}$ = 0 MHz, $f_{(ACLK)}$ = 32,768 Hz, SCG0 = 1		T_A = –40°C	V_{CC} = 2.2 V		1	TBD	μA
			T_A = 25°C			0.9	TBD	
			T_A = 85°C			2.7	TBD	
			T_A = –40°C	V_{CC} = 3 V		2	TBD	μA
			T_A = 25°C			1.9	TBD	
			T_A = 85°C			3.9	TBD	
$I_{(LPM4)}$	Low-power mode, (LPM4) $f_{(MCLK)}$ = 0 MHz, $f_{(SMCLK)}$ = 0 MHz, $F_{(ACLK)}$ = 0 Hz, SCG0 = 1		T_A = –40°C	V_{CC} = 2.2 V		0.1	TBD	μA
			T_A = 25°C			0.1	TBD	
			T_A = 85°C			1.6	TBD	
			T_A = –40°C	V_{CC} = 3 V		0.1	TBD	μA
			T_A = 25°C			0.1	TBD	
			T_A = 85°C			1.9	TBD	

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electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

Current consumption of active mode versus system frequency, F-version

I(AM) = I(AM) [1 MHz] × f(System) [MHz]

Current consumption of active mode versus supply voltage, F-version

$I_{(AM)} = I_{(AM)[3 V]} + 120 \mu A/V \times (V_{CC} - 3 V)$

SCHMITT-trigger inputs – Ports P1, P2, P3, P4, P5, and P6

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	V_{CC} = 2.2 V	1.1		1.3	V
		V_{CC} = 3 V	1.5		1.8	
V_{IT-}	Negative-going input threshold voltage	V_{CC} = 2.2 V	0.4		0.9	V
		V_{CC} = 3 V	0.90		1.2	
$V_I - V_O$	Input/output voltage differential, (hysteresis)	V_{CC} = 2.2 V	0.3		1	V
		V_{CC} = 3 V	0.5		1.4	

standard inputs – RST/NMI; JTAG: TCK, TMS, TDI, TDO/TDI

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage	V_{CC} = 2.2 V / 3 V	V_{SS}		V_{SS}+0.6	V
V_{IH}	High-level input voltage		0.8×V_{CC}		V_{CC}	V

outputs – Port 1: P1.0 to P1.7; Port 2: P2.0 to P2.5 (see Note 13)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH(max)}$ = –1.5 mA,	V_{CC} = 2.2 V,	See Note 14	V_{CC}–0.25		V_{CC}	V
		$I_{OH(max)}$ = –6 mA,	V_{CC} = 2.2 V,	See Note 15	V_{CC}–0.6		V_{CC}	
		$I_{OH(max)}$ = –1.5 mA,	V_{CC} = 3 V,	See Note 14	V_{CC}–0.25		V_{CC}	
		$I_{OH(max)}$ = –6 mA,	V_{CC} = 3 V,	See Note 15	V_{CC}–0.6		V_{CC}	
V_{OL}	Low-level output voltage	$I_{OL(max)}$ = 1.5 mA,	V_{CC} = 2.2 V,	See Note 14	V_{SS}		V_{SS}+0.25	V
		$I_{OL(max)}$ = 6 mA,	V_{CC} = 2.2 V,	See Note 15	V_{SS}		V_{SS}+0.6	
		$I_{OL(max)}$ = 1.5 mA,	V_{CC} = 3 V,	See Note 14	V_{SS}		V_{SS}+0.25	
		$I_{OL(max)}$ = 6 mA,	V_{CC} = 3 V,	See Note 15	V_{SS}		V_{SS}+0.6	

NOTES: 14. In LF mode, the LFXT1 oscillator requires a 5.1-MΩ resistor connected from XOUT to V_{SS} when $V_{CC} \le 2.5V$. All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current. The current consumptions in LPM2, LPM3, and LPM4 are measured with active ACLK selected.

15. The maximum total current, $I_{OH(max)}$ and $I_{OL(max)}$, for all outputs combined, should not exceed ±12 mA to satisfy the maximum specified voltage drop.

16. The maximum total current, $I_{OH(max)}$ and $I_{OL(max)}$, for all outputs combined, should not exceed ±48 mA to satisfy the maximum specified voltage drop.

Input frequency – Ports P1 to P6

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$f_{(IN)}$	$t_{(h)} = t_{(L)}$	V_{CC} = 2.2 V			8	MHz
		V_{CC} = 3 V			10	

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

12-bit ADC, power supply and input range conditions (see Note 29)

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
AV_{CC}	Analog supply voltage	AV_{CC} and DV_{CC} are connected together AV_{SS} and DV_{SS} are connected together $V_{(AVSS)} = V_{(DVSS)} = 0$ V		1.8		3.6	V
V_{REF+}	Positive built-in reference voltage output	2_5 V = 1 for 2.5 V built-in reference 2_5 V = 0 for 1.5 V built-in reference $I_{V(REF)+} \le 1$ mA	3 V	2.4	2.5	2.6	V
			2.2 V/3 V	1.44	1.5	1.56	
I_{VREF+}	Load current out of V_{REF+} terminal		2.2 V	0.01		–0.5	mA
			3 V			–1	
$I_{L(VREF)+}$	Load-current regulation V_{REF+} terminal	$I_{V(REF)+}$ = 500 µA +/– 100 µA Analog input voltage ~0.75 V; 2_5 V = 0	2.2 V			±1	LSB
			3 V			±1	
		$I_{V(REF)+}$ = 500 µA ± 100 µA Analog i/p voltage ~1.25 V; 2_5 V = 1	3 V			±1	LSB
$I_{DL(VREF)+}$	Load current regulation V_{REF+} terminal	$I_{V(REF)+}$ =100 µA → 900 µA, VCC=3 V, ax ~0.5 x V_{REF+} Error of conversion result ≤ 1 LSB	C_{VREF+}=0 pF			600	ns
			C_{VREF+}=5 µF			20	
V_{eREF+}	Positive external reference voltage input	$V_{eREF+} > V_{eREF-}/V_{eREF-}$ (see Note 30)		1.4		V_{AVCC}	V
V_{REF-}/V_{eREF-}	Negative external reference voltage input	$V_{eREF+} > V_{eREF-}/V_{eREF-}$ (see Note 31)		0		V_{AVCC} – 1.4	V
(V_{eREF+} – V_{REF-}/V_{eREF-})	Differential external reference voltage input	$V_{eREF+} > V_{eREF-}/V_{eREF-}$ (see Note 32)		1.4		V_{AVCC}	V
$V_{(P6.x/Ax)}$	Analog input voltage range (see Note 33)	All P6.0/A0 to P6.7/A7 terminals. Analog inputs selected in ADC12MCTLx register and P6Sel.x=1 $0 \le x \le 7$; $V_{(AVSS)} \le V_{P6.x/Ax} \le V_{(AVCC)}$		0		V_{AVCC}	V
I_{ADC12}	Operating supply current into AV_{CC} terminal (see Note 34)	$f_{ADC12CLK}$ = 5.0 MHz ADC12ON = 1, REFON = 0	2.2 V		0.65	1.3	mA
			3 V		0.8	1.6	
I_{REF+}	Operating supply current into AV_{CC} terminal (see Note 35)	$f_{ADC12CLK}$ = 5.0 MHz ADC12ON = 0, REFON = 1, 2_5V = 1	3 V		0.5	0.8	mA
I_{REF+}	Operating supply current (see Note 35)	$f_{ADC12CLK}$ = 5.0 MHz ADC12ON = 0, REFON = 1, 2_5V = 0	2.2 V		0.5	0.8	mA
			3 V		0.5	0.8	

NOTES: 29. The leakage current is defined in the leakage current table with P6.x/Ax parameter.
30. The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.
31. The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.
32. The accuracy limits minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.
33. The analog input voltage range must be within the selected reference voltage range V_{R+} to V_{R-} for valid conversion results.
34. The internal reference supply current is not included in current consumption parameter I_{ADC12}.
35. The internal reference current is supplied via terminal AV_{CC}. Consumption is independent of the ADC12ON control bit, unless a conversion is active. The REFON bit enables to settle the built-in reference before starting an A/D conversion.

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electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

12-bit ADC, built-in reference (see Note 39)

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
I_{VeREF+}	Static input current (see Note 36)	$0V \le V_{eREF+} \le V_{AVCC}$	2.2 V/3 V			±1	µA
$I_{VREF-/VeREF-}$	Static input current (see Note 36)	$0V \le V_{eREF-} \le V_{AVCC}$	2.2 V/3 V			±1	µA
C_{VREF+}	Capacitance at pin V_{REF+} (see Note 37)	REFON =1, $0\ mA \le I_{VREF+} \le I_{V(REF)+(max)}$	2.2 V/3 V			200	pF
C_i	Input capacitance (see Note 38)	REFON =1, $0\ mA \le I_{V(REF)^+} \le I_{V(REF)+(max)}$	2.2 V/3 V	5			µF
Z_i	Input MUX ON resistance(see Note 38)	Only one terminal can be selected at one time, P6.x/Ax	2.2 V		18	30	Ω
		$0V \le V_{Ax} \le V_{AVCC}$	3 V			2000	
T_{REF+}	Temperature coefficient of built-in reference	$I_{V(REF)^+}$ is a constant in the range of $0\ mA \le I_{V(REF)^+} \le 1\ mA$	2.2 V/3 V	20		1000	ppm/°C

NOTES: 36. The external reference is used during conversion to charge and discharge the capacitance array. The dynamic impedance should follow the recommendations on analog-source impedance to allow the charge to settle for 12-bit accuracy.
37. The internal buffer operational amplifier and the accuracy specifications require an external capacitor. The external capacitance has two limits: the first is a capacitance of 0 to the maximum data (pF-range), and the second is an external capacitor of greater than the minimum data (µF-range). The output amplifier operates in the safe area in both ranges.
38. The input capacitance is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 12-bit accuracy.
39. The voltage source on V_{eREF+} and V_{REF-}/V_{eREF-}) needs to have low dynamic impedance for 12-bit accuracy. A minimum of 470 nF of the reference supply allows the charge to settle for the 12-bit accuracy.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

12-bit ADC, timing parameters

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
$t_{REF(ON)}$	Settle time of internal reference voltage (see Figure 11 and Note 40)	$I_{V(REF)+}$ = 0.5 mA, $C_{V(REF)+}$ = 10 µF, V_{REF+} = 1.5 V, V_{AVCC} = 2.2 V				17	ms
		$I_{V(REF)+}$ = 0.5 mA, 0 ≤ $C_{V(REF)+}$ ≤ 200pF, V_{REF+} = 1.5 V, V_{AVCC} = 2.2 V		2.17		20	µs
$t_{CONVERT}$	Conversion time (see Figure 12	$AV_{CC(min)} \le V_{AVCC} \le AV_{CC(max)}$, $C_{VREF+} \ge 5$ µF, Internal oscillator, f_{OSC} = 4 MHz to 6 MHz		2.17		3.6	µs
	Conversion time	$AV_{CC(min)} \le V_{AVCC} \le AV_{CC(max)}$, External $f_{ADC12(CLK)}$ from ACLK or MCLK or SMCLK: ADC12SSEL ≠ 0			13×ADC12DIV× 1/$f_{ADC12(CLK)}$		µs
$t_{ADC12ON}$	Settle time of the ADC	$AV_{CC(min)} \le V_{AVCC} \le AV_{CC(max)}$ (see Note 41)				100	ns
t_{Sample}	Sampling time	$V_{AVCC(min)} \le V_{AVCC} \le V_{AVCC(max)}$ $R_{i(source)}$ = 400 Ω, Z_i = 1000 Ω, C_i = 30 pF $\tau = [R_{i(source)} + Z_i] \times C_i$;(see Note 42)	3 V	1220			ns
			2.2 V	1400			

NOTES: 40. The condition is that the error in a conversior started after $t_{REF(ON)}$ is less than ±0.5 LSB. The settling time depends on the external capacitive load. The feedback of the binary-weighted capacitor array to the reference voltage requires a *large* external capacitor. Small external capacitors need greater conversion time (decreased $f_{ADC12CLK}$).

41. The condition is that the error in a conversion started after $t_{ADC12ON}$ is less than ±0.5 LSB. The reference used is already settled.

42. Ten Tau (τ) are needed to get an error of less than ±0.5 LSB. t_{Sample} = 10 x (Ri + Zi) + 800 ns

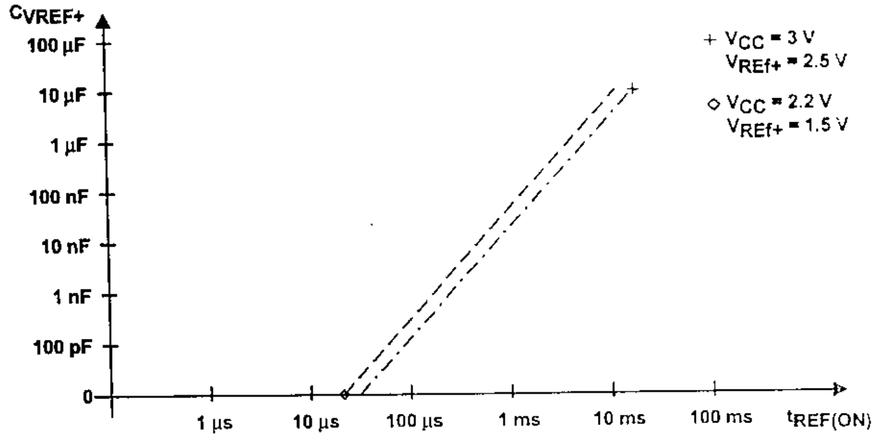

Figure 11. Maximum Settling Time of Internal Reference $t_{REF(ON)}$ vs External Capacitor on V_{REF+}

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electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

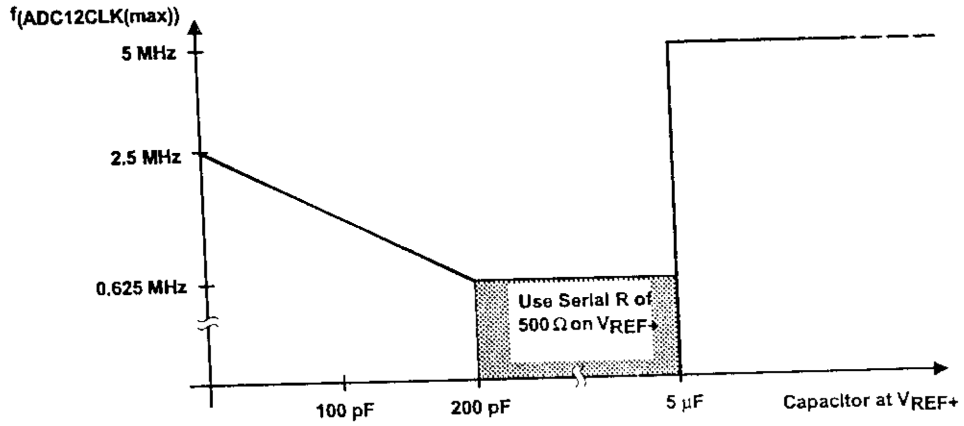


Figure 12. Maximum Frequency $f_{ADC12(CLK)}$ vs External Capacitor on V_{REF+}

12-bit ADC, linearity parameters

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
E_I	Integral linearity error	$(V_{eREF+} - V_{REF-}/V_{eREF-})_{min} \leq (V_{eREF+} - V_{REF-}/V_{eREF-})$	2.2 V/3 V		±1	TBD	LSB
E_D	Differential linearity error	$(V_{eREF+} - V_{REF-}/V_{eREF-})_{min} \leq (V_{eREF+} - V_{REF-}/V_{eREF-})$	2.2 V/3 V		±1	TBD	LSB
E_O	Offset error	$(V_{eREF+} - V_{REF-}/V_{eREF-})_{min} \leq (V_{eREF+} - V_{REF-}/V_{eREF-})$, Internal impedance of source R_i < 100 Ω	2.2 V/3 V		±2	TBD	LSB
E_G	Gain error	$(V_{eREF+} - V_{REF-}/V_{eREF-})_{min} \leq (V_{eREF+} - V_{REF-}/V_{eREF-})$	2.2 V/3 V		±1.1	TBD	LSB
E_T	Total unadjusted error	$(V_{eREF+} - V_{REF-}/V_{eREF-})_{min} \leq (V_{eREF+} - V_{REF-}/V_{eREF-})$	2.2 V/3 V		±2	TBD	LSB

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

12-bit ADC, temperature sensor and built-in Vmid

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
I_{SENSOR}	Operating supply current into AV_{CC} terminal (see Note 43)	V_{REFON} = 0, INCH = 0Ah, ADC12ON=NA., T_A = 25°C	2.2 V		135	TBD	µA
			3 V		135	TBD	
V_{SENSOR}		ADC12ON = 1, INCH = 0Ah, T_A = 0°C	2.2 V		986	986±5%	mV
			3 V		986	986±5%	
TC_{SENSOR}		ADC12ON = 1, INCH = 0Ah	2.2 V		3.55	3.55±3%	mV/°C
			3 V		3.55	3.55±3%	
$t_{SENSOR(ON)}$	On-time if channel 10 is selected (see Note 44)	ADC12ON = 1, INCH = 0Ah, Error of conversion result ≤ 1 LSB	2.2 V			25	µs
			3 V			21	
I_{VMID}	Current into divider at channel 11	ADC12ON = 1, INCH = 0Bh, (see Note 45)	2.2 V			NA	µA
			3 V			NA	
V_{MID}	AV_{CC} divider at channel 11	ADC12ON = 1, INCH = 0Bh, V_{MID} is −0.5 x V_{AVCC}	2.2 V		0.9	0.90±0.04	V
			3 V		1.5	1.50±0.04	
$t_{ON(VMID)}$	On-time if channel 11 is selected (see Note 46)	ADC12ON = 1, INCH = 0Bh, Error of conversion result ≤ 1 LSB	2.2 V			NA	ns
			3 V			NA	

NOTES: 43. The sensor current I_{SENSOR} is consumed if (ADC12ON = 1 and V_{REFON}=1), or (ADC12ON=1 AND INCH=0Ah and sample signal is high).
44. The typical equivalent impedance of the sensor is 51 kΩ. The sample time needed is the sensor-on time $t_{SENSOR(ON)}$
45. No additional current is needed. The V_{MID} is anyway used during conversion.
46. The on-time $t_{ON(VMID)}$ is identical to sampling time t_{Sample}; no additional on time is needed.

JTAG, program memory and fuse

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	NOM	MAX	UNIT
$f_{(TCK)}$	JTAG/Test	TCK frequency	2.2 V	DC		5	MHz
			3 V	DC		10	
		Pullup resistors on TMS, TCK, TDI (see Note 47)	2.2 V/ 3V	25	60	90	kΩ
V_{FB}	JTAG/fuse (see Note 48)	Fuse-blow voltage, F versions (see Note 49)	2.2 V/3 V	6.0		7.0	V
I_{FB}		Supply current on TDI with fuse blown				100	mA
		Time to blow the fuse				1	ms
$I_{(DD-PGM)}$	F-versions only	Current from DV_{CC} when programming is active	2.7 V/3.6 V		3	5	mA
$I_{(DD-Erase)}$	F-versions only	Programming time, single pulse	2.7 V/3.6 V		3	5	mA
$t_{(retention)}$	F-versions only	Write/erase cycles		10^4	10^5		cycles
		Data retention T_J = 25°C		100			years

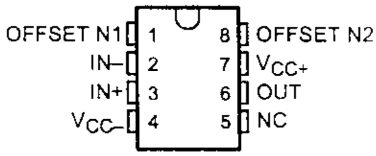
NOTES: 47. TMS, TDI, and TCK pull-up resistors are implemented in all F versions.
48. Once the fuse is blown, no further access to the MSP430 JTAG/test feature is possible. The JTAG block is switched to bypass mode.
49. The supply voltage to blow the fuse is applied to the TDI pin.
50. $f_{(TCK)}$ may be restricted to meet the timing requirements of the module selected. Duration of the program/erase cycle is determined by $f_{(FTG)}$ applied to the flash timing controller. It can be calculated as follows:

$t_{(word\ write)} = 33 \times 1/f_{(FTG)}$
$t_{(segment\ write,\ byte\ 0)} = 30 \times 1/f_{(FTG)}$
$t_{(segment\ write,\ byte\ 1-63)} = 20 \times 1/f_{(FTG)}$
$t_{(mass\ erase)} = 5296 \times 1/f_{(FTG)}$
$t_{(page\ erase)} = 4817 \times 1/f_{(FTG)}$

PRODUCT PREVIEW

- **Low Noise**
- **No External Components Required**
- **Replace Chopper Amplifiers at a Lower Cost**
- **Wide Input-Voltage Range ... 0 to ±14 V Typ**
- **Wide Supply-Voltage Range ... ±3 V to ±18 V**
- **Essentially Equivalent to Fairchild µA714 Operational Amplifiers**
- **Direct Replacements for PMI OP07C and OP07D**

OP07C . . . D OR P PACKAGE
OP07D . . . D, P, OR PS PACKAGE
(TOP VIEW)



NC – No internal connection

description

These devices offer low offset and long-term stability by means of a low-noise, chopperless, bipolar-input-transistor amplifier circuit. For most applications, external components are not required for offset nulling and frequency compensation. The true differential input, with a wide input-voltage range and outstanding common-mode rejection, provides maximum flexibility and performance in high-noise environments and in noninverting applications. Low bias currents and extremely high input impedances are maintained over the entire temperature range. The OP07 is unsurpassed for low-noise, high-accuracy amplification of very-low-level signals.

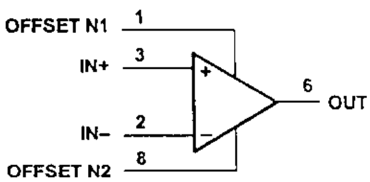
These devices are characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

T_A	V_{IO} MAX AT 25°C	PACKAGE	
		SMALL OUTLINE (D, PS)	PLASTIC DIP (P)
0°C to 70°C	150 µV	OP07CD	OP07CP
		OP07DD OP07DPS	OP07DP

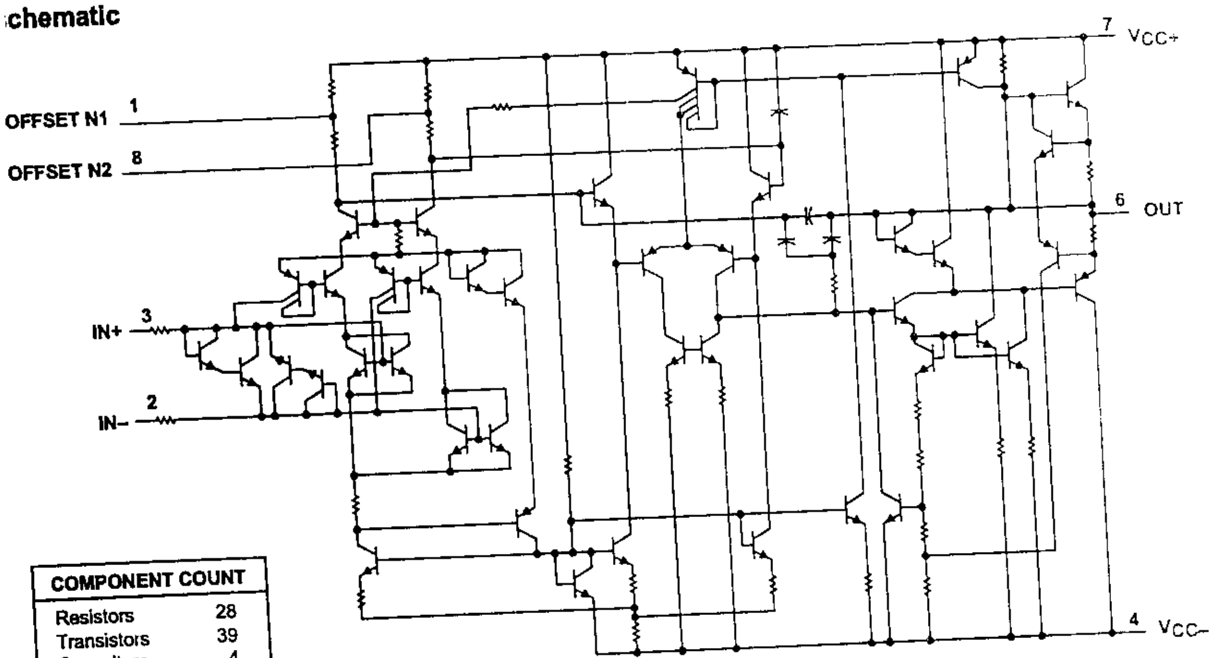
The D package is available taped and reeled. Add the suffix R to the device type (e.g., OP07CDR). The PS package is available only taped and reeled.

symbol



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

chematic



COMPONENT COUNT	
Resistors	28
Transistors	39
Capacitors	4

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage: V_{CC+} (see Note 1) . . . . 22 V
V_{CC-} (see Note 1) . . . . –22 V
Differential input voltage (see Note 2) . . . . ±30 V
Input voltage, V_I (either input, see Note 3) . . . . ±22 V
Duration of output short circuit (see Note 4) . . . . Unlimited
Package thermal impedance, θ_{JA} (see Note 5): D package . . . . 97°C/W
P package . . . . 85°C/W
PS package . . . . 95°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . 260°C
Storage temperature range, T_{stg} . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at IN+ with respect to IN–.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
4. The output may be shorted to ground or either power supply.
5. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

			MIN	MAX	UNIT
$V_{CC\pm}$	Supply voltage		±3	±18	V
V_{IC}	Common-mode input voltage	$V_{CC\pm}$ = ±15 V	–13	13	V
T_A	Operating free-air temperature		0	70	°C

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		T_A	OP07C			OP07D			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$,	$R_S = 50\ \Omega$	25°C		60	150		60	150	μV
				0°C to 70°C		85	250		85	250	
α_{VIO}	Temperature coefficient of input offset voltage	$V_O = 0$,	$R_S = 50\ \Omega$	0°C to 70°C		0.5	1.8		0.7	2.5	μV/°C
	Long-term drift of input offset voltage	See Note 6				0.4			0.5		μV/mo
	Offset adjustment range	$R_S = 20$ kΩ,	See Figure 1	25°C		±4			±4		mV
I_{IO}	Input offset current			25°C		0.8	6		0.8	6	nA
				0°C to 70°C		1.6	8		1.6	8	
α_{IIO}	Temperature coefficient of input offset current			0°C to 70°C		12	50		12	50	pA/°C
I_{IB}	Input bias current			25°C		±1.8	±7		±2	±12	nA
				0°C to 70°C		±2.2	±9		±3	±14	
α_{IIB}	Temperature coefficient of input bias current			0°C to 70°C		18	50		18	50	pA/°C
V_{ICR}	Common-mode input voltge range			25°C	±13	±14		±13	±14		V
				0°C to 70°C	±13	±13.5		±13	±13.5		
V_{OM}	Peak output voltage	$R_L \geq 10$ kΩ		25°C	±12	±13		±12	±13		V
		$R_L \geq 2$ kΩ			±11.5	±12.8		±11.5	±12.8		
		$R_L \geq 1$ kΩ				±12			±12		
		$R_L \geq 2$ kΩ		0°C to 70°C	±11	±12.6		±11	±12.6		
A_{VD}	Large-signal differential voltage amplification	$V_{CC\pm} = \pm 3$ V, $R_L \geq 500$ kΩ	$V_O = \pm 0.5$ V,	25°C	100	400			400		V/mV
		$V_O = \pm 10$ V,	$R_L = 2$ kΩ	25°C	120	400		120	400		
				0°C to 70°C	100	400		100	400		
B_1	Unity-gain bandwidth			25°C	0.4	0.6		0.4	0.6		MHz
r_i	Input resistance			25°C	8	33		7	31		MΩ
CMRR	Common-mode rejection ratio	$V_{IC} = \pm 13$ V,	$R_S = 50\ \Omega$	25°C	100	120		94	110		dB
				0°C to 70°C	97	120		94	106		
k_{SVS}	Supply-voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	$V_{CC\pm} = \pm 3$ V to ±18 V, $R_S = 50\ \Omega$		25°C		7	32		7	32	μV/V
				0°C to 70°C		10	51		10	51	
P_D	Power dissipation	$V_O = 0$,	No load	25°C		80	150		80	150	mW
		$V_{CC\pm} = \pm 3$ V, No load	$V_O = 0$,			4	8		4	8	

† All characteristics are measured under open-loop conditions with zero common-mode input voltage, unless otherwise noted.

NOTE 6: Since long-term drift cannot be measured on the individual devices prior to shipment, this specification is not intended to be a warranty. It is an engineering estimate of the averaged trend line of drift versus time over extended periods after the first thirty days of operation.

operating characteristics, $V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS†	OP07C TYP	OP07D TYP	UNIT
V_n	Equivalent input noise voltage	f = 10 Hz	10.5	10.5	nV/√Hz
		f = 100 Hz	10.2	10.3	
		f = 1 kHz	9.8	9.8	
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 10 Hz	0.38	0.38	μV
I_n	Equivalent input noise current	f = 10 Hz	0.35	0.35	pA/√Hz
		f = 100 Hz	0.15	0.15	
		f = 1 kHz	0.13	0.13	
$I_{N(PP)}$	Peak-to-peak equivalent input noise current	f = 0.1 Hz to 10 Hz	15	15	pA
SR	Slew rate	$R_L \geq 2$ kΩ	0.3	0.3	V/μs

† All characteristics are measured under open-loop conditions with zero common-mode input voltage, unless otherwise noted.

APPLICATION INFORMATION

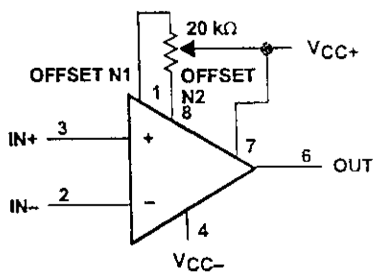


Figure 1. Input Offset-Voltage Null Circuit

REG1117
REG1117A

SBVS001B – OCTOBER 2001

800mA and 1A Low Dropout Positive Regulator
1.8V, 2.5V, 2.85V, 3.3V, 5V, and Adjustable

FEATURES

- FIXED AND ADJUSTABLE VERSIONS
- 2.85V MODEL FOR SCSI-2 ACTIVE TERMINATION
- OUTPUT CURRENT:
  REG1117: 800mA max
  REG1117A: 1A max
- OUTPUT TOLERANCE: ±1% max
- DROPOUT VOLTAGE:
  REG1117: 1.2V max at I_O = 800mA
  REG1117A: 1.3V max at I_O = 1A
- INTERNAL CURRENT LIMIT
- THERMAL OVERLOAD PROTECTION
- SOT-223 AND DDPAK SURFACE-MOUNT PACKAGES

APPLICATIONS

- SCSI-2 ACTIVE TERMINATION
- HAND-HELD DATA COLLECTION DEVICES
- HIGH EFFICIENCY LINEAR REGULATORS
- BATTERY POWERED INSTRUMENTATION
- BATTERY MANAGEMENT CIRCUITS FOR NOTEBOOK AND PALMTOP PCs
- CORE VOLTAGE SUPPLY: FPGA, PLD, DSP, CPU

DESCRIPTION

The REG1117 is a family of easy-to-use three-terminal voltage regulators. The family includes a variety of fixed- and adjustable-voltage versions, two currents (800mA and 1A) and two package types (SOT-223 and DDPAK). See the chart below for available options.

Output voltage of the adjustable versions is set with two external resistors. The REG1117's low dropout voltage allows its use with as little as 1V input-output voltage differential.

Laser trimming assures excellent output voltage accuracy without adjustment. An NPN output stage allows output stage drive to contribute to the load current for maximum efficiency.

	800mA		1A	
VOLTAGE	SOT-223	DDPAK	SOT-223	DDPAK
1.8V			✓	✓
2.5V			✓	✓
2.85V	✓			
3.3V	✓	✓		
5V	✓			✓
Adj.	✓		✓	✓

CKAGE/ORDERING INFORMATION

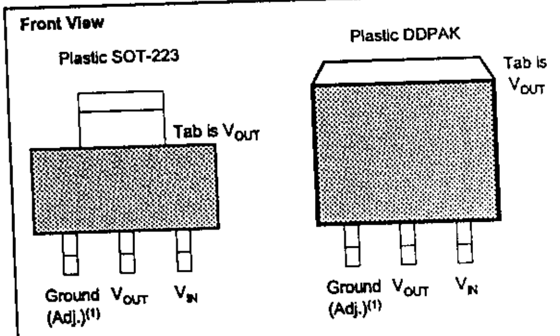
RODUCT	V_O/I_O	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
00mA Output							
:EG1117-2.85	2.85/800mA	SOT223-3	DCY	0°C to +125°C	BB11172	REG1117-2.85	Rails, 80
"	"/"	"		"	"	REG1117-2.85	Tape and Reel, 2500
‹EG1117-3.3	3.3/800mA	SOT223-3	DCY	0°C to +125°C	BB11174	REG1117-3.3	Rails, 80
"	"/"	"		"	"	REG1117-3.3	Tape and Reel, 2500
ℶEG1117F-3.3	3.3/800mA	DDPAK-3	KTT	0°C to +125°C	BB1117F4	REG1117F-3.3	Rails, 49
"	"/"	"		"	"	REG1117F-3.3	Tape and Reel, 500
REG1117-5	5V/800mA	SOT223-3	DCY	0°C to +125°C	BB1' 175	REG1117-5	Rails, 80
"	"/"	"		"	"	REG1117-5	Tape and Reel, 2500
REG1117	Adj./800mA	SOT223-3	DCY	0°C to +125°C	BB1117	REG1117	Rails, 80
"	"/"	"		"	"	REG1117	Tape and Reel, 2500
1A Output							
REG1117A-1.8	1.8V/1A	SOT223-3	DCY	0°C to +125°C	R111718	REG1117A-1.8	Rails, 80
"	"/"	"		"	"	REG1117A-1.8	Tape and Reel, 2500
REG1117FA-1.8	1.8/1A	DDPAK-3	KTT	0°C to +125°C	REG1117FA1.8	REG11:7FA-1.8	Rails, 49
"	"/"	"		"	"	REG1117FA-1.8	Tape and Reel, 500
REG1117A-2.5	2.5/1A	SOT223-3	DCY	0°C to +125°C	R111725	REG1117A-2.5	Rails, 80
"	"/"	"		"	"	REG1117A-2.5	Tape and Reel, 2500
REG1117FA-2.5	2.5/1A	DDPAK-3	KTT	0°C to +125°C	REG1117FA2.5	REG1117FA-2.5	Rails, 49
"	"/"	"		"	"	REG1117FA-2.5	Tape and Reel, 500
REG1117FA-5	5/1A	DDPAK-3	KTT	0°C to +125°C	REG1117FA5.0	REG1117FA-5.0	Rails, 49
"	"/"	"		"	"	REG1117FA-5.0	Tape and Reel, 500
REG1117A	Adj./1A	SOT223-3	DCY	0°C to +125°C	BB1117A	REG1117A	Rails, 80
"	"/"	"		"	"	REG1117A	Tape and Reel, 2500
REG1117FA	Adj./1A	DDPAK-3	KTT	0°C to +125°C	REG1117FA	REG1117FA	Rails, 49
"	"/"	"		"	"	REG1117FA	Tape and Reel, 500

ABSOLUTE MAXIMUM RATINGS(1)

Power Dissipation	Internally Limited
Input Voltage	15V
Operating Junction Temperature Range	0°C to +125°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (soldering, 10s)(2)	+300°C

NOTE: (1) Stresses above these ratings may cause permanent damage. (2) See "Soldering Methods."

CONNECTION DIAGRAM



NOTE: (1) Adjustable-Voltage Model.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ELECTRICAL CHARACTERISTICS

At T_J = +25°C, unless otherwise noted.

PARAMETER	CONDITIONS	REG1117, REG1117A MIN	TYP	MAX	UNITS
OUTPUT VOLTAGE					
REG1117-2.85 See Note 1	I_O = 10mA, V_{IN} = 4.85V	2.820	2.85	2.880	V
	I_O = 0 to 800mA, V_{IN} = 4.05 to 10V	2.790	2.85	2.910	V
REG1117-3.3 See Note 1	I_O = 10mA, V_{IN} = 5.3V	3.270	3.30	3.330	V
	I_O = 0 to 800mA, V_{IN} = 4.8 to 10V	3.240	3.30	3.360	V
REG1117-5 See Note 1	I_O = 10mA, V_{IN} = 7V	4.950	5.00	5.050	V
	I_O = 0 to 800mA, V_{IN} = 6.5 to 10V	4.900	5.00	5.100	V
REG1117A-1.8 See Note 1	I_O = 10mA, V_{IN} = 3.8V	1.782	1.8	1.818	V
	I_O = 0 to 1A, V_{IN} = 3.8V to 10V	1.764	1.8	1.836	V
REG1117A-2.5 See Note 1	I_O = 10mA, V_{IN} = 4.5V	2.475	2.5	2.525	V
	I_O = 0 to 1A, V_{IN} = 4.5V to 10V	2.450	2.5	2.550	V
REG1117A-5 See Note 1	I_O = 10mA, V_{IN} = 7V	4.950	5.0	5.050	V
	I_O = 0 to 1A, V_{IN} = 7V to 10V	4.900	5.0	5.100	V
REFERENCE VOLTAGE					
REG1117 (Adjustable) See Note 1	I_O = 10mA, $V_{IN} - V_O$ = 2V	1.238	1.250	1.262	V
	I_O = 10 to 800mA, $V_{IN} - V_O$ = 1.4 to 10V	1.225	1.250	1.280	V
REG1117A (Adjustable) See Note 1	I_O = 10mA, $V_{IN} - V_O$ = 2V	1.238	1.250	1.262	V
	I_O = 10mA to 1A, $V_{IN} - V_O$ = 1.4 to 10V	1.225	1.250	1.280	V
LINE REGULATION					
REG1117-2.85[1]	I_O = 0, V_{IN} = 4.25 to 10V		1	7	mV
REG1117-3.3[1]	I_O = 0, V_{IN} = 4.8 to 10V		2	7	mV
REG1117-5[1]	I_O = 0, V_{IN} = 6.5 to 15V		3	10	mV
REG1117 (Adjustable)[1]	I_O = 10mA, $V_{IN} - V_O$ = 1.5 to 13.75V		0.1	0.4	%
REG1117A (Adjustable)[1]	I_O = 10mA, $V_{IN} - V_O$ = 1.5 to 13.75V		0.1	0.4	%
REG1117A-1.8[1]	I_O = 0, V_{IN} = 3.8V to 10V		1	7	mV
REG1117A-2.5[1]	I_O = 0, V_{IN} = 4.5V to 10V		1	7	mV
REG1117A-5.0[1]	I_O = 0, V_{IN} = 7V to 15V		3	10	mV
LOAD REGULATION					
REG1117-2.85[1]	I_O = 0 to 800mA, V_{IN} = 4.25V		2	10	mV
REG1117-3.3[1]	I_O = 0 to 800mA, V_{IN} = 4.8V		3	12	mV
REG1117-5[1]	I_O = 0 to 800mA, V_{IN} = 6.5V		3	15	mV
REG1117 (Adjustable)[1][2]	I_O = 10 to 800mA, $V_{IN} - V_O$ = 3V		0.1	0.4	%
REG1117A (Adjustable)[1][2]	I_O = 10mA to 1A, $V_{IN} - V_O$ = 3V		0.1	0.4	%
REG1117A-1.8	I_O = 0 to 1A, V_{IN} = 3.8V		2	10	mV
REG1117A-2.5	I_O = 0 to 1A, V_{IN} = 4.5V		2	10	mV
REG1117A-5	I_O = 0 to 1A, V_{IN} = 7.0V		3	15	mV
DROPOUT VOLTAGE[3]					
All Models[1] See Note 1	I_O = 100mA		1.00	1.10	V
	I_O = 500mA		1.05	1.15	V
	I_O = 800mA		1.10	1.20	V
REG1117 Models[1]	I_O = 1A		1.2	1.30	V
REG1117A See Note 1	I_O = 1A		1.2	1.55	V
CURRENT LIMIT					
REG1117 Models	$V_{IN} - V_O$ = 5V	800	950	1200	mA
REG1117A	$V_{IN} - V_O$ = 5V	1000	1250	1600	mA
MINIMUM LOAD CURRENT Adjustable Models[1][2]	$V_{IN} - V_O$ = 13.75V		1.7	5	mA
QUIESCENT CURRENT Fixed-Voltage Models[1]	$V_{IN} - V_O$ = 5V		4	10	mA
Adjust Pin Current[1][2]	I_O = 10mA, $V_{IN} - V_O$ = 1.4 to 10V		50	120	µA
vs Load Current, REG1117[1]	I_O = 10mA to 800mA, $V_{IN} - V_O$ = 1.4 to 10V		0.5	5	µA
vs Load Current, REG1117A[1]	I_O = 10mA to 1A, $V_{IN} - V_O$ = 1.4 to 10V		0.5	5	µA
THERMAL REGULATION All Models[4]	30ms Pulse		0.01	0.1	%/W
RIPPLE REJECTION All Models	f = 120Hz, $V_{IN} - V_{OUT}$ = 3V + 1Vp-p Ripple		62		dB
TEMPERATURE DRIFT					
Fixed-Voltage Models	T_J = 0°C to +125°C		0.5		%
Adjustable Models	T_J = 0°C to +125°C		2		%

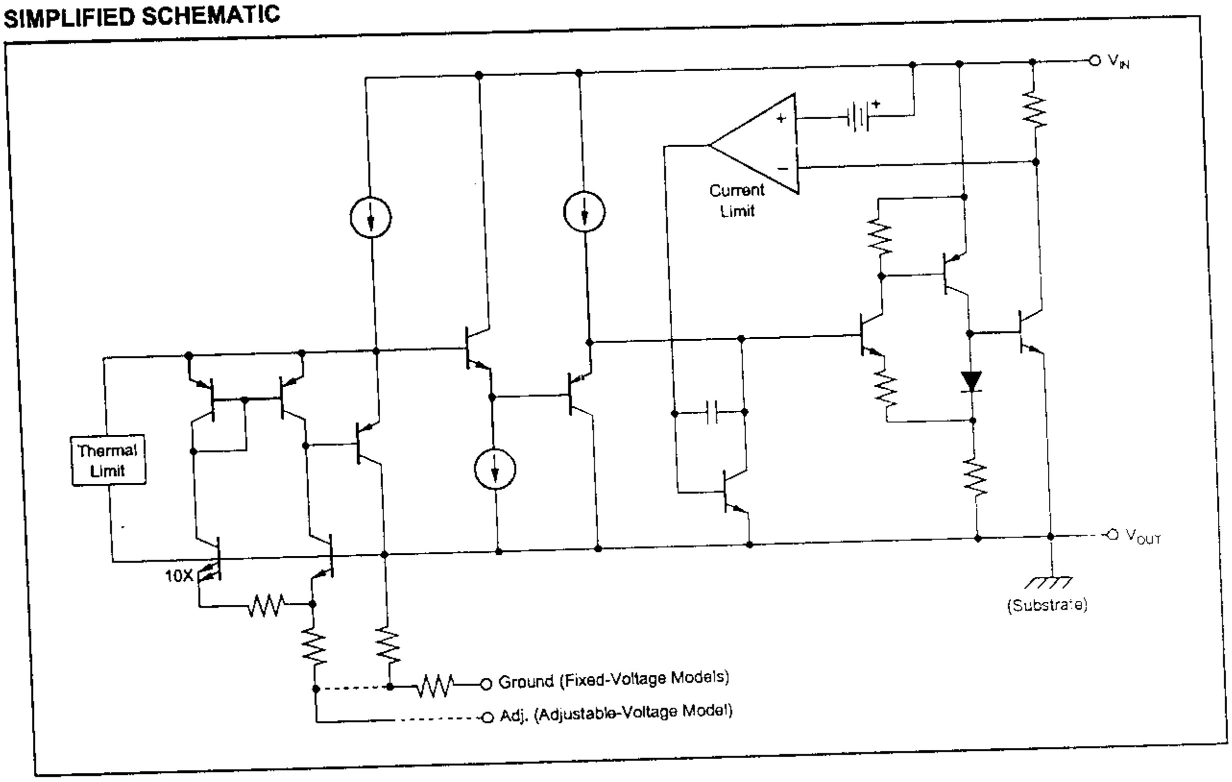
LECTRICAL CHARACTERISTICS (Cont.)

T_J = +25°C, unless otherwise noted.

ARAMETER	CONDITIONS	REG1117, REG1117A MIN	TYP	MAX	UNITS
ONG-TERM STABILITY					
All Models	T_A = +125°C, 1000Hr		0.3		%
UTPUT NOISE					
rms Noise, All Models	f = 10Hz to 10kHz		0.003		%
HERMAL RESISTANCE					
Operating Junction Temperature Range		0		+125	°C
Storage Range		–65		+150	°C
Thermal Resistance, θ_{JC}	(Junction-to-Case at Tab)				
3-Lead SOT-223 Surface-Mount			15		°C/W
3-Lead DDPAK Surface-Mount	f > 50Hz		2		°C/W
	dc		3		°C/W
Thermal Resistance, θ_{JA}	(Junction-to-Case at Tab)				
3-Lead DDPAK Surface-Mount	No Heat Sink		65		°C/W

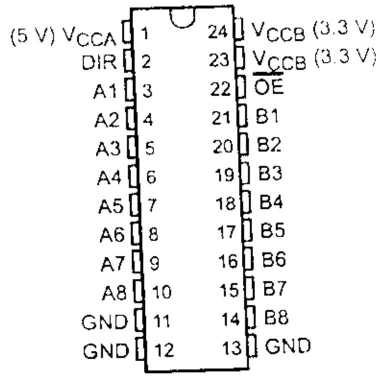
NOTES: (1) Specification applies over the full operating Junction temperature range, 0°C to +125°C. (2) REG1117 and REG1117A adjustable versions require a minimum load current for ±3% regulation. (3) Dropout voltage is the input voltage minus output voltage that produces a 1% decrease in output voltage. (4) Percentage change in unloaded output voltage before versus after a 30ms power pulse of I_O = 800mA (REG1117 models), I_O = 1A (REG1117A). $V_{IN} - V_O$ = 1.4V (Reading taken 10ms after pulse).

SIMPLIFIED SCHEMATIC



- **Bidirectional Voltage Translator**
- **5.5 V on A Port and 2.7 V to 3.6 V on B Port**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

DB, DW, OR PW PACKAGE
(TOP VIEW)



description/ordering information

This 8-bit (octal) noninverting bus transceiver contains two separate supply rails; B port has V_{CCB}, which is set at 3.3 V, and A port has V_{CCA}, which is set at 5 V. This allows for translation from a 3.3-V to a 5-V environment, and vice versa.

The SN74LVC4245A is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so the buses are effectively isolated.

The SN74LVC4245A pinout allows the designer to switch to a normal all-3.3-V or all-5-V 20-pin '245 device without board re-layout. The designer uses the data paths for pins 2–11 and 14–23 of the SN74LVC4245A to align with the conventional '245 pinout.

ORDERING INFORMATION

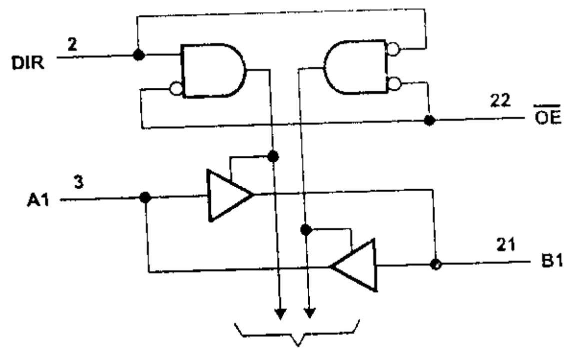
T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SOIC – DW	Tube	SN74LVC4245ADW	LVC4245A
		Tape and reel	SN74LVC4245ADWR	
	SSOP – DB	Tape and reel	SN74LVC4245ADBR	LJ245A
	TSSOP – PW	Tape and reel	SN74LVC4245APWR	LJ245A

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

jic diagram (positive logic)



To Seven Other Channels

ıbsolute maximum ratings over operating free-air temperature range for V_{CCA} = 4.5 V to 5.5 V unless otherwise noted)†

Supply voltage range, V_{CCA}	–0.5 V to 6.5 V
Input voltage range, V_I: A port (see Note 1)	–0.5 V to V_{CCA} + 0.5 V
Control inputs	–0.5 V to 6 V
Output voltage range, V_O: A port (see Note 1)	–0.5 V to V_{CCA} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through each V_{CCA} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 2): DB package	63°C/W
DW package	46°C/W
PW package	88°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. This value is limited to 6 V maximum.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

absolute maximum ratings over operating free-air temperature range for V_{CCB} = 2.7 V to 3.6 V (unless otherwise noted)†

Supply voltage range, V_{CCB}	–0.5 V to 4.6 V
Input voltage range, V_I: B port (see Note 3)	–0.5 V to V_{CCB} + 0.5 V
Output voltage range, V_O: B port (see Note 3)	–0.5 V to V_{CCB} + 0.5 V
Input clamp current, I_{IK} (V_I < 0)	–50 mA
Output clamp current, I_{OK} (V_O < 0)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through V_{CCB} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 2): DB package	63°C/W
DW package	46°C/W
PW package	88°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 2. The package thermal impedance is calculated in accordance with JESD 51-7.
3. This value is limited to 4.6 V maximum.

recommended operating conditions for V_{CCA} = 4.5 V to 5.5 V (see Note 4)

		MIN	MAX	UNIT
V_{CCA}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CCA}	V
V_O	Output voltage	0	V_{CCA}	V
I_{OH}	High-level output current		–24	mA
I_{OL}	Low-level output current		24	mA
T_A	Operating free-air temperature	–40	85	°C

NOTE 4: All unused inputs of the device must be held at the associated V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

recommended operating conditions for V_{CCB} = 2.7 V to 3.6 V (see Note 4)

			MIN	MAX	UNIT
V_{CCB}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CCB} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CCB} = 2.7 V to 3.6 V		0.8	V
V_I	Input voltage		0	V_{CCB}	V
V_O	Output voltage		0	V_{CCB}	V
I_{OH}	High-level output current	V_{CCB} = 2.7 V		–12	mA
		V_{CCB} = 3 V		–24	
I_{OL}	Low-level output current	V_{CCB} = 2.7 V		12	mA
		V_{CCB} = 3 V		24	
T_A	Operating free-air temperature		–40	85	°C

NOTE 4: All unused inputs of the device must be held at the associated V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range for V_{CCA} = 4.5 V to 5.5 V (unless otherwise noted) (see Note 5)

PARAMETER		TEST CONDITIONS		V_{CCA}	MIN	TYP†	MAX	UNIT
V_{OH}		I_{OH} = –100 µA		4.5 V	4.3			V
				5.5 V	5.3			
		I_{OH} = –24 mA		4.5 V	3.7			
				5.5 V	4.7			
V_{OL}		I_{OL} = 100 µA		4.5 V			0.2	V
				5.5 V			0.2	
		I_{OL} = 24 mA		4.5 V			0.55	
				5.5 V			0.55	
I_I	Control inputs	V_I = V_{CCA} or GND		5.5 V			±1	µA
I_{OZ}‡	A port	V_O = V_{CCA} or GND		5.5 V			±5	µA
I_{CCA}		V_I = V_{CCA} or GND,	I_O = 0	5.5 V			80	µA
ΔI_{CCA}§		One input at 3.4 V,	Other inputs at V_{CCA} or GND	5.5 V			1.5	mA
C_i	Control inputs	V_I = V_{CCA} or GND		Open		5		pF
C_{io}	A port	V_O = V_{CCA} or GND		5 V		11		pF

† All typical values are measured at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.
§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or the associated V_{CC}.
NOTE 5: V_{CCB} = 2.7 V to 3.6 V

electrical characteristics over recommended operating free-air temperature range for V_{CCB} = 2.7 V to 3.6 V (unless otherwise noted) (see Note 6)

PARAMETER		TEST CONDITIONS		V_{CCB}	MIN	TYP¶	MAX	UNIT
V_{OH}		I_{OH} = –100 µA		2.7 V to 3.6 V	V_{CC}–0.2			V
		I_{OH} = –12 mA		2.7 V	2.2			
				3 V	2.4			
		I_{OH} = –24 mA		3 V	2			
V_{OL}		I_{OL} = 100 µA		2.7 V to 3.6 V			0.2	V
		I_{OL} = 12 mA		2.7 V			0.4	
		I_{OL} = 24 mA		3 V			0.55	
I_{OZ}‡	B port	V_O = V_{CCB} or GND		3.6 V			±5	µA
I_{CCB}		V_I = V_{CCB} or GND,	I_O = 0	3.6 V			50	µA
ΔI_{CCB}§		One input at V_{CCB} – 0.6 V,	Other inputs at V_{CCB} or GND	2.7 V to 3.6 V			0.5	mA
C_{io}	B port	V_O = V_{CCB} or GND		3.3 V		11		pF

‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.
§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or the associated V_{CC}.
¶ All typical values are measured at V_{CC} = 3.3 V, T_A = 25°C.
NOTE 6: V_{CCA} = 5 V ± 0.5 V

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCA} = 5 V ± 0.5 V, V_{CCB} = 2.7 V TO 3.6 V MIN	MAX	UNIT
t_{PHL}	A	B	1	6.3	ns
t_{PLH}			1	6.7	
t_{PHL}	B	A	1	6.1	ns
t_{PLH}			1	5	
t_{PZL}	$\overline{OE}$	A	1	9	ns
t_{PZH}			1	8.1	
t_{PZL}	$\overline{OE}$	B	1	8.8	ns
t_{PZH}			1	9.8	
t_{PLZ}	$\overline{OE}$	A	1	7	ns
t_{PHZ}			1	5.8	
t_{PLZ}	$\overline{OE}$	B	1	7.7	ns
t_{PHZ}			1	7.8	

operating characteristics, V_{CCA} = 4.5 V to 5.5 V, V_{CCB} = 2.7 V to 3.6 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 0, f = 10 MHz	39.5	pF
		Outputs disabled		5	

power-up considerations†

TI level-translation devices offer an opportunity for successful mixed-voltage signal design. A proper power-up sequence always should be followed to avoid excessive supply current, bus contention, oscillations, or other anomalies caused by improperly biased device pins. Take these precautions to guard against such power-up problems.

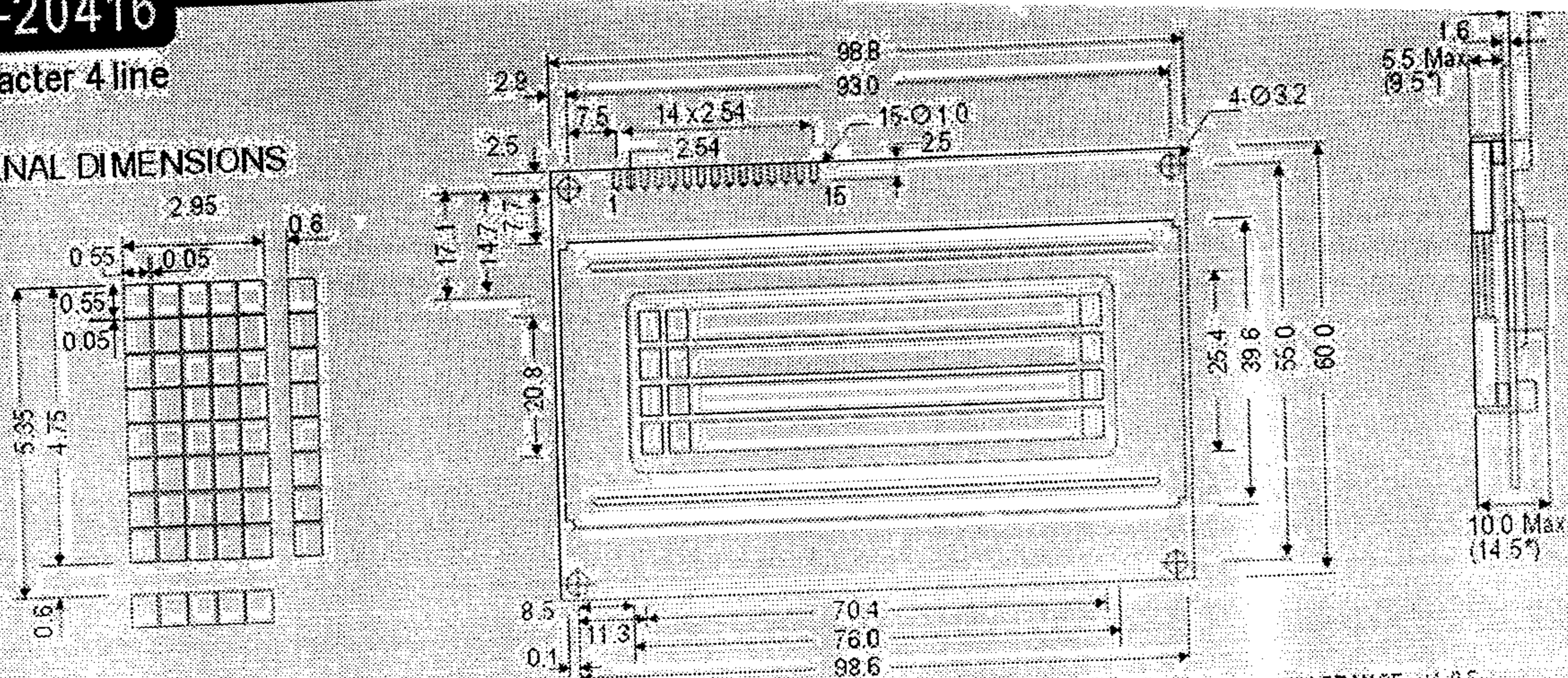
1. Connect ground before any supply voltage is applied.
2. Next, power up the control side of the device (V_{CCA} for all four of these devices).
3. Tie $\overline{OE}$ to V_{CCA} with a pullup resistor so that it ramps with V_{CCA}.
4. Depending on the direction of the data path, DIR can be high or low. If DIR high is needed (A data to B bus), ramp it with V_{CCA}. Otherwise, keep DIR low.

† Refer to the TI application report, *Texas Instruments Voltage-Level-Translation Devices*, literature number SCEA021.

ODM-20416

20 Character 4 line

EXTERNAL DIMENSIONS



DISPLAY PATTERN DIMENSIONS

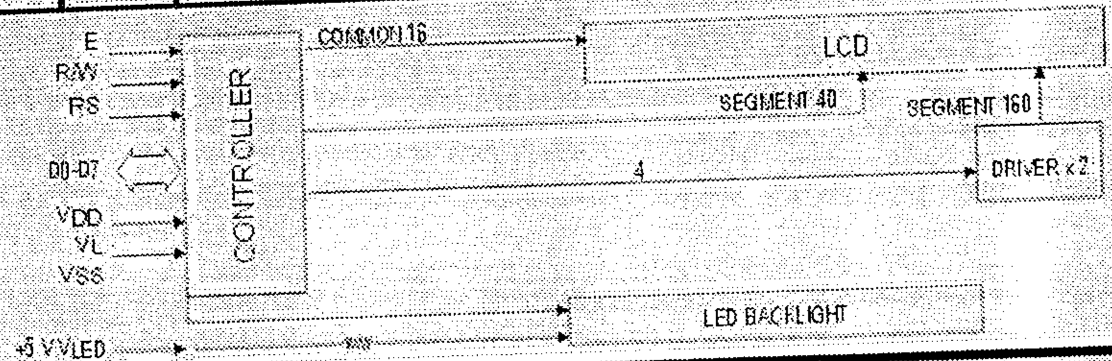
Specification marked * pertains to Backlight Version

GENERAL TOLERANCE +/-0.5

UNIT : mm

BLOCK DIAGRAM

PIN NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
SYMBOL	VSS	VDD	VL	RS	R/W	E	D0	D1	D2	D3	D4	D5	D6	D7	+VLED



ev. No. 01/2K1/01/JN

Table 6 : Instruction Table

Instruction	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	Description	Execution time (max) (when fcp or fosc is 250 kHz)
Clear Display	0	0	0	0	0	0	0	0	0	1	Clears entire display and returns cursor to home position. (Address 0)	1.64 ms
Return Home	0	0	0	0	0	0	0	0	1	*	Returns the cursor to the home position (Address 0). Also returns display being shifted to original position DD RAM contents remain unchanged.	1.64 ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	SH	Sets cursor move direction and specifies shift of display. These operations are performed during data write and read.	40 µs
Display ON/OFF Control	0	0	0	0	0	0	1	D	C	B	Sets ON/OFF of entire display (D), cursor ON/OFF (C) and blink of cursor position character (B)	40 µs
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	*	*	Moves cursor and shifts display without changing DD RAM contents.	40 µs
Function Set	0	0	0	0	1	DL	N	F	*	*	Sets interface data length (DL), number of display lines (N) and character font (F)	40 µs
Set CG RAM Address	0	0	0	1	ACG						Sets CG RAM address. CG RAM data is sent and received after this setting.	40 µs
Set DD RAM Address	0	0	1	ADD							Sets DD RAM address. DD RAM data is sent and received after this setting.	40 µs
Read Busy Flag & Address	0	1	BF	AC							Reads Busy flag (BF) indicating internal operations are being performed and reads address counter contents.	0 µs
Write Data to CG or DD RAM	1	0	Write data								Writes data into DD RAM or CG RAM	40 µs
Read Data from CG or DD RAM	1	1	Read Data								Reads data from DD RAM or CG RAM	40 µs

I/D = 1 : Increment
I/D = 0 : Decrement
SH = 1 : Accompanies display shift
S/C = 1 : Display shift
S/C = 0 : Cursor move
R/L = 1 : Shift to the right
R/L = 0 : Shift to the left
DL = 1 : 8 Bits, DL = 0 : 4 Bits
N = 1 : 2 Lines, N = 0 : 1 Lines
F = 1 : 5 x 10 Dots, F = 0 : 5 x 7 Dots
BF = 1 : Internally operating
BF = 0 : Can accept instruction

DD RAM : Display data RAM
CG RAM : Character generator RAM
ACG : CG RAM address
ADD : DD RAM address corresponds to cursor address
AC : Address counter used for both DD and CG RAM address

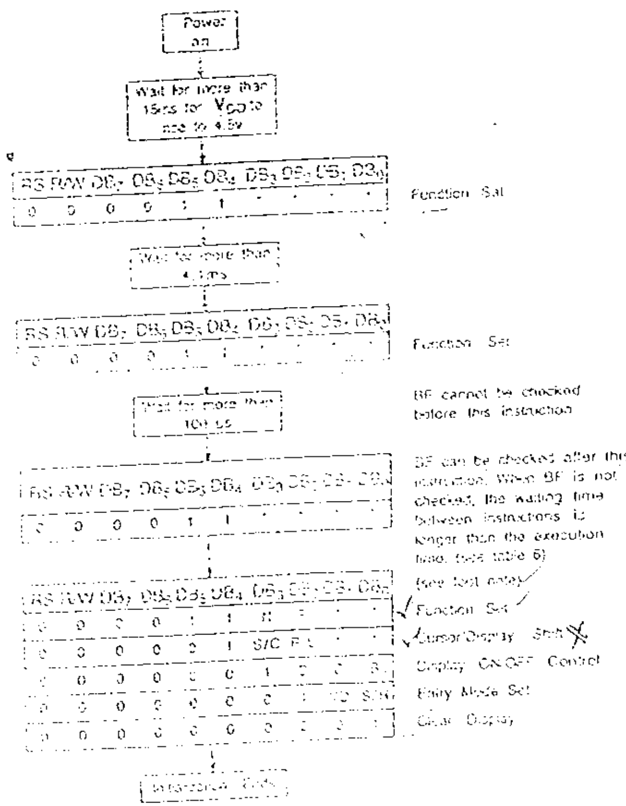
Execution time changes when frequency changes. [illegible]

* No effect

11.1 INITIALIZING BY INSTRUCTIONS

If the power supply conditions for correctly operating the internal reset circuit are not met, or if the function set is required to be modified, then initializing by instruction code is necessary. Following procedure should be adopted for initialization:

1. When the interface is 8-bits long :



[illegible]

Table 5 : Font Table for 5 x 10 Dot Characters

Lower 4 Bits \ Higher 4 Bits	0000	0010	0011	0100	0101	0110	0111	1010	1011	1100	1101	1110	1111
0000	CG RAM (0)		0	@	P	`	p		ー	タ	ミ	α	p
0001	(1)	!	1	A	Q	a	q	。	ア	チ	ム	ä	q
0010	(2)	"	2	B	R	b	r	「	イ	ツ	メ	β	θ
0011	(3)	#	3	C	S	c	s	」	ウ	テ	モ	ε	∞
0100	(4)	$	4	D	T	d	t	、	エ	ト	ヤ	μ	Ω
0101	(5)	%	5	E	U	e	u	・	オ	ナ	ユ	σ	ü
0110	(6)	&	6	F	V	f	v	ヲ	カ	ニ	ヨ	ρ	Σ
0111	(7)	'	7	G	W	g	w	ァ	キ	ヌ	ラ	g	π
1000	(0)	(	8	H	X	h	x	ィ	ク	ネ	リ	√	x̄
1001	(1)	)	9	I	Y	i	y	ゥ	ケ	ノ	ル	⁻¹	y
1010	(2)	*	:	J	Z	j	z	ェ	コ	ハ	レ	j	千
1011	(3)	+	;	K	[	k	{	ォ	サ	ヒ	ロ	ˣ	万
1100	(4)	,	<	L	¥	l	|	ャ	シ	フ	ワ	¢	円
1101	(5)	-	=	M	]	m	}	ュ	ス	ヘ	ン	£	÷
1110	(6)	.	>	N	^	n	→	ョ	セ	ホ	゛	ñ	
1111	(7)	/	?	O	_	o	←	ッ	ソ	マ	゜	ö	█

NOTE :CGRAM is a CHARACTER GENERATOR RAM having a storage function of character pattern which enable to change freely by users program. When line setting at initialization is 2 lines (N = 1), pattern becomes 5 x 7 dots.

ORIOLE DISPLAY MODULE

Table 4 : Font Table For 5 x 7 Dot Characters.

Lower 4 Bits \ Higher 4 Bits	0000	0010	0011	0100	0101	0110	0111	1010	1011	1100	1101	1110	1111
0000	CG RAM (0)		0	@	P	`	p		ー	タ	ミ	α	p
0001	(1)	!	1	A	Q	a	q	。	ア	チ	ム	ä	q
0010	(2)	"	2	B	R	b	r	「	イ	ツ	メ	β	θ
0011	(3)	#	3	C	S	c	s	」	ウ	テ	モ	ε	∞
0100	(4)	$	4	D	T	d	t	、	エ	ト	ヤ	μ	Ω
0101	(5)	%	5	E	U	e	u	・	オ	ナ	ユ	σ	ü
0110	(6)	&	6	F	V	f	v	ヲ	カ	ニ	ヨ	ρ	Σ
0111	(7)	'	7	G	W	g	w	ァ	キ	ヌ	ラ	g	π
1000	(0)	(	8	H	X	h	x	ィ	ク	ネ	リ	√	x̄
1001	(1)	)	9	I	Y	i	y	ゥ	ケ	ノ	ル	⁻¹	y
1010	(2)	*	:	J	Z	j	z	ェ	コ	ハ	レ	j	千
1011	(3)	+	;	K	[	k	{	ォ	サ	ヒ	ロ	ˣ	万
1100	(4)	,	<	L	¥	l	|	ャ	シ	フ	ワ	¢	円
1101	(5)	-	=	M	]	m	}	ュ	ス	ヘ	ン	£	÷
1110	(6)	.	>	N	^	n	→	ョ	セ	ホ	゛	ñ	
1111	(7)	/	?	O	_	o	←	ッ	ソ	マ	゜	ö	█

NOTE : CGRAM is a CHARACTER GENERATOR RAM having a storage function of character pattern which enable to change freely by users program.