Programmable Controller

Project Report

P-141

Submitted in Partial fulfilment of the requirements for the award of the Degree of Bachelor of Engineering in Electrical & Electronics Engineering of the Eharathiar University Coimbatore-641 046

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Certificate

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In partial fulfilment for the award of Bachelor of Engineering in the Electrical and Electronics Engineering Branch of the Bharathiyar University Coimbatore-641 046 during the acadamic **year 1991-92**.

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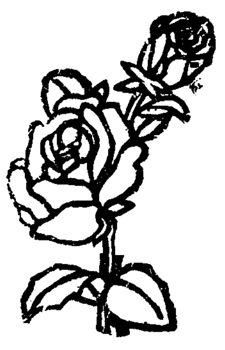

Acknowledgement

A C K N O W L E D G E M E N T

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S Y N O P S I S

Controlling of Ac and Dc loads is achieved by programmable controller. It can be programmed by the use of thumb wheel switches. The programmed value can also be varied by varying the pulse width (ON-OFF time) or frequency of the astable multivibrator which is used as timer.

The processor chip ICM 7217, which has got the special features of up/down counter & seven segment display driver will count the no. of pulses produced by the astable multivibrator. When the no. of pulses triggered is equal to the programmed value, the counter will reset automatically.

The relay is energised as soon as the counter and programmed values are equal. Thus the load is controlled.

This project aims at design, fabrication and testing of a programmable controller. Test results are presented in this report.

C O N T E N T S

INTRODUCTION

Generlaly speaking electronics can assist the engineer in industry in the solution of two fundamental types of problem viz. the transformation of electrical energy and the execution of process analogues for functions, such as measuring, counting, sorting etc. By the combination of the above two applications, various types of energy transformation and their control are possible. Here it is proposed to control the loads using counters.

1.1. PROGRAMMABLE CONTROLLER

PRPM controller consists of

1. Processor unit
2. Decimal to BCD converter
3. Switching units
4. Pulse generating units
5. Display
6. Relay section

The block diagram of the programmable controller is shown in fig. 1.1.

1.1.1. PROCESSOR UNIT

The processor unit consists of the main IC - ICM 7217 IJI CMOS IC. This is a four digit presettable up/down counters, each with an on board presettable register continuosly compared to the counter.

1.1.2. DECIMAL TO BCD CONVERTER

Decimal to BCD converter consist of Thumb wheel switches. It will produce BCD outputs. This value (BCD) is applied to the input of the processor unit. Thumb wheel switch sets value from 0 to 9, cascade of four thumb wheel switches set 0000 to 9999.

1.1.3. SWITCHING UNIT

This block consists of reset control and register control. At the end of the counted value, the system will reset automatically. In the mean time if there is any need for resetting the values, the reset switch can be operated manually. It provides negative signal to the 14th terminal of processor IC through PNP transistor driver unit. The register switch is used to program the values in the thumb wheel switches to the main IC - ICM 7271 IJI.

1.1.4. PULSE GENERATING CIRCUIT

Pulses are generated by astable multivibrator. This pulse signal frequency is varied up on varying the values of RA, RB & C. Astable multivibrator can be designed using 555 Timer IC. This triggering signal is applied to the 8th Terminal of the ICM 7217 IJI.

1.1.5. DISPLAY UNIT

This block consist of 4 seven segment LED display connected incommon anode mode. We can note down the counted values on the LED display. LED display is operated on a multiplexed mode by the main processor IC.

1.1.6. RELAY SECTION

Relay consists of 5 terminals. 2 terminals for coil winding, One terminal is normally opened, one is normally closed and another one is common. The relay controls both ac and dc for programming value.

1.2 WORKING PRINCIPLE

The thumb wheel switch is internally available for decimal to BCD converter circuit. This BCD signal is applied to the BCD input of the programmable up/down counter IC (ICM 7217 IJI). Thus the BCD signal is programmed in the processor IC.

The input pulse applied to this ircuit is produced by 555 timer, which will act as astable multivibrator. When the programmed value (Thumb wheel switch readings) and the total number of applied pulses are equal. The processor IC will produce $\overline{\text{equal}}$ signal and $\overline{\text{zero}}$ signal. The $\overline{\text{zero}}$ signal is applied to the relay coil through driver unit. The driver unit is constructed by transisters SL100 & BC107. Now the relay is energised by $\overline{\text{zero}}$ signal and the load state is changed (NPN Transisters).

The $\overline{\text{equal}}$ signal is applied to the $\overline{\text{reset}}$ (14th) terminal of the IC ICM 7217 IJI. The $\overline{\text{equal}}$ signal resets the counter. Thus the counter has been reset automatically. External reset control are also available. While programming the values the register switch must be pressed. Then the programmed value will be stored in the memory of the processor IC.

When the 10th terminal of the CMOS IC ICM 7217, IJI is connected to +5V, the counter will count upward. When it is given -5V supply, then the counter will count down ward. The circuit diagram is shown in fig. 1.2.

1.3 ELECTRONIC COUNTERS

Electronic counters are capable of making many measurements involving frequency, time, phase angle, radiation events and totalizing electric events.

The electronic counter normally employs a frequency divider circuit known as a scalar. A scalar produces a single pulse for every set of number of input pulse. For example a 2:1 scalar produces one output pulse for 2 input pulses. A scalar is essentially a frequency divisor. The basic of counters is frequency division. This is done by a 2:1 scalar called a bistable multivibrator or a flip-flop (FF) circuit.

R.S. FLIP-FLOP

A flip-flop is a bistable multivibrator which has an output which is either a high or a low voltage. The low voltage output is called 0 and the high voltage is called 1. Thus a flip flop has two stable states, either 0 or 1. The output stays in its original state either 0 or 1. Unless the circuit is driven by an input called trigger. On application of trigger, the output changes its state. Thus if a trigger is applied when output is in 1 state, it changes to 0 state while if the output is in 0 state, it changes to 1 state. It should be understood that in a bistable multivibrator the output continuous to be in its original state indefinitely unless triggered. Therefore it can be said that a flip-flop has a memory fig. 1.5 shows an R.S. flip-flop.

There are two similar transistors Q1 and Q2. They are NPN type. The collector of each transistor is cross coupled to the base of the transistor. The cross coupling between collector and base results in a positive feed back. If Q1 is conducting there is a large voltage drop in resistance R1 and therefore Q1 is saturated and voltage VCE and Y is only about 0.1V. This voltage is applied to the base of transistor Q2 and is required a voltage of VBE = 0.7V (assuming that both Q1 and Q2 are silicon transistors). Thus transistor Q2 is cut off. Under these conditions output $\overline{Y}$ = 0 and Y = 1.

Similarly if by some means we get transistor Q2 to conduct there will be large voltage drop across resistor R2 and therefore the transistor Q2 gets saturated. The potential at Y becomes 0.1V forcing the transistor Q1 to cut off. Hence under these conditions $\overline{Y}$ = 1 and Y = 0.

Hence there are two stable states for the flip-flop and these are,

(i) $\overline{Y}$ = 1 and Y = 0

(ii) $\overline{Y}$ = 0 and Y = 1

In order to control the flip-flop, trigger inputs are applied. If a positive going pulse is applied to the S (set) input terminal, then Q1 conducts heavily (gets saturated) and Q2 is cut off. Similarly when a positive going pulse is applied to R (reset) input temrinal Q2 gets saturated and Q1 is cut off.

Thus application of a positive going pulse to S input terminal is called setting the flip-flop and result in a binary output where Y = 1 and Y = 0. Application of a positive going pulse to the R input terminal is called Resetting of the flip-flop and results in a binary output where Y = 0 and Y = 1.

The truth table for an R.S. flip-flop is:

R	S	Y
0	0	Last Value
0	1	1
1	0	0

The input condition R = 1 and S = 1 is for bidden as it means that we are trying to get Y = 1 and Y = 0 simultaneously which makes no sense the logic symbol for a R.S flip-flop is shown in figure 1.6.

T AND RST FLIP-FLOP

Fig. 1.7 shows a toggle (T) flip-flop. A train of narrow pulse is applied to the T input terminal. This circuit uses two and gates and a R.S flip-flop. Every time a pulse is applied, the output of the flip-flop changes state. Suppose Y = 0 and $\overline{Y}$ = 1 just before the pulse A is applied to terminal T. on application of this pulse the inputs to the top and gate are 1 and 1 and therefore the top gate is enabled (opened).

A pulse is applied to terminals. On the other hand the two inputs to bottom and gate are 1 and 0 and is thus disabled (closed) and no intput is applied to terminal R.

Hence the flip-flop is set or Y = 1 and $\overline{Y}$ = 0 when the next pulse B is applied to terminal T, the input to the top gate is 1 and 0 (since $\overline{Y}$ = 0) and hence it is disabled. Therefore no pulse is applied to terminal S. On the other hand the bottom and gate is enabled as the two inputs to it are 1 as Y = 1 and therefore a pulse is applied to terminal R. This resets the flip-flop resulting in Y = 0 and $\overline{Y}$ = 1.

Thus each incoming positive pulse is alternately stored into the set and reset inputs, and hence the flip-flop toggles ie. alternately sets and resets producing 1 or 0 states at the output. Therefore two input pulses produce one output pulse. This means that the frequency of the output is half of that of the input. Thus a T flip-flop acts as a frequency divisor which divides the input frequency by two.

We have till now considered flip-flops which respond to positive going pulse. However many a designs are possible for a T flip-flop. For example it is possible to build a T flip-flop that responds to a negative going pulse. Hence, onwards we will discuss T flip-flop which responds to negative edge of a square wave. Fig. 1.8 shows a T flip-flop. The flip-flop changes its state only on the negative edge of the input signal.

A RST flip-flop combines an R.S. flip-flop and a T flip-flop. It can set, reset (or) toggle. The most important flip-flop is the one which sets or reset to positive going R and S input and toggles for negative going inputs. The symbol for an RST flip-flop is shown in fig. 1.9.

INPUTS	SETS/RESETS/TOGGLES	FINAL STATE
+Ve to S	Sets	Y = 1, $\bar{Y}$ = 0
+Ve to R	Resets	Y = 0, $\bar{Y}$ = 1
-Ve to T	Toggles	Switches from 1 to 0 and 0 to 1

DECADE COUNTER

Four flip-flop can be in cascade to act as counters for the input pulses. A decade counter uses four RST flip-flops. A, B, C, D Fig. 1.10 shows four RST flip-flop in cascade. A square wave is input to the counters. This square wave is called a 'clock'. The output from flip-flop A, drives the flip-flop B. The outpt of flip-flop B, drives flip-flop C which in turn drives flip-flop D.

To start the operation, all the flip-flop, are reset and therefore the states of four R.S flip-flop are

DCBA = 0000 and $\overline{DCBA}$ = 1111 when the first clock pulse is applied to T input terminal of RS flip-flop A, it changes its state on the negative going edge of the pulse. Thus at the end of the first pulse the state of the flip-flop is

$$DCBA = 0001 \quad \text{and} \quad \overline{DCBA} = 1110$$

The two inputs to the and gate are A and D and both are 1 state, therefore the and gate is enabled (opened). A positive going pulse is applied to the T terminal of B flip-flop and therefore it does not changes its state. It remains at 0 state and so do C and D flip-flop. On the application of 2nd pulse, A goes from 1 to 0. Since the and gate is open, a negative going pulse is applied to B flip-flop. This changes the state of flip-flop B. It changes from 0 to 1. Therefore a positive going pulse is applied to flip-flop 'C' and it remain in its original state and so does flip-flop D.

The states at the end of 2nd pulse are

$$DCBA = 0010 \quad \text{and} \quad \overline{DCBA} = 1101$$

This disables (closes) the and gate since A = 0, $\overline{D}$ = 1. On application of the third pulse, flip-flop A changes its state from 0 to 1. Since the and gate is closed no pulse are applied to flip-flops B, C and D and their states remain unchanged. Thus at the end of third pulse, the states are

$$DCBA - 0011 \text{ and } \overline{DCBA} = 1100$$

The and gate is disabled (closed) on the application of 5th pulse, Flip-flop A changes its state from 0 to 1. Since the and is closed no pulse is applied to flip-flop A, B, C, D and they therefore remain in their original state. Thus at the end of 5th pulse the state of the flip-flops are;

$$DCBA = 0101 \text{ and } \overline{DCBA} = 1010$$

This means that the and gate is enabled (open) again. On the application of 6th pulse, flip-flop A changes its states from 1 to 0. Since the and gate is open its output is applied to flip-flop B which does not change its state and so flip-flop C and D. Therefore at the end of 6th pulse the states of flip-flops are

$$DCBA = 0110 \text{ and } \overline{DCBA} = 1001$$

The and gate is closed as $A = 0$ and $\overline{D} = 1$

On the application of 7th pulse, flip-flop A changes its state from 0 to 1. As the and gate is closed and therefore flip-flops B, C and D remain in their original state. Hence, at the end of the 7th the pulse, states of flip-flops are;

$$DCBA = 0111 \text{ and } \overline{DCBA} = 1000$$

The and gate is open now as A = 1 and $\overline{D}$ = 1. On application of 8th pulse flip-flop A goes from 1 to 0. This applies a negative going pulse to flip-flop B which goes from 1 to 0.

The output from flip-flop B is applied to flip-flop C which also receives a negative going pulse and therefore it goes from 1 to 0. So a negative going pulse is applied to flip-flop D changing its state from 0 to 1. The states at the end of 8th pulse are;

$$DCBA = 1000 \text{ and } \overline{DCBA} = 0111$$

Since the inputs to the and gate are A = 0 and $\overline{D}$ = 0 it is closed.

On the application of 9th pulse, A changes its state from 0 to 1. Since the gate is closed the other three flip-flops D, C, B remain in their original state. Hence at the end of 9th pulse, the states are;

$DCBA = 1001$ and $\overline{DCBA} = 0110$

The and gate is closed as A = 1 and $\overline{D} = 0$. On application of 10th pulse, A changes its state from 1 to 0. Since the gate is closed no pulse is applied to flip-flops B and C and they remain intheir original state. A changes from 0 to 1. This positive pulse is applied to R terminal of flip-flop D which resets it self. It was in 1 state and therefore comes to 0 state.

Thus at the end of 10th pulse, the states are

$DBCA = 0000$ and $\overline{DBCA} = 1111$

The counting now can start all over again. Thus we get one output pulse for ten input pulses.

Hence a decade counter acts as a decade frequency divider since it divides the frequency by 10 therefore it is called a decade dividing assembly (DDA).

1.4 REGISTERS

Registers are often used to momentarily store binary information appearing at the output of an encoding matrix. A register might be used to accept input data from an alpha numeric key board and then present this data at the input of a microprocessor chip. For instance, a register could be used to accept output data from a microprocessor chip and then present this data to the circuitry used to drive the display on a CRT screen. Thus registers form a very important link between the main digital system and the input-output channels. A binary registers also forms the basis for some very important arithmetic operations.

A register is simply a group of flip-flops that can be used to store a binary number. There must be one flip-flop for each bit in the binary number. For instance a register used to store an 8-bit binary number must have eight flip-flops. Naturally the flip-flops must be connected such that the binary number can be entered (shifted) into the register and possibly shifted out.

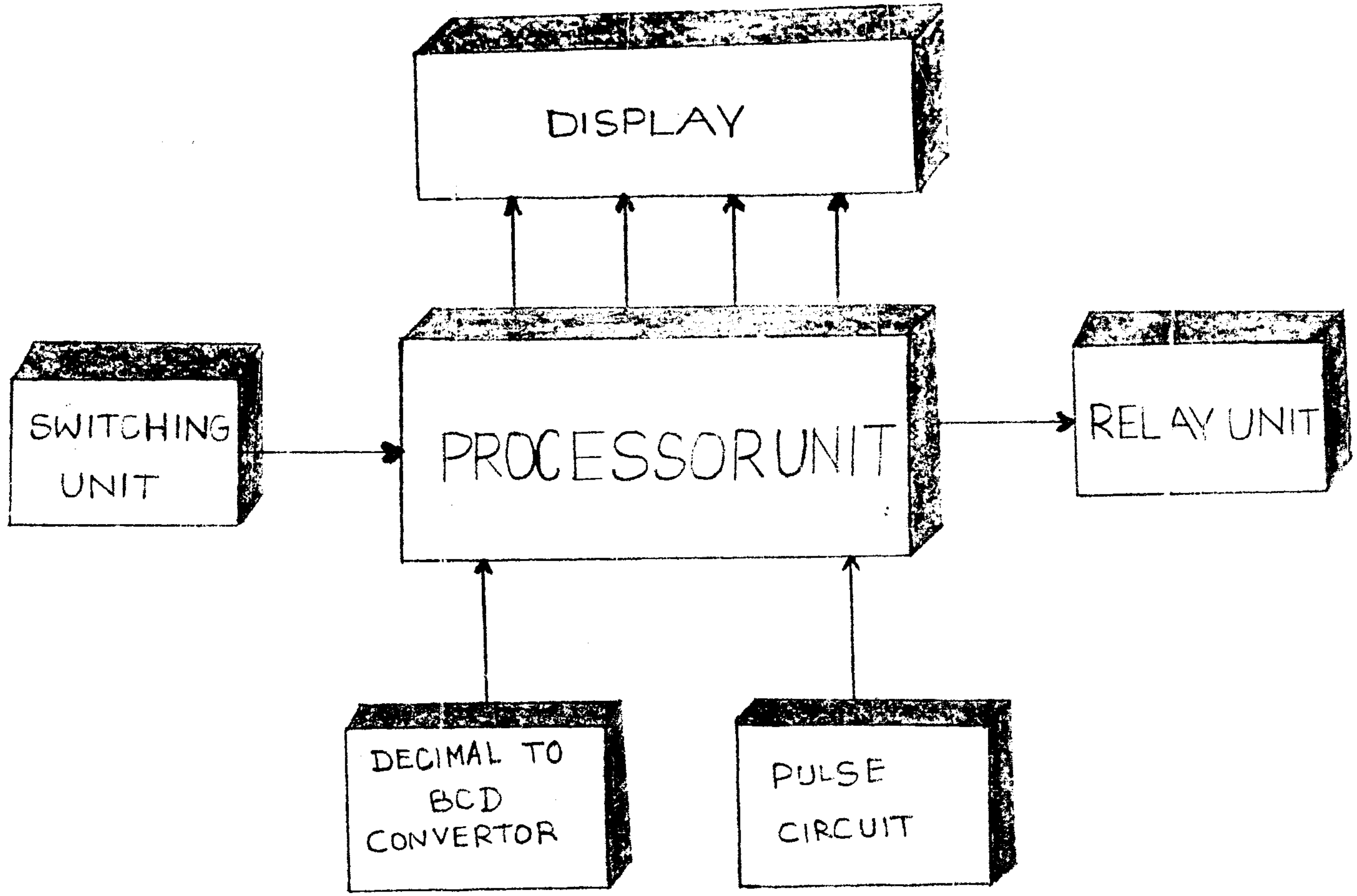


fig 1.1
BLOCK DIAGRAM

circuit diagram

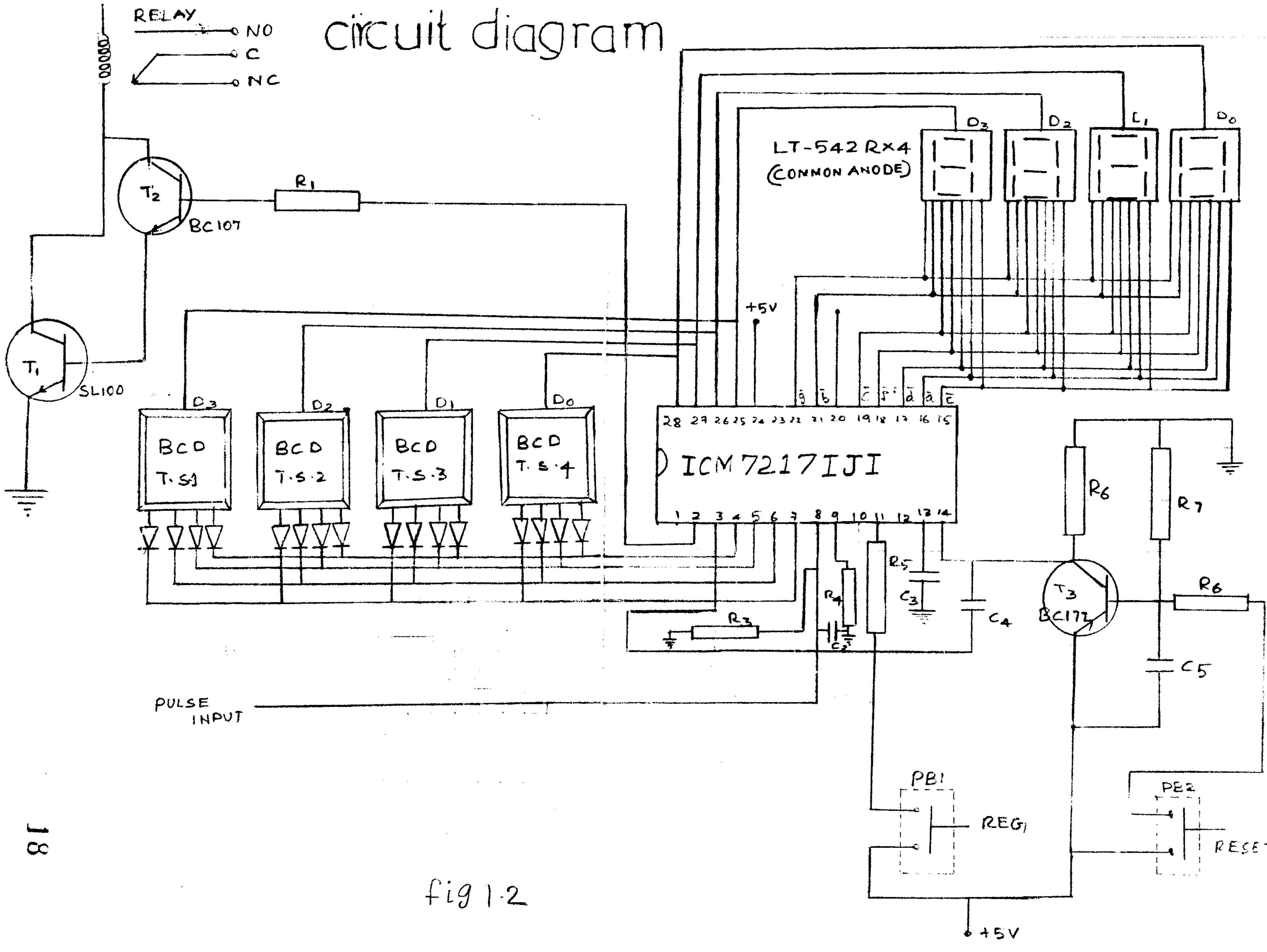


fig 1·2

RESET DRIVER UNIT

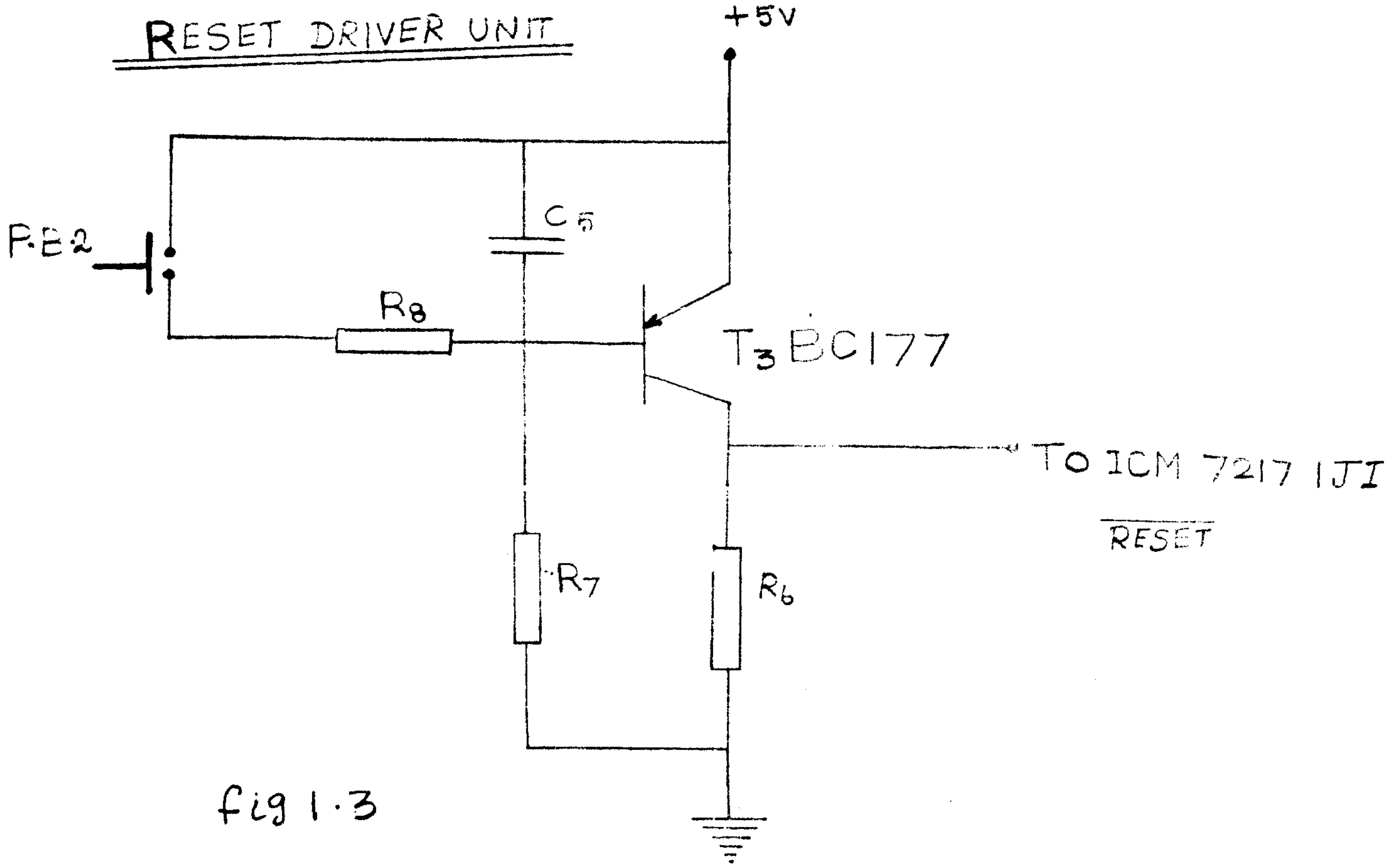


fig 1.3

RELAY DRIVER UNIT

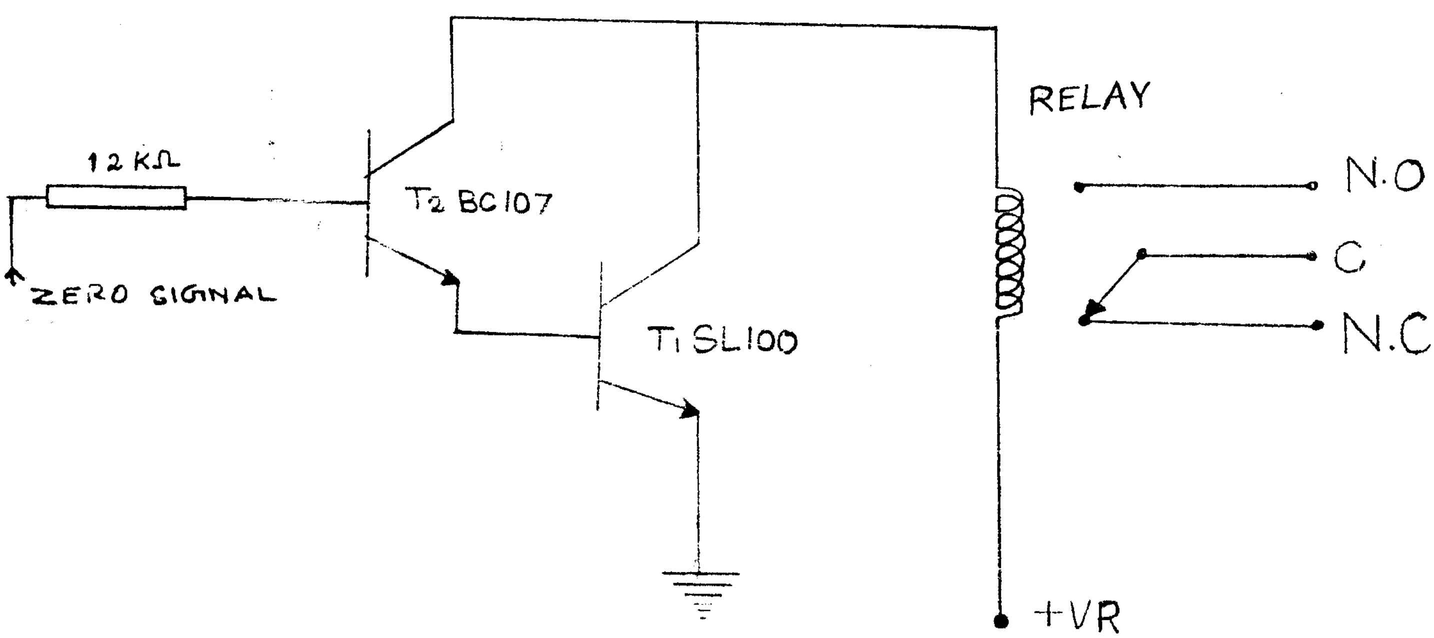


fig 1.4

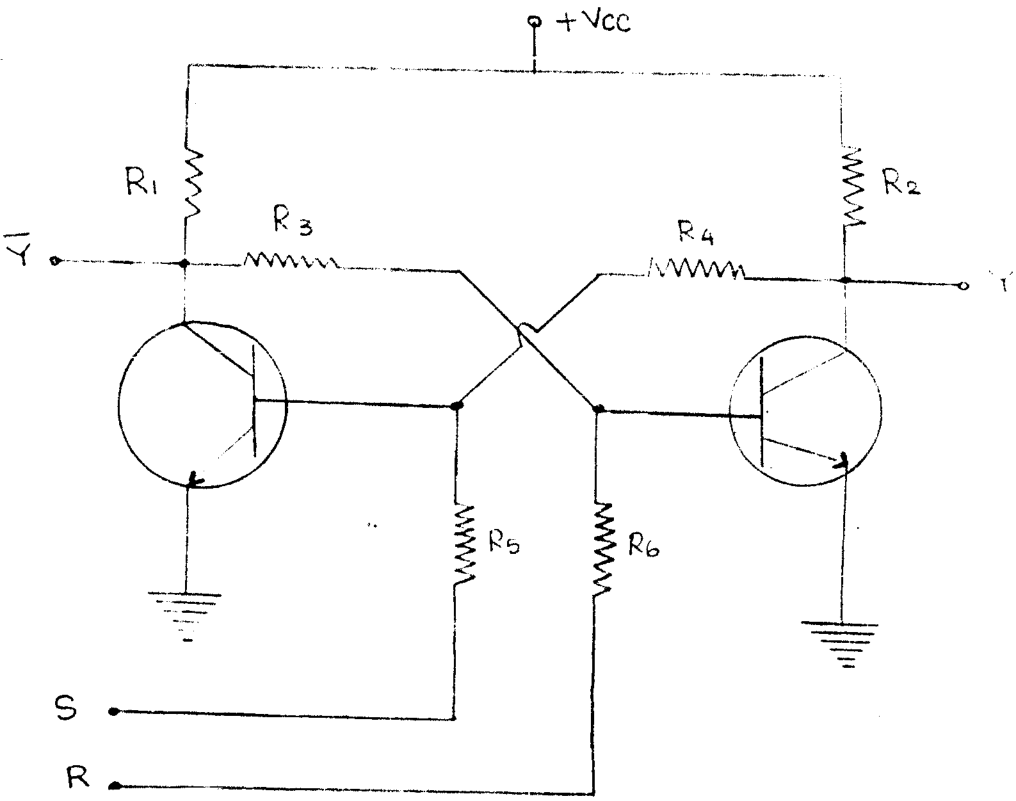


fig 1·5 RS FLIP-FLOP(BISTABLE MULTIVIBRATOR)

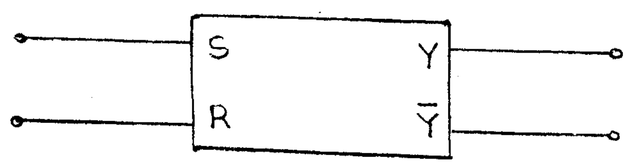


fig 1·6: LOGIC SYMBOL FOR RS FLIP-FLOP

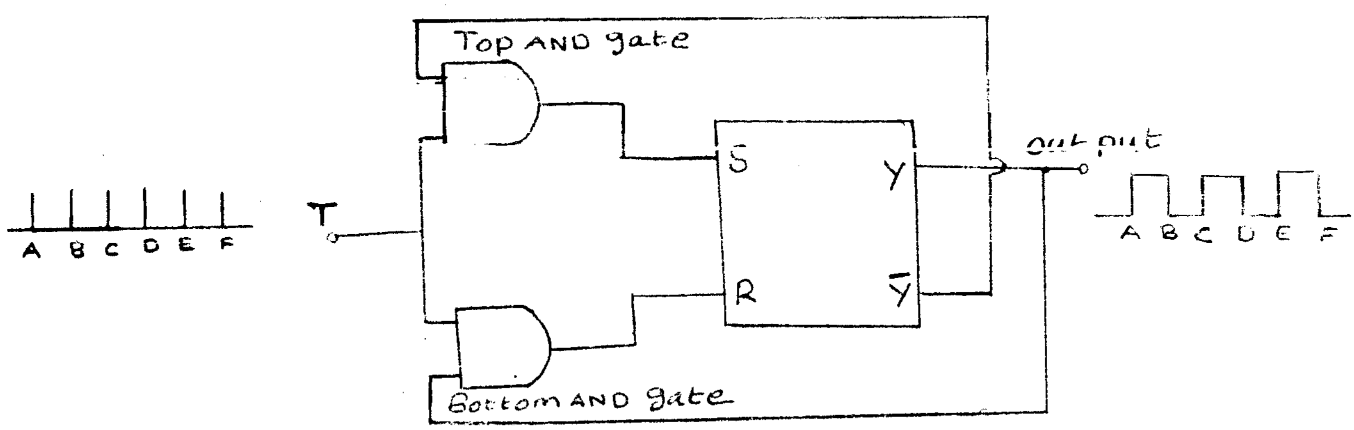


fig 1·7: T-flip flop

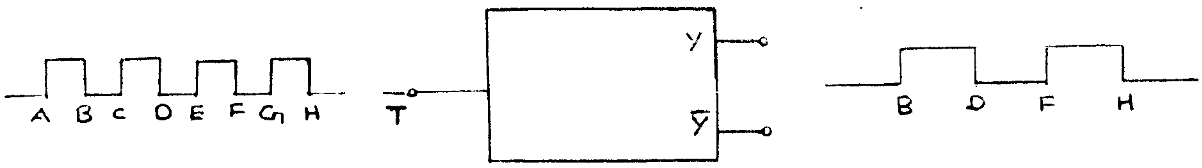


fig 1.8. T flip-flop

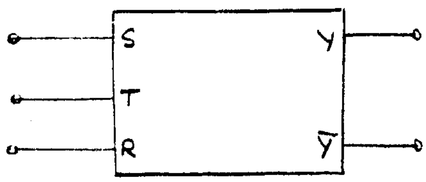


fig 1.9: RST flip-flop

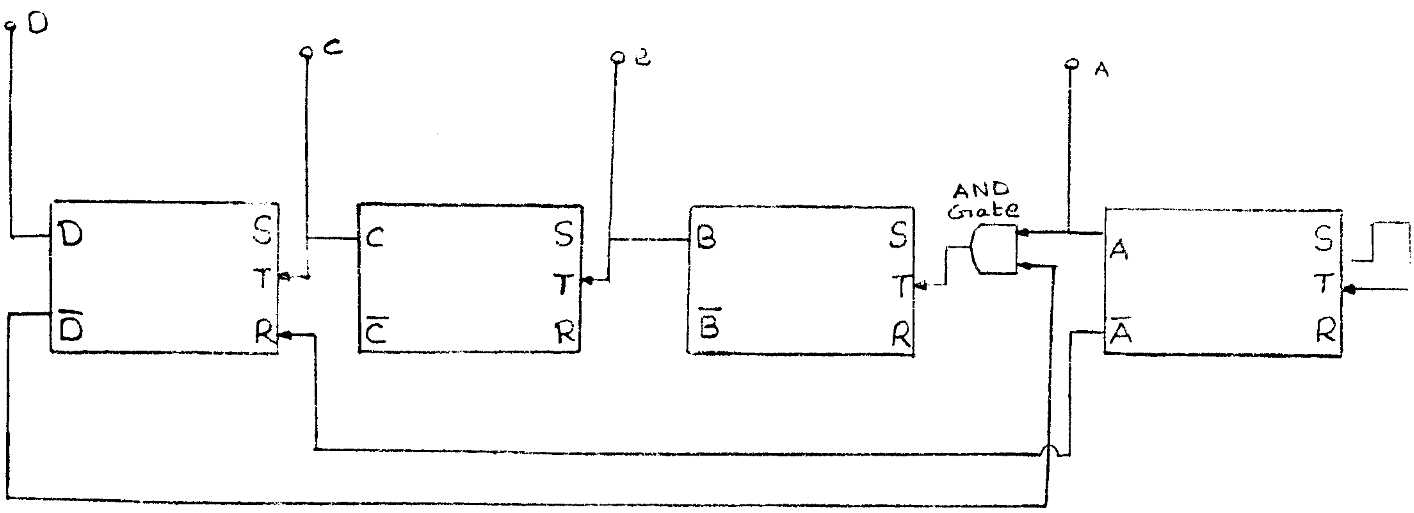


fig 1.10 A decade counter

ASTABLE MULTIVIBRATOR

2.1 OPERATION OF ASTABLE MULTIVIBRATOR

The multivibrator is one form of relaxation oscillator. Multivibrators may be self excited (also called free running), requiring no external excitation. Or they may be driven oscillators whose operation and frequency are controlled by external driving or triggering voltages. Free running multivibrators are called astable. The frequency of astable multivibrators may be controlled by external synchronizing pulses.

Transistors may be used as the amplifying device for multivibrator circuits. Transistor multivibrators are either collector coupled or emitter coupled.

The properties of transistors which explain multivibrator action are as follows:

1. An increase in base current causes an increase in collector current, and conversely a decrease in base current causes a decrease in collector current.

2. An increase in forward bias in the base-emitter junction increases base current, a decrease in forward bias reduces base current.

3. In a PNP transistor, forward bias is increased in the base emitter junction as the base is driven more negative relative to the emitter. However, a point may be reached where a further increase in bias will not result in an increase in collector current. At that bias level, collector saturation has been reached.

4. In an NPN transistor forward bias in the base emitter junction is increased by driving the base more positive relative to the emitter.

5. An increase in collector current flowing in the collector load resistor causes the voltage at the collector to decrease. Therefore an increase in collector current in an NPN transistor will cause the collector voltage to go more negative while an increase in collector current in a PNP transistor will cause the collector voltage to go more positive.

6. A decrease in current in the collector load reistor will cause the voltage at the collector to increase. Therefore a decrease in collector current in an NPN transistor will cause the collector voltage to go more positive, while in a PNP transistor the collector voltage will go more negative.

7. The voltage across a capacitor cannot change instantanecoulsy, that is, it takes time to charge or discharge a capacitor. A measure of this time is called the time constant. In an RC circuit, one time constant in seconds is equal to the product of the resistance R (through which the capacitor is charging or discharging) in ohms times the capance C in farads. Ohms times microfarads, of course, yields microseconds.

OPERATION OF COLLECTOR COUPLED MULTIVIBRATOR

Figure 2.1 is the circuit of a collector coupled multivibrator. Q1 and Q2 are NPN transistors whose collectors are connected to the positive voltage source Vcc through load resistors RL1 and RL2 respectively. The bases of Q1 and Q2 are biased, respectively, by resistors R1 and R2. Any change in voltage at the collector of Q1 is coupled by C1 to the base of Q2 and similarly any voltage change at the collector of Q2 is coupled by C2 to the base of Q1. It will be shown that C1 and C2 provide regenerative feedback to sustain oscillation in this RC coupled oscillator.

To analyze circuit operation let us assume that the two circuits are symmetrical that is Q1 and Q2 are the same type transistor. RL1 = RL2, R1 = R2 and C1 = C2. When switch S1 is closed, power is applied to both transistors. Current starts to flow in the collectors of Q1 and Q2. Since it is not conceivable that both transistors draw exactly the same amount of current, assume that the collector of Q1 draws more current than that of Q2. Therefore the voltage at the collector of Q1 will go more negative than the collector voltage of Q2. This negative voltage change of Q1 will be coupled by C1 to the base of Q2, reducing the forward bias on Q2. Accordingly collector current in Q2 will decrease, and the collector voltages of Q2 will go more positive. This positive change is coupled by C2 to the base of Q1, increasing Q1 base current and collector current. The voltage at the collector of Q1 will go more negative, driving the base of Q2 more negative, reducing Q2 collector current further, thus driving the collector voltage of Q2 even more positive. In very short order this regnerative feedback from the collector of one transistor to the base of the next will cause Q1 collector current to reach saturation while Q2 collector current is cut off. We say that Q1 is ON and Q2 is OFF. The action is practically instantaneous.

How long does Q1 remain ON and Q2 OFF? The time constant C1R2 (approximately) determines this. Let us see how. Assume (1) that Vcc = +10V and (2) that, after power is applied and Q1 saturates the collector voltage. Vc1 of Q1 drops practically to 0 that is the collector to emitter resistance of Q1 approaches 0. This 10V battery to C1 and at the instant of change of circuit to C1 "looks" like that in fig. 2.2 (c). Since the voltage across C1 cannot change instantaneously, the entire 20V must appear across R2 and the voltage with respect to ground at the junction of C1 and R2 (point B2, the base of Q2) must measure -10V, cutting off Q2 Capacitor C1 starts discharging through the emitter collector reistance of Q1 and through R2 toward Vcc (see fig 2.2 (a). Since the emitter collector resistance of Q1 saturated is very low, the effective discharge time constant for C1 is R2 x C1. The voltage VB2 at the base of Q2 will changes as C1 discharges, in the manner shown in fig. 2.3.

When the voltage at the base of Q2 has increased from -10V to 0V to a low value of positive voltage, Q2 is brought out of cutoff to conduction. Q2 base currnt and collector current start to flow. The voltage VC2 at the collector of Q2 drops, and this negative voltage change is coupled by C2 to the base of Q1, reducing base current and collector current in Q1. As collector current in Q1 reduced, the collector voltage of Q1, VC1 rises. Thispositive change at the collector of Q1 is coupled by C1 to the base of Q2, increasing Q2 base and collector current. Collector voltage at Q2 goes more negative, driving the base of Q1 more negative. Again almost instantaneously, as Q2 starts conducting, the regenerative feedback action turns Q2 ON and turns Q1 OFF. Q2 remains ON as long as Q1 is OFF. The length of time Q1 remains OFF is determined by the C2R1 time constant, for the voltage VB1 at the base of Q1 is determined by the discharge of C2 through the emitter collector resistance of Q2 and through R1 as in Fig. 2-2b and 2-3.

When Q1 starts to conduct, it switches Q2 OFF. When Q2 starts to conduct it switches Q1 OFF. The length of time Q1 conducts is determined by the length of time Q2 is OFF (see waveform) VB2. Fig. 2.3. The length of time Q2 conducts is determined by the length of time Q1 is cut off (See VB1 Fig. 2.3).

The idealized waveforms in fig. 2.3. merit some discussion. We see that as the base voltage VB2 of Q2 is driven 10 V negative during the interval t1, the collector voltage VC2 of Q2 goes 10V positive, Vcc. We might expect that the voltage at the collector of Q2 would rise to vcc the moment Q2 is switched Off. However, this is not so, since capacitor C2 cannot charge up instantaneously to Vcc. Therefore VC2 rises to Vcc at the rate determined by the charge of C2 through RL2 in series with the emitter base resistance of Q1. See Fig. 2.4. for the charging path of C2. The exponential rise in voltage of VC2 represents the charge of C2. At the end of the time interval t1 when VB1 has risen from cut off to conduction, the voltage at the collector of Q2 drops from +Vcc to a very low value (close to 0). At that instant Q1 is switched OFF and the voltage VC1, at the collector of Q1 starts rising from 0 toward +Vcc. The exponential rise in VC1 is the result of C1 charging toward +Vcc through RL1. At the end of period t2, when VB1 has risen from -10V to a slight positive voltage, Q1 is switched ON and Q2 OFF, and the cycle is repeated.

It will be noted that the ON-OFF time of each transistor is equal, since the circuits are symmertical. That is the time duration of the positive and negative alternations of Q1 and Q2 are equal t1 = t2. The waveforms at the collectors of Q1 and Q2 are 180° out of phase. Similarly, the waveforms at the bases of Q1 and Q2 are 180° out of phase.

FREQUENCY OF COLLECTOR COUPLED MULTIVIBRATOR

The period of a complete cycle of the "square" wave at the collector of Q1 or Q2 is represented by the time interval AC (Fig.2.3) that is

$$t = t1 + t2 \qquad \ldots\ldots \qquad 1$$

The frequency f of the multivibrator is therefore the inverse of the period t, or

$$f = \frac{1}{t} = \frac{1}{t1 + t2} \quad \ldots \quad 2$$

We can approximate the time intervals t1 and t2 and thus arrive at an approximate equation for frequency.

$$f = \frac{1}{0.7\ C1R1 + 0.7\ C2R1} \quad \ldots \quad 3$$

The reason for Eq 3 becomes apparent when we examine fig. 2.2 & 2.3. The interval t1 is determined by the time it takes C1 to discharge through R2 from a level of -10 to 0V (approx). This is a change of 10 V, out of possible change of 20 V (note that C1 discharges from -10 toward +10V). This is a 50 percent change in charge. Reference to the universal chanrge and discharge time-constant chart, fig. 2.5 shows that a 50 percent charge of discharge requires 0.7 of time constant. Hence

$$t1 = 0.7\ C1R2$$

Similarly,

$$t2 = 0.7\ C2R1$$

2.2 THE 555 TIMER

FLIP FLOP REVIEW

Before discussing the 555 timer, we need to review the flip flop. fig. 2.6 shows a simplified version of the earlier flip-flop. Each collector drives the opposite base through a 100 kΩ resistor. On power up, the transistor with the higher β saturates and the other cuts off.

For instance, suppose the right hand transistor is saturated. Then its collector voltage is approximately 0 V. This means no base drive or the left hand transistor, so it goes into cutoff and its collector voltage approaches +15V. This high voltage produces more than enough base current in the right hand transistor to sustain its saturation. In other words, the overall circuit is latched or struck in this state, left hand transistor cutoff and right transistor saturated. In this case output Q is approximately 0 V.

The foregoing analysis works just as well as the other way. The left hand transistor canbe saturated, and the right hand transistor cut off. For this state, output Q is approximately 15 V.

Q can be either low or high, approximately 0 or 15 V. A circuit like this is called a memory element because it can store binary information. Computers use thousands of memory elements.

RS FLIP FLOP

Figure 2.7 shows one way to trigger a flip flop. A high set (S) input forces the left hand transistor to saturate if it is not already saturated. As soon as the left hand trnsistor saturates, the overall circuit lathes and

$$Q = 15 \text{ V}$$

A high S input therefore sets the output to 15 V. Here it remains, even though you later remove the S input.

A high reset (R) input drives the right hand transistor into saturation if it is not already saturated. Once this happens, the overall circuit remains latched even though you remove the R input. In this state,

$$Q = 0 \text{ V}$$

Figure 2.7 is an example of how to build an RS flip-flop a transistorized memory element with set and reset inputs. Q is the output. Incidentally, a complementary out Q is available from the collector of the left hand transistor. This may or may not be used depending on the application.

Figure 2.8 shows the schematic symbol for an RS flip-flop of any design. Whenever you see this symbol, remember the action. The circuit latches in either of two states. A high S input sets Q to high, a high R input resets Q to low. Output Q remains in a given state until triggered into the opposite state.

BASIC TIMING CONCEPT

Figure 2.9 (a) illustrates some basic ideas needed in our later discussion of the 555 timer. Assume output Q is high. This saturates the transistor and clamps the capacitor voltage at ground. In other words, the capacitor is shorted and cannot charge.

The noninverting input voltage of the op amp is called the thershold voltage, and the invertinginput voltage is referred to as the control voltage. With the RS flip-flop set, the saturated transistor holds the thershold voltage at 0. The control voltage, on the other hand, is fixed at +10V because of the voltage divider.

Suppose we apply a high voltage to the R input. This resets the RS flip-flop. Output Q goes to 0 and this cuts off the transistor. Capacitor C is now free to charge. As the capacitor charges, the threshold voltage increases.

Eventually the threshold voltage becomes slightly greater than the control voltage (+10V). The output of the op amp then goes high, forcing the RS flip-flop to set. The high Q output saturates the transistor and this quickly discharges the capacitor.

Notice the two waveforms in fig. 2.9 (b). An exponential rise is acros the capacitor, and a positive going pulse appears at the Q output.

555 BLOCK DIAGRAM

The NE555 timer introduced by Signetics is an 8-pin IC that can be connected to external components for either astable or monostable operation. Figure 2.10 shows a simplified block diagram. Notice the upper op amp has a threshold input (pin 6) and a control input (pin 5) In most applications, the control input is not used, so that the control voltage equals +2Vcc/3. As before, whenever the threshold voltage exceeds the control voltage, the high output from the op amp will set the flip-flop.

The collector of the discharge transistor goes to pin 7. When this pin is connected to an external timing capacitor, a high Q output from the flip-flop will saturate the transistor and discharge the capacitor. When Q is low, the transistor opens and the capacitor can charge as previously described.

The complementary signal out of the flip-flop goes to pin 3, the output. When the external reset (pin 4) is grounded, it inhibits the device (prevents it from working).

This on-off feature is useful sometimes. In most applications, however the external reset is not used and pin 4 is tied directly to the supply voltage.

Notice the lower op amp. Its inverting input is called the trigger (pin 2) Because of the voltage divider, the noninverting input has a fixed voltage of +Vcc/3. When the trigger input voltage is slightly less than +Vcc/3, the op amp output goes high and resets the flip-flop.

Finally pin 1 is the chip ground, while pin 8 is the supply pin. The 555 timer will work with any supply voltage between 4.5 and 16 V.

ASTABLE OPERATION

Figure 2.11 (a) shows the 555 timer connected for astable operation. When Q is low, the transistor is cut off and the capacitor is charging through a total resistance of RA + RB. Because of this, the charging time constant is (RA + RB)C. As the capacitor charges, the threshold voltage increases.

Eventually the threshold voltage exceeds +2Vcc/3; then the upper op amp has a high output and this sets the flip-flop. With Q high, the transistor saturates and grounds pin 7. Now the capacitor discharges through RB. Therefore, the discharging time constant is RbC. When the capacitor voltage drops slightly below +Vcc/3, the lower op amp has a high output and this resets the flip-flop.

Figure 3.11(b) illustrates the waveforms. As you see, the timing capacitor has an exponentially rising and falling voltage. The output is a rectangular wave. Since the charging time constant is longer than the discharging time constant, the output is not symmetrical, the high state lasts longer than the low state.

To specify how unsymmetrical the output is, we will use the duty cycle defined as

$$D = \frac{W}{T} \times 100\% \qquad \ldots\ldots \qquad 4$$

As an example, if W = 2ms and T = 2.5 ms, then the duty cycle is

$$D = \frac{2 \text{ ms}}{2.5 \text{ ms}} \times 100\% = 80\%$$

Depending on reistances RA and RB the duty cycle is between 50 and 100 percent.

A mathematical solution to the charging and discharging equations give the following formulas. The output freequency is

$$f = \frac{1.44}{(RA + 2RB)\, C} \quad \ldots.. \quad 5$$

and the duty cycle is

$$D = \frac{RA + RB}{RA + 2RB} \times 100\% \quad \ldots. \quad 6$$

If RA is much smaller than RB, the duty cycle approaches 50 percent.

Figure 2.12 shows theastable 555 timer as it usually appears. Again notice how pin 4 (reset) is tied to the supply voltage and how pin 5 (control) is bypassed to ground through a 0.01 μF capacitor.

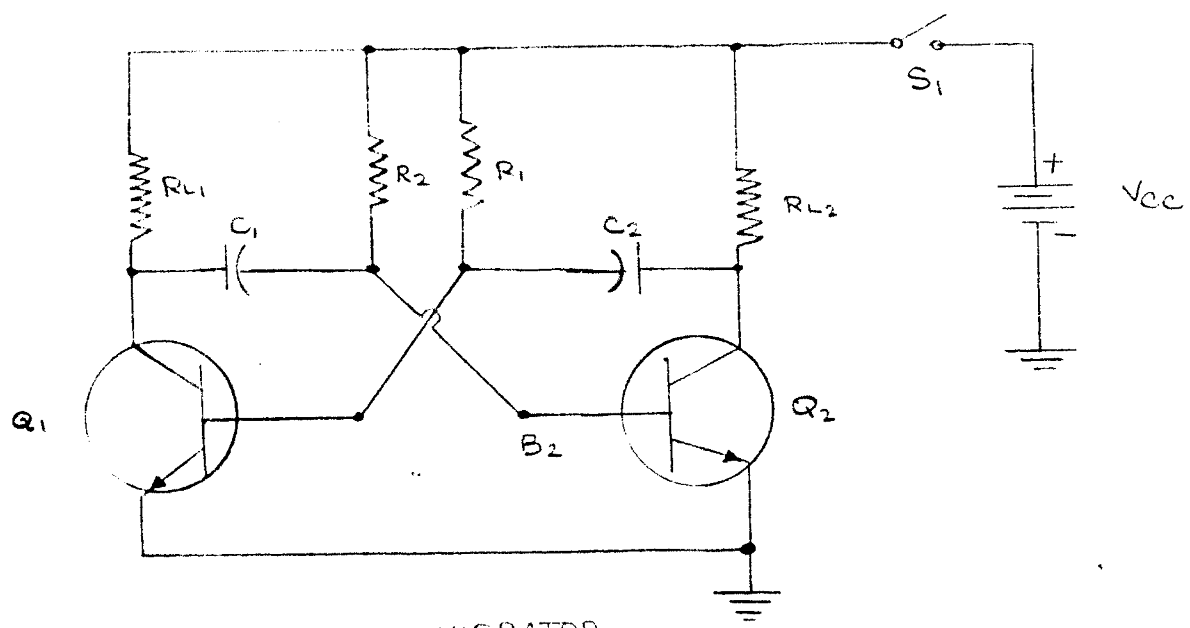
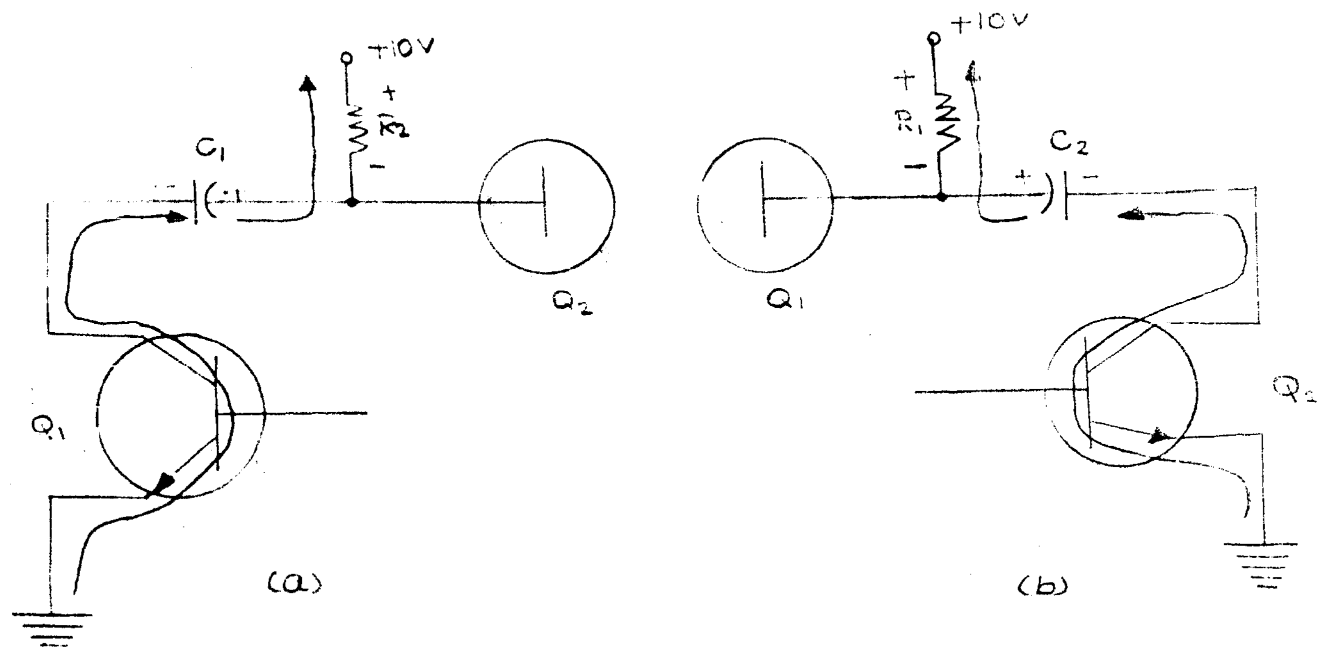
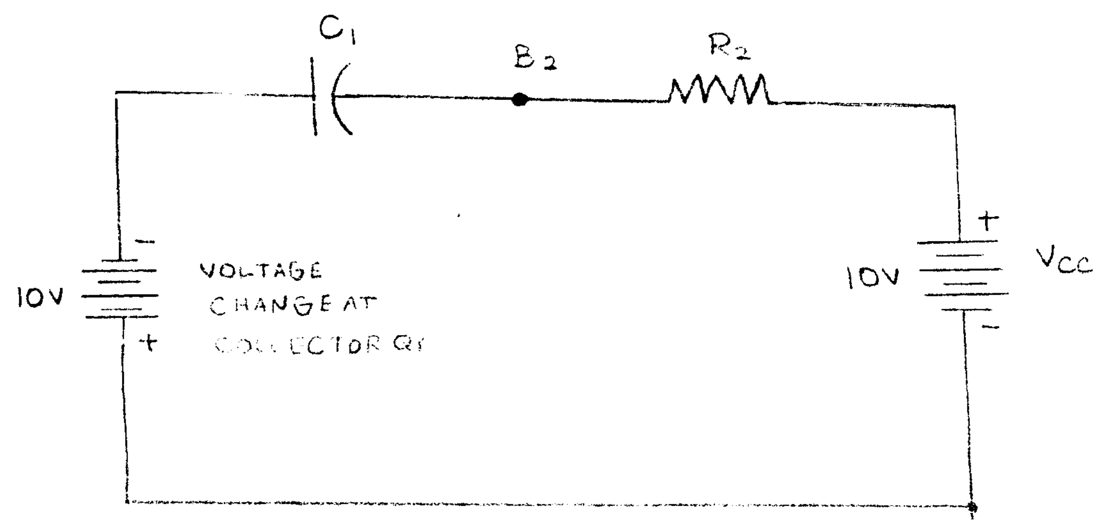


fig 2.1
COLLECTOR-COUPLED MULTIVIBRATOR





(a) Capacitor C_1 discharging through R_2.

Q_1 is ON, Q_2 is OFF.

(b) Capacitor C_2 discharging through R_1.

Q_2 is ON, Q_1 is OFF.

(c) Voltage C_1 "sees" at the instant that Q_1 saturates.

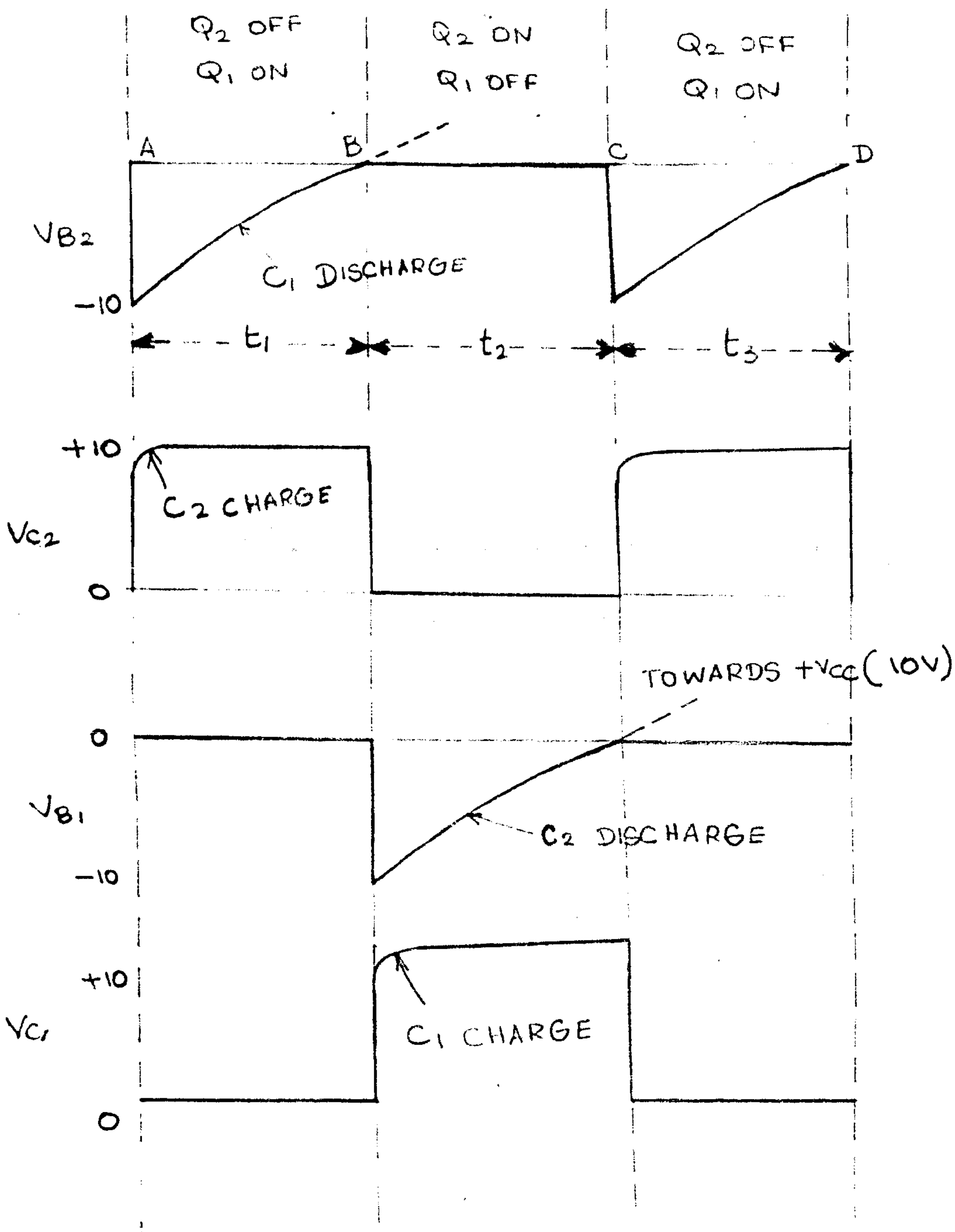


fig 2.3

Voltage wave forms in NPN Collector Coupled Multivibrator

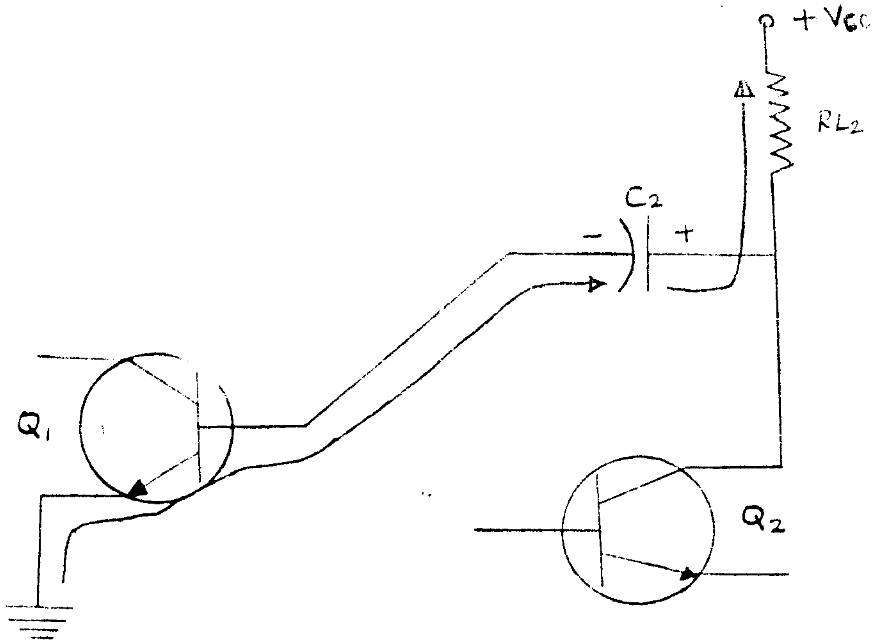


fig 2.4: Charge path for C2. Q2 is cut off, Q1 is ON.

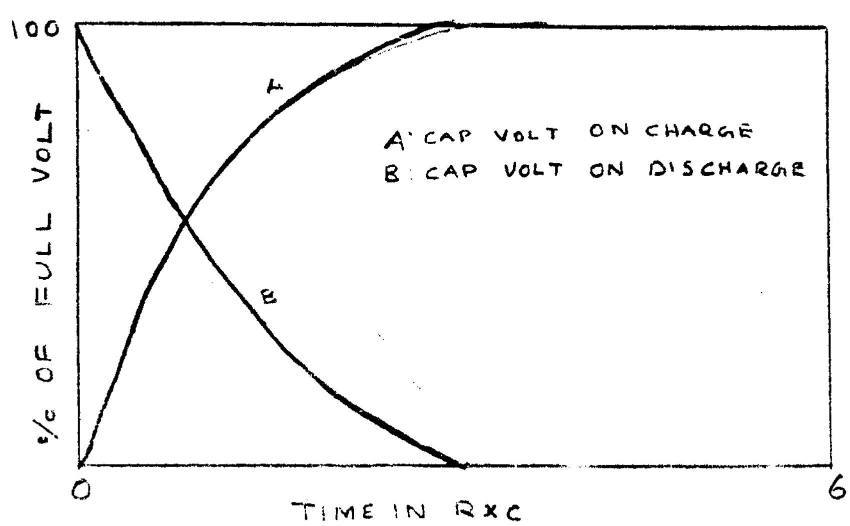


fig 2.5: Universal time constant chart

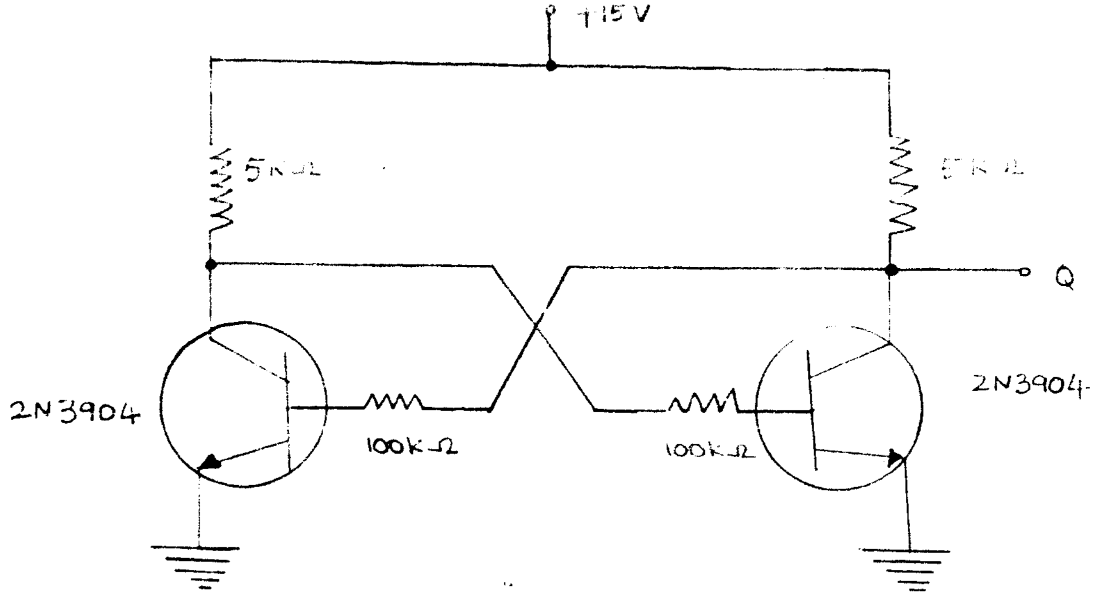


fig 2.6: FLIP-FLOP

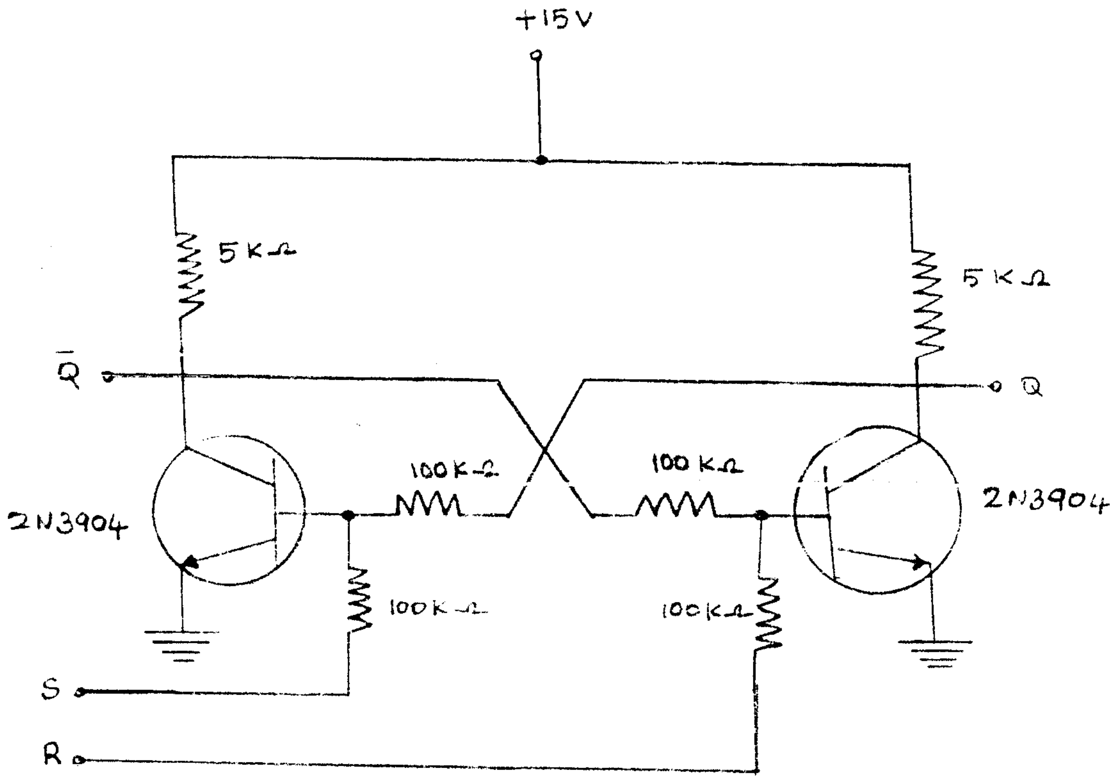


fig 2.7: RS FLIP-FLOP

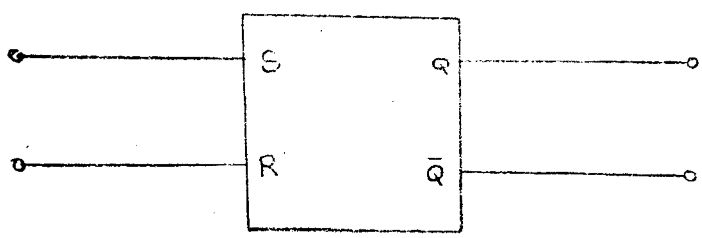
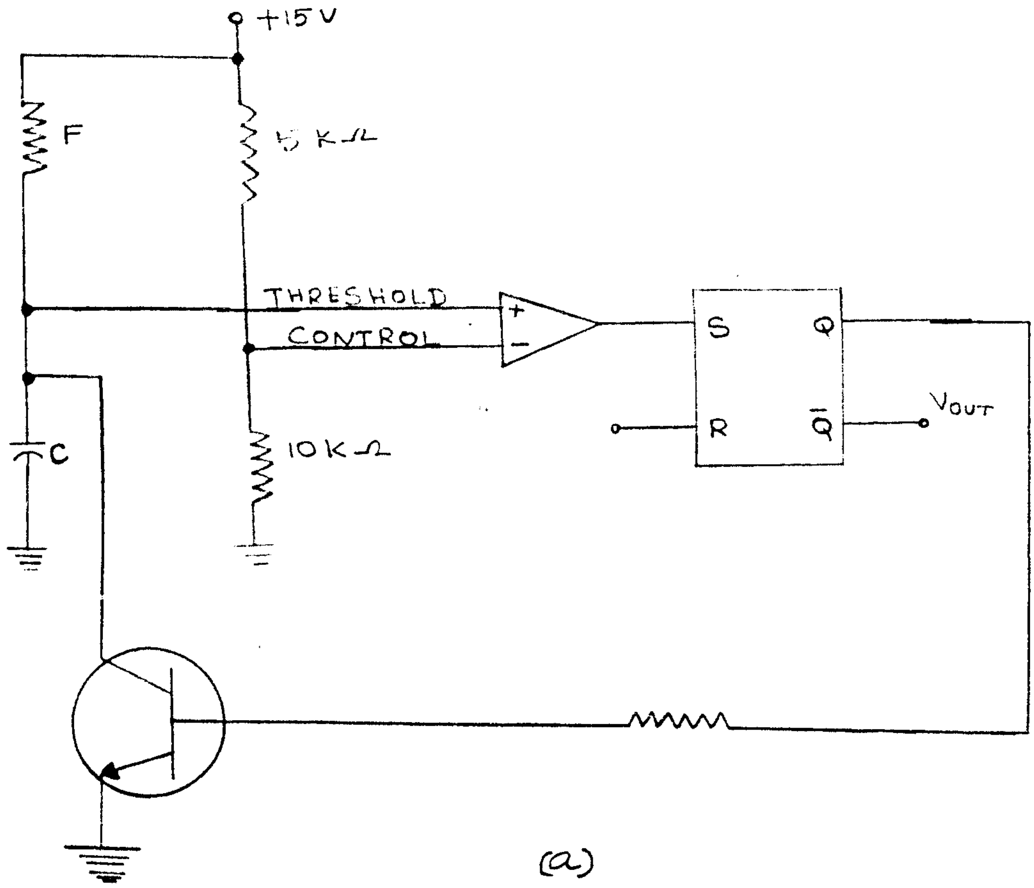
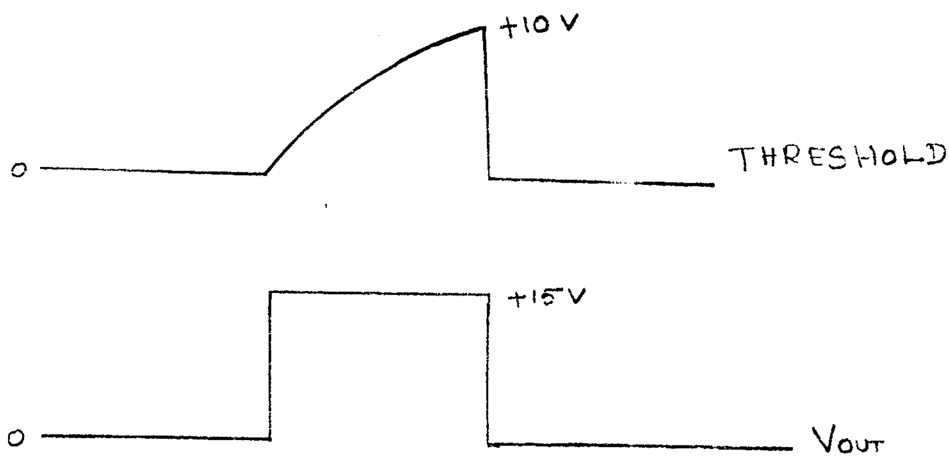


fig 2.8: SYMBOL FOR RS FLIP FLOP



(a)



(b)

fig 2.9 BASIC TIMING CONCEPTS

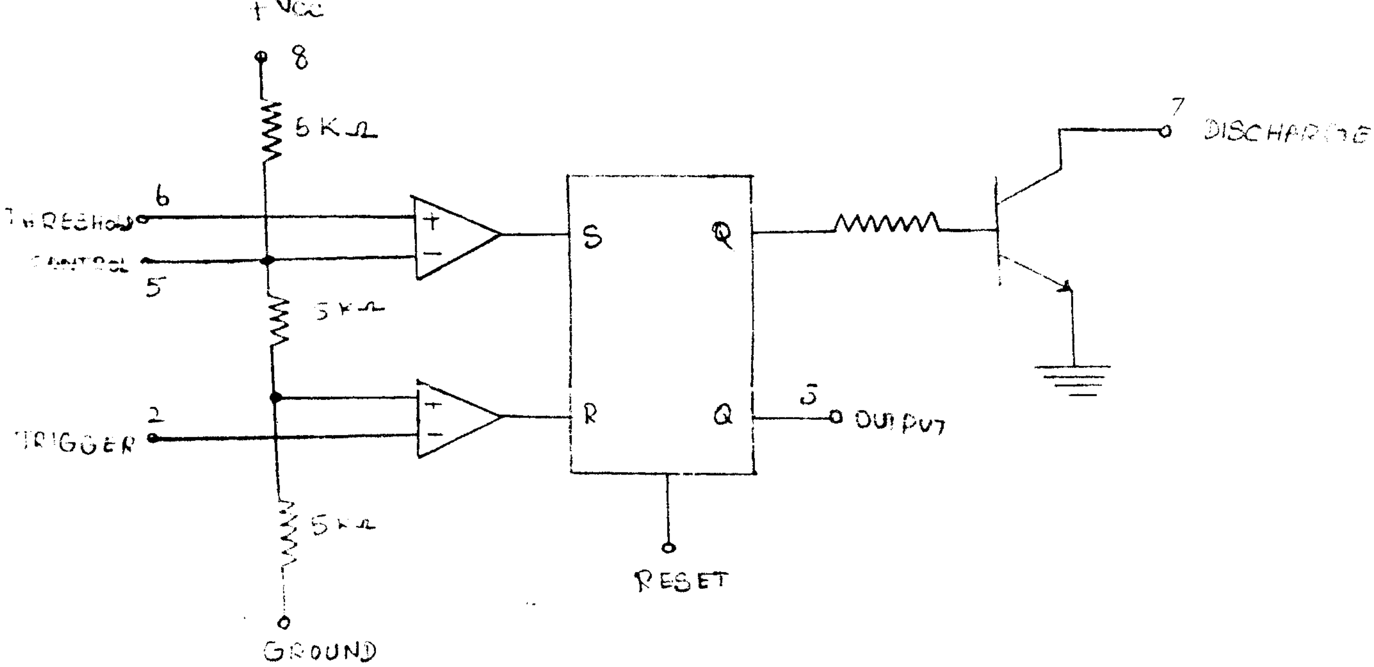


fig 2.10: 555 TIMER

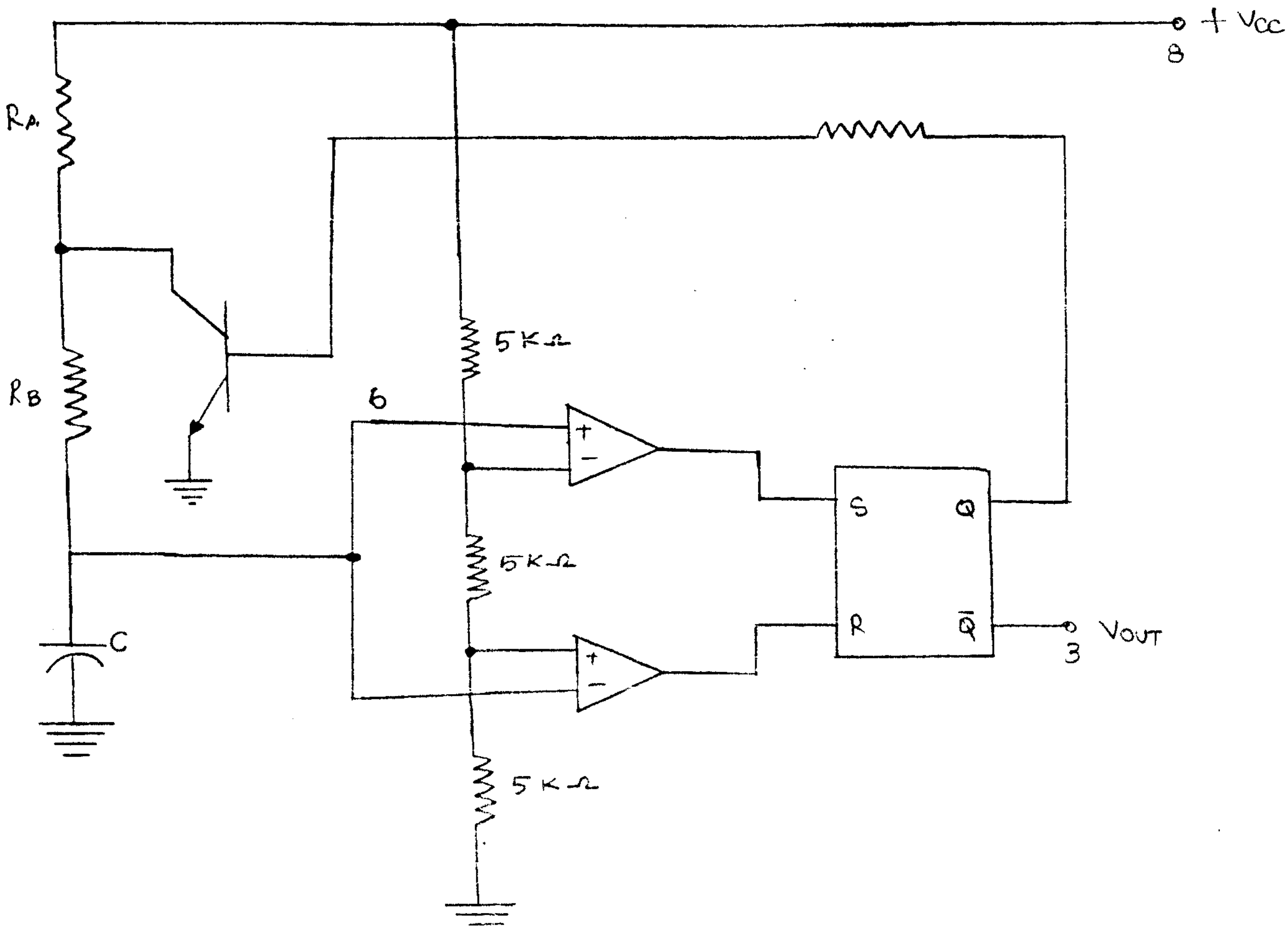


fig 2.11(a): ASTABLE OPERATION.

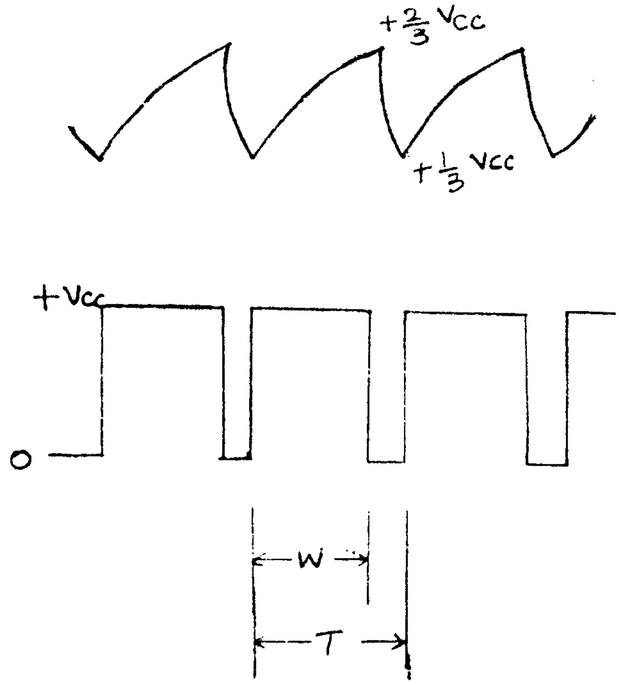


fig 2.11 (b): WAVE FORMS

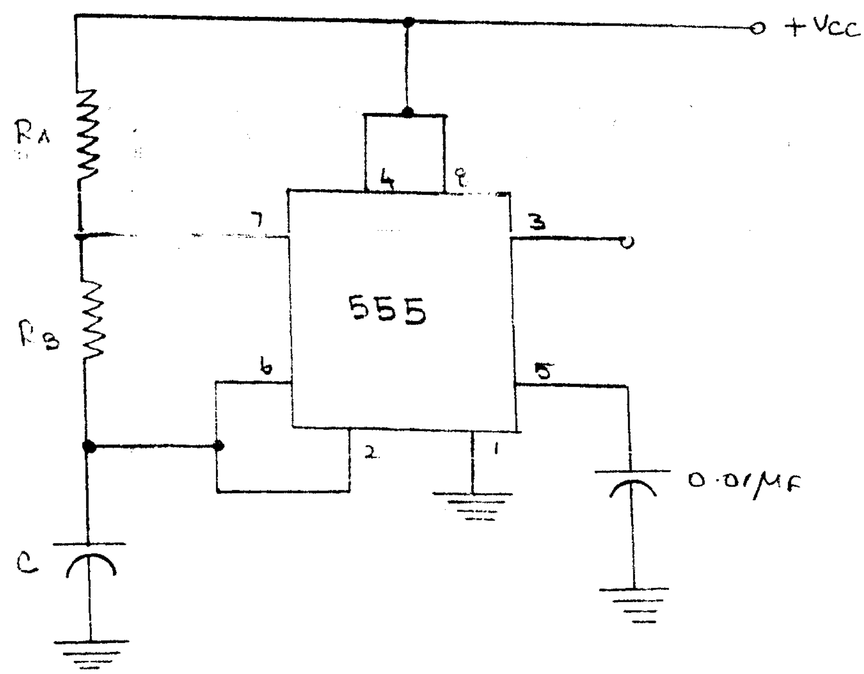


fig 2.12: ASTABLE 555 TIMER.

DISPLAY AND RELAY

3.1 DIGITAL DISPLAY METHODS

In digital instruments output device indicate the value of measured quantity in decimal digits. This is done by using a Digital display device. A digital display device may receive digital information in any form, but it converts that information to decimal form. Thus the display device indicates the value directly in decimal digits. The number of digits corresponds to the significant figures needed to represent the value. The basic element in a digital display device is the display, For a single digit because a multiple digit display is nothing else but a group of single digit displays. fig. 3.1. shows a multiple digit display consisting of 4 single digit displays.

A single digit display is capable of indicating the numbers from 0 to 9. There is also usually provision for a decimal point between each of the numerals. One of these is selected and activated in accordance with the range selection controls of the instrument. It should be understood that the signal should be decoded and decoding circuits are a part of the display units.

3.1.2. LIGHT EMITTING DIODE

A relatively new family of display devices utilizes 'light emitting diodes'. The LED is perhaps the most important of the display devices available today for use in instrumentation systems. The LED is a PN junction device which emits light when a current passes through it in the forward direction.

Charge carrier recombination occurs at a PN junction as electrons cross. From N side and recombines with holes on the P side, when recombination takes place, the charge carriers give up energy in the form of heat and light. If the semiconducting material is translucent the light is emitted, and the junction is source of light. This is the light emitting diode ie. LED.

Fig. 3.2 shows a cross sectional view of a typical LED charge carrier recombinations takes place in the P type materials. Therefore the P region becomes the surface of the devices. For maximum light emission, a metal film anode is deposited around the edge of the P type material. The cathode connection for the device is usually a gold film at the bottom of the N type region. This helps in reflecting the light to the surface.

Semi conductor material used for manufacture of LED is gallium arsenide phonphide (Ga AsP) which emits red or yellow light of gallium arsenide which gives green or red light emission. LEDs are used extensively in segmental and dot matrix displays of numeric and alpha numeric characters. Several LEDs are used in series to form one segment while a single LED may be used to form a decimal point. LEDs are available in many colours like green, yellow, amber and red.

The major advantages of LEDS in electronic displays are:

(i) LEDS are miniature in size and they can be stacked together to form numeric and alpha numeric dispalys in high density matrix.

(ii) The light out put from an LED is a function of the current flowing through it. There fore intensity of light emitted from LEDS can be smoothly controlled.

(iii) LEDS have a high efficiency as emitters of electro magnatic radiation. They require moderate power for their operation. A typical voltage drop of 1.2V and a current of 20MA is required for full brightness. There fore, LEDS are useful where miniaturization with low d.c.power are important.

(iv) The switching time is less than 1 ns and there fore they are very useful where dynamic operation at large number of arrays is involved.

(v) LEDS are manufactured with the same type of technology as is used for transistors and ICs and there fore they are economical and have a high degree of reliability.

(vi) LEDS are rugged and can there fore with stand shocks and vibrations. They can be operated over a wide range of temperature say 0-70° C.

DISPLAY SYSTEMS

In the case of segmental displays, or more than one light sources may be involved in the display of a particular character supposing digit 0 is to be displayed by a 7 segment display as shown in fig 3.3. This requires that segments a,b,c,d,e,and f should be lit up. Similarly for digit 2, segments a,b,c,d,e and g should be lit up thus by properly choosing the segments any number from 0 to 9 can be displayed.

A common supply voltage drives the anodes of the LEDs and when a switch closes, the corresponding LED is forward biased and emits light.

3.2 DECODERS

Electronic displays serve as output units of instrumentation systems. The digital data resulting from a measurement application is binary coded decimal (BCD) form. Thus in display applications, where machine communicates with a human being some sort of decoding is required. If the language of the machine of the machine is BCD, we have to decode (translate) it in to a decimal code. than it can be easily understood by the human operation. The decoder converts the binary code, such as BCD in to a non binary code that can be understand by man, such as seven segment or decimal code. Thus decimal code has 10 different symbals while the 7 segment code has 7 separate lines used in activating 7 segment decimal displays.

3.2.1. BCD TO DECIMAL DECODER

A typical truth table (1) and logic diagram for 8-4.2.1. BCD to decimal decoders is shown in fig. 3.4. The circuits uses NAND gates as is commonly done in TTL ICS.

3.2.2. BCD TO 7 SEGMENT DECODER

A typical truth table (2) and logic diagram for BCD to 7 segment numeric characters is shown in fig. 3.5. Multiplexers are used for driving more than one digit.

3.3. RELAY

The serious 57 miniature relays are specially designed for communication and industrial control applications where space and cost are critical.

The relays are available with contacts rated for 6 amps and have direct P.C. terminals. These miniature relays are ideally suited for high density P.C. board applications.

SPECIFICATIONS

Enclosure	:	Polycarbonate
Contact form	:	A, B and C
Contact managements	:	7 pole
Contact rating at 28V DC and 230V AC	:	6 amps resistive
Contact material	:	Silver cadmium oxide
Contact resistance	:	0-50 ohm max Initial 100 ohms max after life
Life expactancy	:	Mechanical 10^6 operations Rated load 10^5 operations
Ambient Temperature	:	-40° C to +65° C
Terminals	:	Printed circuits
Dielectric strength	:	1000 volts RMS
Insulation resistance	:	10,000 M ohm of 500V DC
Max. operate time	:	0.012 Sec.
Max. release time	:	0.008 sec.
Coil dissipation	:	1.5 watts
Sensitivity	:	0.75 watts

Such a relay has more than one contacts which are mostly change over type. A small current flowing through the electromagnetical can activate these contacts to change over from one position to another. The normally open contacts will close and the normally closed contacts will open. Such a relay may require a coil current is between 20 and 200 mA. The operating voltage is generally 12V or 24V etc. The higher is the voltage, the lower is the current.

An electromechanical or solid state devices are operated by cariations in the input which in turn, operate or control other devices connected to the output. They are used in a wide variety of application throughout industry. Such as in telephone exchange, digital computer, motor etc. Highly sophisticated relay are utilised to protect electric power block outs as well as to regulate and control the generation and distribution of power.

Relays using discrete solid state components, operate amplifiers or microprocessor each provide more sophisticated designs. Their use is increasing, particularly in application where the relay and associated equipments are packaged together.

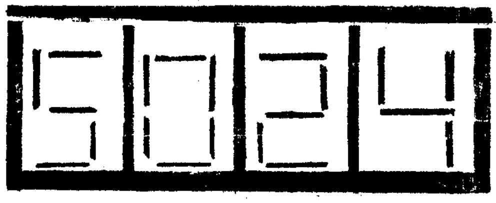


fig 3.1: MULTIPLE DIGIT DISPLAY

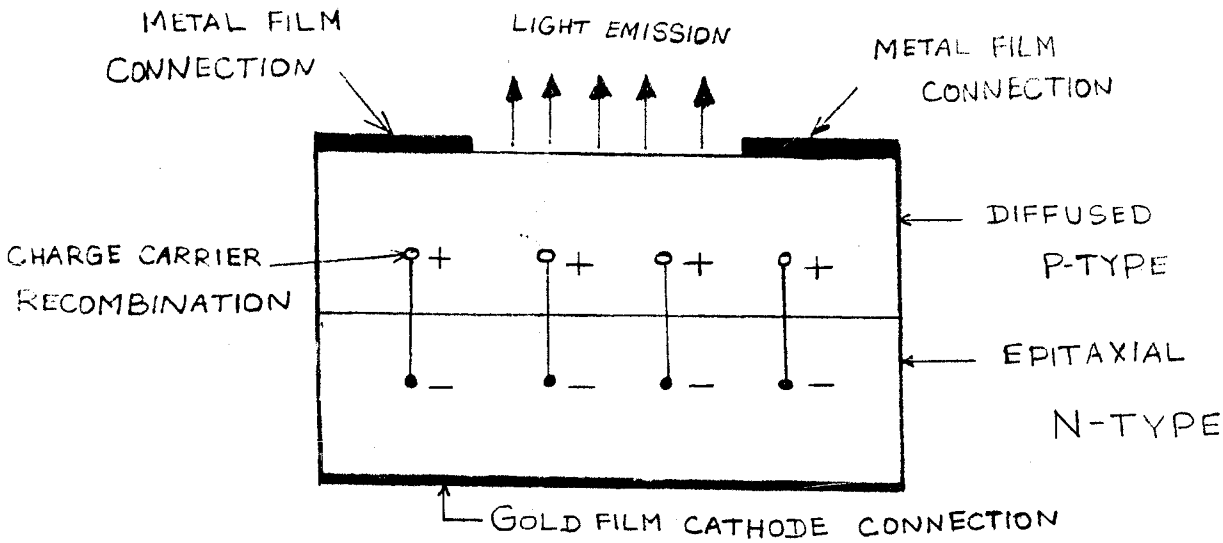


fig 3.2: LED CROSS-SECTION

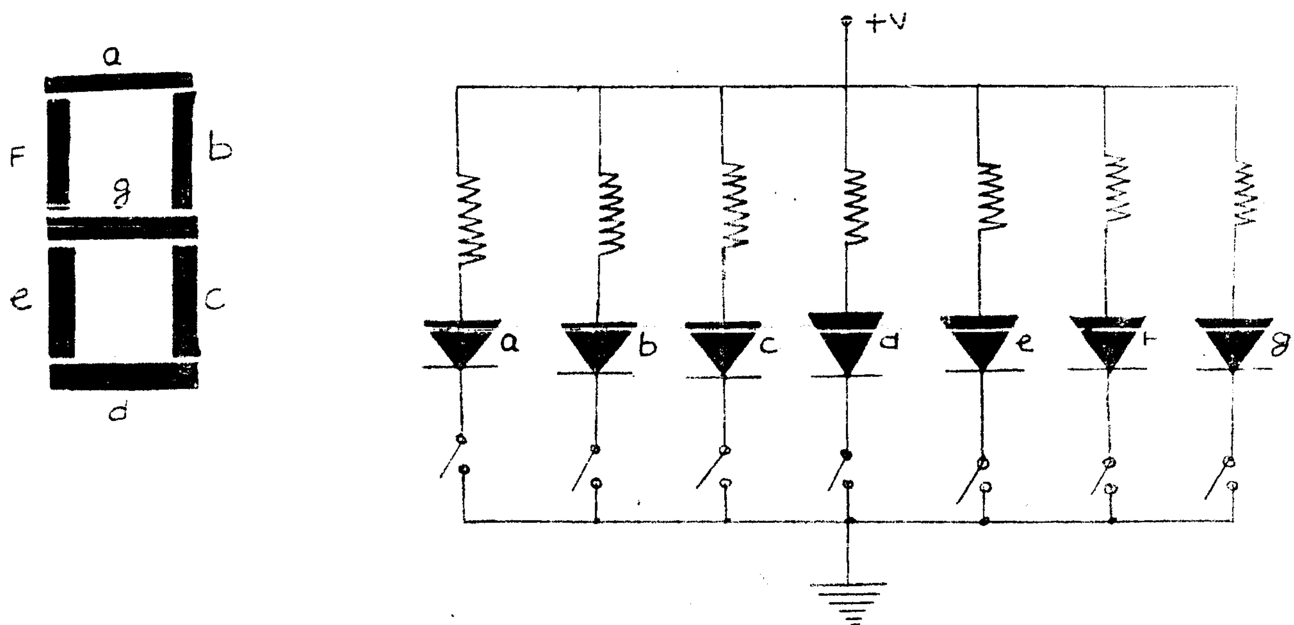


fig 3.3: SEVEN SEGMENT READOUT AND CIRCUIT (COMMON ANODE)

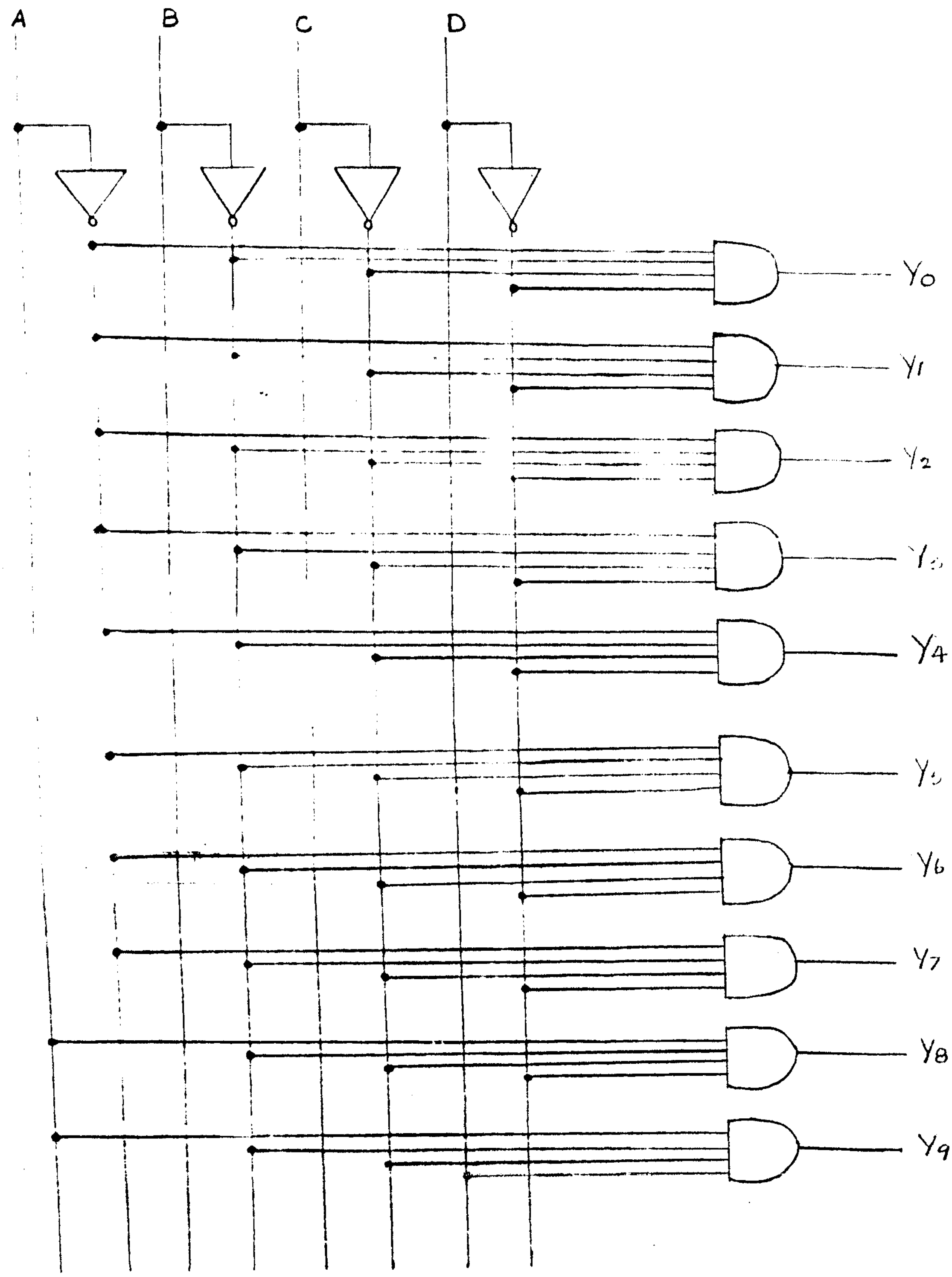


fig 5.4 BCD TO DECIMAL DECODER

TRUTH TABLE - 1

NO.	INPUTS				OUTPUTS									
	A	B	C	D	Yo	Y1	Y2	Y3	Y4	Y5	Y6	Y7	Y8	Y9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

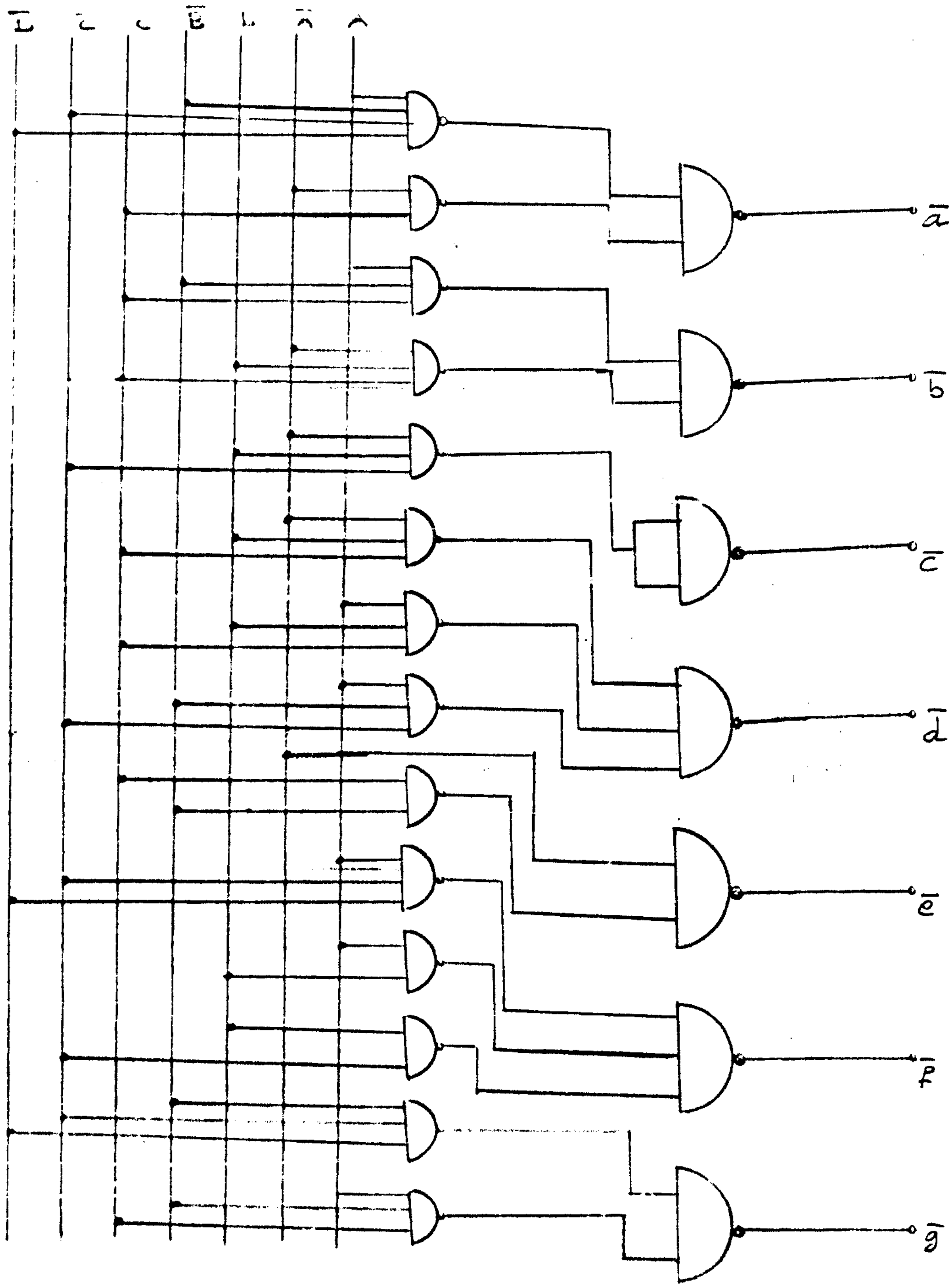


fig 3.5: BCD to 7 Segment Converter

TRUTH TABLE -2

BCD TO 7 SEGMENT CONVERSION

DECIMAL	BCD CODE				7 SEGMENT OUTPUT						
NUMBER	D	C	B	A	a	b	c	d	e	f	g
0	0	0	0	0	1	1	1	1	1	1	0
1	0	0	0	1	0	1	1	0	0	0	0
2	0	0	1	0	1	1	0	1	1	0	1
3	0	0	1	1	1	1	1	1	0	0	1
4	0	1	0	0	0	1	1	0	0	1	1
5	0	1	0	1	1	0	1	1	0	1	1
6	0	1	1	0	0	0	1	1	1	1	1
7	0	1	1	1	1	1	1	0	0	0	0
8	1	0	0	0	1	1	1	1	1	1	1
9	1	0	0	1	1	1	1	0	0	1	1

REGULATED POWER SUPPLY

POSITIVE VOLTAGE REGULATOR SERIES WITH SEVEN VOLTAGE OPTIONS

The 7800 series consists of three terminals positive voltage regulators with seven voltage options. These Ics are designed as Fixed voltage regulators and with adequate heat sinking can deliver output currents inexcess of 1A. Although these devices do not require external components, such components can be used to obtain adjust[redacted]able voltages and currents. These Ics also have internal thermal overload protection and internal short circuit current limiting. As shown in Fig. 4.1 (b) proper operation requires a common ground between input and output voltages. In addition, the difference between intput and output voltages (Vin - Vo) called dropout voltage, must be typically 2.0V even during the low point on the ripple voltage. Further, the capacitor Ci is required if the regulator is located an appreciable distance from a power supply filter. Even through Co is not needed, it may be used to improve the transient response of the regulator.

Typical performance parameters for voltage regulators are line regulation, load regulation, temperature stability and ripple rejection.

DEVICE TYPE	OUTPUT VOLTAGE (V)	MAXIMUM INPUT VOLTAGE (V)
7805	5.0	
7806	6.0	
7808	8.0	
7812	12.0	35
7815	15.0	
7818	18.0	
7824	24.0	40

Line or input regulation is defined as the change in output voltage for a change in the input voltage and is usually expressed in milli volts or as a percentage or output voltage Vo. Load reulation is the change in output voltage for a change in load current and is also expressed in milli volts or as a percentage of Vo. Temperature stability or average temperature co-efficient of output voltage (TCVo) is the change in output voltage per unit change in termperature and is expressed in either milli volts/ °C or parts per million (PPM)/ °C. Ripple rejection is the measure of a regulator's ability to reject ripple voltages. It is usually expressed in dB. The smaller the value of line regulation, load regulation, and temperature stability, the better the regulator.

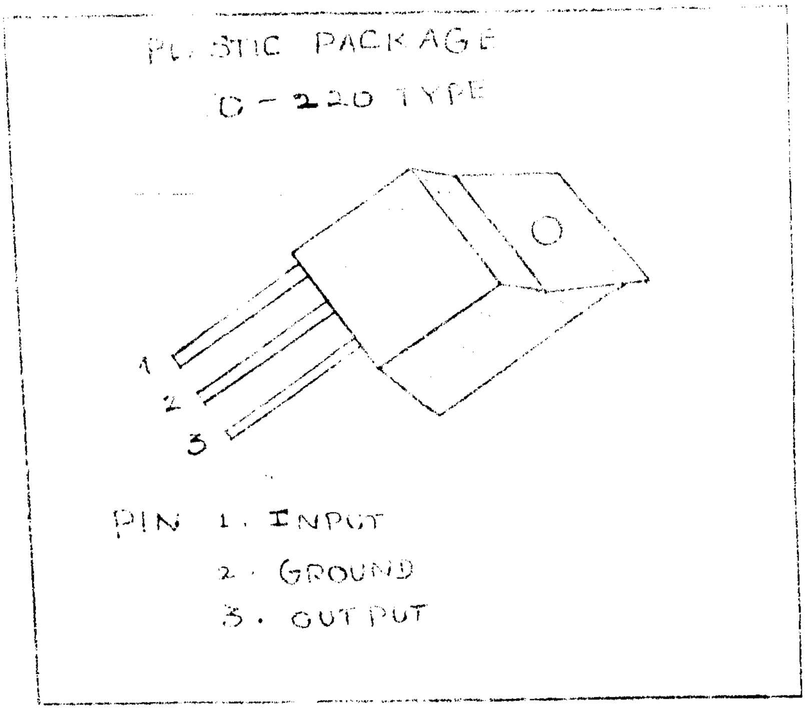


fig 4.1 (a)

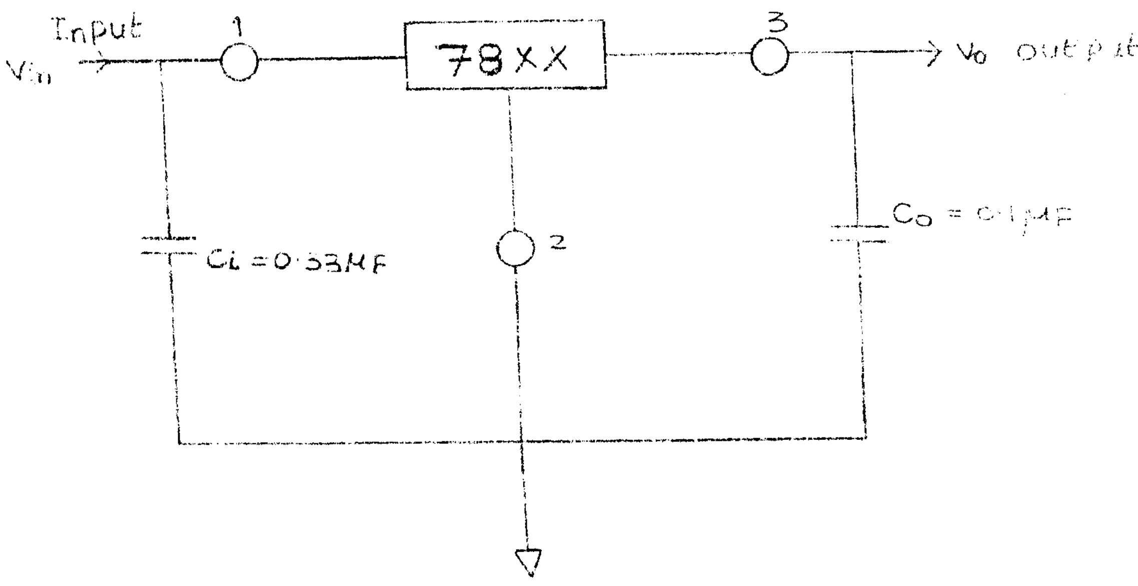


fig 4.1 (b)

7800 Series Regulators.

(a) Package Type.

(b) Standard Application.

· POWER SUPPLY

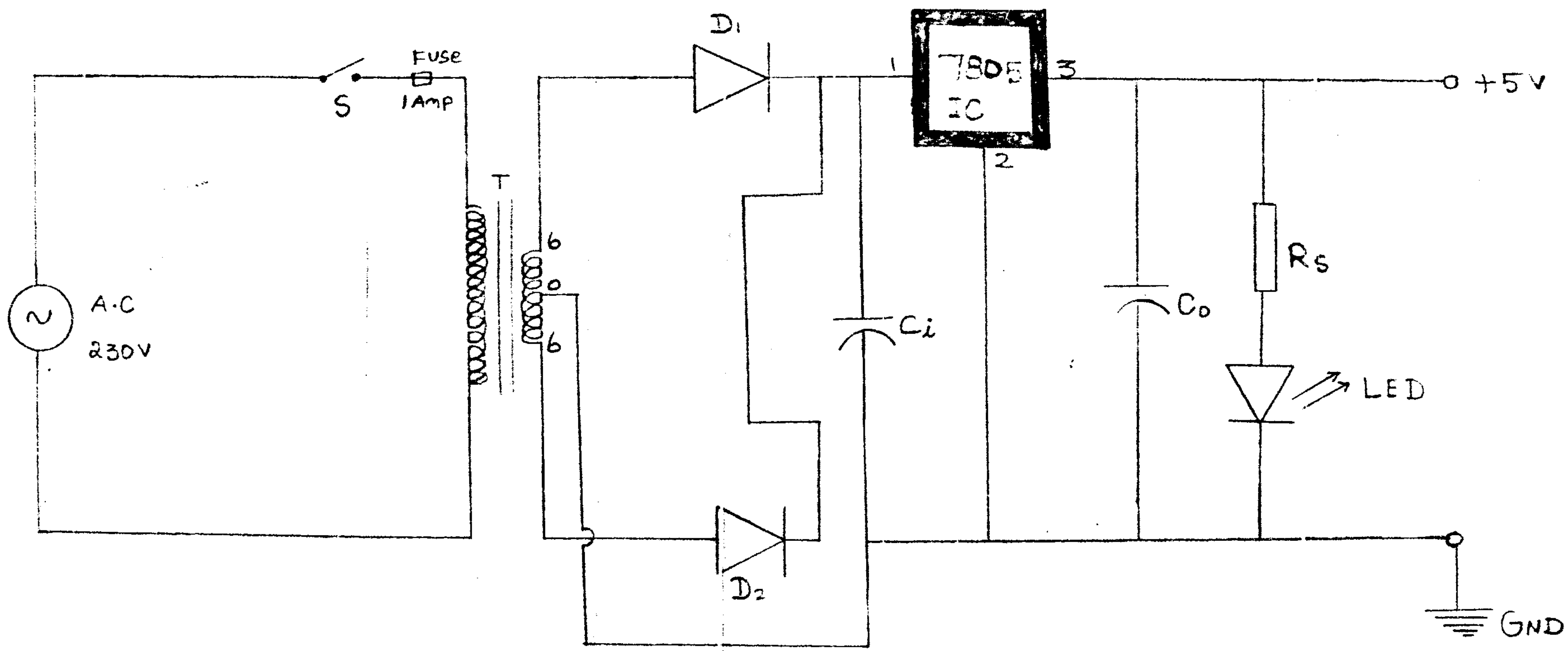


fig 4·2 S — SPST Switch

T — Step Down Transformer (230V to 6-0-6, 1 Amp)

D_1 & D_2 — Diodes (IN 4001)

Ci & Co — Capacitors (0·33 μF & 0·1 μF)

7805 IC — Regulator IC

Rs — Resistors (100 Ω)

PCB PREPARATION

Printed Circuit Boards are certainly the most important element in the fabrication of electronic equipment. The design of a printed circuit Board can, as many will agree, be considered as the last step in electronic circuit design as well as a first major step in the production of PCBS. It forms a distinct factor in electronic circuit performance and reliability. The producibility of a PCB and its assembly and serviceability also deponds on the design. All these factors finally get reflected in the price for the electronic equipment of which, PCBS take away approximately 20% of the cost. From this, it is evident that the task of engineers involved in PCB design is not very simple or always straight forward. Intimate knowledge of all the implications is very much required and can only be gradually acquired, mostly by experience.

However, there are certain standard practices in PCB designing which are followed by most designers. They can serve as a guide line.

The designing of a PCB consists of the designing of the layout followed by the generation or preparation of the art work. The layout, therefore should include all the relevant aspects and details of the PCB design. We can say that layout design is the stage where engineering capacity combined with creativity are the governing inputs, while practical skills paired with technical commonsense have to be predominant in art work preparation.

Automatted art work draughting and computer aided design has been explained with the block diagram in the next pages.

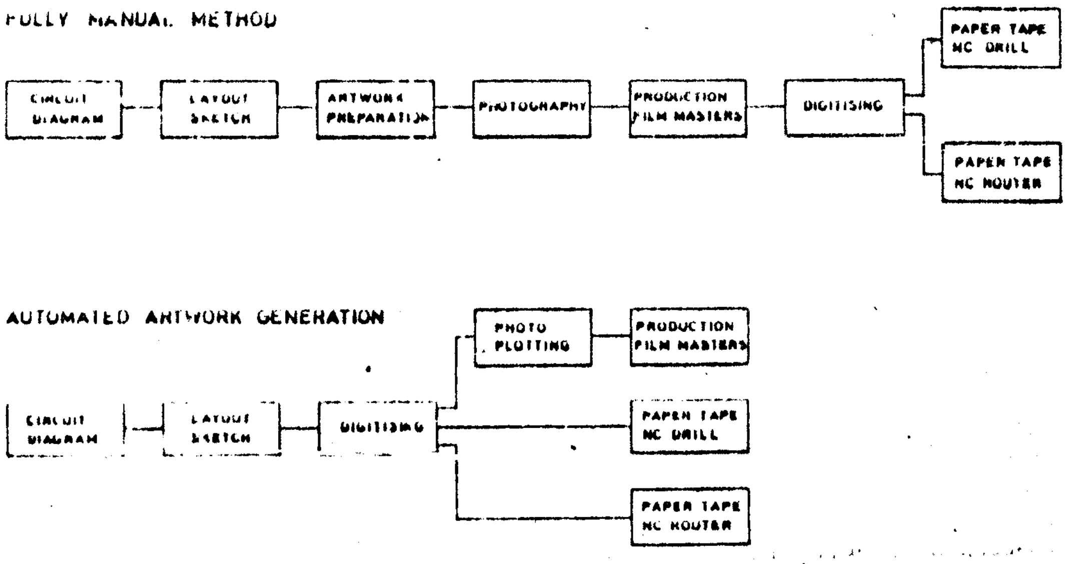


fig 5.1

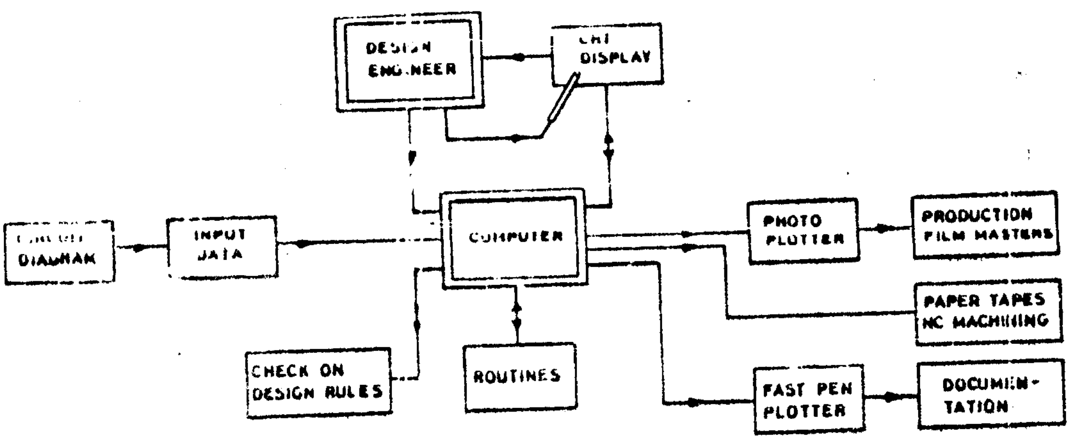


fig 5.2 [redacted] Typical equipment configuration for computer-aided layout design with automated artwork generation

C O N C L U S I O N

A programmable controller for controlling the AC & DC Loads is designed, fabricated and tested. The instrument is found working satisfactorily.

The various parts of the project such as counters, registers, seven segment display, frequency generator have been explained in the preceding chapters. And also various difficulties in preparation of PCB are discussed. It can be used in automobiles, communications, industrial automation, process control and so on. Since Electronic counters are capable of making many measurements involving frequency, time, phase angle, radiation events and totalizing electric events, the principle of this project may be used for the above purposes.

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COMPONENT LIST

S.NO	NAME	RANGE	QUANTITY
1.	Transformer	230V - 6-0-6/1A	1
2.	Diodes DA & Dc	IN4001	2
3.	Regulator IC	IM7805	1
4.	Capacitors	.33µF & .1 µF	1
5.	Register R3	100 ohm	1
6.	Switch	SPST	1
7.	LED		1
8.	IC	ICM 7217 IJI	1
9.	Seven Segment	LT542R	4
10.	Relay		1
11.	Transistors (T1)	SL100	1
	(T2)	BC107	1
	(T3)	BC177	1
12.	Thumbwheel Swtich		4
13.	Diodes D1 to D16	IN34	16
14.	P.S.I & P.S.2	N.O	2

15.	Resistors	(R1)	1.2K	1
		(R2)	560 ohm	1
		(R6) & (R7)	10 k	3
		(R4)	68K	1
		(R5)	33k	1
		(R8)	100 ohm	1
16.	Capacitors			
	(C1, C2 & C5)		0.047 μF	3
		(C3)	0.1 μF	1
		(C4)	0.1 μF	1
17.	555 Timer IC			

ICM7217/ICM7227

4-Digit LED Display Programmable Up/Down Counter

INTERSIL

GENERAL DESCRIPTION

The ICM7217 and ICM7227 are four digit, presettable up/down counters, each with an onboard presettable register continuously compared to the counter. The ICM7217 versions are intended for use in hardwired applications where thumbwheel switches are used for loading data, and simple SPDT switches are used for chip control. The ICM7227 versions are for use in processor-based systems, where presetting and control functions are performed under processor control.

These circuits provide multiplexed 7 segment LED display outputs, with common anode or common cathode configurations available. Digit and segment drivers are provided to directly drive displays of up to 0.8" character height (common anode) at a 25% duty cycle. The frequency of the onboard multiplex oscillator may be controlled with a single capacitor, or the oscillator may be allowed to free run. Leading zeros can be blanked. The data appearing at the 7 segment and BCD outputs is latched; the content of the counter is transferred into the latches under external control by means of the Store pin.

The ICM7217/7227 (common anode) and ICM7217A/7227A (common cathode) versions are decade counters, providing a maximum count of 9999, while the ICM7217B, 7227B (common anode) and ICM7217C/7227C (common cathode) are intended for timing purposes, providing a maximum count of 5959.

FEATURES

- **Four Decade, Presettable Up-Down Counter With Parallel Zero Detect**
- **Settable Register With Contents Continuously Compared to Counter**
- **Directly Drives Multiplexed 7 Segment Common Anode or Common Cathode LED Displays**
- **On-Board Multiplex Scan Oscillator**
- **Schmitt Trigger On Count Input**
- **TTL Compatible BCD I/O Port, Carry/Borrow, Equal, and Zero Outputs**
- **Display Blank Control for Lower Power Operation; Quiescent Power Dissipation <5mW**
- **All Terminals Fully Protected Against Static Discharge**
- **Single 5V Supply Operation**

These circuits provide 3 main outputs; a CARRY/BORROW output, which allows for direct cascading of counters; a $\overline{ZERO}$ output, which indicates when the count is zero; and an $\overline{EQUAL}$ output, which indicates when the count is equal to the value contained in the register. Data is multiplexed to and from the device by means of a three-state BCD I/O port. The CARRY/BORROW, $\overline{EQUAL}$, $\overline{ZERO}$ outputs, and the BCD port will each drive one standard TTL load.

To permit operation in noisy environments and to prevent multiple triggering with slowly changing inputs, the count input is provided with a Schmitt trigger.

Input frequency is guaranteed to 2MHz, although the device will typically run with f_{in} as high as 5MHz. Counting and comparing ($\overline{EQUAL}$ output) will typically run 750kHz maximum.

ORDERING INFORMATION

Part Number	Temperature Range	Package	Display Option	Count Option Max Count
ICM7217IJI	−25°C to +85°C	28 Lead CERDIP	Common Anode	Decade/9999
ICM7217AIPI	−25°C to +85°C	28 Lead PLASTIC	Common Cathode	Decade/9999
ICM7217BIJI	−25°C to +85°C	28 Lead CERDIP	Common Anode	Timer/5959
ICM7217CIPI	−25°C to +85°C	28 Lead PLASTIC	Common Cathode	Timer/5959
ICM7227IJI	−25°C to +85°C	28 Lead CERDIP	Common Anode	Decade/9999
ICM7227AIPI	−25°C to +85°C	28 Lead PLASTIC	Common Cathode	Decade/9999
ICM7227BIJI	−25°C to +85°C	28 Lead CERDIP	Common Anode	Timer/5959
ICM7227CIPI	−25°C to +85°C	28 Lead PLASTIC	Common Cathode	Timer/5959

202816-003

NOTE: All typical values have been characterized but are not tested

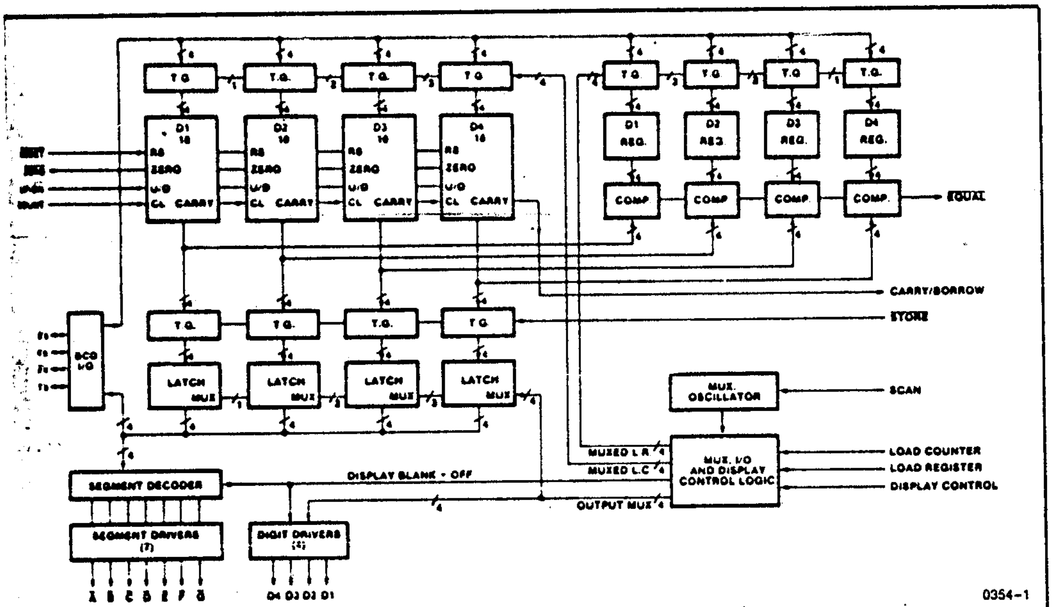


Figure 1: ICM7217 Functional Diagram

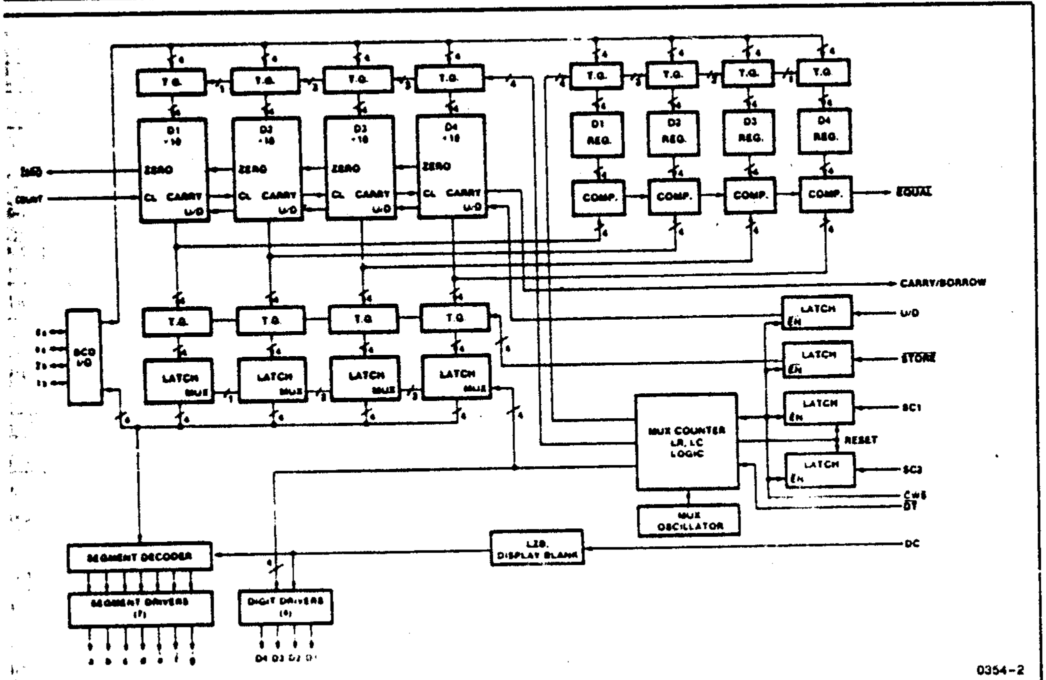


Figure 2: ICM7227 Functional Diagram

INTERSIL'S SOLE AND EXCLUSIVE WARRANTY OBLIGATION WITH RESPECT TO THIS PRODUCT SHALL BE THAT STATED IN THE WARRANTY ARTICLE OF THE CONDITION OF SALE. THIS WARRANTY SHALL BE EXCLUSIVE AND SHALL BE IN LIEU OF ALL OTHER WARRANTIES, EXPRESS, IMPLIED OR STATUTORY, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR USE.

‡ All typical values have been characterized but are not tested.

ICM7217/ICM7227

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ($V_{DD} - V_{SS}$) 6V
Input Voltage (any terminal) .... (V_{DD} + 0.3V to V_{SS} − 0.3V) Note 2
Power Dissipation (common anode/Cerdip) .... 1W Note 1
Power Dissipation (common cathode/Plastic) .... 0.5W Note 1
Operating Temperature Range .... −25°C to +85°C
Storage Temperature Range .... −65°C to +150°C
Lead Temperature (Soldering, 10sec) .... 300°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

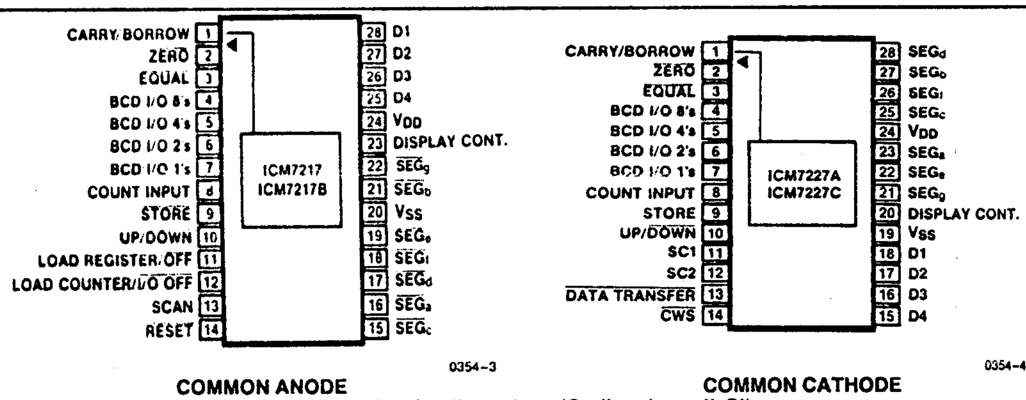


Figure 3: Pin Configurations (Outline dwgs JI, PI)

ELECTRICAL CHARACTERISTICS

(V_{DD} = 5V, V_{SS} = 0V, T_A = 25°C, Display Diode Drop 1.7V, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{DD} (7217)	Supply Current (Lowest power mode)	Display Off, LC, DC, UP/DN, ST, RS, BCD I/O Floating or at V_{DD} (Note 3)		350	500	μA
I_{DD} (7227)	Supply current (Lowest power mode)	Display off (Note 3)		300	500	μA
I_{OP}	Supply Current OPERATING	Common Anode, Display On, all "8's"	140	200		mA
		Common Cathode, Display On, all "8's"	50	100		mA
V_{DD}	Supply Voltage		4.5	5	5.5	V
I_{DIG}	Digit Driver output current	Common anode, $V_{OUT} = V_{DD} - 2.0V$	140	200		mA peak
I_{SEG}	SEGment driver output current	Common anode, V_{OUT} = +1.5V	−20	−35		mA peak
I_{DIG}	Digit Driver output current	Common cathode, V_{OUT} = +1.0V	−50	−75		mA peak
I_{SEG}	SEGment driver output current	Common cathode $V_{OUT} = V_{DD} - 2V$	9	12.5		mA peak
I_P	ST, RS, UP/DN input pullup current	$V_{OUT} = V_{DD} - 2V$ (See Note 3)	5	25		μA
Z_{IN}	3 level input impedance		40		350	kΩ

NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (Continued) (V_{DD} = 5V, V_{SS} = 0V, T_A = 25°C, Display Diode Drop 1.7V, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{BIH}	BCD I/O input high voltage	ICM7217 common anode (Note 4)	1.5			V
		ICM7217 common cathode (Note 4)	4.40			V
		ICM7227 with 50pF effective load	3			V
V_{BIL}	BCD I/O input low voltage	ICM7217 common anode (Note 4)			0.60	V
		ICM7217 common cathode (Note 4)			3.2V	V
		ICM7227 with 50pF effective load			1.5	V
I_{BPU}	BCD I/O input pullup current	ICM7217 common cathode $V_{IN} = V_{DD} - 2V$ (Note 3)	5	25		μA
I_{BPD}	BCD I/O input pulldown current	ICM7217 common anode $V_{IN} = +2V$ (Note 3)	5	25		μA
V_{OH}	BCD I/O, $\overline{ZERO}$, $\overline{EQUAL}$ Outputs output high voltage	I_{OH} = 100μA	3.5			V
V_{OL}	BCD I/O, CARRY/BORROW $\overline{ZERO}$, $\overline{EQUAL}$ Outputs output low voltage	I_{OL} = −1.6mA			0.4	V
f_{in}	Count input frequency (Guaranteed)	$-20°C < T_A < +70°C$	0	5	2	MHz
V_{TH}	Count input threshold	(Note 5)		2		V
V_{HYS}	Count input hysteresis	(Note 5)		0.5		V
V_{CIL}	Count input LO				0.40	V
V_{CIH}	Count Input HI		3.5			V
f_{ds}	Display scan oscillator frequency	Free-running (SCAN terminal open circuit)			10	kHz

NOTES: 1. These limits refer to the package and will not be obtained during normal operation.

2. Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to a voltage greater than V_{DD} or less than V_{SS} may cause destructive device latchup. For this reason it is recommended that the power supply to the device be established before any inputs are applied and that in multiple systems the supply to the ICM7217/7227 be turned on first.

3. In the ICM7217 the UP/DOWN, STORE, RESET and the BCD I/O as inputs have pullup or pulldown devices which consume power when connected to the opposite supply. Under these conditions, with the display off, the device will consume typically 750 μA. The ICM7227 devices do not have these pullups or pulldowns and thus are not subject to this condition.

4. These voltages are adjusted to allow the use of thumbwheel switches for the ICM7217 versions. Note that a positive level is taken as an input logic zero for ICM7217 common-cathode versions.

5. Parameters not tested (Guaranteed by Design)

14

NOTE. All typical values have been characterized but are not tested

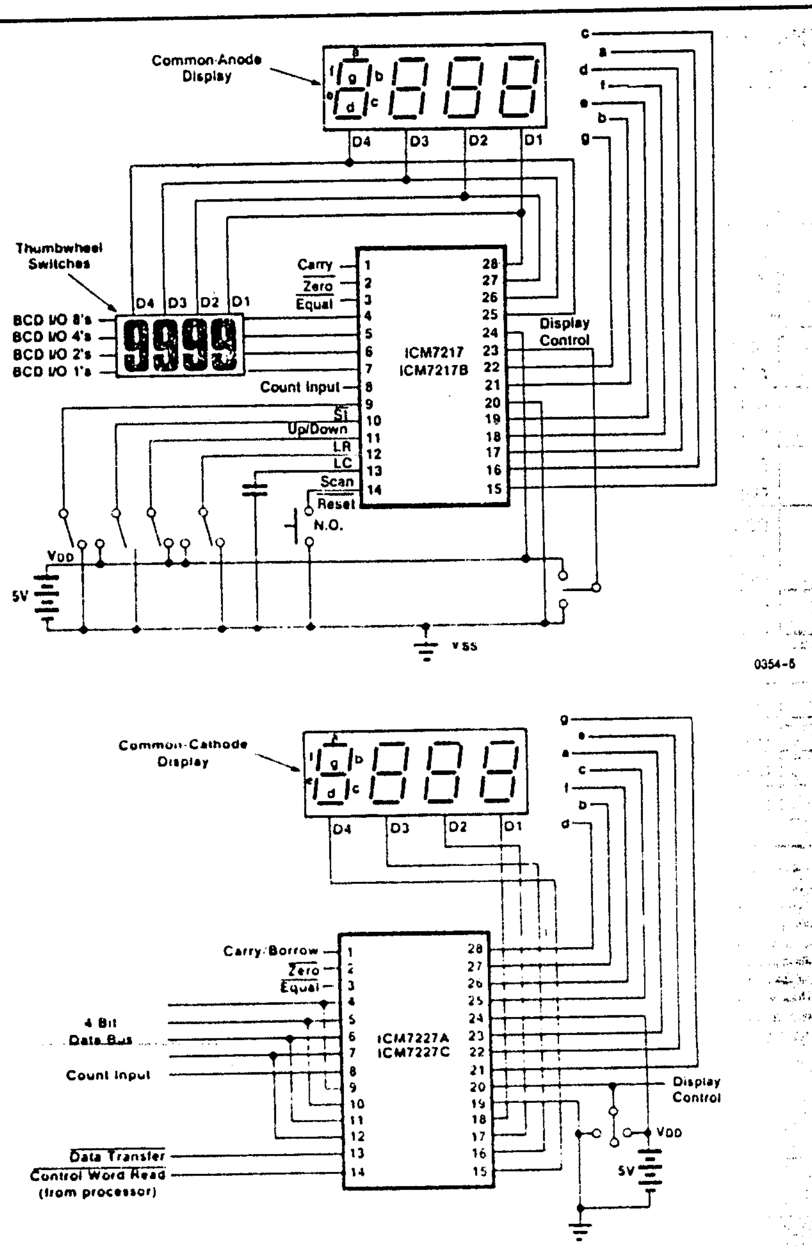
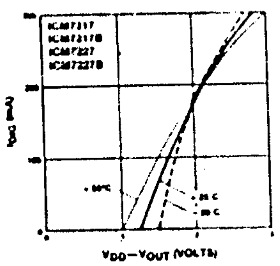


Figure 4: Test Circuits, showing the ICM7217 in the Common-Anode Version and the ICM7227 in the Common-Cathode Version

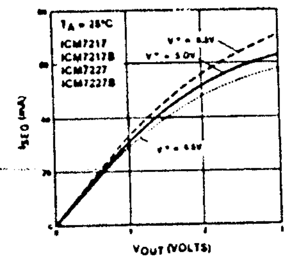
NOTE: All typical values have been characterized but are not tested

TYPICAL PERFORMANCE CHARACTERISTICS (DIGIT AND SEGMENT DRIVERS)



0354-7

Typical I_{DIG} vs. $V_{+} - V_{OUT}$, $4.5V \leq V^{+} \leq 6.0V$



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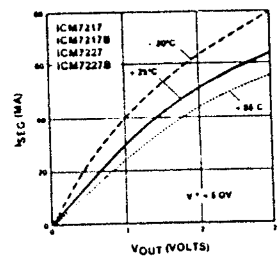
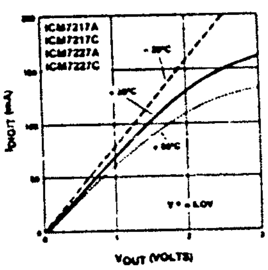


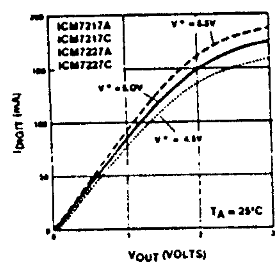
0354-9

Typical I_{SEG} vs. V_{OUT}



0354-10

Typical I_{DIGIT} vs. V_{OUT}



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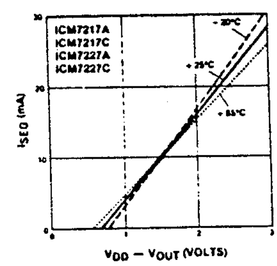

0354-12

Typical I_{SEG} vs. $V_{DD} - V_{OUT}$, $4.5 \leq V_{DD} - V_{SS} \leq 6.0V$

Table 2: Control Input Definitions ICM7217

Input	Terminal	Voltage	Function
$\overline{\text{STORE}}$	9	V_{DD} (or floating) V_{SS}	Output latches not updated Output latches updated
UP/$\overline{\text{DOWN}}$	10	V_{DD} (or floating) V_{SS}	Counter counts up Counter counts down
$\overline{\text{RESET}}$	14	V_{DD} (or floating) V_{SS}	Normal Operation Counter Reset
LOAD COUNTER/ $\overline{\text{I/O OFF}}$	12	Unconnected V_{DD} V_{SS}	Normal operation Counter loaded with BCD data BCD port forced to Hi Z condition
LOAD REGISTER/ OFF	11	Unconnected V_{DD} V_{SS}	Normal operation Register loaded with BCD data Display drivers disabled; BCD port forced to Hi Z condition, mpx counter reset to D4; mpx oscillator inhibited
DISPLAY CONTrol (DC)	23 Common Anode 20 Common Cathode	Unconnected V_{DD} V_{SS}	Normal Operation Segment drivers disabled Leading zero blanking inhibited

NOTE: All typical values have been characterized but are not tested.

Table 3: Control Input Definitions ICM7227

Input		Terminal	Voltage	Function
	DATA TRANSFER	13	V_{DD} V_{SS}	Normal Operation Causes transfer of data as directed by select code
Control Word Port	STORE	9	V_{DD} (During $\overline{CWS}$ Pulse) V_{SS}	Output latches updated Output latches not updated
"	UP/$\overline{DOWN}$	10	V_{DD} (During $\overline{CWS}$ Pulse) V_{SS}	Counter counts up Counter counts down
" 2"	Select Code Bit 1 (SC1) Select Code Bit 2 (SC2)	11 12	V_{DD} = "1" V_{SS} = "0"	SC1, SC2 control:— 00 Change store and up/$\overline{down}$ latches. No data transfer. 01 Output latch data active 10 Counter to be preset 11 Register to be preset
	Control Word Strobe ($\overline{CWS}$)	14	V_{DD} V_{SS}	Normal operation Causes control word to be written into control latches
	DISPLAY CONTrol (DC)	23 Common Anode 20 Common Cathode	Unconnected V_{DD} V_{SS}	Normal operation Display drivers disabled Leading zero blanking inhibited

DETAILED DESCRIPTION

OUTPUTS

The CARRY/BORROW output is a positive going pulse occurring typically 500ns after the positive going edge of the COUNT INPUT. It occurs when the counter is clocked from 9999 to 0000 when counting up and from 0000 to 9999 when counting down. This output allows direct cascading of counters.

The $\overline{EQUAL}$ output assumes a negative level when the contents of the counter and register are equal.

The $\overline{ZERO}$ output assumes a negative level when the content of the counter is 0000.

The CARRY/BORROW, $\overline{EQUAL}$ and $\overline{ZERO}$ outputs will drive a single TTL load over the full range of supply voltage and ambient temperature; for a logic zero, these outputs will sink 1.6mA @ 0.4V (on resistance 250Ω), and for a logic one, the outputs will source >60μA. A 10kΩ pull-up resistor to V_{DD} on the $\overline{EQUAL}$ or $\overline{ZERO}$ outputs is recommended for highest speed operation, and on the CARRY/BORROW output when it is being used for cascading.

The Digit and SEGment drivers provide a decoded 7 segment display system, capable of directly driving common anode LED displays at typical peak currents of 40mA/seg. This corresponds to average currents of 10mA/seg at a 25% multiplex duty cycle. For the common cathode versions, peak segment currents are 12.5mA, corresponding to average segment currents of 3.1mA. Figure 5 shows the multiplex timing, while Figure 6 shows the Output Timing. The DISPLAY pin controls the display output using three level logic. The pin is self-biased to a voltage approximately ½ (V_{DD}); this corresponds to normal operation. When this pin is connected to V_{DD}, the segments are inhibited, and when connected to V_{SS}, the leading zero blanking feature is inhibited. For normal operation (display on with leading zero blanking) the pin may be left open. The display may be controlled with a 3 position SPDT switch; see Figure 4.

NOTE: All typical values have been characterized but are not tested.

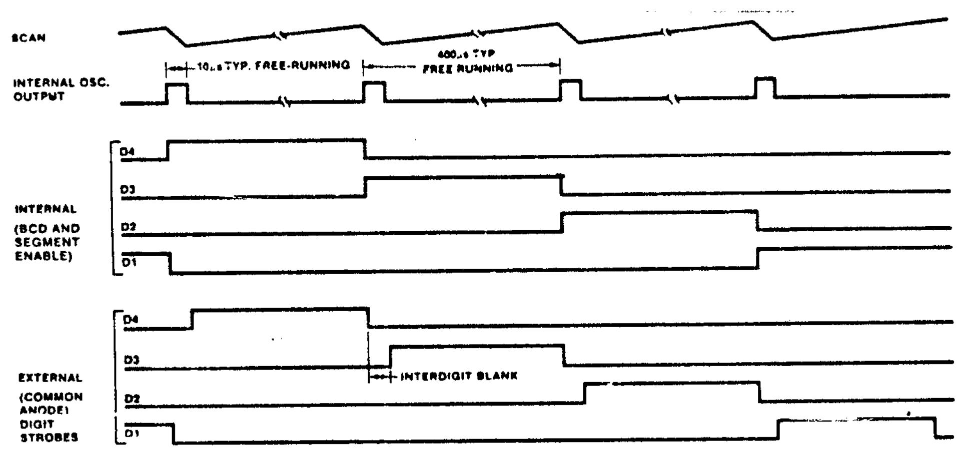

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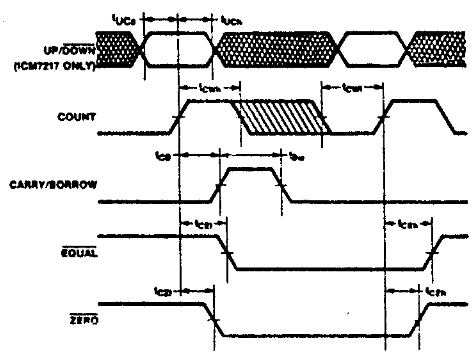
Figure 5: Multiplex Timing



Symbol	Description	Min	Typ	Max	Unit
t_{UCs}	UP/DOWN setup time (min)		300		
t_{UCh}	UP/DOWN hold time (min)		0		
t_{CUh}	COUNT pulse high (min)		100	250	ns
t_{CUl}	COUNT pulse low (min)		100	250	
t_{CB}	COUNT to CARRY/ BORROW delay		750		
t_{Bw}	CARRY/BORROW pulse width		100		
t_{CEl}	COUNT to EQUAL delay		500		
t_{CZl}	COUNT to ZERO delay		300		

0354-14

Figure 6: ICM7217/27 COUNT and Output Timing

Multiplex SCAN Oscillator

The on-board multiplex scan oscillator has a nominal free-running frequency of 2.5kHz. This may be reduced by the addition of a single capacitor between the SCAN pin and the positive supply (ICM7217 only). Capacitor values and corresponding nominal oscillator frequencies, digit repetition rates, and loading times are shown in Table 1 below.

The internal oscillator output has a duty cycle of approximately 25:1, providing a short pulse occurring at the oscillator frequency. This pulse clocks the four-state counter which provides the four multiplex phases. The short pulse width is used to delay the digit driver outputs, thereby providing inter-digit blanking which prevents ghosting. The digits are scanned from MSD (D4) to LSD (D1). See Figure 4 for the display digit multiplex timing.

Table 1: ICM7217 Multiplexed Rate Control

Scan Capacitor	Nominal Oscillator Frequency	Digit Repetition Rate	Scan Cycle Time (4 digits)
None	2.5kHz	625Hz	1.6ms
20pF	1.25kHz	300Hz	3.2ms
90pF	600Hz	150Hz	8ms

NOTE: All typical values have been characterized but are not tested.

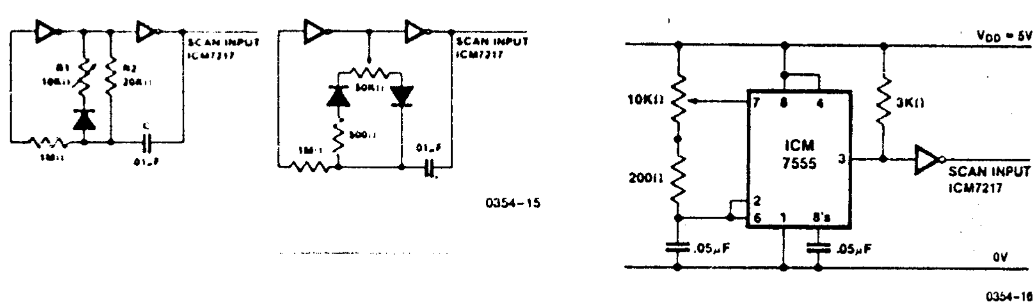


Figure 7: Brightness Control Circuits

During **load counter** and **load register** operations, the multiplex oscillator is disconnected from the SCAN input and is allowed to free-run. In all other conditions, the oscillator may be directly overdriven to about 20kHz, however the internal oscillator signal will be of the same duty cycle and phase as the overdriving signal, and the digits are blanked during the time the external signal is at a positive level. To insure proper leading zero blanking, the interdigit blanking time should not be less than about 2μs. Overdriving the oscillator at less than 200Hz may cause display flickering.

The display brightness may be altered by varying the duty cycle. Figure 7 shows several variable-duty-cycle oscillators suitable for brightness control at the ICM7217 SCAN input. The inverters should be CMOS CD4000 series and the diodes may be any inexpensive device such as IN914.

Counting Control

As shown in Figure 6, the counter is incremented by the rising edge of the COUNT INPUT signal when UP/$\overline{\text{DOWN}}$ is high. It is decremented when UP/$\overline{\text{DOWN}}$ is low. A Schmitt trigger on the COUNT INPUT provides hysteresis to prevent double triggering on slow rising edges and permits operation in noisy environments. The COUNT INPUT is inhibited during reset and **load counter** operations.

The $\overline{\text{STORE}}$ pin controls the internal latches and consequently the signals appearing at the 7-segment and BCD outputs. Bringing the $\overline{\text{STORE}}$ pin low transfers the contents of the counter into the latches.

The counter is asynchronously reset to 0000 by bringing the $\overline{\text{RESET}}$ pin low. The circuit performs the reset operation by forcing the BCD input lines to zero, and "presetting" all four decades of counter in parallel. This affects register loading; if LOAD REGISTER is activated when the $\overline{\text{RESET}}$ input is low, the register will also be set to zero. The STORE, RESET and UP/DOWN pins are provided with pull-up resistors of approximately 75kΩ.

BCD I/O Pins

The BCD I/O port provides a means of transferring data to and from the device. The ICM7217 versions can multiplex data into the counter or register via thumbwheel switches, depending on inputs to the LOAD COUNTER or LOAD REGISTER pins; (see below). When functioning as outputs, the BCD I/O pins will drive one standard TTL load. Common anode versions have internal pull down resistors and common cathode versions have internal pull up resistors on the four BCD I/O lines when used as inputs.

LOADing the COUNTER and REGISTER

The BCD I/O pins, the LOAD COUNTER (LC), and LOAD REGISTER (LR) pins combine to provide presetting and compare functions. LC and LR are three-level inputs, being self-biased at approximately ½V_{DD} for normal operation. With both LC and LR open, the BCD I/O pins provide a multiplexed BCD output of the latch contents, scanned from MSD to LSD by the display multiplex.

When either the LOAD COUNTER (Pin 12) or LOAD REGISTER (Pin 11) is taken high, the drivers are turned off and the BCD pins become high-impedance inputs. When LC is connected to V_{DD}, the count input is inhibited and the levels at the BCD pins are multiplexed into the counter. When LR is connected to V_{DD}, the levels at the BCD pins are multiplexed into the register without disturbing the counter. When both are connected to V_{DD}, the count is inhibited and both register and counter will be loaded.

The LOAD COUNTER and LOAD REGISTER inputs are edge-triggered, and pulsing them high for 500ns at room temperature will initiate a full sequence of data entry cycle operations (see Figure 7). When the circuit recognizes that either or both of the LC or LR pins input is high, the multiplex oscillator and counter are reset (to D4). The internal oscillator is then disconnected from the SCAN pin and the

NOTE: All typical values have been characterized but are not tested.

reset circuitry is enabled. The oscillator starts and runs at a frequency determined by its internal capacitor, (which may vary from chip to chip). When the chip finishes a full 4 digit multiplex cycle (loading each digit from D4 to D3 to D2 to D1 in turn), it again samples the LOAD REGISTER and LOAD COUNTER inputs. If either or both is still high, it repeats the load cycle. If both are floating or low, the oscillator is reconnected to the SCAN pin and the chip returns to normal operation. Total load time is digit "on" time multiplied by 4. If the Digit outputs are used to strobe the BCD data into the BCD I/O inputs, the input will be automatically synchronized to the appropriate digit (Figure 8). Input data must be valid at the trailing edge of the digit output.

When LC is connected to GROUND, the oscillator is inhibited, the BCD I/O pins go to the high impedance state, and the segment and digit drivers are turned off. This allows the display to be used for other purposes and minimizes power consumption. In this display off condition, the circuit will continue to count, and the CARRY/BORROW, $\overline{\text{EQUAL}}$, $\overline{\text{ZERO}}$, UP/$\overline{\text{DOWN}}$, $\overline{\text{RESET}}$ and $\overline{\text{STORE}}$ functions operate as normal. When LC is connected to ground, the BCD I/O pins are forced to the high impedance state without disturbing the counter or register. See "Control Input Definitions" (Table 2) for a list of the pins that function as three-state self-biased inputs and their respective operations.

Note that the ICM7217 and 7217B have been designed to drive common anode displays. The BCD inputs are high true, as are the BCD outputs.

The ICM7217A and the 7217C are used to drive common cathode displays, and the BCD inputs are low true. BCD outputs are high true.

Notes on Thumbwheel Switches & Multiplexing

The thumbwheel switches used with these circuits (both common anode and common cathode) are TRUE BCD coded, i.e. all switches open corresponds to 0000. Since the thumbwheel switches are connected in parallel, diodes must be provided to prevent crosstalk between digits. See Figure 8. In order to maintain reasonable noise margins, these diodes should be specified with low forward voltage drops (IN914). Similarly, if the BCD outputs are to be used, resistors should be inserted in the Digit lines to avoid loading problems.

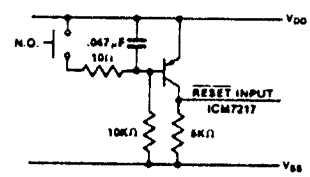
Output and Input Restrictions

The CARRY/BORROW output is not valid during load counter and reset operations.

The $\overline{\text{EQUAL}}$ output is not valid during load counter or load register operations.

The $\overline{\text{ZERO}}$ output is not valid during a load counter operation.

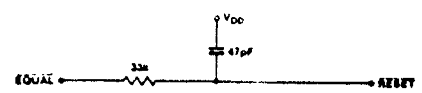
The $\overline{\text{RESET}}$ input may be susceptible to noise if its input rise time (coming out of reset) is greater than about 500µs. This will present no problems when this input is driven by active devices (i.e., TTL or CMOS logic) but in hardwired systems adding virtually any capacitance to the $\overline{\text{RESET}}$ input can cause trouble. A simple circuit which provides a reliable power-up reset and a fast rise time on the $\overline{\text{RESET}}$ input is shown below.



0354-17

Figure 8

When using the circuit as a programmable divider (÷ by n with equal outputs) a short time delay (about 1µs) is needed from the $\overline{\text{EQUAL}}$ output to the $\overline{\text{RESET}}$ input to establish a pulse of adequate duration. (See Figure 9)



0354-18

Figure 9

When the circuit is configured to reload the counter or register with a new value from the BCD lines (upon reaching $\overline{\text{EQUAL}}$), loading time will be digit "on" time multiplied by four. If this load time is longer than one period of the input count, a count can be lost. Since the circuit will retain data in the register, the register need only be updated when a new value is to be entered. $\overline{\text{RESET}}$ will not clear the register.

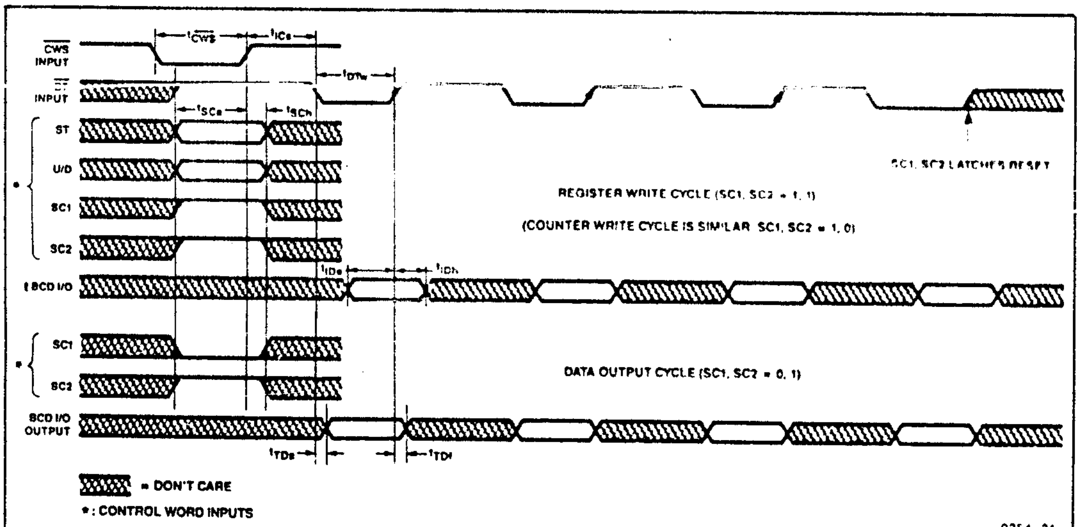


Figure 12: ICM7227 I/O Timing (see Table 4)

CONTROL OF ICM7227 VERSIONS

The ICM7227 series has been designed to permit microprocessor control of the inputs. BCD inputs and outputs are active high.

In these versions, the STORE, UP/$\overline{\text{DOWN}}$, SC1 and SC2 (Select Code bits 1 and 2) pins form a four-bit control word input. A negative-going pulse on the $\overline{\text{CWS}}$ (Control Word Strobe) pin writes the data on these pins into four internal control latches, and resets the multiplex counter in preparation for sequencing a data transfer operation. The select code 00 is reserved for changing the state of the Store and/or Up/$\overline{\text{Down}}$ latches without initiating a data transfer. Writing a one into the Store latch sets the latch and causes the data in the counter to be transferred into the output latches, while writing a zero resets the latches causing them to retain data and not be updated. Similarly, writing a one into the Up/$\overline{\text{Down}}$ latch causes the counter to count up and writing a zero causes the counter to count down. The state of the Store and Up/$\overline{\text{Down}}$ latches may also be changed with a non-zero select code.

Writing a nonzero select code initiates a **data transfer** operation. Writing select code of 01 (SC1, SC2) indicates that the data in the output latches will be active and enables the BCD I/O port to output the data. Writing a select code of 11 indicates that the register will be preset, and a 10 indicates that the counter will be preset.

When a nonzero select code is read, the clock of the four-state multiplex counter is switched to the $\overline{\text{DATA TRANSFER}}$ pin. Negative-going pulses at this pin then sequence a digit-by-digit data transfer, either outputting data or presetting the counter or register as determined by the select code. The output drivers of the BCD I/O port will be enabled only while $\overline{\text{DT}}$ is low during a data transfer initiated with a 01 select code.

The sequence of digits will be D4-D3-D2-D1, i.e. when outputting, the data from D4 will be valid during the first $\overline{\text{DT}}$ pulse, then D3 will be valid during the second pulse, etc. When presetting, the data for D4 must be valid at the positive-going transition (trailing edge) of the first $\overline{\text{DT}}$ pulse, the data for D3 must be valid during the second $\overline{\text{DT}}$ pulse, etc.

At the end of a **data transfer** operation, on the positive going transition of the fourth $\overline{\text{DT}}$ pulse, the SC1 and SC2 control latches will automatically reset, terminating the data transfer and reconnecting the multiplex counter clock to the oscillator. In the ICM7227 versions, the multiplex oscillator is always free-running, except during a **data transfer** operation when it is disabled.

Figure 12 shows the timing of data transfers initiated with a 11 select code (writing into the register) and a 01 select code (reading out of the output latches). Typical times during which data must be valid at the control word and BCD I/O ports are indicated in Table 4.

Table 4: ICM7227 I/O Timing Requirements

Symbol	Description	Min	Typ	Max	Units
$t_{\overline{CWS}}$	Control Word Strobe Width (min)		275		ns
t_{ICs}	Internal Control Set-up (min)		2.5	3	µs
$t_{\overline{DT}w}$	DATA TRANSFER pulse width (min)		300		ns
t_{SCs}	Control to Strobe setup (min)		300		ns
t_{SCh}	Control to Strobe hold (min)		300		ns
t_{IDs}	Input Data setup (min)		300		ns
t_{IDh}	Input Data Hold (min)		300		ns
t_{TDacc}	Output Data access		300		ns
t_{TDf}	Output Transfer to Data float		300		ns

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NOTE: All typical values have been characterized but are not tested.

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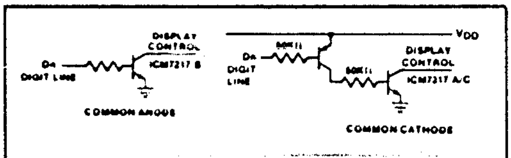
APPLICATIONS

FIXED DECIMAL POINT

In the common anode versions, a fixed decimal point may be activated by connecting the D.P. segment lead from the appropriate digit (with separate digit displays) through a 39Ω series resistor to Ground. With common cathode devices, the D.P. segment lead should be connected through a 75Ω series resistor to V_{DD}.

To force the device to display leading zeroes after a fixed decimal point, use a bipolar transistor and base resistor in a configuration like that shown below with the resistor connected to the digit output driving the D.P. for left hand D.P. displays, and to the next least significant digit output for right hand D.P. display. See Performance Characteristics for a similarly operating multi-digit connection.

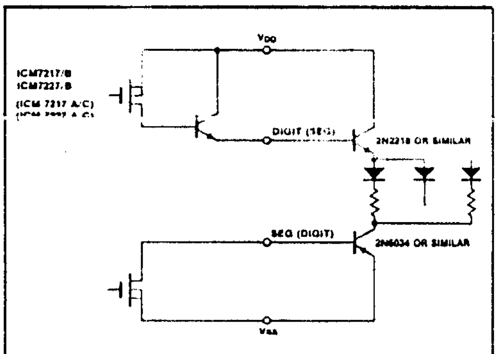


0354-22

Figure 13: Forcing Leading Zero Display

DRIVING LARGER DISPLAYS

For displays requiring more current than the ICM7217/7227 can provide, the circuits of Figure 14 can be used.



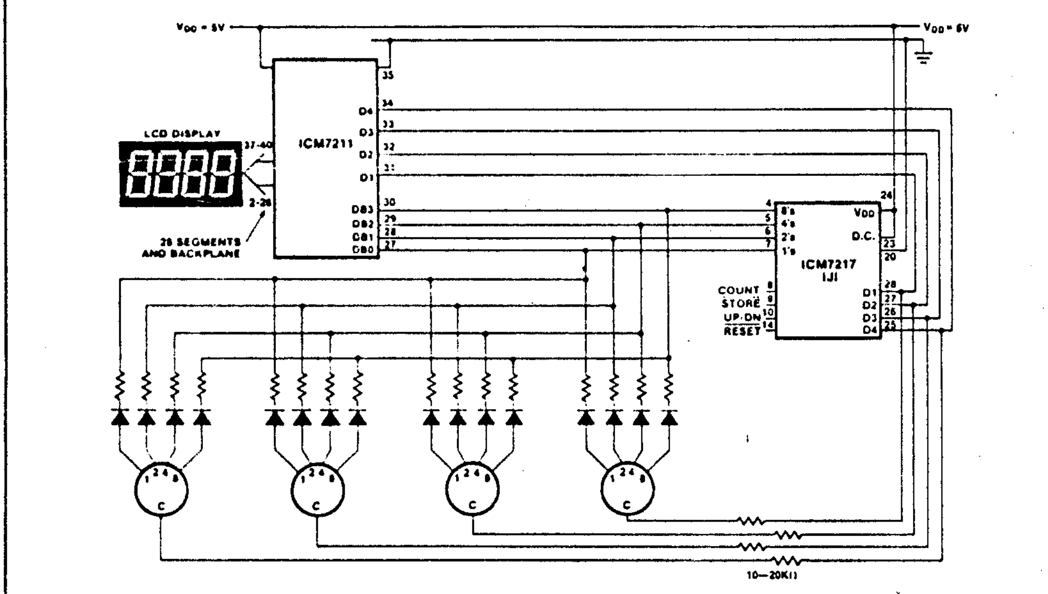
0354-23

Figure 14: Driving High Current Displays

LCD DISPLAY INTERFACE

The low-power operation of the ICM7217 makes an LCD interface desirable. The Intersil ICM7211 4 digit BCD to LCD display driver easily interfaces to the ICM7217 as shown in Figure 15. Total system power consumption is less than 5mW. System timing margins can be improved by using capacitance to ground to slow down the BCD lines. A similar circuit can be used to drive Vacuum Fluorescent displays, with the ICM7235.

The 10 - 20kΩ resistors on the switch BCD lines serve to isolate the switches during BCD output.



0354-24

Figure 15: LCD Display Interface (with Thumbwheel Switches)

NOTE: All typical values have been characterized but are not tested.

ICM7217/ICM7227

UNIT COUNTER WITH BCD OUTPUT

The simplest application of the ICM7217 is a 4 digit unit counter (Figure 16). All that is required is an ICM7217, a power supply and a 4 digit display. Add a momentary switch for reset, an SPDT center-off switch to blank the display or view leading zeroes, and one more SPDT switch for up/down control. Using an ICM7217A with a common-cathode calculator type display results in the least expensive digital counter/display system available.

INEXPENSIVE FREQUENCY COUNTER/ TACHOMETER

This circuit uses the low power ICM7555 (CMOS 555) to generate the gating, STORE and RESET signals as shown in Figure 17. To provide the gating signal, the timer is configured as an astable multivibrator, using R_A, R_B and C to provide an output that is positive for approximately one second and negative for approximately 300 – 500μs. The positive waveform time is given by $t_{wp} = 0.693 (R_A + R_B)C$ while the negative waveform is given by $t_{wn} = 0.693 R_B C$. The system is calibrated by using a 5MΩ potentiometer for R_A as a "coarse" control and a 1kΩ potentiometer for R_B as a "fine" control. CD40106B's are used as a monostable multivibrator and reset time delay.

TAPE RECORDER POSITION INDICATOR/CONTROLLER

The circuit in Figure 18 shows an application which uses the up/down counting feature of the ICM7217 to keep track of tape position. This circuit is representative of the many applications of up/down counting in monitoring dimensional position. For example, an ICM7227 as a peripheral to a processor can monitor the position of a lathe bed or digitizing head, transfer the data to the processor, drive interrupts to the processor using the $\overline{\text{EQUAL}}$ or $\overline{\text{ZERO}}$ outputs, and serve as a numerical display for the processor.

In the tape recorder application, the LOAD REGISTER, $\overline{\text{EQUAL}}$ and $\overline{\text{ZERO}}$ outputs are used to control the recorder. To make the recorder stop at a particular point on the tape, the register can be set with the stop point and the $\overline{\text{EQUAL}}$ output used to stop the recorder either on fast forward, play or rewind.

To make the recorder stop before the tape comes free of the reel on rewind, a leader should be used. Resetting the counter at the starting point of the tape, a few feet from the end of the leader, allows the $\overline{\text{ZERO}}$ output to be used to stop the recorder on rewind, leaving the leader on the reel.

The 1MΩ resistor and .0047μF capacitor on the COUNT INPUT provide a time constant of about 5ms to debounce the reel switch. The Schmitt trigger on the COUNT INPUT of the ICM7217 squares up the signal before applying it to the counter. This technique may be used to debounce switch-closure inputs in other applications.

PRECISION ELAPSED TIME/ COUNTDOWN TIMER

The circuit in Figure 19 uses an ICM7213 precision one minute/one second timebase generator using a 4.1943MHz crystal for generating pulses counted by an ICM7217B. The thumbwheel switches allow a starting time to be entered into the counter for a preset-countdown type timer, and allow the register to be set for compare functions. For instance, to make a 24-hour clock with BCD output the register can be preset with 2400 and the $\overline{\text{EQUAL}}$ output used to reset the counter. Note the 10k resistor connected between the LOAD COUNTER terminal and Ground. This resistor pulls the LOAD COUNTER input low when not loading, thereby inhibiting the BCD output drivers. This resistor should be eliminated and SW4 replaced with an SPDT center-off switch if the BCD outputs are to be used.

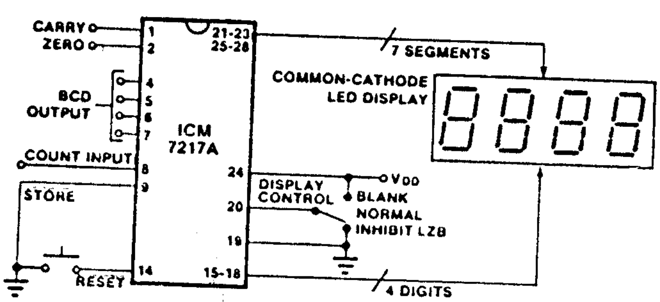
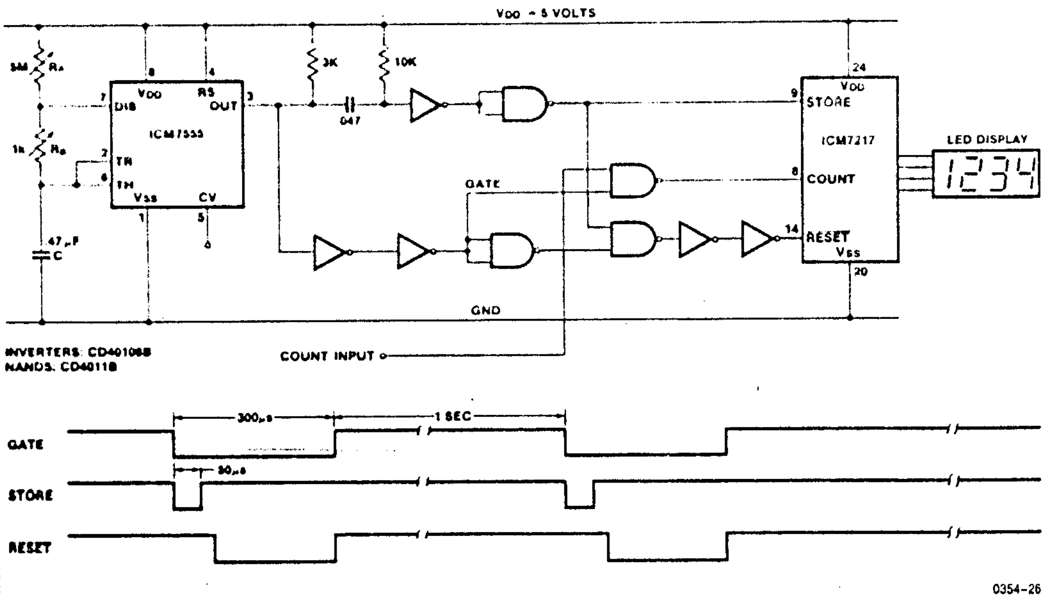


Figure 16: Unit Counter

0354-25

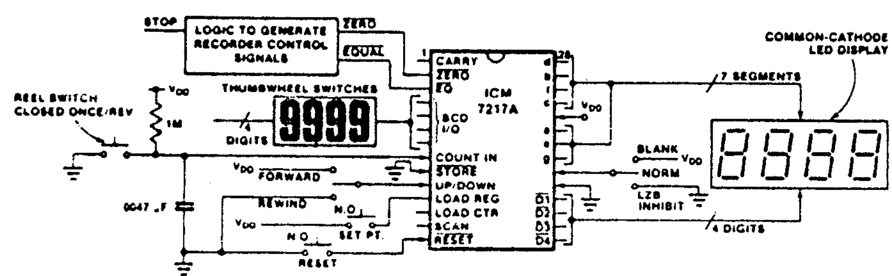
NOTE: All typical values have been characterized but are not tested.

ICM7217/ICM7227



0354-26

Figure 17: Inexpensive Frequency Counter



0354-27

Figure 18: Tape Recorder Position Indicator

NOTE: All typical values have been characterized but are not tested.

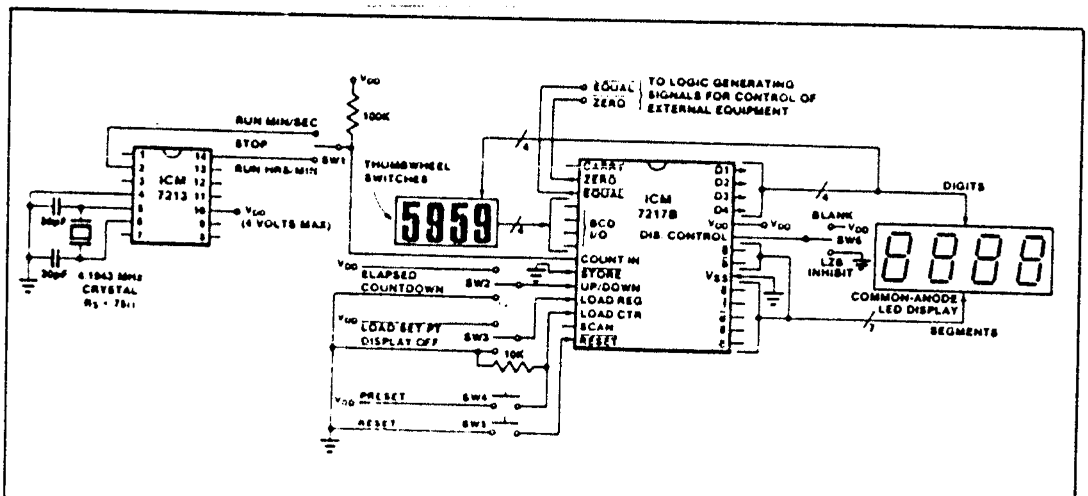


Figure 19: Precision Timer

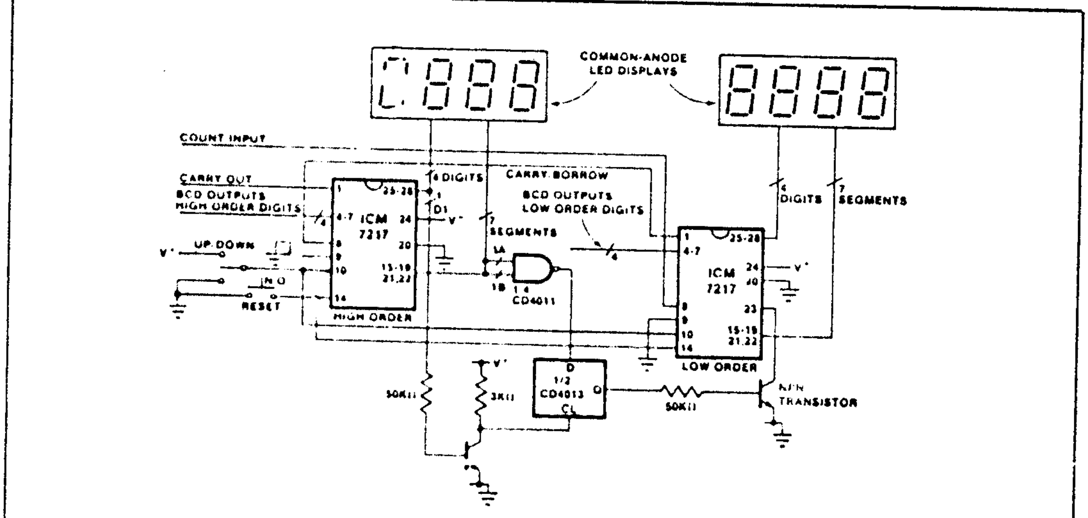
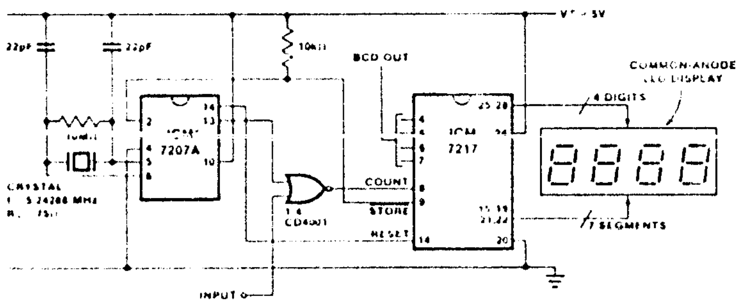


Figure 20: 8 Digit Up/Down Counter

NOTE: All typical values have been characterized but are not tested.

ICM7217/ICM7227



0354-30

Figure 21: Precision Frequency Counter (MHz Maximum)

This technique may be used on any 3-level input. The 100kΩ pullup resistor on the count input is used to ensure proper logic voltage swing from the ICM7213. For a less expensive (and less accurate) timebase, an ICM7555 timer may be used in a configuration like that shown in Figure 17 to generate a 1Hz reference.

8-DIGIT UP/DOWN COUNTER

This circuit (Figure 20) shows how to cascade counters and retain correct leading zero blanking. The NAND gate detects whether a digit is active since one of the two segments $\bar{a}$ or $\bar{b}$ is active on any unblanked number. The flip flop is clocked by the least significant digit of the high order counter, and if this digit is not blanked, the Q output of the flip flop goes high and turns on the NPN transistor, thereby inhibiting leading zero blanking on the low order counter.

It is possible to use separate thumbwheel switches for presetting, but since the devices load data with the oscillator free-running, the multiplexing of the two devices is difficult to synchronize. This presents no problems with the ICM7227 devices, since the two devices are operated as peripherals to a processor.

PRECISION FREQUENCY COUNTER/ TACHOMETER

The circuit shown in Figure 21 is a simple implementation of a four digit frequency counter, using an ICM7207A to provide the one second gating window and the $\overline{\text{STORE}}$ and $\overline{\text{RESET}}$ signals. In this configuration, the display reads hertz directly. With Pin 11 of the ICM7027A connected to V_{DD}, the gating time will be 0.1 second; this will display tens of hertz as the least significant digit. For shorter gating times, an ICM7207 may be used (with a 6.5536MHz crystal), giving a 0.01 second gating with Pin 11 connected to V_{DD}, and a 0.1 second gating with Pin 11 open.

To implement a four digit tachometer, the ICM7207A with one second gating should be used. To get the display to read directly in RPM, the rotational frequency of the object to be measured must be multiplied by 60. This can be done electronically using a phase-locked loop, or mechanically by using a disc rotating with the object with the appropriate number of holes drilled around its edge to interrupt the light from an LED to a photo-dector. For faster updating, use 0.1 second gating, and multiply the rotational frequency by 600.

For more "intelligent" instrumentation, the ICM7227 interfaced to a microprocessor may be more convenient (see Figure 21). For example, an ICM7207A can be used with two ICM7227's to provide an 8 digit, 2MHz frequency counter. Since the ICM7207A gating output has a 50% duty cycle, there is 1 second for the processor to respond to an interrupt, generated by the negative going edge of this signal while it inhibits the count. The processor can respond to the interrupt using ROM based subroutines, to store the data, reset the counter, and read the data into main memory. To add simultaneous period display, the processor inverts the data and an ICM7218 Universal Display Driver stores and displays it.

AUTO-TARE SYSTEM

This circuit uses the count-up and count-down functions of the ICM7217, controlled via the $\overline{\text{EQUAL}}$ and $\overline{\text{ZERO}}$ outputs, to count in SYNC with an ICL7109 A/D Converter as shown in Figure 22. By $\overline{\text{RESET}}$ing the ICM7217 on a "tare" value conversion, and $\overline{\text{STORE}}$-ing the result of a true value conversion, an automatic tare subtraction occurs in the result.

The ICM7217 stays in step with the ICL7019 by counting up and down between 0 and 4095, for 8192 total counts, the same number as the ICL7109 cycle. See A047 for more details.